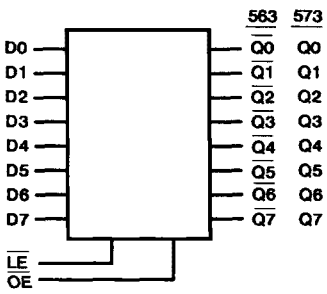
CD54/74FCT563, CD54/74FCT563AT
CD54/74FCT573, CD54/74FCT573AT

July 1990



FUNCTIONAL DIAGRAM

Octal Transparent Latch, 3-State

CD54/74FCT563, CD54/74FCT563AT - Inverting
CD54/74FCT573, CD54/74FCT573AT - Non-Inverting

Type Features:

- *Buffered inputs*
- *Typical propagation delay: 3.9ns @ VCC = 5V, TA = +25°C, CL = 50pF (FCT573AT)*

The CD54/74FCT563, 563AT, 573 and 573AT octal transparent latches use a small-geometry BiCMOS technology. The output stage is a combination of bipolar and CMOS transistors that limits the output-HIGH level to two diode drops below VCC. This resultant lowering of output swing (0V to 3.7V) reduces power bus ringing (a source of EMI) and minimizes VCC bounce and ground bounce and their effects during simultaneous output switching. The output configuration also enhances switching speed and is capable of sinking 32 to 48 milliamperes.

The CD54/74FCT563, 563AT, 573 and 573AT outputs are transparent to the inputs when the Latch Enable ($\overline{LE}$) is HIGH. When the Latch Enable ($\overline{LE}$) goes LOW, the data is latched. The Output Enable ($\overline{OE}$) controls the 3-state outputs. When the Output Enable ($\overline{OE}$) is HIGH, the outputs are in the high-impedance state. The latch operation is independent of the state of the Output Enable.

The CD54/74FCT563, 563AT, 573 and 573AT are supplied in 20-lead dual-in-line plastic packages (E suffix) and in 20-lead dual-in-line small-outline plastic packages (M suffix). Both package types are operable over two temperature ranges: Commercial (0°C to +70°C) and Extended Industrial (-55°C to +125°C).

The CD54FCT563 and 573 are also available in chip form (H suffix). These unpackaged devices are operable over the -55°C to +125°C temperature range.

Family Features:

- *SCR-latchup-resistant BiCMOS process and circuit design*
- *FCTXXX Types - Speed of bipolar FAST*/AS/S; FCTXXXAT Types - 30% faster than FAST/AS/S with significantly reduced power consumption*
- *48/32-mA output sink current (commercial/extended industrial)*
- *Output voltage swing limited to 3.7V @ VCC = 5V*
- *Controlled output-edge rates*
- *Input/output isolation to VCC*
- *BiCMOS technology with low quiescent power*

* FAST is a registered trademark of Fairchild Semiconductor Corp.

TRUTH TABLE

$\overline{OUTPUT}$ ENABLE	$\overline{LATCH}$ ENABLE	DATA	563, 563AT OUTPUT	573, 573AT OUTPUT
L	H	H	L	H
L	H	L	H	L
L	L	l	H	L
L	L	h	L	H
H	X	X	Z	Z

H = High voltage level.
L = Low voltage level.
l = Low voltage level one set-up time prior to the high-to-low latch enable transition.
h = High voltage level one set-up time prior to the high-to-low latch enable transition.
X = Irrelevent.
Z = High-impedance.

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY-VOLTAGE (VCC) ..... -0.5V to 6V
DC INPUT DIODE CURRENT, IIK (for VI < -0.5V) ..... -20mA
DC OUTPUT DIODE CURRENT, IOK (for VO < -0.5V) ..... -50mA
DC OUTPUT SINK CURRENT per Output Pin, IO ..... +70mA
DC OUTPUT SOURCE CURRENT per Output Pin, IO ..... -30mA
DC VCC CURRENT (ICC) 140mA
DC GROUND CURRENT (IGND) 400mA
POWER DISSIPATION PER PACKAGE (PD):
For TA = -55°C to +100°C (PACKAGE TYPE E) 500mW
For TA = +100°C to +125°C (PACKAGE TYPE E) ..... Derate Linearly at 8mW/°C to 300mW
For TA = -55°C to +70°C (PACKAGE TYPE M) 400mW
For TA = +70°C to +125°C (PACKAGE TYPE M) ..... Derate Linearly at 6mW/°C to 70mW
OPERATING-TEMPERATURE RANGE (TA):
PACKAGE TYPE E, M ..... -55°C to +125°C
STORAGE TEMPERATURE (Tstg) ..... -65°C to +150°C
LEAD TEMPERATURE (DURING SOLDERING):
At distance 1/16 in. ± 1/32 in. (1.59mm ± 0.79mm) from case for 10s maximum ..... +265°C
Unit inserted into PC board min. thickness 1/16 in. (1.59mm) with solder contacting lead tips only ..... +300°C

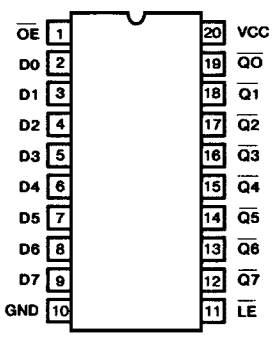
RECOMMENDED OPERATING CONDITIONS:

The following are normal operating ranges for these devices. For maximum reliability, devices should always be operated within these ranges.

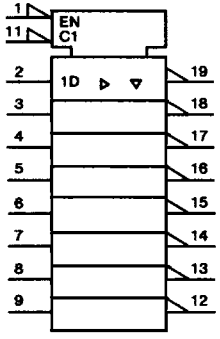
CHARACTERISTIC		LIMITS MIN	LIMITS MAX	UNITS
Supply-Voltage Range, VCC*:	CD74 Series, TA = 0°C to 70°C	4.75	5.25	V
	CD54 Series, TA = -55°C to +125°C	4.5	5.5	V
DC Input Voltage, VI		0	VCC	V
DC Output Voltage, VO		0	≤VCC	V
Operating Temperature, TA		-55	+125	°C
Input Rise and Fall Slew Rate, dt/dv		0	10	ns/V

* Unless otherwise specified, all voltages are referenced to ground.

CD54/74FCT563, CD54/74FCT563AT TYPES

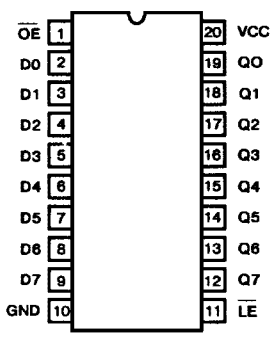


TERMINAL ASSIGNMENT



IEC LOGIC SYMBOL

CD54/74FCT573, CD54/74FCT573AT TYPES



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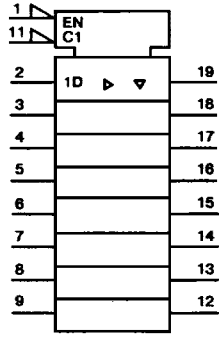


IEC LOGIC SYMBOL

STATIC ELECTRICAL CHARACTERISTICS

FCT Series: 74FCT Commercial Temperature Range, 0°C to +70°C; VCC max = 5.25V, VCC min = 4.75V
54FCT Extended Industrial Temperature Range, −55°C to +125°C; VCC max = 5.5V, VCC min = 4.5V

CHARACTERISTICS		TEST CONDITIONS VI (V)	TEST CONDITIONS IO (mA)	VCC (V)	AMBIENT TEMPERATURE (TA) +25°C MIN	+25°C MAX	0°C to +70°C MIN	0°C to +70°C MAX	−55°C to +125°C MIN	−55°C to +125°C MAX	UNITS
High-Level Input Voltage	VIH			4.5 to 5.5	2	–	2	–	2	–	V
Low-Level Input Voltage	VIL			4.5 to 5.5	–	0.8	–	0.8	–	0.8	V
High-Level Output Voltage	VOH	VIH or	−15	MIN	2.4	–	2.4	–	–	–	V
		VIL	−12	MIN	2.4	–	–	–	2.4	–	V
Low-Level Output Voltage	VOL	VIH or	48	MIN	–	0.55	–	0.55	–	–	V
		VIL	32	MIN	–	0.55	–	–	–	0.55	V
High-Level Input Current	IIH	VCC		MAX	–	0.1	–	1	–	1	µA
Low-Level Input Current	IIL	GND		MAX	–	−0.1	–	−1	–	−1	µA
3-State Leakage Current	IOZH	VCC		MAX	–	0.5	–	10	–	10	µA
	IOZL	GND		MAX	–	−0.5	–	−10	–	−10	µA
Short-Circuit Output Current *	IOS	VCC or GND VO = 0		MAX	−60	–	−60	–	−60	–	mA
Input Clamp Voltage	VIK	VCC or GND	−18	MIN	–	−1.2	–	−1.2	–	−1.2	V
Quiescent Supply Current, MSI	ICC	VCC or GND	0	MAX	–	8	–	80	–	500	µA
Additional Quiescent Supply Current per Input Pin TTL Inputs High, 1 Unit Load	ΔICC	3.4V†		MAX	–	1.6	–	1.6	–	2	mA

* Not more than one output should be shorted at one time. Test duration should not exceed 100ms.
† Inputs that are not measured are at VCC or GND.

FCT Input Loading: All inputs are 1 unit load. Unit load is ΔICC limit specified in Static Characteristics Chart, e.g., 1.6mA max. @ +70°C.

PREREQUISITE FOR SWITCHING

CHARACTERISTICS	SYMBOL	V_{CC} (V)	CD54/74FCT563, 573					CD54/74FCT563AT, 573AT					UNITS
			AMBIENT TEMPERATURE (T_A)										
			+25°C	0°C to +70°C		-55°C to +125°C		+25°C	0°C to +70°C		-55°C to +125°C		
			TYP	MIN	MAX	MIN	MAX	TYP	MIN	MAX	MIN	MAX	
$\overline{LE}$ Pulse Width	tW	5†	-	6	-	6	-	-	5	-	6	-	ns
Setup Time Data to $\overline{LE}$	tSU	5	-	2	-	2	-	-	2	-	1.5	-	ns
Hold Time Data to $\overline{LE}$	tH	5	-	1.5	-	1.5	-	-	1.5	-	2	-	ns

†5V: min. is @ 4.5V
5V: min. is @ 4.75V for 0°C to +70°C
typ is @ 5V

SWITCHING CHARACTERISTICS: t_r, t_f = 2.5ns, C_L = 50pF, R_L = See Figure 4

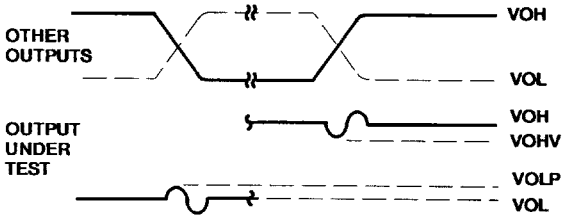
CHARACTERISTICS		SYMBOL	V_{CC} (V)	CD54/74FCT563, 573					CD54/74FCT563AT*, 573AT					UNITS
				AMBIENT TEMPERATURE (T_A)										
				+25°C	0°C to +70°C		-55°C to +125°C		+25°C	0°C to +70°C		-55°C to +125°C		
				TYP	MIN	MAX	MIN	MAX	TYP	MIN	MAX	MIN	MAX	
Propagation Delays: Data to Outputs	FCT563/AT	tPLH, tPHL	5†	5	1.5	8	1.5	8.5						ns
	FCT573/AT	tPLH, tPHL	5	5	1.5	8	1.5	8.5	3.9	1.5	5.7	1.5	6.5	ns
$\overline{LE}$ to Outputs	FCT563/AT	tPLH, tPHL	5	9	1.5	13	1.5	14						ns
	FCT573/AT	tPLH, tPHL	5	9	2	13	2	15	4.4	2	7	2	7.5	ns
Output Enable Times	FCT563/AT	tPZL, tPZH	5	6.5	1.5	11	1.5	12.5						ns
	FCT573/AT	tPZL, tPZH	5	7	1.5	12	1.5	13.5	6	1.5	8	1.5	9.5	ns
Output Disable Times	FCT563/AT	tPLZ, tPHZ	5	5.6	1.5	7	1.5	8.5						ns
	FCT573/AT	tPLZ, tPHZ	5	6	1.5	7.5	1.5	10	4	1.5	5.8	1.5	6.5	ns
Power Dissipation Capacitance	FCT563/AT	CPD§	-	34 Typical					34 Typical					pF
	FCT573/AT	CPD§	-	34 Typical					34 Typical					pF
Min. (Valley) VOHV During Switching of Other Outputs (Output Under Test Not Switching)		VOHV See Fig. 1	5	0.5 Typical @ +25°C										V
Max. (Peak) VOLP During Switching of Other Outputs (Output Under Test Not Switching)		VOLP See Fig. 1	5	1 Typical @ +25°C										V
Input Capacitance		CI	-	-	-	10	-	10	-	-	10	-	10	pF
3-State Output Capacitance		CO	-	-	-	15	-	15	-	-	15	-	15	pF

†5V: min. is @ 5.5V
max. is @ 4.5V
5V: min. is @ 5.25V for 0°C to +70°C
max. is @ 4.75V for 0°C to +70°C
typ is @ 5V

* Contact local Sales Office for availability

§CPD, measured per function, is used to determine the dynamic power consumption.
PD (per package) = VCC ICC + Σ (VCC² fi CPD + VO² fo CL + VCC ΔICC D) where:
VCC = supply voltage
ΔICC = flow through current x unit load
CL = output load capacitance
D = duty cycle of input high
fo = output frequency
fi = input frequency

PARAMETER MEASUREMENT INFORMATION



NOTES:

1. VOLP is measured with respect to a ground reference near the output under test. VOHV is measured with respect to VOH.
2. Input pulses have the following characteristics: PRR $\leq$ 1MHz, tr = 2.5ns, tf = 2.5ns, skew 1ns.
3. R.F. fixture with 700-MHz design rules required. IC should be soldered into test board and bypassed with 0.1µF capacitor. Scope and probes require 700-MHz bandwidth.

Figure 1 - Simultaneous switching transient waveforms.

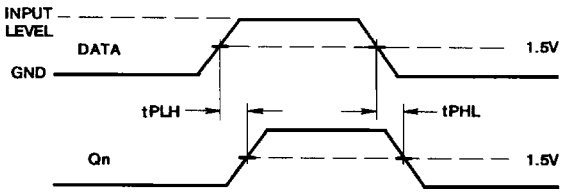


Figure 2 - Data to Qn output propagation delays.

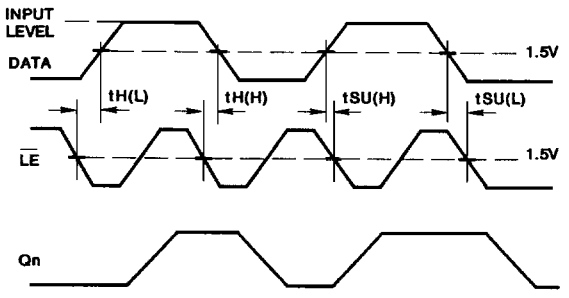
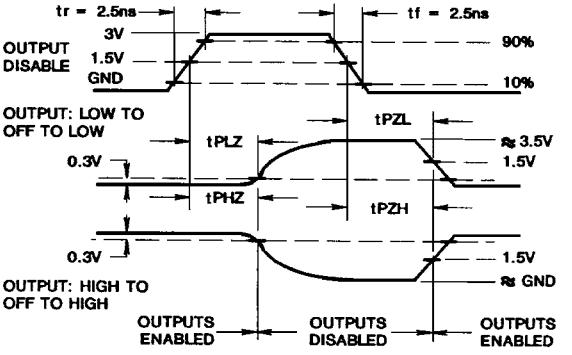
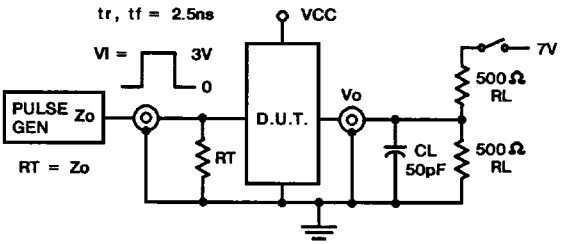


Figure 3 - Latch Enable prerequisite times.





TEST	SWITCH POSITION
tPLZ, tPZL, OPEN DRAIN	CLOSED
tPHZ, tPZH, tPLH, tPHL	OPEN

Figure 4 - Three-state propagation delay times and test circuit.

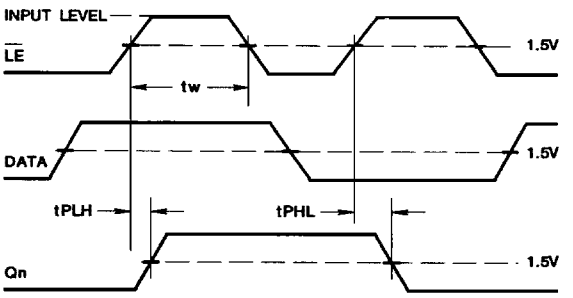


Figure 5 - Latch Enable propagation delays.