MB39A135

1ch DC/DC Converter IC with PFM/PWM Synchronous Rectification

Description

MB39A135 is 1ch step-down DC/DC converter IC of the current mode N-ch/N-ch synchronous rectification method.
It contains the enhanced protection features, and supports the ceramic capacitor. MB39A135 realizes rapid response, high efficiency, and low ripple voltage, and its high-frequency operation enables the miniaturization of inductor and I/O capacitors.

Features

- High efficiency
- For frequency setting by external resistor : 100 kHz to 1 MHz
- Error Amp threshold voltage : 0.7 V ± 1.0 %
- Minimum output voltage value : 0.7 V
- Wide range of power-supply voltage : 4.5 V to 25 V
- PFM/PWM auto switching mode and fixed PWM mode selectable
- With built-in over voltage protection function
- With built-in under voltage protection function
- With built-in over current protection function
- With built-in over-temperature protection function
- With built-in soft start/stop circuit without load dependence
- With built-in synchronous rectification type output steps for N-ch MOS FET
- Standby current : 0 µA (Typ)
- Small package : TSSOP-16

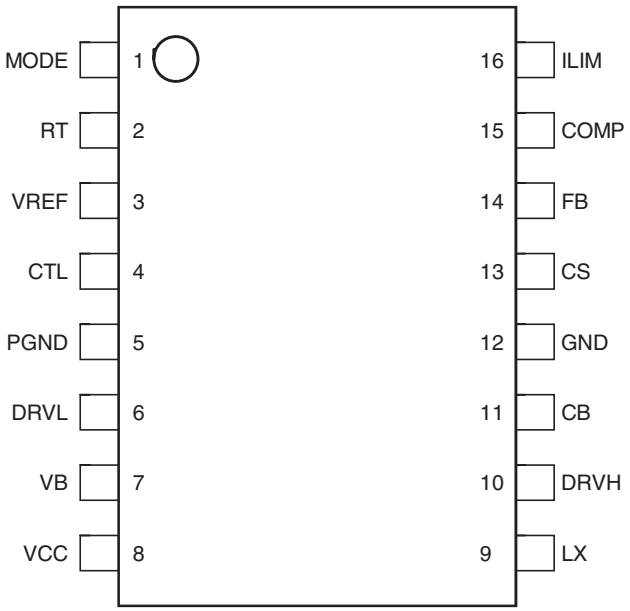
Applications

- Digital TV
- Photocopiers
- Surveillance cameras
- Set-top boxes (STB)
- DVD players, DVD recorders
- Projectors
- IP phones
- Vending machines
- Consoles and other non-portable devices

Contents

1. Pin Assignment

(TOP VIEW)

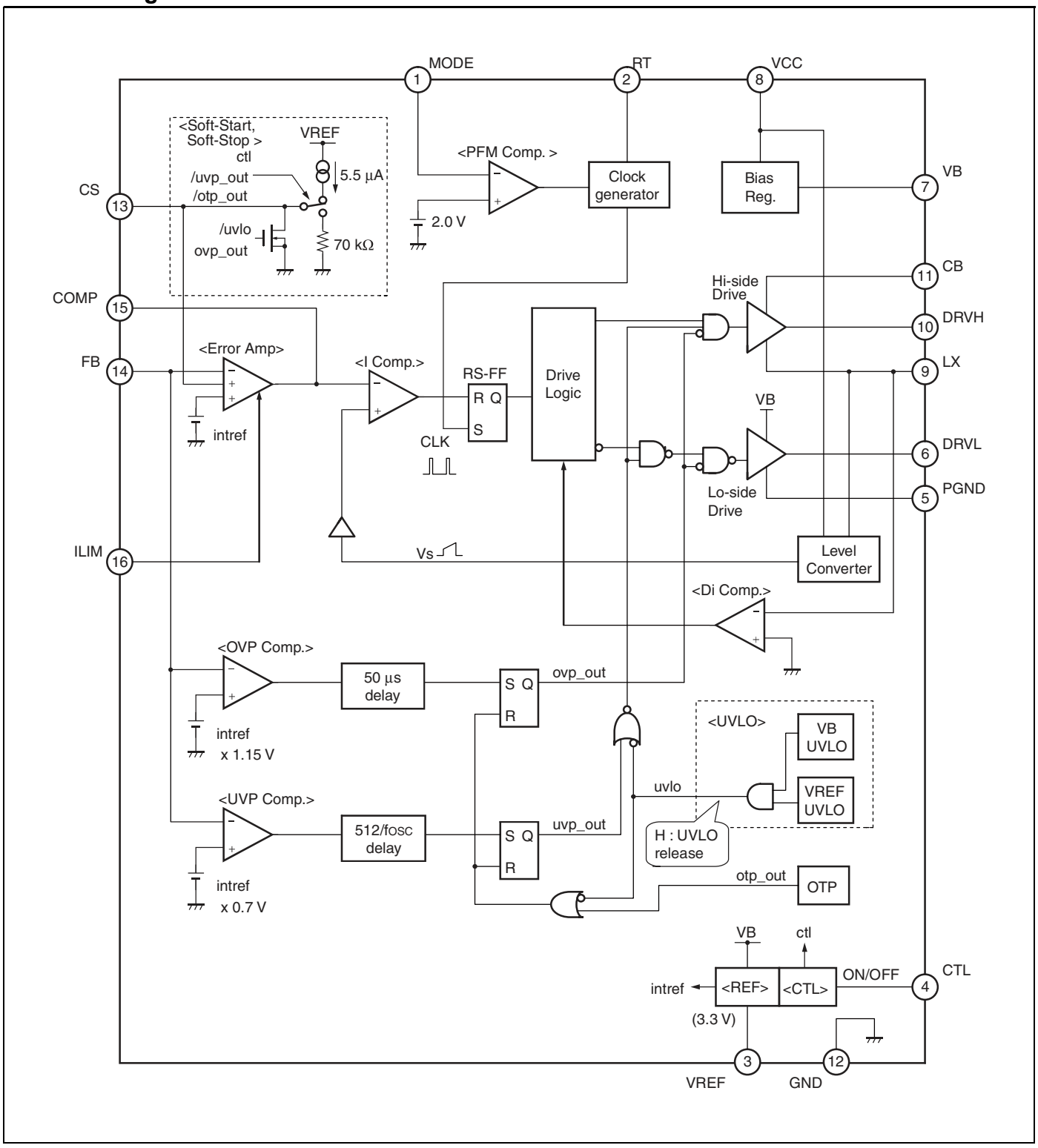


(STB016)

2. Pin Descriptions

Pin No.	Pin Name	I/O	Description
1	MODE	I	PFM/PWM switch pin. It becomes fixed PWM operation with the VREF connection, and it becomes PFM/PWM operation with the GND connection.
2	RT	—	Resistor connection pin for oscillation frequency setting.
3	VREF	O	Reference voltage output pin.
4	CTL	I	Control pin.
5	PGND	—	Ground pin.
6	DRVL	O	Output pin for external low-side FET gate drive.
7	VB	O	Bias voltage output pin.
8	VCC	—	Power supply pin for reference voltage and control circuit.
9	LX	—	Inductor and external high-side FET source connection pin.
10	DRVH	O	Output pin for external high-side FET gate drive.
11	CB	—	The connection pin for boot strap capacitor.
12	GND	—	Ground pin.
13	CS	I	Soft-start time setting capacitor connection pin.
14	FB	I	Error amplifier inverted input pin.
15	COMP	O	Error amplifier (Error Amp) output pin.
16	ILIM	I	Over current detection level setting voltage input pin.

3. **Block Diagram**



4. Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating		Unit
			Min	Max	
Power supply voltage	V_{VCC}	VCC pin	—	27	V
CB pin input voltage	V_{CB}	CB pin	—	32	V
LX pin input voltage	V_{LX}	LX pin	—	27	V
Voltage between CB and LX	V_{CBLX}	—	—	7	V
Control input voltage	V_I	CTL pin	—	27	V
Input voltage	V_{FB}	FB pin	—	V_{VREF} + 0.3	V
	V_{ILIM}	ILIM pin	—	V_{VREF} + 0.3	V
	V_{CS}	CS pin	—	V_{VREF} + 0.3	V
	V_{MODE}	MODE pin	—	V_{VB} + 0.3	V
Output current	I_{OUT}	DC, DRVL pin, DRVH pin	—	60	mA
Power dissipation	P_D	Ta ≤ + 25°C	—	1237	mW
Storage temperature	T_{STG}	—	−55	+ 150	°C

WARNING: Semiconductor devices can be permanently damaged by application of stress (voltage, current, temperature, etc.) in excess of absolute maximum ratings. Do not exceed these ratings.

5. Recommended Operating Conditions

Parameter	Symbol	Condition	Value			Unit
			Min	Typ	Max	
Power supply voltage	V_{VCC}	—	4.5	—	25.0	V
CB pin input voltage	V_{CB}	—	—	—	30	V
Reference voltage output current	I_{VREF}	—	−100	—	—	µA
Bias output current	I_{VB}	—	−1	—	—	mA
CTL pin input voltage	V_I	CTL pin	0	—	25	V
Input voltage	V_{FB}	FB pin	0	—	V_{VREF}	V
	V_{ILIM}	ILIM pin	0.3	—	1.94	V
	V_{CS}	CS pin	0	—	V_{VREF}	V
	V_{MODE}	MODE pin	0	—	V_{VREF}	V
Peak output current	I_{OUT}	DRVH pin, DRVL pin Duty ≤ 5% ($t = 1 / f_{OSC} \times$ Duty)	−1200	—	+ 1200	mA
Operation frequency range	f_{OSC}	—	100	500	1000	kHz
Timing resistor	R_{RT}	—	—	47	—	kΩ
Soft start capacitor	C_{CS}	—	0.0075	0.0180	—	µF
CB pin capacitor	C_{CB}	—	—	0.1	1.0	µF
Reference voltage output capacitor	C_{VREF}	—	—	0.1	1.0	µF
Bias voltage output capacitor	C_{VB}	—	—	1.0	10	µF
Operating ambient temperature	Ta	—	−30	+ 25	+ 85	°C

WARNING: The recommended operating conditions are required in order to ensure the normal operation of the semiconductor device. All of the device's electrical characteristics are warranted when the device is operated within these ranges.

Always use semiconductor devices within their recommended operating condition ranges.
Operation outside these ranges may adversely affect reliability and could result in device failure.
No warranty is made with respect to uses, operating conditions, or combinations not represented on the data sheet. Users considering application outside the listed conditions are advised to contact their representatives beforehand.

6. Electrical Characteristics

(Ta = +25°C, VCC pin = 15 V, CTL pin = 5 V, VREF pin = 0 A, VB pin = 0 A)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Reference Voltage Block [REF]	Output voltage	V_{VREF}	3	—	3.24	3.30	3.36	V
	Input stability	VREF LINE	3	VCC pin = 4.5 V to 25 V	—	1	10	mV
	Load stability	VREF LOAD	3	VREF pin = 0 A to −100 µA	—	1	10	mV
	Short-circuit output current	VREF IOS	3	VREF pin = 0 V	−14.5	−10.0	−7.5	mA
Bias Voltage Block [VB Reg.]	Output voltage	V_{VB}	7	—	4.85	5.00	5.15	V
	Input stability	VB LINE	7	VCC pin = 6 V to 25 V	—	10	100	mV
	Load stability	VB LOAD	7	VB pin = 0 A to −1 mA	—	10	100	mV
	Short-circuit output current	VB IOS	7	VB pin = 0 V	−130	−90	−65	mA
Under voltage Lockout Protection Circuit Block [UVLO]	Threshold voltage	V_{TLH1}	7	VB pin	4.0	4.2	4.4	V
		V_{THL1}	7	VB pin	3.4	3.6	3.8	V
	Hysteresis width	V_{H1}	7	VB pin	—	0.6*	—	V
	Threshold voltage	V_{TLH2}	3	VREF pin	2.7	2.9	3.1	V
		V_{THL2}	3	VREF pin	2.5	2.7	2.9	V
	Hysteresis width	V_{H2}	3	VREF pin	—	0.2*	—	V
Soft-start / Soft-stop Block [Soft-Start, Soft-Stop]	Charge current	I_{CS}	13	CTL pin = 5 V, CS pin = 0 V	−7.9	−5.5	−4.2	µA
	Soft-start end voltage	V_{CS}	13	CTL pin = 5 V	2.2	2.4	2.6	V
	Electrical discharge resistance at soft-stop	R_{DISCG}	13	CTL pin = 0 V, CS pin = 0.5 V	49	70	91	kΩ
	Soft-stop end voltage	V_{DISCG}	13	CTL pin = 0 V	—	0.1*	—	V
Clock Generator Block [OSC]	Oscillation frequency	f_{OSC}	2	RT pin = 47 kΩ	450	500	550	kHz
	Oscillation frequency when under voltage is detected	f_{SHORT}	2	RT pin = 47 kΩ	—	62.5	—	kHz
	Frequency Temperature variation	df/dT	2	Ta = −30°C to + 85°C	—	3*	—	%

(Ta = +25°C, VCC pin = 15 V, CTL pin = 5 V, VREF pin = 0 A, VB pin = 0 A)

Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Error Amp Block [Error Amp]	Threshold voltage	EV_{TH}	14	—	0.693	0.700	0.707	V
		EV_{THT}	14	Ta = −30°C to +85°C	0.689*	0.700*	0.711*	V
	Input current	I_{FB}	14	FB pin = 0 V	−0.1	0	+0.1	µA
	Output current	I_{SOURCE}	15	FB pin = 0 V, COMP pin = 1 V	−390	−300	−210	µA
		I_{SINK}	15	FB pin = VREF pin, COMP pin = 1 V	8.4	12.0	16.8	mA
	Output clamp voltage	V_{ILIM}	15	FB pin = 0 V, ILIM pin = 1.5 V	1.35	1.50	1.65	V
	ILIM pin input current	I_{ILIM}	16	FB pin = 0 V, ILIM pin = 1.5 V	−1	0	+1	µA
Over-voltage Protection Circuit Block [OVP Comp.]	Over-voltage detecting voltage	V_{OVP}	14	FB pin	0.776	0.805	0.835	V
	Over-voltage detection time	t_{OVP}	14	—	49	70	91	µs
Under-voltage Protection Circuit Block [UVP Comp.]	Under-voltage detecting voltage	V_{UVP}	14	FB pin	0.450	0.490	0.531	V
	Under-voltage detection time	t_{UVP}	14	—	—	512/ f_{OSC}	—	s
Over-temperature Protection Circuit Block [OTP]	Detection temperature	T_{OTPH}	—	Junction temperature	—	+160*	—	°C
		T_{OTPL}	—	Junction temperature	—	+135*	—	°C
PFM Control Circuit Block [MODE]	Synchronous rectification stop voltage	V_{THLX}	9	LX pin	—	0*	—	mV
	PFM/PWM mode condition	V_{PFM}	1	MODE pin	0	—	1.4	V
	Fixed PWM mode condition	V_{PWM}	1	MODE pin	2.2	—	V_{VREF}	V
	MODE pin input current	I_{MODE}	1	MODE pin = 0 V	−1	0	+1	µA

(Ta = +25°C, VCC pin = 15 V, CTL pin = 5 V, VREF pin = 0 A, VB pin = 0 A)

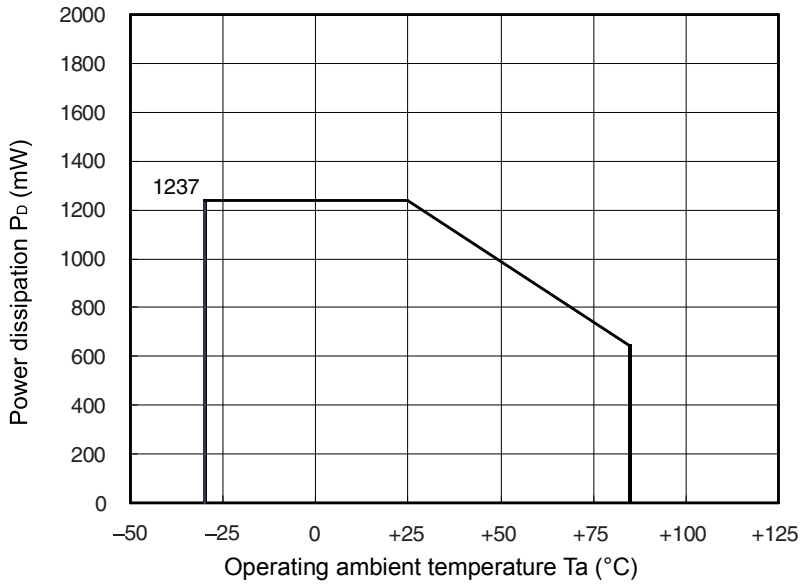
Parameter		Symbol	Pin No.	Condition	Value			Unit
					Min	Typ	Max	
Output Block [DRV]	High-side output on-resistance	R_{ON_MH}	10	DRVH pin = −100 mA	—	4	7	Ω
		R_{ON_ML}	10	DRVH pin = 100 mA	—	1.0	3.5	Ω
	Low-side output on-resistance	R_{ON_SH}	6	DRVL pin = −100 mA	—	4	7	Ω
		R_{ON_SL}	6	DRVL pin = 100 mA	—	0.75	1.70	Ω
	Output source current	I_{SOURCE}	10,6	LX pin = 0 V, CB pin = 5 V DRVH, DRVL pins = 2.5 V Duty ≤ 5%	—	−0.5*	—	A
	Output sink current	I_{SINK}	10	LX pin = 0 V, CB pin = 5 V DRVH pin = 2.5 V Duty ≤ 5%	—	0.9*	—	A
			6	LX pin = 0 V, CB pin = 5 V DRVL pin = 2.5 V Duty ≤ 5%	—	1.2*	—	A
	Minimum on time	t_{ON}	10	COMP pin = 1 V	—	250*	—	ns
	Maximum on-duty	D_{MAX}	10	—	75	80	—	%
	Dead time	t_D	10, 6	LX pin = 0 V, CB pin = 5 V	—	60	—	ns
Level Converter Block [LVCNV]	Maximum current sense voltage	V_{RANGE}	9	VCC pin−LX pin	—	220*	—	mV
	Voltage conversion gain	A_{LV}	9	—	5.4	6.8	8.2	V/V
	Offset voltage at voltage conversion	V_{IO}	9	—	—	300	—	mV
	Slope compensation inclination	SLOPE	9	—	—	2*	—	V/V
	LX pin input current	I_{LX}	9	LX pin = VCC pin	320	420	600	µA
Control Block [CTL]	ON condition	V_{ON}	4	CTL pin	2	—	25	V
	OFF condition	V_{OFF}	4	CTL pin	0	—	0.8	V
	Hysteresis width	V_H	4	CTL pin	—	0.4*	—	V
	Input current	I_{CTLH}	4	CTL pin = 5 V	—	25	40	µA
		I_{CTLL}	4	CTL pin = 0 V	—	0	1	µA
General	Standby current	I_{CCS}	8	CTL pin = 0 V	—	0	10	µA
	Power-supply current	I_{CC}	8	LX pin = 0 V, FB pin = 1.0 V MODE pin = VREF pin	—	1.9	2.7	mA

* : This value isn't be specified. This should be used as a reference to support designing the circuits.

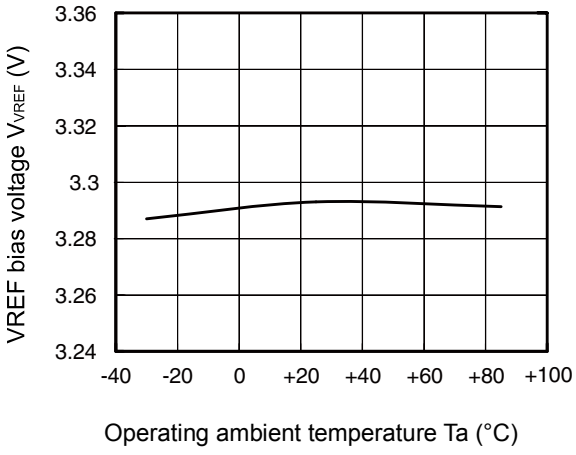
7. Typical Characteristics

■ Power dissipation

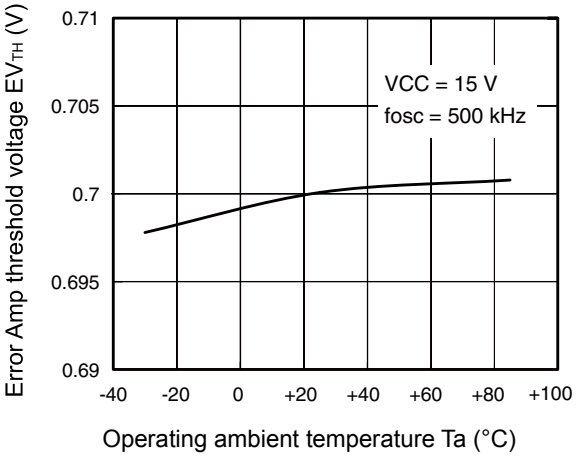
Power dissipation vs. Operating ambient temperature



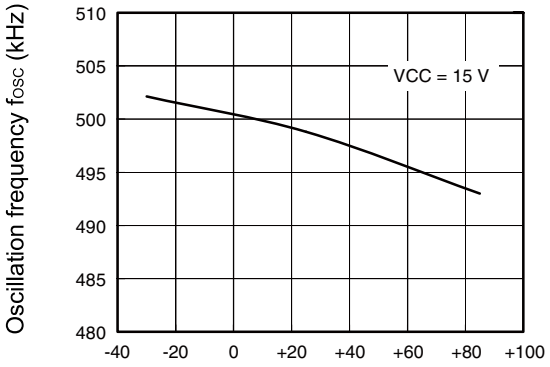
VREF bias voltage vs.
Operating ambient temperature



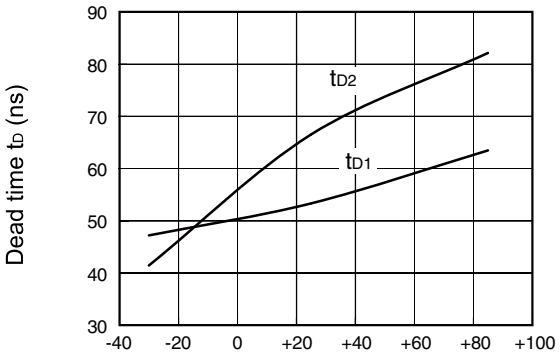
Error Amp threshold voltage vs.
Operating ambient temperature



Oscillation frequency vs.
Operating ambient temperature

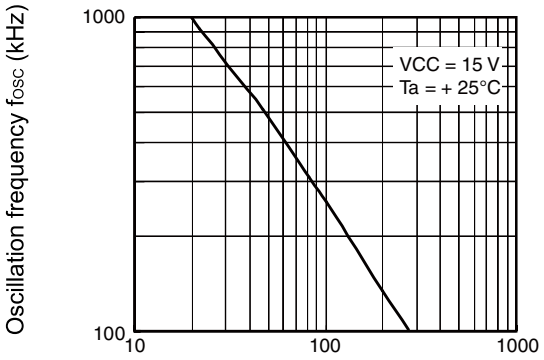


Dead time vs.
Operating ambient temperature

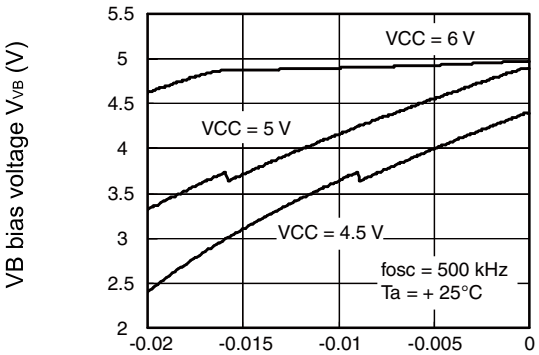


t_{D1} : period from DRVL off to DRVH on
t_{D2} : period from DRVH off to DRVL on

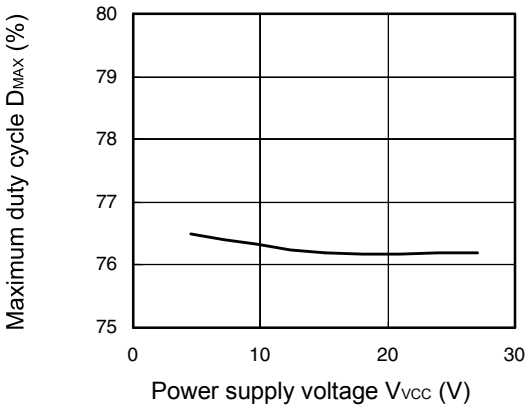
Oscillation frequency vs. Timing resistor value



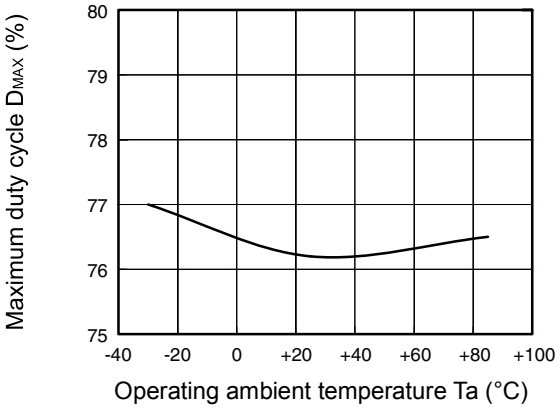
VB bias voltage vs. VB bias output current



Maximum duty cycle vs. Power supply voltage



Maximum duty cycle vs.
Operating ambient temperature



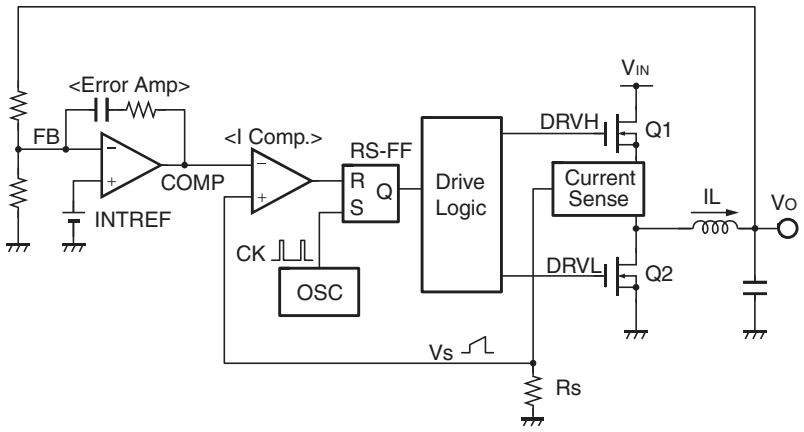
8. Function Description

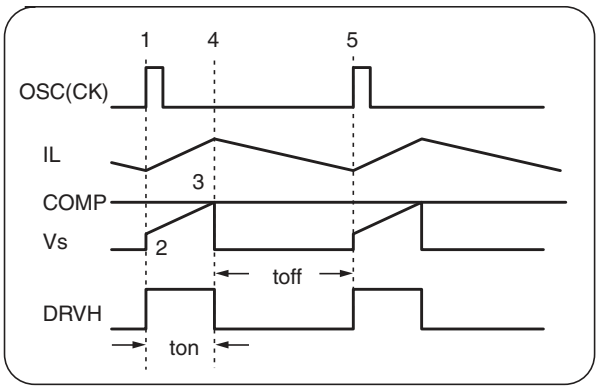
8.1 Current Mode

It uses the current waveform from the switching (Q1) as a control waveform to control the output voltage, as described below:

1. The clock (CK) from the internal clock generator (OSC) sets RS-FF and turns on the high-side FET.
2. Turning on the high-side FET causes the inductor current (IL) rise. Generate Vs that converts this current into the voltage.
3. The current comparator (I Comp.) compares this Vs with the output (COMP) from the error amplifier (Error Amp) that is negative-feedback from the output voltage (Vo).
4. When I Comp. detects that Vs exceeds COMP, it resets RS-FF and turns off high side FET.
5. The clock (CK) from the clock generator (OSC) turns on the high-side FET again.

Thus, switching is repeated.
Operate so that the FB electrical potential may become INTREF electrical potential, and stabilize the output voltage as a feedback control.





8.1.1 Reference Voltage Block (REF)

The reference voltage circuit (REF) generates a temperature-compensated reference voltage (3.3[V] Typ) using the voltage supplied from the VCC pin. The voltage is used as the reference voltage for the IC's internal circuit. The reference voltage can be used to supply a load current of up to 100 µA to an external device through the VREF pin.

8.1.2 Bias Voltage Block (VB Reg.)

Bias Voltage Block (VB Reg.) generates the reference voltage used for IC's internal circuit, using the voltage supplied from the VCC pin. The reference voltage is a temperature-compensated stable voltage (5[V] Typ) to supply a current of up to 100 mA through the VB pin.

8.1.3 Under Voltage Lockout Protection Circuit Block (UVLO)

The circuit protects against IC malfunction and system destruction/deterioration in a transitional state or a momentary drop when a bias voltage (VB) or an internal reference voltage (VREF) starts. It detects a voltage drop at the VB pin or the VREF pin and stops IC operation. When voltages at the VB pin and the VREF pin exceed the threshold voltage of the under voltage lockout protection circuit, the system is restored.

8.1.4 Soft-start/Soft-stop Block (Soft-Start, Soft-Stop)

Soft-start

It protects a rush current or an output voltage (V_O) from overshooting at the output start. Since the lamp voltage generated by charging the capacitor connecting to the CS pin is used for the reference voltage of the error amplifier (Error Amp), it can set the soft-start time independent of a load of the output (V_O). When the IC starts with “H” level of the CTL pin, the capacitor at the CS pin (CS) starts to be charged at 5.5 µA. The output voltage (V_O) during the soft-start period rises in proportion to the voltage at the CS pin generated by charging the capacitor at the CS pin.

During the soft-start with, 0.8 V > voltage at CS pin, operations are as follows:

- Fixed PWM operation only (fixed PWM even if MODE pin is set to “L”)
- Over-voltage protection function and under-voltage protection function are invalid.

Soft-stop

It discharges electrical charges stored in a smoothing capacitor at output stop. Setting the CTL pin to “L” level starts the soft-stop function independent of a load of output (Vo). Since the capacitor connecting to the CS pin starts to discharge through the IC-built-in soft-stop discharging resistance (70[kΩ] Typ) when the CTL pin sets at “L” level enters its lamp voltage into the error amplifier (Error Amp), the soft-stop time can be set independent of a load of output (V_O). When discharging causes the voltage at the CS pin to drop below 100 mV (Typ), the IC shuts down and changes to the stand-by state. In addition, the soft-stop function operates after the under voltage protection circuit block (UVP Comp.) is latched or after the over-temperature protection circuit block (OTP) detects over-temperature.

During the soft-stop with, 0.8 V > voltage at CS pin, operations are as follows:

- Fixed PWM operation only (fixed PWM even if MODE pin is set to “L”)
- Over-voltage protection function and under-voltage protection function are invalid.

8.1.5 Clock Generator Block (OSC)

The clock generator has the built-in oscillation frequency setting capacitor and generates a clock by connecting the oscillation frequency setting resistor to the RT pin.

8.1.6 Error Amp Block (Error Amp)

The error amplifiers (Error Amp) detect the output voltage from the DC/DC converter and output to the current comparators (I Comp.). The output voltage setting resistor externally connected to FB pin allows an arbitrary output voltage to be set.
In addition, since an external resistor and an external capacitor serially connected between COMP and FB pins allow an arbitrary loop gain to be set, it is possible for the system to compensate a phase stably.

8.1.7 Over Current Detection (Protection) Block (ILIM)

It is the current detection circuit to restrict an output current (I_O). The over current detection block (ILIM) compares an output waveform of the level converter (see “(12) Level Converter Block (LVCNV)”) with the ILIM pin voltage in every cycle. As a load resistance (R_O) drops, a load current (I_O) increases. Therefore, the output waveform of the level converter exceeds the ILIM pin voltage At this time, the output current can be restricted by turning off FET on the high-side and suppressing a peak value of the inductor current.
As a result, the output voltage (V_O) should drop.
Furthermore, if the output voltage drops and the electrical potential at the FB pin drops below 0.3 V, the oscillation frequency (f_{OSC}) drops to 1/8.

8.1.8 Over-voltage Protection Circuit Block (OVP Comp.)

The circuit protects a device connecting to the output when the output voltage (V_O) rises.
It compares 1.15 times (Typ) of the internal reference voltage (INTREF) (0.7 V) that is non-inverting-entered into the error amplifier with the feed-back voltage that is inverting-entered into the error amplifier and if it detects the state where the latter is higher than the former by 50 µs (Typ). It stops the voltage output by setting the RS latch, setting the DRVH pin to “L” level, setting the DRVL pin to “H” level, turning off the high side FET and turning on the low-side FET.
The conditions below cancel the protection function:

- Setting CTL to “L”.
- Setting the power supply voltage below the UVLO threshold voltage (V_{THL1} and V_{THL2}).

8.1.9 Under-voltage Protection Circuit Block (UVP Comp.)

It protects a device connecting to the output by stopping the output when the output voltage (V_O) drops.
It compares 0.7 times (Typ) of the internal reference voltage (INTREF) (0.7 V) that is non-inverting-entered into the error amplifier with the feed-back voltage that is inverting-entered into the error amplifier and if it detects the state where the latter is lower than the former by 512/fosc [s](Typ), it stops the voltage output by setting the RS latch.
The conditions below cancel the protection function:

- Setting CTL to “L”.
- Setting the power supply voltage below the UVLO threshold voltage (V_{THL1} and V_{THL2}).

8.1.10 Over Temperature Protection Circuit Block (OTP)

The circuit protects an IC from heat-destruction. If the temperature at the joint part reaches +160°C, the circuit stops the voltage output by discharging the capacitor connecting to the CS pin through the soft-stop discharging resistance (70[kΩ] Typ) in the IC.
In addition, if the temperature at the joint part drops to +135°C, the output restarts again through the soft-start function.
Therefore, make sure to design the DC/DC power supply system so that the over temperature protection does not start frequently.

8.1.11 PFM Control Circuit Block (MODE)

It sets the control mode of the IC and makes control at automatic PFM/PWM switching.

MODE Pin Connection	Control Mode	Features
“L” (GND)	Automatic PFM/PWM switching	Highly-efficient at light load
“H” (VREF)	Fixed PWM	Stable oscillation frequency Stable switching ripple voltage Excellent in rapid load change characteristic at heavy load to light load

Automatic PFM/PWM switching mode operation

It compares the LX pin voltage with GND electrical potential at Di Comp. In the comparison, the negative voltage at the LX pin causes low-side FET to set on, positive voltage causes it to set off (Di Comp. method). As a result, the method restricts the back flow of the inductor current at a light load and makes the switching of the inductor current discontinuous (DCM). Such an operation allows the oscillation frequency to drop, resulting in high efficiency at a light load.

8.1.12 Output Block (DRV)

The output circuit is configured in CMOS type for both of the high-side and the low-side, allowing the external N-ch MOS FET to drive.

8.1.13 Level Converter Block (LVCNV)

The circuit detects and converts the current when the high-side FET turns on. It converts the voltage waveform between drain side (VCC pin voltage) and the source side (LX pin voltage) on the high-side FET into the voltage waveform for GND reference.

8.1.14 Control Block (CTL)

The circuit controls on/off of the output from the IC.

Control function table

CTL	DC/DC Converter	Remarks
L	OFF	Standby
H	ON	—

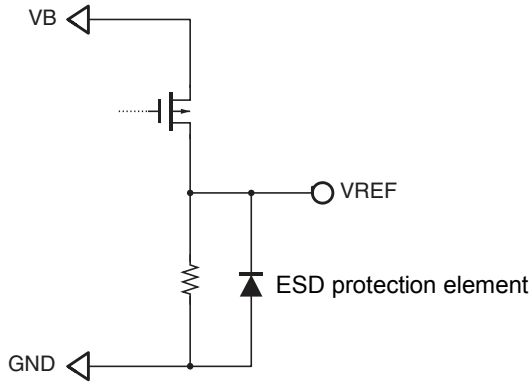
9. Protection Function Table

The following table shows the state of each pins when each protection function operates.

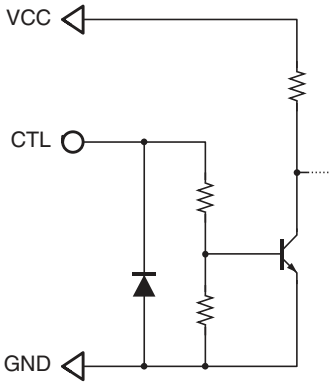
Protection Function	Detection Condition	Output of Each Pin After Detection				DC/DC Output Dropping Operation
		VREF	VB	DRVH	DRVL	
Under Voltage Lock Out (UVLO)	VB< 3.6 V VREF< 2.7 V	< 2.7 V	< 3.6V	L	L	Self-discharge by load
Under Voltage Protection (UVP)	FB< 0.49V	3.3 V	5 V	L	L	Electrical discharge by soft-stop function
Over Voltage Protection (OVP)	FB > 0.805V	3.3 V	5 V	L	H	0 V clamping
Over current protection (ILIM)	COMP > ILIM	3.3 V	5 V	switching	switching	The output voltage is dropping to keep constant output current.
Over Temperature Protection (OTP)	Tj > ＋160°C	3.3 V	5 V	L	L	Electrical discharge by soft-stop function
CONTROL (CTL)	CTL : H→L (CS > 0.1 V)	3.3 V	5 V	L	L	

10. I/O Pin Equivalent Circuit Diagram

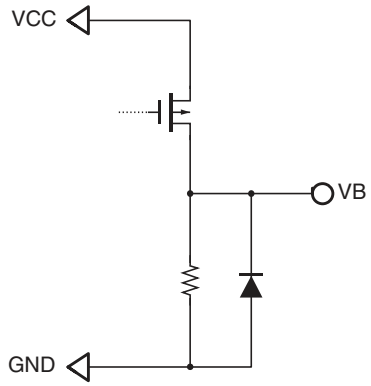
VREF pin



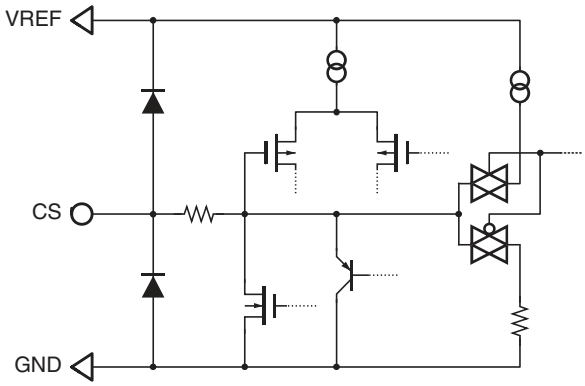
CTL pin



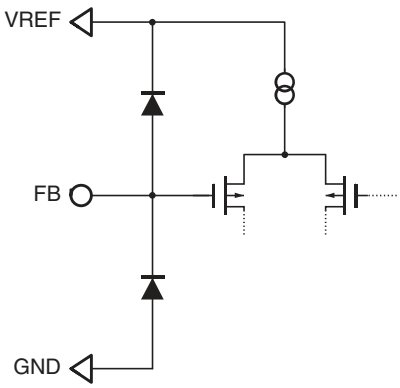
VB pin



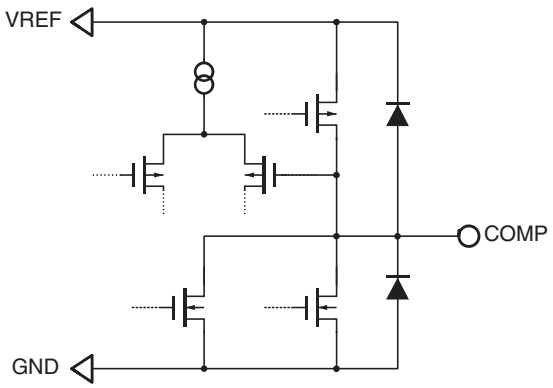
CS pin



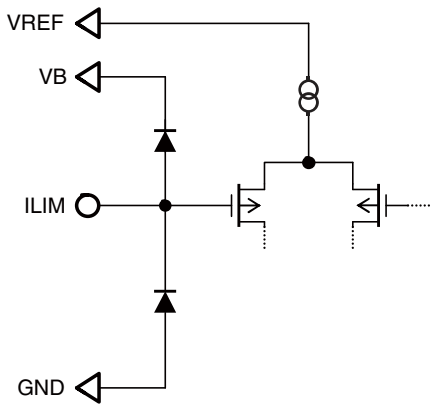
FB pin



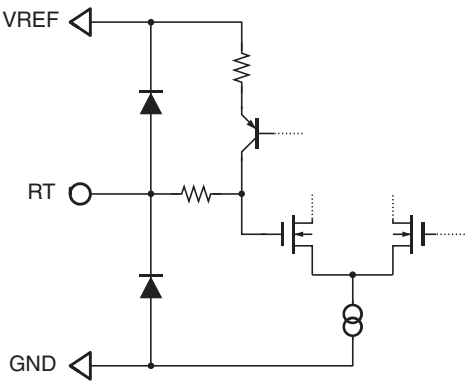
COMP pin



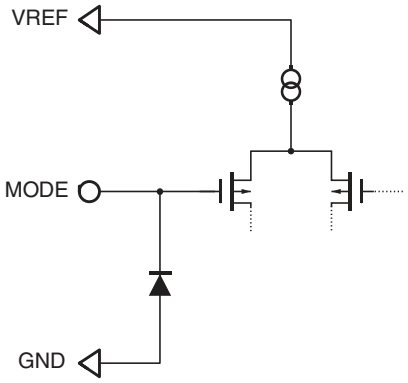
ILIM pin



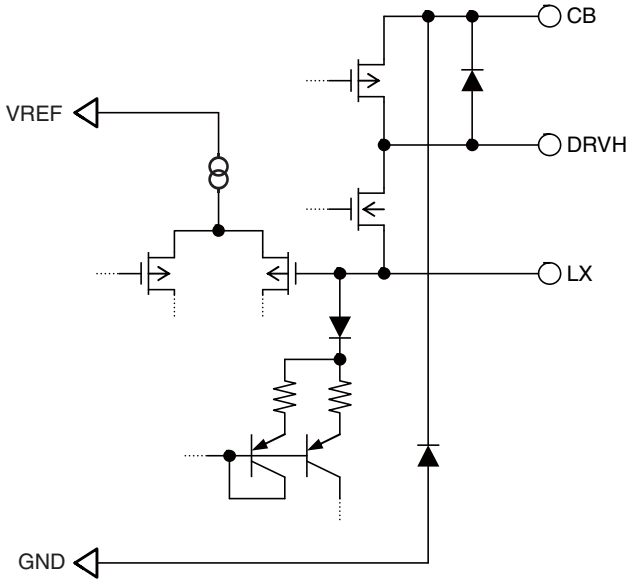
RT pin



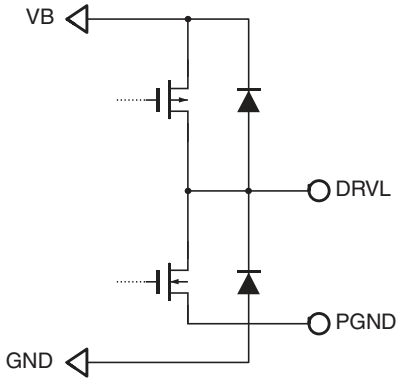
MODE pin



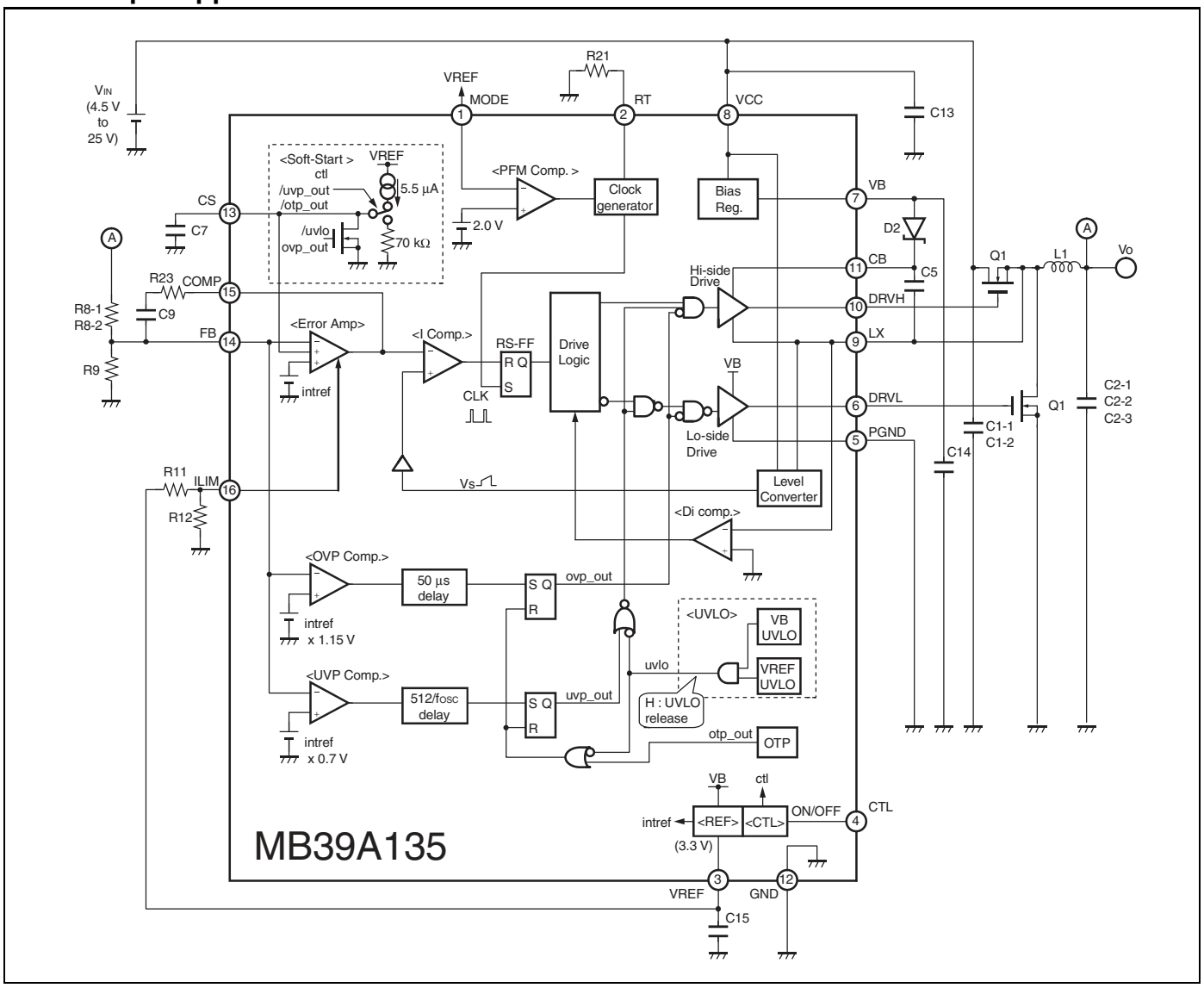
CB, DRVH, LX pins



DRVL pin



11. Example Application Circuit



12. Parts List

Component	Item	Specification	Vendor	Package	Parts Name	Remark
Q1	N-ch FET	VDS = 30 V, ID = 8 A, Ron = 21 mΩ	RENESAS	SO-8	μPA2755	Dual type (2 elements)
D2	Diode	VF = 0.35 V at IF = 0.2 A	Onsemi	SOD-523	BAT54XV2T1G	
L1	Inductor	1.5 μH (6.2 mΩ, 8.9 A)	TDK	—	VLF10040T-1R5N	
C1-1 C1-2	Ceramic capacitor Ceramic capacitor	22 μF (25 V) 22 μF (25 V)	TDK TDK	3225 3225	C3225JB1E226M C3225JB1E226M	2 capacitors in parallel
C2-1 C2-2 C2-3	Ceramic capacitor Ceramic capacitor Ceramic capacitor	22 μF (10 V) 22 μF (10 V) 22 μF (10 V)	TDK TDK TDK	3216 3216 3216	C3216JB1A226M C3216JB1A226M C3216JB1A226M	3 capacitors in parallel
C5	Ceramic capacitor	0.1 μF (50 V)	TDK	1608	C1608JB1H104K	
C7	Ceramic capacitor	0.022 μF (50 V)	TDK	1608	C1608JB1H223K	
C9	Ceramic capacitor	820 pF (50 V)	TDK	1608	C1608CH1H821J	
C13	Ceramic capacitor	0.01 μF (50 V)	TDK	1608	C1608JB1H103K	
C14	Ceramic capacitor	1.0 μF (16 V)	TDK	1608	C1608JB1C105K	
C15	Ceramic capacitor	0.1 μF (50 V)	TDK	1608	C1608JB1H104K	
R8-1 R8-2	Resistor Resistor	1.6 kΩ 9.1 kΩ	SSM SSM	1608 1608	RR0816P162D RR0816P912D	2 resistors in serial
R9	Resistor	15 kΩ	SSM	1608	RR0816P153D	
R11	Resistor	56 kΩ	SSM	1608	RR0816P563D	
R12	Resistor	56 kΩ	SSM	1608	RR0816P463D	
R21	Resistor	82 kΩ	SSM	1608	RR0816P823D	
R23	Resistor	22 kΩ	SSM	1608	RR0816P223D	

RENESAS : Renesas Electronics Corporation
Onsemi : ON Semiconductor
TDK : TDK Corporation
SSM : SUSUMU Co.,Ltd.

13. Application Note

13.1 Setting Method for PFM/PWM and Fixed PWM Modes

For the setting method for each mode, see “PFM Control Circuit Block (MODE)”.

13.2 Cautions at PFM/PWM Mode

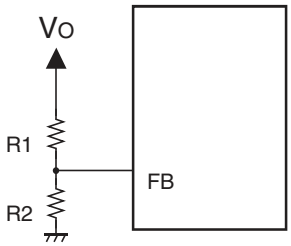
If a load current drops rapidly because of rapid load change and others, it tends to take a lot of time to restore overshooting of an output voltage.
As a result, the over-voltage protection may operate.
In this case, solution are possible by the addition of the load resistance of value to be able to restore the output voltage in the over-voltage detection time.

13.3 Setting Method of Output Voltage

Set it by adjusting the output voltage setting zero-power resistance ratio.

$$V_O = \frac{R1 + R2}{R2} \times 0.7$$

V_O : Output setting voltage [V]
R1, R2 : Output setting resistor value [Ω]



Make sure that the setting does not exceed the maximum on-duty.
Calculate the on-duty by the following formula.

$$D_{MAX\_Min} = \frac{V_O + R_{ON\_Sync} \times I_{OMAX}}{V_{IN} - R_{ON\_Main} \times I_{OMAX} + R_{ON\_Sync} \times I_{OMAX}}$$

D_{MAX_Min} : Minimum value of the maximum on-duty cycle
V_{IN} : Power supply voltage of switching system [V]
V_O : Output setting voltage [V]
R_{ON_Main} : High-side FET ON resistance [Ω]
R_{ON_Sync} : Low-side FET ON resistance [Ω]
I_{OMAX} : Maximum load current [A]

13.4 Oscillation Frequency Setting Method

Set it by adjusting the RT pin resistor value.

$$f_{OSC} = \frac{1.09}{R_{RT} \times 40 \times 10^{-12} + 300 \times 10^{-9}}$$

R_{RT} : RT resistor value [Ω]
f_{OSC} : Oscillation frequency [Hz]

The oscillation frequency must set for on-time (t_{ON}) to become 300 ns or more.
Calculate the on-time by the following formula.

$$t_{ON} = \frac{V_O}{V_{IN} \times f_{OSC}}$$

t_{ON} : On-time [s]
V_{IN} : Power supply voltage of switching system [V]
V_O : Output setting voltage [V]
f_{OSC} : Oscillation frequency [Hz]

13.5 Setting Method of Soft-start Time

Calculate the soft-start time by the following formula.

$$t_S = 1.4 \times 10^5 \times C_{CS}$$

ts : Soft-start time [s] (Time to becoming output 100%)
C_{CS} : CS pin capacitor value [F]

Calculate delay time until the soft-start beginning by the following formula:

$$t_{d1} = 30 \times C_{VB} + 290 \times C_{VREF} + 1.455 \times 10^4 \times C_{CS}$$

t_{d1} : Delay time including VB voltage and VREF voltage starts [s]
C_{CS} : CS pin capacitor value [F]
C_{VB} : VB pin capacitor value [F]
C_{VREF} : VREF pin capacitor value [F] (0.1 µF Typ)

Calculate the discharge time at the soft-stop by the following formula:

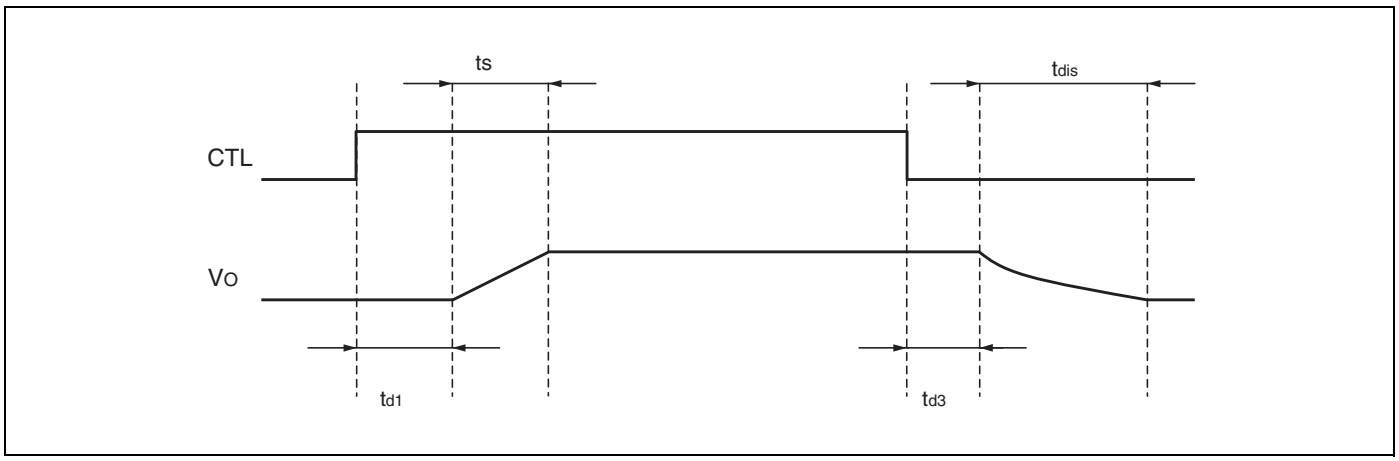
$$t_{dis} = 1.44 \times 10^5 \times C_{CS}$$

t_{dis} : Discharge time [s]
C_{CS} : CS pin capacitor value [F]

In addition, calculate the delay time to the discharge starting by the following formula:

$$t_{d3} = 7.87 \times 10^4 \times C_{CS}$$

t_{d3} : Delay time until discharge start [s]
C_{CS} : CS pin capacitor value [F]



13.6 Setting Method of Over Current Detection Value

It is possible to set it by adjusting the over current detection setting zero-power resistance ratio when over current detection (I_{LIM}) is used.

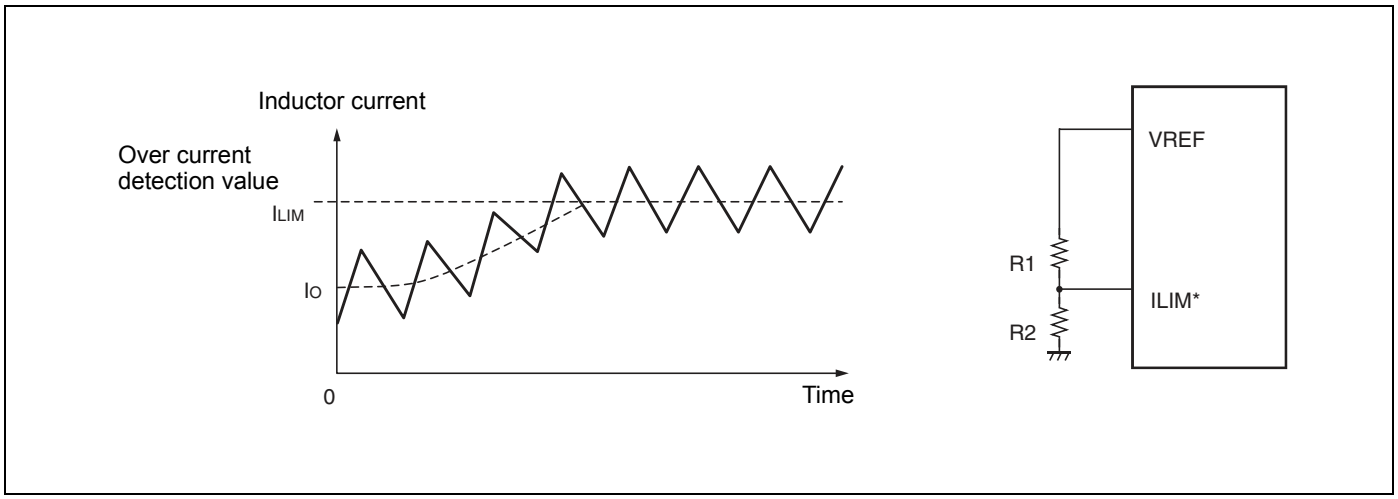
Calculate the over current detection setting resistor value by the following formula.

$$I_{LIM} = \frac{\frac{3.3 \times R2}{R1 + R2} - 0.3}{6.8 \times R_{ON}} + \frac{V_{IN} - V_O}{L} \times \left(200 \times 10^{-9} - \frac{V_O}{2 \times f_{OSC} \times V_{IN}}\right)$$

$$200 \times 10^3 \geq R1 + R2 \geq 30 \times 10^3$$

I_{LIM}	: Over current detection value [A]
R1, R2	: I_{LIM} setting resistor value [Ω]*
L	: Inductor value [H]
V_{IN}	: Power supply voltage of switching system [V]
V_O	: Output setting voltage [V]
f_{OSC}	: Oscillation frequency [Hz]
R_{ON}	: High-side FET ON resistance [Ω]

* : Since the over current detection value depends on the on-resistance of FET, the over current detection setting resistor value ratio should be adjusted in consideration of the temperature characteristics of the on-resistance.
When the temperature at the FET joint part rises by +100°C, the on-resistance of FET increases to about 1.5 times.



* : If the over current detection function is not used, connect the ILIM pin to the VREF pin.

13.7 Selection of Smoothing Inductor

The inductor value selects the value that the ripple current peak-to-peak value of the inductor becomes 50% or less of the maximum load current as a rough standard. Calculate the inductor value in this case by the following formula.

$$L \geq \frac{V_{IN}-V_O}{LOR \times I_{OMAX}} \times \frac{V_O}{V_{IN} \times f_{OSC}}$$

L	: Inductor value [H]
I_{OMAX}	: Maximum load current [A]
LOR	: Ripple current peak-to-peak value of Maximum load current ratio (=0.5)
V_{IN}	: Power supply voltage of switching system [V]
V_O	: Output setting voltage [V]
f_{OSC}	: Oscillation frequency [Hz]

An inductor ripple current value limited on the principle of operation is necessary for this device. However, when it uses the high-side FET of the low Ron resistance, the switching ripple voltage become small, and the ripple current value be insufficient. This should be solved by the oscillation frequency or reducing the inductor value.
Select the one of the inductor value that meets a requirement listed below.

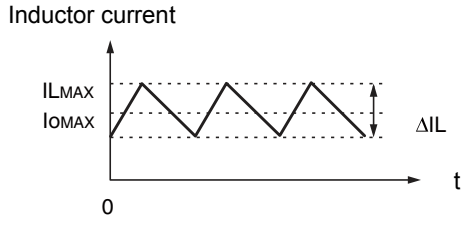
$$L \leq \frac{V_{IN}-V_O}{\Delta V_{RON}} \times \frac{V_O}{V_{IN} \times f_{OSC}} \times R_{ON}$$

L	: Inductor value [H]
V_{IN}	: Power supply voltage of switching system [V]
V_O	: Output setting voltage [V]
f_{OSC}	: Oscillation frequency [Hz]
ΔV_{RON}	: Ripple voltage [V] (20 mV or more is recommended)
R_{ON}	: High-side FET ON resistance [Ω]

It is necessary to calculate the maximum current value that flows to the inductor to judge whether the electric current that flows to the inductor is a rated value or less. Calculate the maximum current value of the inductor by the following formula.

$$I_{LMAX} \geq I_{OMAX} + \frac{\Delta IL}{2}, \quad \Delta IL = \frac{V_{IN}-V_O}{L} \times \frac{V_O}{V_{IN} \times f_{OSC}}$$

I_{LMAX}	: Maximum current value of inductor [A]
I_{OMAX}	: Maximum load current [A]
ΔIL	: Ripple current peak-to-peak value of inductor [A]
L	: Inductor value [H]
V_{IN}	: Power supply voltage of switching system [V]
V_O	: Output setting voltage [V]
f_{OSC}	: Oscillation frequency [Hz]



13.8 Selection of SWFET

The switching ripple voltage generated between drain and sources on high-side FET is necessary for this device operation. Select the one of the SWFET of on-resistance that satisfies the following formula.

$$R_{ON\_Main} \geq \frac{\Delta V_{RON\_Main}}{\Delta IL}, \quad R_{ON\_Main} \leq \frac{V_{RONMAX}}{I_{LIM} + \frac{\Delta IL}{2}}$$

R_{ON_Main} : High-side FET ON resistance [Ω]
ΔIL : Ripple current peak-to-peak value of inductor [A]
ΔV_{RON_Main} : High-side FET ripple voltage [V] (20 mV or more is recommended)
I_{LIM} : Over current detection value [A]
V_{RONMAX} : Maximum current sense voltage [V] (240 mV or less is recommended)

Select FET ratings with a margin enough for the input voltage and the load current. Ratings with the over-current detection setting value or more are recommended.

Calculate a necessary rated value of high side FET and low-side FET by the following formula.

$$I_D > I_{OMAX} + \frac{\Delta IL}{2}$$

I_D : Rated drain current [A]
I_{OMAX} : Maximum load current [A]
ΔIL : Ripple current peak-to-peak value of inductor [A]

$$V_{DS} > V_{IN}$$

V_{DS} : Rated voltage between drain and source [V]
V_{IN} : Power supply voltage of switching system [V]

$$V_{GS} > V_B$$

V_{GS} : Rated voltage between gate and source [V]
V_B : VB voltage [V]

Moreover, it is necessary to calculate the loss of SWFET to judge whether a permissible loss of SWFET is a rated value or less. Calculate the loss on high-side FET by the following formula.

$$P_{MainFET} = P_{RON\_Main} + P_{SW\_Main}$$

$P_{MainFET}$: High-side FET loss [W]
P_{RON_Main} : High-side FET conduction loss [W]
P_{SW_Main} : High-side FET SW loss [W]

High-side FET conduction loss

$$P_{RON\_Main} = I_{OMAX}^2 \times \frac{V_O}{V_{IN}} \times R_{ON\_Main}$$

P_{RON_Main} : High-side FET conduction loss [W]
I_{OMAX} : Maximum load current [A]
V_{IN} : Power supply voltage of switching system [V]
V_O : Output voltage [V]
R_{ON_Main} : High-side FET ON resistance [Ω]

High-side FET SW loss

$$P_{SW\_Main} = \frac{V_{IN} \times f_{OSC} \times (I_{btm} \times t_r + I_{top} \times t_f)}{2}$$

P_{SW_Main} : High-side FET SW loss [W]
V_{IN} : Power supply voltage of switching system [V]
f_{OSC} : Oscillation frequency [Hz]
I_{btm} : Ripple current bottom value of inductor [A]
I_{top} : Ripple current top value of inductor [A]
t_r : Turn-on time on high-side FET [s]
t_f : Turn-off time on high-side FET [s]

Calculate the I_{btm}, I_{top}, t_r and the t_f simply by the following formula.

$$I_{btm} = I_{OMAX} - \frac{\Delta IL}{2}$$

$$I_{top} = I_{OMAX} - \frac{\Delta IL}{2}$$

$$t_r = \frac{Q_{gd} \times 4}{5 - V_{gs\ (on)}} \qquad t_f = \frac{Q_{gd} \times 1}{V_{gs\ (on)}}$$

I_{OMAX} : Maximum load current [A]
ΔIL : Ripple current peak-to-peak value of inductor [A]
Q_{gd} : Quantity of charge between gate and drain on high-side FET [C]
$V_{gs\ (on)}$: Voltage between gate and sources in Q_{gd} on high-side FET [V]

Calculate the loss on low-side FET by the following formula.

$$P_{SyncFET} = P_{Ron\_Sync}{}^{*} = Io_{MAX}{}^{2} \times \left(1 - \frac{V_O}{V_{IN}}\right) \times R_{on\_Sync}$$

$P_{SyncFET}$: Low-side FET loss [W]
P_{Ron_Sync} : Low-side FET conduction loss [W]
Io_{MAX} : Maximum load current [A]
V_{IN} : Power supply voltage of switching system [V]
V_O : Output voltage [V]
R_{on_Sync} : Low-side FET on-resistance [Ω]

* : The transition voltage of the voltage between drain and source on low-side FET is generally small, and the switching loss is omitted here for the small one as it is possible to disregard it.

The gate drive power of SWFET is supplied by LDO in IC, therefore all of SWFET allowable maximum total charge (QgTotalMax) is determined by the following formula.

$$QgTotalMax \leq \frac{0.095}{f_{OSC}}$$

QgTotalMax : SWFET allowable maximum total charge [C]
f_{OSC} : Oscillation frequency [Hz]

13.9 Selection of Fly-back Diode

When the conversion efficiency is valued, the improved property of the conversion efficiency is possible by the addition of the fly-back diode. thought it is usually unnecessary. The effect is achieved in the condition where the oscillation frequency is high or output voltage is lower. Select schottky barrier diode (SBD) that the forward current is as small as possible. In this DC/DC control IC, the period for the electric current flows to fly-back diode is limited to synchronous rectification period (60 ns × 2) because of using the synchronous rectification method. Therefore, select the one that the electric current of fly-back diode doesn't exceed ratings of forward current surge peak (IFSM).Calculate the forward current surge peak ratings of fly-back diode by the following formula.

$$I_{FSM} \geq Io_{MAX} + \frac{\Delta IL}{2}$$

I_{FSM} : Forward current surge peak ratings of fly-back diode [A]
Io_{MAX} : Maximum load current [A]
ΔIL : Ripple current peak-to-peak value of inductor [A]

Calculate ratings of the fly-back diode by the following formula:

$V_{R\_Fly} > V_{IN}$

V_{R_Fly} : Reverse voltage of fly-back diode direct current [V]
V_{IN} : Power supply voltage of switching system [V]

13.10 Selection of Output Capacitor

This device supports a small ceramic capacitor of the ESR. The ceramic capacitor that is low ESR is an ideal to reduce the ripple voltage compared with other capacitor. Use the tantalum capacitor and the polymer capacitor of the low ESR when a mass capacitor is needed as the ceramic capacitor can not support. To the output voltage, the ripple voltage by the switching operation of DC/DC is generated. Discuss the lower bound of output capacitor value according to an allowable ripple voltage. Calculate the output ripple voltage from the following formula.

$$\Delta V_O = \left(\frac{1}{2\pi \times f_{osc} \times C_O} + ESR \right) \times \Delta IL$$

ΔV_O : Switching ripple voltage [V]
ESR : Series resistance component of output capacitor [Ω]
ΔIL : Ripple current peak-to-peak value of inductor [A]
C_O : Output capacitor value [F]
f_{osc} : Oscillation frequency [Hz]

Notes:

- The ripple voltage can be reduced by raising the oscillation frequency and the inductor value besides capacitor.
- Capacitor has frequency characteristic, the temperature characteristic, and the electrode bias characteristic, etc. The effective capacitor value might become extremely small depending on the condition. Note the effective capacitor value in the condition.

Calculate ratings of the output capacitor by the following formula:

$V_{CO} > V_O$

V_{CO} : Withstand voltage of the output capacitor [V]
V_O : Output voltage [V]

Note:

Select the capacitor rating with withstand voltage allowing a margin enough for the output voltage.

In addition, use the allowable ripple current with an enough margin, if it has a rating. Calculate an allowable ripple current of the output capacitor by the following formula.

$$Irms \geq \frac{\Delta IL}{2\sqrt{3}}$$

Irms : Allowable ripple current (effective value) [A]
ΔIL : Ripple current peak-to-peak value of inductor [A]

13.11 Selection of Input Capacitor

Select the input capacitor whose ESR is as small as possible. The ceramic capacitor is an ideal. Use the tantalum capacitor and the polymer capacitor of the low ESR when a mass capacitor is needed as the ceramic capacitor can not support. To the power supply voltage, the ripple voltage by the switching operation of DC/DC is generated. Discuss the lower bound of input capacitor according to an allowable ripple voltage. Calculate the ripple voltage of the power supply from the following formula.

$$\Delta V_{IN} = \frac{I_{OMAX}}{C_{IN}} \times \frac{V_O}{V_{IN} \times f_{OSC}} + ESR \times \left(I_{OMAX} + \frac{\Delta IL}{2}\right)$$

ΔV_{IN}	: Switching system power supply ripple voltage peak-to-peak value [V]
I_{OMAX}	: Maximum load current value [A]
C_{IN}	: Input capacitor value [F]
V_{IN}	: Power supply voltage of switching system [V]
V_O	: Output setting voltage [V]
f_{OSC}	: Oscillation frequency [Hz]
ESR	: Series resistance component of input capacitor [Ω]
ΔIL	: Ripple current peak-to-peak value of inductor [A]

Notes:

- The ripple voltage can be reduced by raising the oscillation frequency besides capacitor.
- Capacitor has frequency characteristic, the temperature characteristic, and the electrode bias characteristic, etc. The effective capacitor value might become extremely small depending on the condition. Note the effective capacitor value in the condition.

Calculate ratings of the input capacitor by the following formula:

$V_{CIN} > V_{IN}$

V_{CIN}	: Withstand voltage of the input capacitor [V]
V_{IN}	: Power supply voltage of switching system [V]

Note:

Select the capacitor rating with withstand voltage with margin enough for the input voltage.

In addition, use the allowable ripple current with an enough margin, if it has a rating. Calculate an allowable ripple current by the following formula.

$$Irms \geq I_{OMAX} \times \frac{\sqrt{V_O \times (V_{IN} - V_O)}}{V_{IN}}$$

Irms	: Allowable ripple current (effective value) [A]
I_{OMAX}	: Maximum load current value [A]
V_{IN}	: Power supply voltage of switching system [V]
V_O	: Output voltage [V]

13.12 Selection of Boot Strap Diode

Select Schottky barrier diode (SBD), that forward current is as small as possible. The electric current that drives the gate of high-side FET flows to SBD of the bootstrap circuit. Calculate the mean current by the following formula. Select it so as not to exceed the electric current ratings.

$I_D \geq Q_g \times f_{OSC}$

I_D : Forward current [A]
Q_g : Total quantity of charge of gate on high-side FET [C]
f_{OSC} : Oscillation frequency [Hz]

Calculate ratings of the boot strap diode by the following formula:

$V_{R\_BOOT} > V_{IN}$

V_{R_BOOT} : Reverse voltage of boot strap diode direct current [V]
V_{IN} : Power supply voltage of switching system [V]

13.13 Selection of Boot Strap Capacitor

To drive the gate of high-side FET, the bootstrap capacitor must have enough stored charge. Therefore, a minimum value as a target is assumed the capacitor which can store electric charge 10 times that of the Qg on high-side FET. And select the boot strap capacitor.

$$C_{BOOT} \geq 10 \times \frac{Q_g}{V_B}$$

C_{BOOT} : Boot strap capacitor value [F]
Q_g : Amount of gate charge on high-side FET [C]
V_B : VB voltage [V]

Calculate ratings of the boot strap capacitor by the following formula:

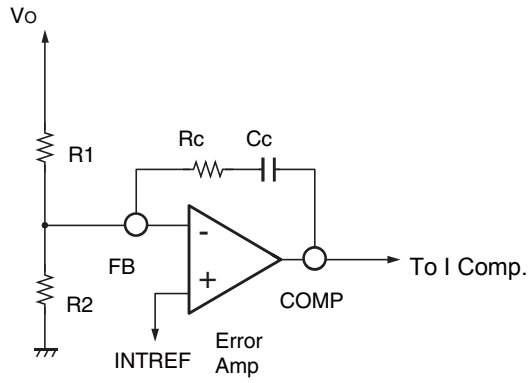
$V_{CBOOT} > V_B$

V_{CBOOT} : Withstand voltage of the boot strap capacitor [V]
V_B : VB voltage [V]

13.14 Design of Phase Compensation Circuit

Assume the phase compensation circuit of 1pole-1zero to be a standard in this device.

13.15 1pole-1zero Phase Compensation Circuit



As for crossover frequency (f_{CO}) that shows the band width of the control loop of DC/DC. The higher it is, the more excellent the rapid response becomes, however, the possibility of causing the oscillation due to phase margin shortage increases. Though this crossover frequency (f_{CO}) can be arbitrarily set, make 1/10 of the oscillation frequencies (fosc) a standard, and set it to the upper limit. Moreover, set the phase margin at least to 30°, and 45° or more if possible as a reference.

Set the constants of Rc and Cc of the phase compensation circuit using the following formula as a target:

$$R_C = \frac{(V_{IN}-V_O)\, A_{LVCNV} \times R_{ON\_Main} \times f_{CO} \times 2\pi \times C_O \times V_O}{V_{IN} \times f_{OSC} \times L \times I_{OMAX}} \times R1$$

$$C_C = \frac{C_O \times V_O}{R_C \times I_{OMAX}}$$

R_C	: Phase compensation resistor value [Ω]
C_C	: Phase compensation capacitor value [F]
V_{IN}	: Power supply voltage of switching system [V]
V_O	: Output setting voltage [V]
f_{OSC}	: Oscillation frequency [Hz]
I_{OMAX}	: Maximum load current value [A]
L	: Inductor value [H]
C_O	: Output capacitor value [F]
R_{ON_Main}	: High-side FET ON resistance [Ω]
R1	: Output setting resistor value [Ω]
A_{LVCNV}	: Level converter voltage gain [V/V] On-duty ≤ 50% : A_{LVCNV} = 6.8 On-duty > 50% : A_{LVCNV} = 13.6
f_{CO}	: Cross-over frequency (arbitrary setting) [Hz]

13.16 VB Pin Capacitor

1 µF is assumed to be a standard, and when Qg of SWFET used is large, it is necessary to adjust it. To drive the gate of high-side FET, the bootstrap capacitor must have enough stored charge. Therefore, a minimum value as a target is assumed the capacitor which can store electric charge 100 times that of the Qg on high-side FET. And select it.

$$C_{VB} \geq 100 \times \frac{Qg}{V_B}$$

C_{VB} : VB pin capacitor value [F]
Qg : Total amount of gate charge of high-side FET and low-side FET [C]
V_B : VB voltage [V]

Calculate ratings of the VB pin capacitor by the following formula:

$$V_{CVB} > V_B$$

V_{CVB} : Withstand voltage of the VB pin capacitor [V]
V_B : VB voltage [V]

13.17 VB Regulator

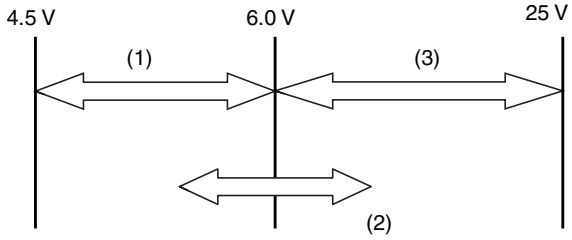
In the condition for which the potential difference between VCC and VB is insufficient, the decrease in the voltage of VB happens because of power output on-resistance and load current (mean current of all external FET gate driving current and load current of internal IC) of the VB regulator. Stop the switching operation when the voltage of VB decreases and it reaches threshold voltage (V_{THL1}) of the under voltage lockout protection circuit. Therefore, set oscillation frequency or external FET or I/O potential difference of the VB regulator using the following formula as a target when you use this IC.

$$V_{CC} \geq VB\ (V_{THL1}) + (Qg \times f_{OSC} + I_{CC}) \times R_{VB}$$

V_{CC} : Power supply voltage [V] (V_{IN})
VB (V_{THL1}) : Threshold voltage of VB under-voltage lockout protection circuit [V](3.8 [V] Max)
Qg : Total amount of gate charge of high-side FET and low-side FET [C]
f_{OSC} : Oscillation frequency [Hz]
I_{CC} : Power supply current [A] (2.7×10^{-3} [A] ≈ Load current of VB (LDO))
R_{VB} : VB output on-resistance [Ω] (100 Ω (The reference value at VCC = 4.5 V))

If the I/O potential difference is small, the problem can be solved by connecting the VB pin and the VCC pin.
The conditions of the input voltage range are as follows:

V_{IN} input voltage ranges:



(1) For 4.5 V < V_{IN} < 6.0 V
→ Connect VB pin to VCC.

(2) When the input voltage range steps over 6.0 V
→ Normal use (VCC to VB not connected)

(3) For 6.0 V ≤ V_{IN}
→ Normal use (VCC to VB not connected)

Note that if the I/O potential difference is not enough when used, use the actual machine to check carefully the operations at the normal operation, start operation, and stop operation. In particular, care is needed when the input voltage range over 6 V.

13.18 Power Dissipation and the Thermal Design

As for this IC, considerations of the power dissipation and thermal design are not necessary in most cases because of its high efficiency. However, they are necessary for the use at the conditions of a high power supply voltage, a high oscillation frequency, high load, and the high temperature.

Calculate IC internal loss (P_{IC}) by the following formula.

$$P_{IC} = V_{CC} \times (I_{CC} + Qg \times f_{OSC})$$

P_{IC}	: IC internal loss [W]
V_{CC}	: Power supply voltage (V_{IN}) [V]
I_{CC}	: Power supply current [A] (2.7[mA] Max)
Qg	: All SWFET total quantity of charge [C] (Total with Vgs = 5 V)
f_{OSC}	: Oscillation frequency [Hz]

Calculate junction temperature (Tj) by the following formula.

$$Tj = Ta + \theta ja \times P_{IC}$$

Tj	: Junction temperature [°C] (+150[°C] Max)
Ta	: Ambient temperature [°C]
θja	: TSSOP-16 Package thermal resistance (101°C/W)
P_{IC}	: IC internal loss [W]

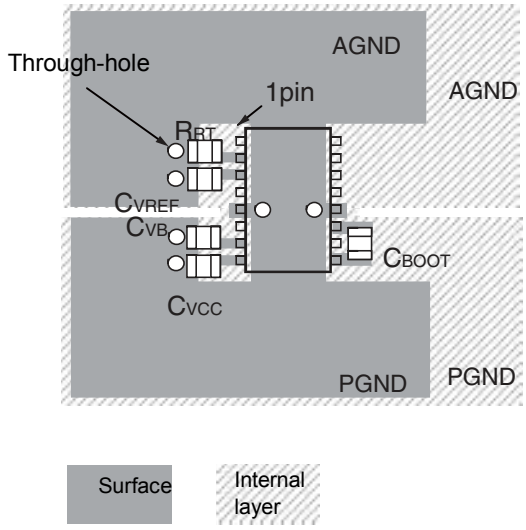
13.19 Board Layout

Consider the points listed below and do the layout design.

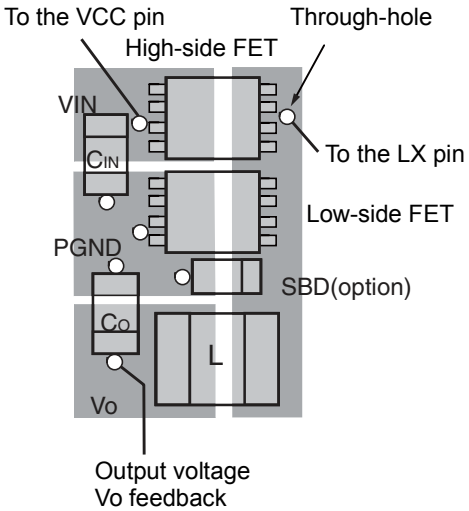
- Provide the ground plane as much as possible on the IC mounted face. Connect bypass capacitor connected with the VCC and VB pins, and GND pin of the switching system parts with switching system GND (PGND). Connect other GND connection pins with control system GND (AGND), and separate each GND, and try not to pass the heavy current path through the control system GND (AGND) as much as possible. In that case, connect control system GND (AGND) and switching system GND (PGND) right under IC.
- Connect the switching system parts as much as possible on the surface. Avoid the connection through the through-hole as much as possible.
- As for GND pins of the switching system parts, provide the through hole at the proximal place, and connect it with GND of internal layer.
- Pay the most attention to the loop composed of input capacitor (C_{IN}), SWFET, and fly-back diode (SBD). Consider making the current loop as small as possible.
- Place the boot strap capacitor (C_{BOOT}) proximal to CB and LX pins of IC as much as possible.
- This device monitors the voltage between drain and source on high-side FET as voltage between VCC and LX pins. Place the input capacitor (C_{IN}) and the high-side FET proximally as much as possible. Draw out the wiring to VCC pin from the proximal place to the input capacitor. As for the net of the LX pin, draw it out from the proximal place to the source pin on high-side FET. Moreover, a large electric current flows momentary in the net of the LX pin. Wire the linewidth of about 0.8 mm to be a standard, as short as possible.
- Large electric current flows momentary in the net of DRVH and DRVL pins connected with the gate of SWFET. Wire the linewidth of about 0.8mm to be a standard, as short as possible.
- By-pass capacitor (C_{VCC}, C_{VREF}, C_{VB}) connected with VREF, VCC, and VB, and the resistor (R_{RT}) connected with the RT pin should be placed close to the pin as much as possible. Also connect the GND pin of the by-pass capacitor with GND of internal layer in the proximal through-hole.
- Consider the net connected with RT, FB, and the COMP pins to keep away from a switching system parts as much as possible because it is sensitive to the noise. Moreover, place the output voltage setting resistor and the phase compensation circuit element connected with this net close to the IC as much as possible, and try to make the net as short as possible. In addition, for the internal layer right under the installing part, provide the control system GND (AGND) of few ripple and few spike noises, or provide the ground plane of the power supply voltage as much as possible.

Switching system parts : Input capacitor (C_{IN}), SWFET, Fly-back diode (SBD), Inductor (L), Output capacitor (C_O)

Layout example of IC



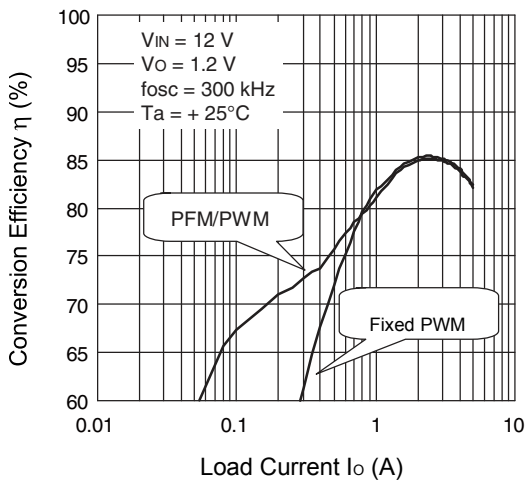
Layout example of switching components



14. Reference Data

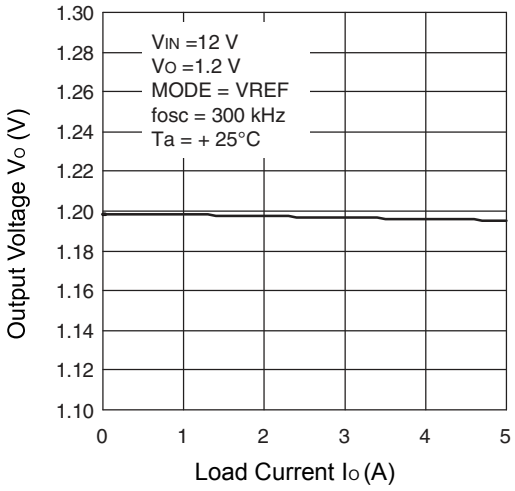
Conversion Efficiency

Conversion Efficiency vs. Load Current

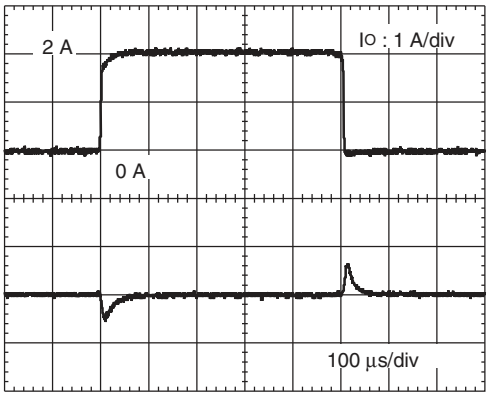


Load Regulation

Output Voltage vs. Load Current



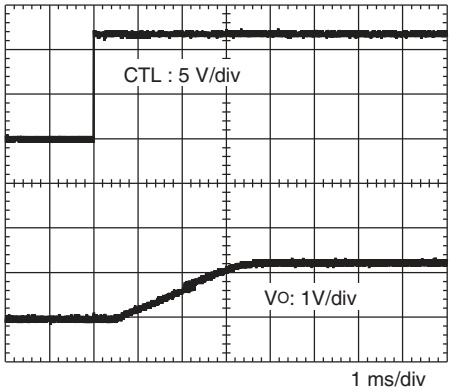
Load Sudden Change Waveform



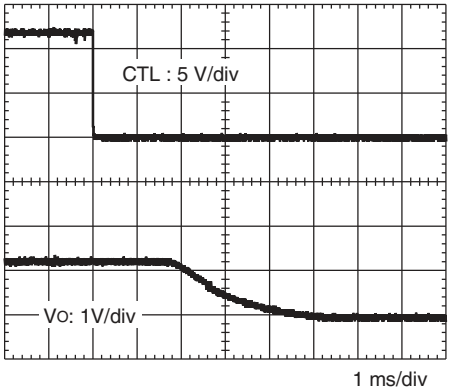
VO : 200 mV/div (1.2 V offset)

V_{IN} = 12 V
V_O = 1.2 V
I_O = 0 ⟷ 2 A
f_{OSC} = 300 kHz,
Ta = + 25°C

CTL Start-up Waveform

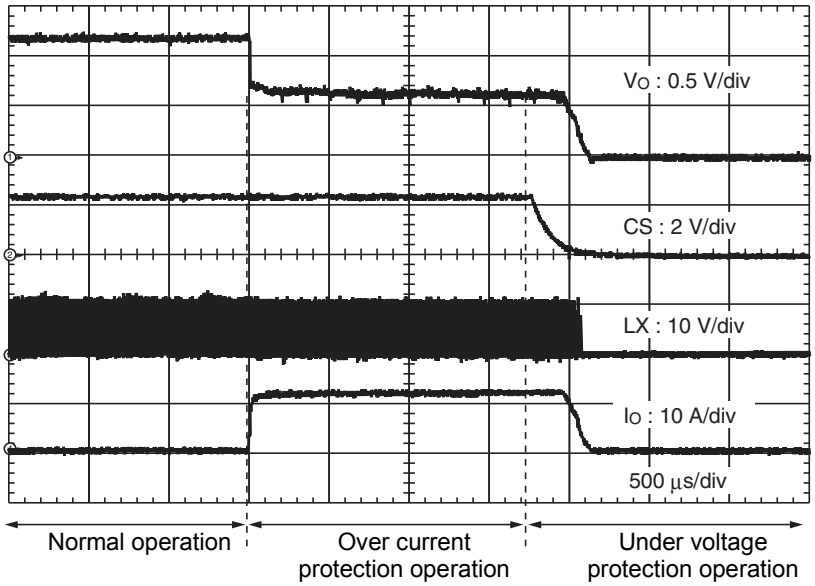


CTL Stop Waveform



V_{IN} = 12 V, V_O = 1.2 V, Io = 5 A (0.24 Ω)
f_{OSC} = 300 kHz, Ta = + 25°C,Soft start setting time = 3.0 ms

Normal operation → Over current protection →
Under voltage protection operation waveform



V_{IN} = 12 V
V_O = 1.2 V
f_{OSC} = 300 kHz
Ta = + 25°C

15. Usage Precaution

1. Do not Configure the IC Over the Maximum Ratings.

If the IC is used over the maximum ratings, the LSI may be permanently damaged.
It is preferable for the device to normally operate within the recommended usage conditions. Usage outside of these conditions can have an adverse effect on the reliability of the LSI.

2. Use the Device Within the Recommended Operating Conditions.

The recommended values guarantee the normal LSI operation under the recommended operating conditions.
The electrical ratings are guaranteed when the device is used within the recommended operating conditions and under the conditions stated for each item.

3. Printed Circuit Board Ground Lines Should be Set up With Consideration for Common Impedance.

4. Take Appropriate Measures Against Static Electricity.

- Containers for semiconductor materials should have anti-static protection or be made of conductive material.
- After mounting, printed circuit boards should be stored and shipped in conductive bags or containers.
- Work platforms, tools, and instruments should be properly grounded.
- Working personnel should be grounded with resistance of 250 kΩ to 1 MΩ in serial body and ground.

5. Do not Apply Negative Voltages.

The use of negative voltages below −0.3 V may make the parasitic transistor activated, and can cause malfunctions.

16. Ordering Information

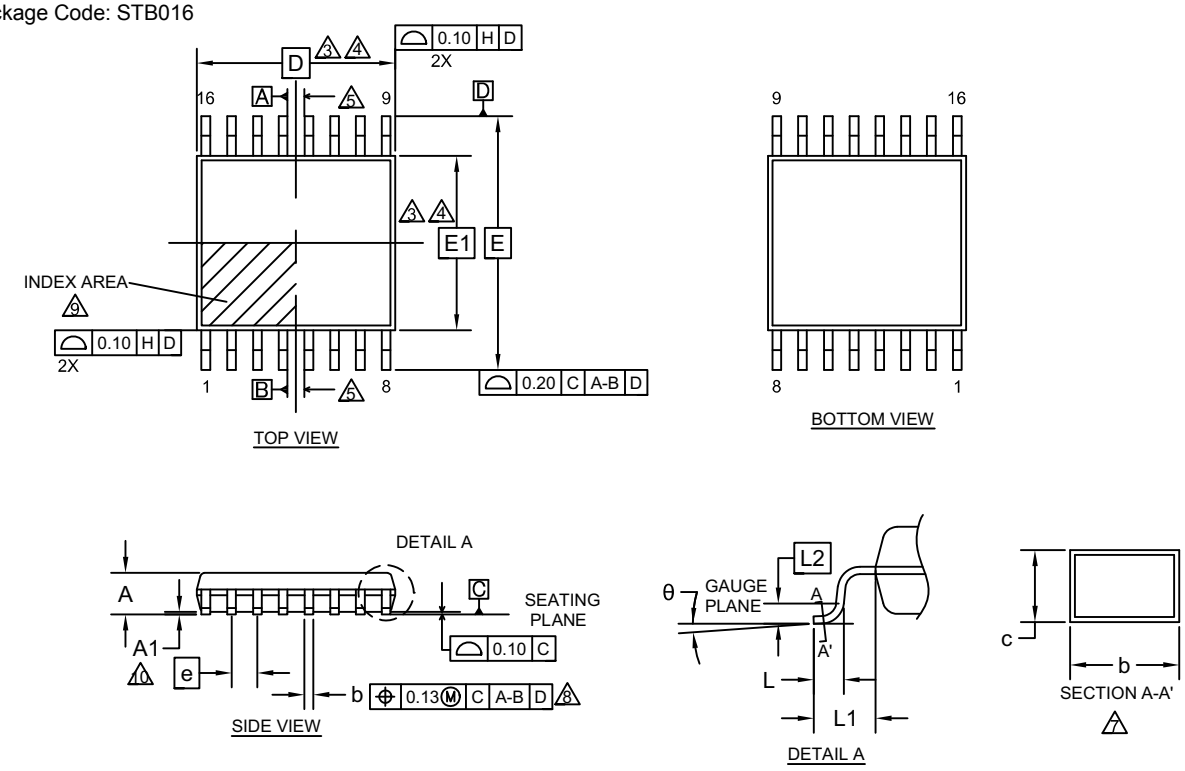
Part Number	Package	Remarks
MB39A135PFT	16-pin plastic TSSOP (STB016)	–

17. RoHS Compliance Information

The LSI products of Cypress with “E1” are compliant with RoHS Directive, and has observed the standard of lead, cadmium, mercury, Hexavalent chromium, polybrominated biphenyls (PBB), and polybrominated diphenyl ethers (PBDE). A product whose part number has trailing characters “E1” is RoHS compliant.

18. Package Dimensions

Package Code: STB016



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	——	——	1.20
A1	0.05	——	0.15
D	4.96 BSC		
E	6.40 BSC		
E1	4.40 BSC		
θ	0°	——	8°
c	0.10	——	0.19
b	0.16	0.24	0.32
L	0.45	0.60	0.75
L 1	1.00 REF		
L 2	0.25 BSC		
e	0.65 BSC		

NOTES

1. ALL DIMENSIONS ARE IN MILLIMETER.
2. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
3. DIMENSIONING D INCLUDE MOLD FLASH, DIMENSIONING E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.025 mm PER SIDE. D and E1 DIMENSION ARE DETERMINED AT DATUM H.
4. THE PACKAGE TOP MAY BE SMALLER THAN THE PACKAGE BOTTOM. DIMENSIONING D and E1 ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY EXCLUSIVE OF MOLD FLASH, THE BAR BURRS, GATE BURRS AND INTERLEAD FLASH, BUT INCLUDING ANY MISMATCH BETWEEN THE TOP AND BOTTOM OF THE PLASTIC BODY.
5. DATUMS A & B TO BE DETERMINED AT DATUM H.
6. "N" IS THE MAXIMUM NUMBER OF TERMINAL POSITIONS FOR THE SPECIFIED PACKAGE LENGTH.
7. THE DIMENSION APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN 0.10 mm TO 0.25mm FROM THE LEAD TIP.
8. DIMENSION "b" DOES NOT INCLUDE THE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.10mm TOTAL IN EXCESS OF THE "b" DIMENSION AT MAXIMUM MATERIAL CONDITION. THE DAMBAR MAY NOT BE LOCATED ON THE LOWER RADIUS OF THE FOOT.
9. THIS CHAMFER FEATURE IS OPTIONAL. LF IT IS NOT PRESENT, THEN A PIN 1 IDENTIFIER MUST BE LOCATED WITHIN THE INDEX AREA INDICATED
10. "A1" IS DEFINED AS THE VERTICAL DISTANCE FROM THE SEATING PLANE TO THE LOWEST POINT ON THE PACKAGE BODY EXCLUDING THE LID AND OR THERMAL ENHANCEMENT ON CAVITY DOWN PACKAGE CONFIGURATIONS.
11. JEDEC SPECIFICATION NO. REF : N/A

002-15914 Rev. **

19. Major Changes

Spansion Publication Number: DS04-27263-3E.

Page	Section	Change Results
7	Electrical Characteristics	Revised the minimum value of “Maximum on-duty” in “Output Block [DRV]”: 72 → 75

NOTE: Please see “Document History” about later revised information.

Document History

Document Title: MB39A135 1ch DC/DC Converter IC with PFM/PWM Synchronous Rectification Document Number: 002-08410				
Revision	**ECN**	**Orig. of Change**	**Submission Date**	**Description of Change**
**	—	TAOA	01/10/2013	Migrated to Cypress and assigned document number 002-08410. No change to document contents or format.
*A	5491361	TAOA	10/24/2016	Updated to Cypress template.
*B	5641441	HIXT	02/28/2017	Updated Pin Assignment: Change the package name from FPT-16P-M08 to STB016 Updated Ordering Information: Change the package name from FPT-16P-M08 to STB016 Deleted “EV Board Ordering Information” Deleted “Marking Format (Lead Free Version)” Deleted “Labeling Sample (Lead Free Version)” Deleted “MB39A135PFT Recommended Conditions Of Moisture Sensitivity Level” Updated Package Dimensions: Updated to Cypress format
*C	5767341	MASG	06/09/2017	Adapted Cypress new logo.

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