

Vishay Siliconix

RoHS

COMPLIANT

N-Channel 2.5-V (G-S) Battery Switch, ESD Protection

PRODUCT SUMMARY				
V _{DS} (V)	R_{DS(on)} (Ω)	I _D (A)		
28	0.033 at V _{GS} = 4.5 V	4.6		
	0.038 at V _{GS} = 3.0 V	4.3		
	0.042 at V _{GS} = 2.5 V	4.1		

FEATURES

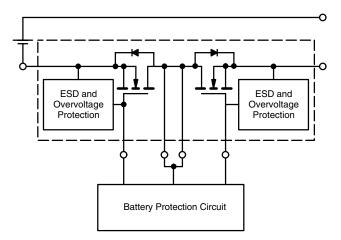
- Halogen-free
- Low R_{DS(on)}
- V_{GS} Max Rating: 14 V
- Exceeds 2 kV ESD Protection
- 28 V V_{DS} Rated
- Symmetrical Voltage Blocking (Off Voltage)

DESCRIPTION

The Si6924AEDQ is a dual N-Channel MOSFET with ESD protection and gate over-voltage protection circuitry incorporated into the MOSFET. The device is designed for use in Lithium Ion battery pack circuits. The common-drain construction takes advantage of the typical battery pack topology, allowing a further reduction of the device's on-resistance. The 2-stage input protection circuit is a unique design, consisting of two stages of back-to-back zener diodes separated by a resistor. The first stage diode is designed to absorb most of the ESD energy. The second

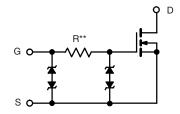
stage diode is designed to protect the gate from any remaining ESD energy and over-voltages above the gates inherent safe operating range. The series resistor used to limit the current through the second stage diode during over voltage conditions has a maximum value which limits the input current to \leq 10 mA at 14 V and the maximum t_{off} to 12 μs . The Si6924AEDQ has been optimized as a battery or load switch in Lithium Ion applications with the advantage of both a 2.5 V $R_{DS(on)}$ rating and a safe 14 V gate-to-source maximum rating.

APPLICATION CIRCUITS



*Thermal connection to drain pins is required to achieve specific performance

Figure 1. Typical Use In a Lithium Ion Battery Pack



**R typical value is 3.3 kΩ by design.

See Typical Characteristics, Gate-Current vs. Gate-Source Voltage, Page 3.

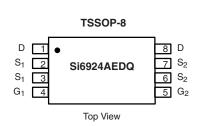
Figure 2. Input ESD and Overvoltage Protection Circuit

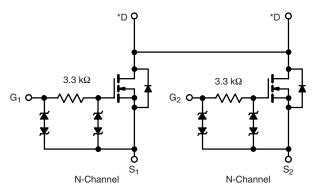
Si6924AEDQ

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FUNCTIONAL BLOCK DIAGRAM AND PIN CONFIGURATION





Ordering Information: Si6924AEDQ-T1-GE3 (Lead (Pb)-free and Halogen-free)

*Thermal connection to drain pins is required to achieve specific performance.

Figure 3.

Figure 4.

ABSOLUTE MAXIMUM RATINGS T_A	= 25 $^{\circ}$ C, unle	ss otherwise n	oted			
Parameter		Symbol	10 s	Steady State	Unit	
Drain-Source Voltage, Source-Drain Voltage		V _{DS}	28		V	
Gate-Source Voltage		V _{GS}	± 14			
	T _A = 25 °C	– I _D	4.6	4.1	٨	
Continuous Drain-to-Source Current $(T_J = 150 \ ^\circ C)^a$	T _A = 70 °C		3.7	3.2		
Pulsed Drain-to-Source Current		I _{DM}	20		A	
Pulsed Source Current (Diode Conduction) ^a		۱ _s	1.2	0.9		
Maximum Power Dissipation ^a	T _A = 25 °C	– P _D	1.3	1.0	W	
	T _A = 70 °C		0.84	0.64		
Operating Junction and Storage Temperature Range		T _J , T _{stg}	- 55 to 150		°C	

THERMAL RESISTANCE RATINGS					
Parameter		Symbol	Typical	Maximum	Unit
	t ≤ 10 s	- R _{thJA} R _{thJF}	71	95	
Maximum Junction-to-Ambient ^a	Steady State		96	125	°C/W
Maximum Junction-to-Foot (Drain)	Steady State		56	70	

Notes:

a. Surface Mounted on FR4 board.



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Parameter	Symbol	Test Conditions Min.		Тур.	Max.	Unit	
Static				•	•		
Gate Threshold Voltage	V _{GS(th)}	$V_{DS} = V_{GS}$, $I_D = 250 \ \mu A$	0.6		1.5	V	
Gate-Body Leakage	I _{GSS} -	$V_{DS} = 0 V, V_{GS} = \pm 4.5 V$			± 1	μA	
		$V_{DS} = 0 V, V_{GS} = \pm 14 V$			± 20	mA	
Zero Gate Voltage Drain Current	I _{DSS}	$V_{DS} = 22.4 \text{ V}, V_{GS} = 0 \text{ V}$			1		
		$V_{DS} = 22.4 \text{ V}, V_{GS} = 0 \text{ V}, T_{J} = 55 \text{ °C}$				μA	
On-State Drain Current ^b	I _{D(on)}	$V_{DS} \ge 5 \text{ V}, V_{GS} = 5 \text{ V}$	10			А	
Drain-Source On-State Resistance ^b	R _{DS(on)}	$V_{GS} = 4.5 \text{ V}, \text{ I}_{D} = 4.6 \text{ A}$		0.022	0.033	Ω	
		$V_{GS} = 3.0 \text{ V}, \text{ I}_{D} = 4.3 \text{ A}$		0.025	0.038		
		$V_{GS} = 2.5 \text{ V}, \text{ I}_{D} = 4.1 \text{ A}$		0.029	0.042		
Forward Transconductance ^b	9 _{fs}	$V_{DS} = 10 \text{ V}, \text{ I}_{D} = 4.6 \text{ A}$		25		S	
Diode Forward Voltage ^b	V _{SD}	I _S = 1.2 A, V _{GS} = 0 V		0.7	1.1	V	
Dynamic ^a	• • •		-		•		
Total Gate Charge	Qg			6.5	10	nC	
Gate-Source Charge	Q _{gs}	V_{DS} = 10 V, V_{GS} = 4.5 V, I_D = 4.6 A		1.2			
Gate-Drain Charge	Q _{gd}			1.5			
Turn-On Delay Time	t _{d(on)}			0.95	1.5		
Rise Time	t _r	V_{DD} = 10 V, R_L = 10 Ω		1.4	2.1	μs	
Turn-Off Delay Time	t _{d(off)}	$I_D \cong$ 1 A, V_{GEN} = 4.5 V, R_G = 6 Ω		7	11		
Fall Time	t _f			3.1	5		

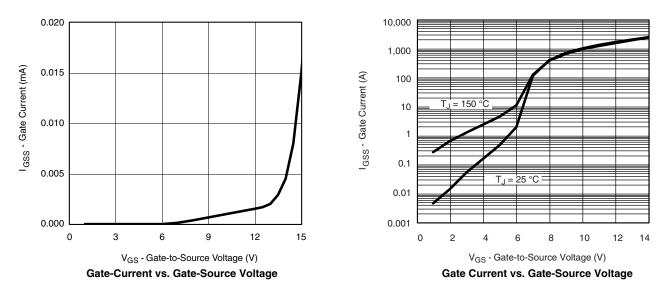
Notes:

a. Guaranteed by design, not subject to production testing.

b. Pulse test; pulse width \leq 300 µs, duty cycle \leq 2 %.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

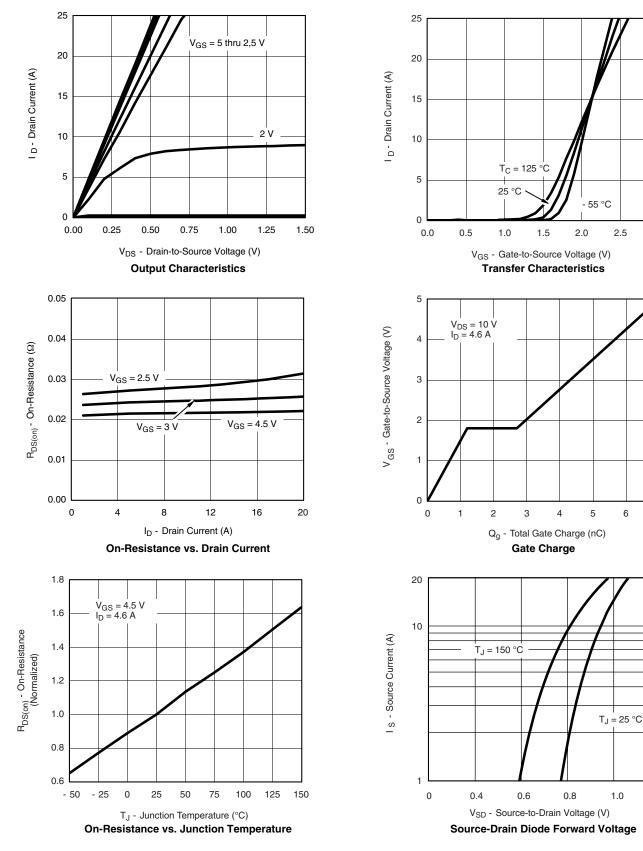
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Si6924AEDQ

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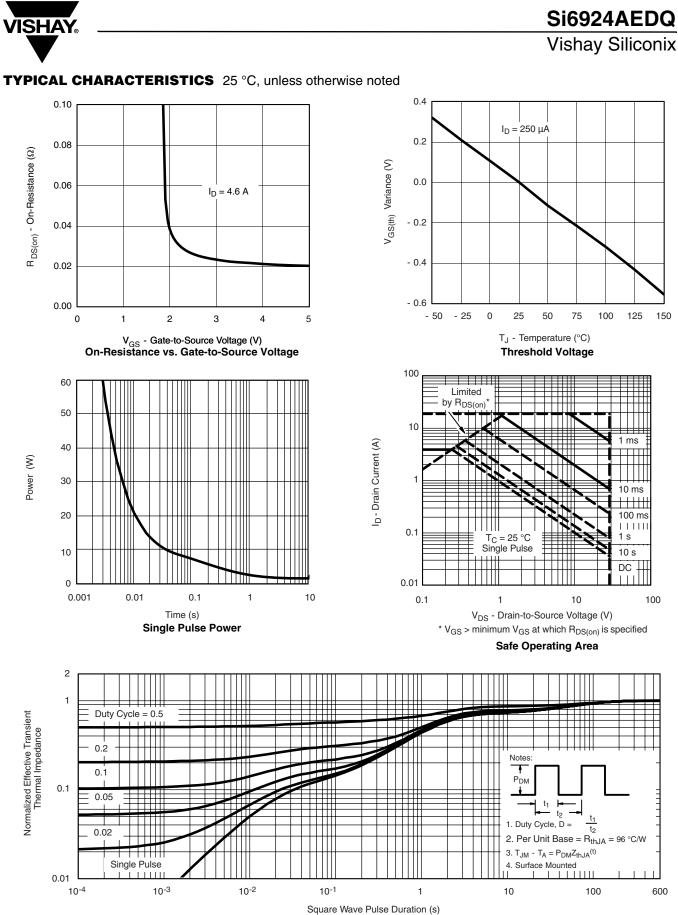




3.0

7

1.2



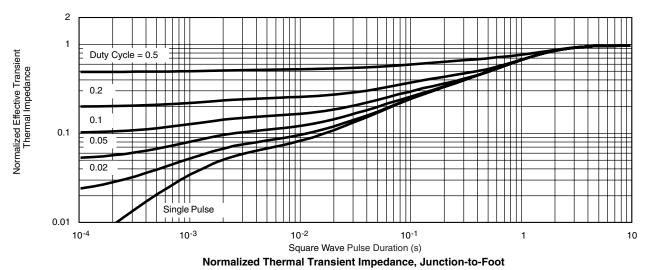
Normalized Thermal Transient Impedance, Junction-to-Ambient

Si6924AEDQ

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TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see http://www.vishay.com/ppg?72215.



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