FLASHlogic

Programmable Logic Device Family

June 1996, ver. 2 — Data Sheet

Features...

- High-performance programmable logic device (PLD) family
  - SRAM-based logic with shadow FLASH memory elements fabricated on advanced CMOS technology
  - Logic densities from 1,600 to 3,200 usable gates (see Table 1)
  - Combinatorial speeds with t_{PD} as low as 10 ns
  - Counter frequencies of up to 80 MHz
- 8 to 16 logic array blocks (LABs) linked by a 100%-connectable programmable interconnect array (PIA) for improved fitting of complex designs
- 24V10 macrocell features available
  - Dual feedback on all I/O pins
  - Product-term allocation matrix supporting up to 16 product terms per macrocell
  - Programmable registers providing D, T, SR, and JK flipflop functionality with clear, preset, and clock controls
  - Fast 12-bit identity compare option
- Fully compliant with ***PCI Local Bus Specification***, version 2.1

Table 1. FLASHlogic Device Features

Feature	EPX880	EPX8160
Usable gates	1,600	3,200
Maximum SRAM bits	10,240	20,480
Macrocells	80	160
Logic array blocks (LABs)	8	16
Package options (maximum user I/O pins)	84-pin PLCC (62) 132-pin PQFP (104)	208-pin PQFP (172)
t_{PD} (ns)	10	10
t_{CO} (ns)	6	6
f_{CNT} (MHz)	80	80

… and More Features

- LABs can be configured as either one of the following:
  - 24V10 logic block with 10 macrocells
  - 128 × 10 SRAM block
- 3.3-V or 5.0-V I/O on all devices (selectable in each LAB)
- Low power consumption (1 mA/MHz in standby mode; 1.5 to 2.5 mA/MHz in active mode)
- 84 to 208 pins available in plastic J-lead (PLCC) and plastic quad flat pack (PQFP) packages (see Table 1)
- Open-drain output option
- Joint Test Action Group (JTAG) IEEE 1149.1-compatible test port
  - Boundary-scan testing (BST) support
  - In-circuit reconfigurability (ICR) support
  - In-system programmability (ISP) support
- Programmable security bit for protection of proprietary designs
- Supported by industry-standard design and programming tools from Altera and other vendors

General Description

FLASHlogic devices are SRAM-based devices with shadow FLASH memory elements. Fabricated on advanced CMOS technology, FLASHlogic devices provide from 1,600 to 3,200 usable gates, pin-to-pin delays as fast as 10 ns, and counter speeds of up to 80 MHz. Table 2 shows the available speed grades for FLASHlogic devices.

Table 2. FLASHlogic Speed Grades

Device	Available Speed Grades	
	-10	-12
EPX880	✓	✓
EPX8160	✓	✓

FLASHlogic devices have a unique combination of features that is ideal for a variety of applications, including communications and bus interface controllers. They provide low power consumption and user-selectable 5.0-V and 3.3-V outputs, making FLASHlogic devices useful for mixed-voltage applications such as portable and embedded systems.

The FLASHlogic device architecture supports 100% TTL emulation and high-density integration of SSI, MSI, and LSI logic functions. In addition, FLASHlogic devices easily integrate multiple programmable logic devices ranging from PALs, GALs, and 22V10s to MACH, pLSI, and FPGA devices. With speed, density, and I/O resources comparable to commonly used masked gate arrays, FLASHlogic devices are ideal for gate array prototyping and PC applications. In addition, FLASHlogic devices in the -10 speed grade are PCI-compliant.

FLASHlogic devices are available in plastic J-lead chip carrier (PLCC) and plastic quad flat pack (PQFP) packages.

FLASHlogic devices contain 8 to 16 LABs linked by a PIA. Each LAB can be defined as either a 24V10 logic block of 10 macrocells or a 128 × 10 SRAM block. When defined as a 24V10 logic block, all 10 macrocells have a programmable-AND/allocatable-OR array and a configurable register with independently programmable clock, clear, and preset functions. To build complex logic functions, product-term allocation allows up to 16 product terms for a single macrocell.

FLASHlogic devices provide dedicated pins compliant with the JTAG IEEE 1149.1-1990 specification. The JTAG pins support BST, ICR, and ISP. ICR and ISP offer the designer greater flexibility in prototyping new designs. These features make FLASHlogic devices ideal for applications in which the final configuration is not fixed.

FLASHlogic devices are supported by industry-standard PC- and workstation-based EDA tools, including the Altera PLDshell Plus development system. The MAX+PLUS II development software also provides programming and configuration support for FLASHlogic devices.

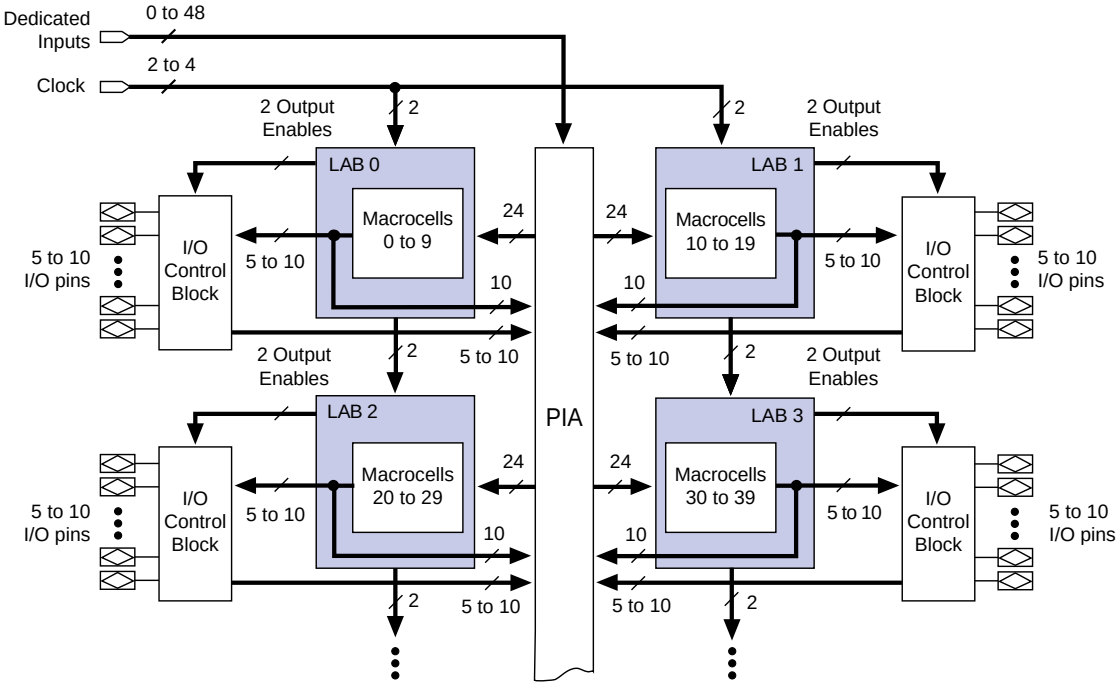
Functional Description

The FLASHlogic device architecture includes the following elements:

- Logic array blocks (LABs)
  - 24V10 configuration
  - SRAM configuration
- Programmable interconnect array (PIA)
- I/O control blocks

Figure 1 shows the block diagram of the FLASHlogic device architecture, which consists of LABs linked by a 100%-connectable PIA.

Figure 1. FLASHlogic Device Block Diagram



Logic Array Blocks

The FLASHlogic device architecture is based on the linking of high-performance, flexible logic array modules called logic array blocks (LABs). Each LAB can be configured as a 24V10 logic block or as a 128 × 10 SRAM block. The LABs are linked via the PIA, which is fed by all dedicated inputs, I/O pins, and either macrocells (in 24V10 configuration) or SRAM outputs (in SRAM configuration). Each LAB is fed by 24 signals from the PIA and 2 global clocks.

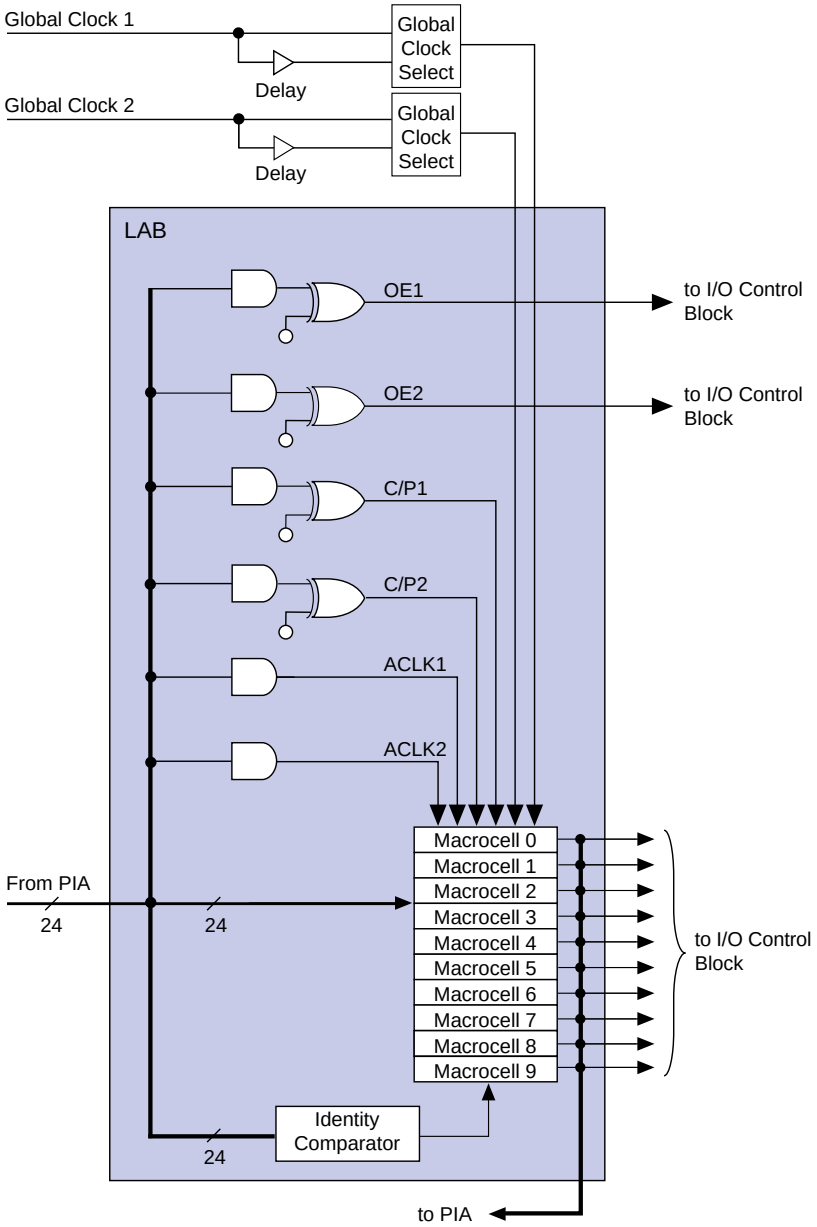
24V10 Configuration

When a LAB is configured as a 24V10 logic block, each block contains the following elements:

- 10 macrocells
- A 12-bit identity comparator
- 2 global clocks
- Control logic for array clocks, and for clear, preset and output enable signals

Figure 2 shows a diagram of a LAB configured as a 24V10 logic block.

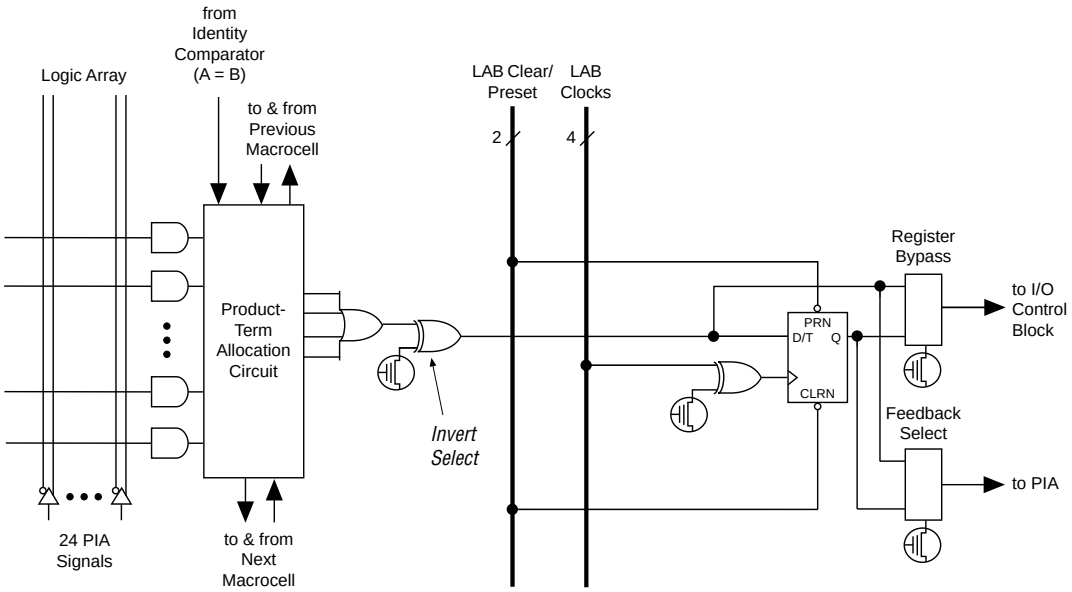
Figure 2. LAB in 24V10 Configuration



Macrocells

Each FLASHlogic macrocell can be individually configured for either sequential or combinatorial logic operation. The macrocell consists of three functional blocks: the logic array, the product-term allocation circuit, and the programmable register. See Figure 3.

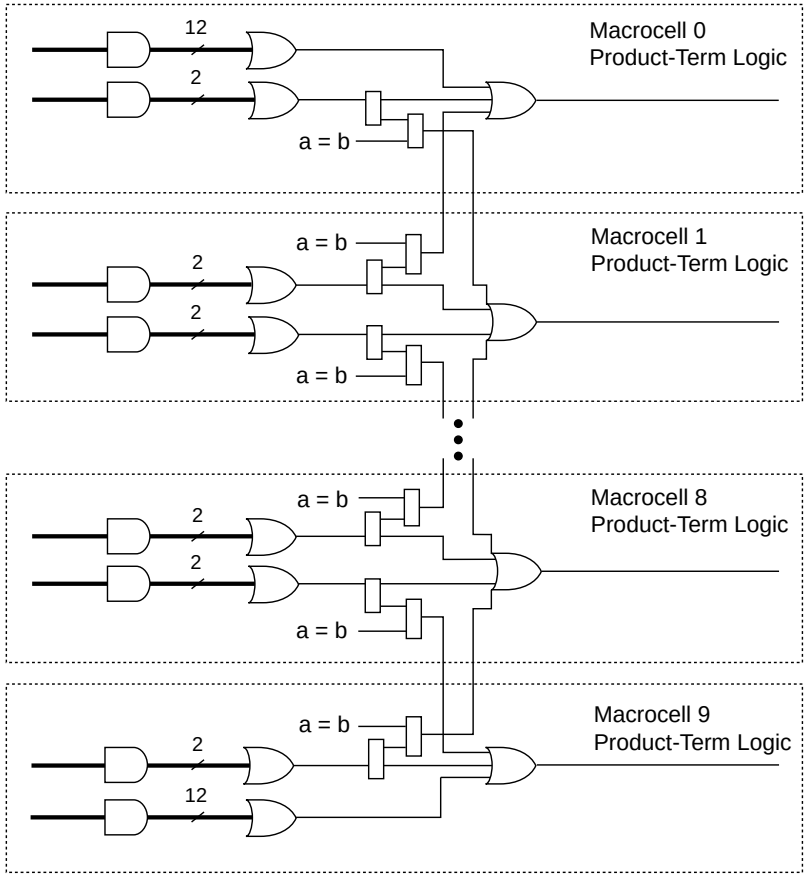
Figure 3. FLASHlogic Device Macrocell



Combinatorial logic is implemented in the logic array, which provides 2 sets of 2 product terms per macrocell. Macrocells 0 and 9 each have 14 product terms, and macrocells 2 through 8 each have 4 product terms. Each macrocell can borrow product terms from adjacent macrocells to increase the total number of product terms per macrocell up to a maximum of 8. The macrocells located at the ends of each LAB have additional product terms and support up to 16 product-term equations. The performance of each macrocell is uniform regardless of whether 2 or 16 product terms are used. Figure 4 shows the flexible product-term allocation circuit.

In registered functions, each macrocell flipflop can be individually programmed to implement D, T, JK, or SR operation with programmable clock, preset, and clear controls. If necessary, the register can be bypassed for combinatorial operation.

Figure 4. LAB Product-Term Allocation



Each LAB supports four clock signals—two global clocks and two array clock signals. The EPX8160 has 4 global clock pins: CLK1 and CLK2 are for LABs 0 through 7, and CLK3 and CLK4 are for LABs 8 through 15. Global clocking is provided by either of two global clock signals or two delayed global clock signals. Array clocking is provided by two LAB product terms. Each register in the LAB can be clocked by the true or the complement of any two of the four clock signals.

Each programmable register can be clocked in three different modes:

- Global mode, by either of two global clock signals. This mode achieves the fastest clock-to-output performance.
- Delayed global mode, by either of two global clock signals with an added local delay (within the LAB).
- Array mode, by either of two array clocks implemented with a product term. In this mode, the register can be clocked by signals from buried macrocells.

These clocking modes give FLASHlogic devices increased timing flexibility, enabling the designer to vary the setup, hold, and clock-to-output times of each register. See Table 3. These clocking modes are particularly useful for integrating devices with short-setup-time microprocessors, such as a Pentium microprocessor.

Table 3. EPX880-10 & EPX8160-10 Sample Clocking Modes

Clock Mode	Setup Time	Hold Time	Clock-to-Output Time	Unit
Global	6.5	0	6	ns
Delayed global	5	2	8	ns
Array	2	5	12	ns

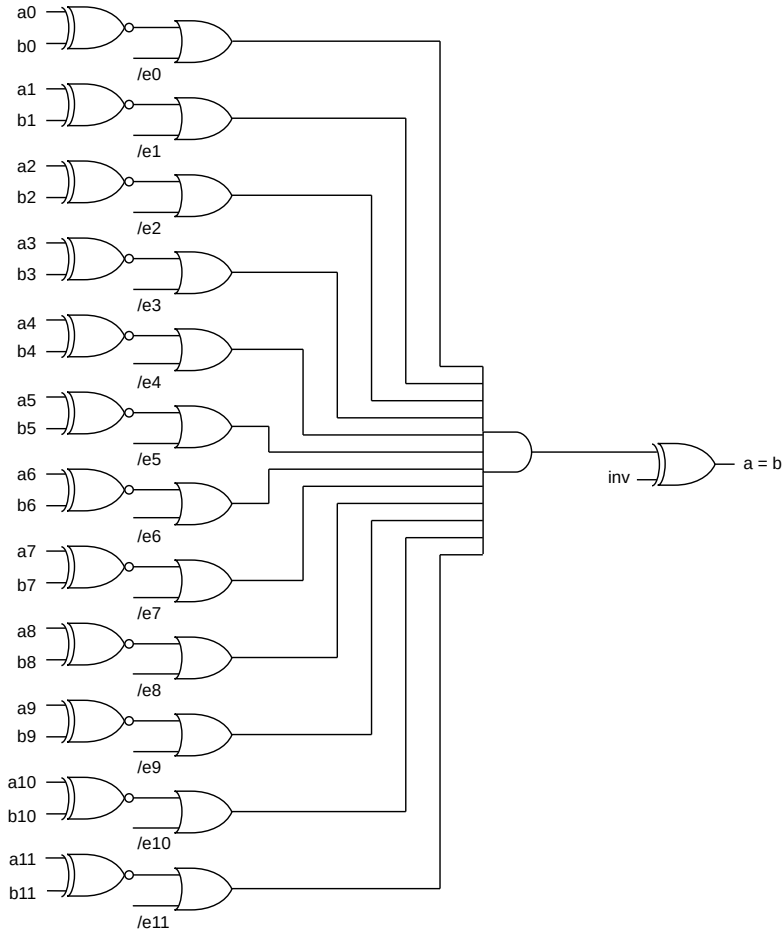
Each register also supports array preset and clear functions. These functions are driven by product terms and can be inverted. See Figure 2 on page 269 for a diagram of this logic.

Comparator Circuit

Each LAB also provides a comparator circuit that compares up to 12 pairs of inputs within the t_{PD} of the device. The product-term allocation matrix allows any one of the 10 macrocells in the LAB to use the output of the comparator circuit. See Figure 5.

Figure 5. 12-Bit Identity Compare Logic

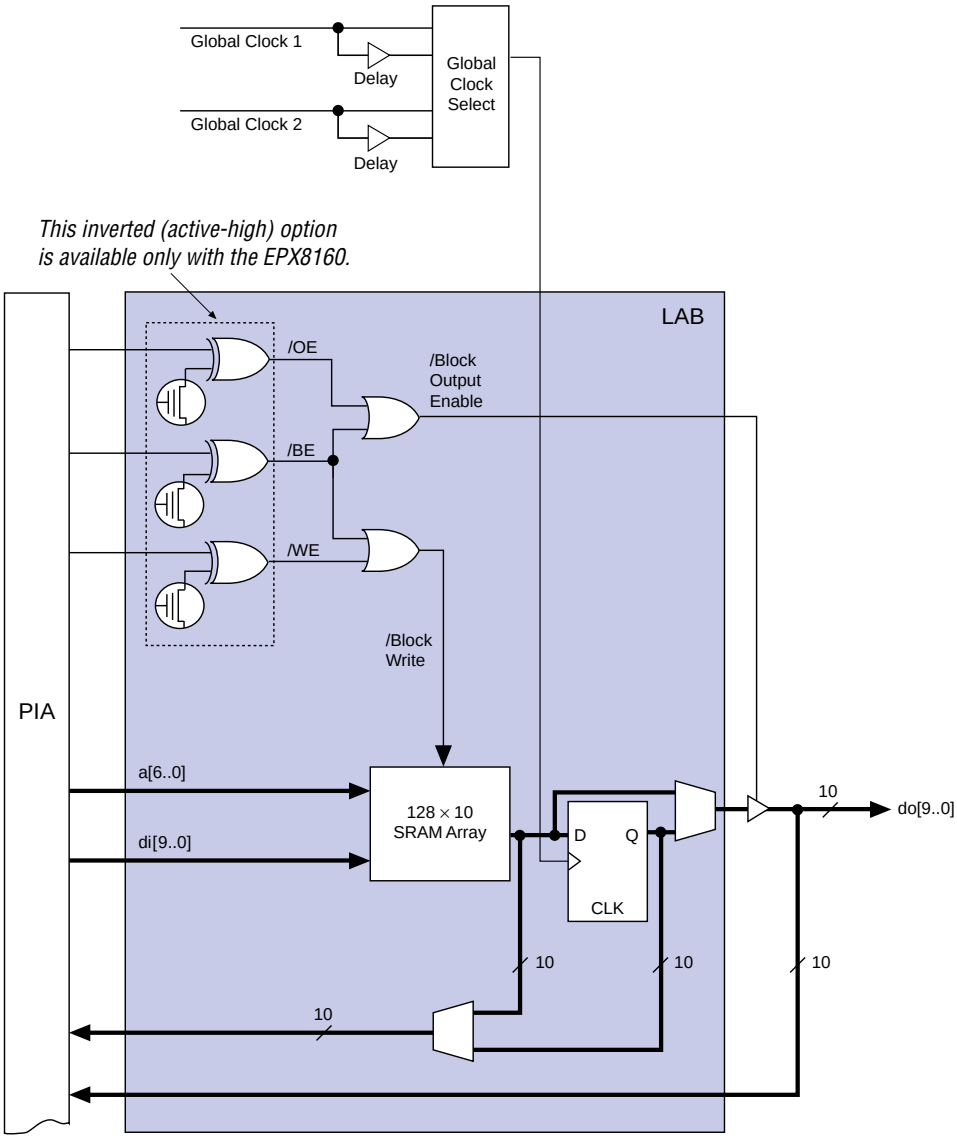
The an and bn signals represent a fan-in pair. The /en signal represents an architecture control bit.



SRAM Configuration

Each FLASHlogic LAB can be configured as a 128 × 10 (128 words by 10 bits) SRAM block, as shown in Figure 6. The SRAM block can be defined with either a bidirectional I/O data bus or with separate input and output data buses.

Figure 6. LAB in SRAM Configuration



The SRAM is accessed using a subset of the 24-signal fan-in from the PIA: 7 bits are for address information; 10 bits are for input data; 3 bits are for block enable (/BE), write enable (/WE), and output enable (/OE) controls, as shown in Table 4.

Table 4. SRAM Functions

Inputs			Cycle	I/O Pins
/BE	/WE	/OE		
1	X	X	None	Disabled
0	1	1	Read	Disabled
0	1	0	Read	Enabled
0	0	1	Write	Disabled
0	0	0	Write	Enabled

During power-up, the SRAM memory elements are initialized by on-chip, nonvolatile configuration cells. During operation, the SRAM contains a copy of the information contained in the nonvolatile configuration FLASH cells unless other data is written to these SRAM blocks. Therefore, the SRAM block can emulate read-only memory (ROM).

When an LAB is configured as SRAM, all product terms are used as SRAM blocks and cannot be used for regular macrocell logic. Multiple LABs can be cascaded to create larger SRAM blocks to increase the width or depth of the memory.

Programmable Interconnect Array

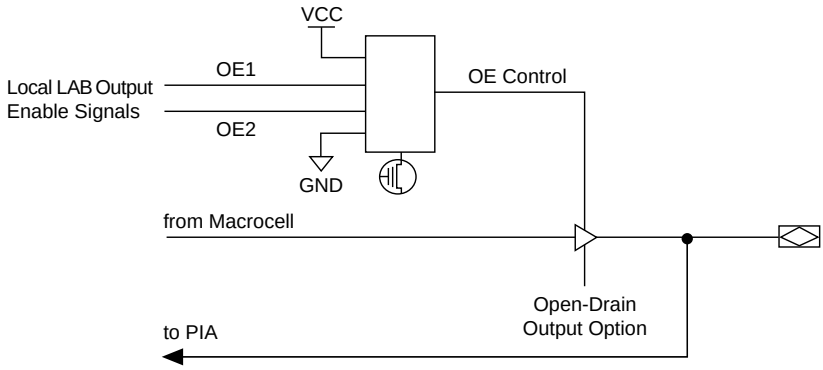
Signals are routed between LABs by the 100%-connectable programmable interconnect array (PIA). This global bus connects any signal source to any destination on the device. All dedicated pins, I/O pins, and macrocell outputs feed into the PIA and are accessible to all LABs. The high degree of connectivity and efficient resource management between LABs minimizes routing problems during design debugging.

The routing delays of channel-based routing schemes in masked or field-programmable gate arrays (FPGAs) are cumulative, variable, and path-dependent. In contrast, the FLASHlogic PIA has a fixed delay. Therefore, the PIA eliminates skew between signals, making timing and performance easy to predict.

I/O Control Blocks

The I/O control block allows each I/O pin to be individually configured for input, output, or bidirectional operation. All I/O pins have a tri-state buffer that is either individually controlled by one of the two local LAB output enable signals generated within each LAB or directly connected to GND or V_{CC}. Figure 7 shows the I/O control block for FLASHlogic devices.

Figure 7. FLASHlogic Device I/O Control Block



When the tri-state buffer control is connected to GND, the output is tri-stated (high-impedance), and the I/O pin can be used as a dedicated input. When the tri-state buffer control is connected to V_{CC}, the output is enabled.

The FLASHlogic architecture provides dual I/O feedback in which macrocell and pin feedbacks are independent. When an I/O pin is configured as an input, the associated macrocell can be used for buried logic.

Input Configuration

Device inputs, as well as I/O pins that are used as inputs, can be optimized for minimum standby current during either CMOS or TTL operation by using the `CMOS_LEVEL` keyword (for 5.0-V CMOS inputs) and the `TTL_LEVEL` keyword (for TTL or 3.3-V CMOS inputs) available in the PLDasm design language supported by PLDshell Plus. `TTL_LEVEL` is the default condition for PLDasm.

Output Configuration

FLASHlogic device outputs can be configured to meet a variety of system-level requirements.

3.3-V or 5.0-V Operation

The pins in an I/O control block can operate at 3.3 V or 5.0 V. This functionality enables the designer to mix 3.3-V outputs and 5.0-V inputs if the appropriate V_{CCO} pins are tied to a 3.3-V power supply. FLASHlogic devices require a V_{CC} of 5.0 V for normal operation. However, the V_{CCO} pin associated with each LAB pair can be connected to either a 5.0-V or 3.3-V power supply to control the output voltages of the I/O pins of that LAB pair. This feature allows FLASHlogic devices to be used in mixed-voltage systems. For example, the devices can be used as an interface between a 3.3-V CPU and 5.0-V peripheral logic.

Power sequencing is required when any or all LABs operate at 3.3-V levels. Thus, the voltage levels of the 5.0-V source must be greater than or equal to the 3.3-V source during power-up and power-down.

Open-Drain Output Option

FLASHlogic devices can be configured to provide an optional open-drain output for each I/O pin. If desired, complex equations can be implemented using multiple open-drain outputs with an externally supplied pull-up resistor to emulate an additional `OR` plane.

CMOS-Compatible Outputs

A weak pull-up resistor is provided for CMOS-compatible outputs. This resistor is always active in both 3.3-V and 5.0-V modes.

I/O Pull-Up Resistor

EPX8160 devices contain active-weak pull-up resistors on the I/O pins that hold the I/O at a logic high during power-up, reconfiguration, and erase/program cycles. This resistor is disabled during normal device operation to reduce power consumption. Dedicated inputs do not have active pull-up resistors.

High Drive Outputs

EPX880 and EPX8160 output buffers are designed specifically for applications requiring high drive current. These buffers enable the devices to drive a bus (including PCI), and concurrently provide 10-ns pin-to-pin performance, which eliminates the need for external buffers and their associated delays.

PCI Compliance

EPX880 and EPX8160 5.0-V output buffers are designed to meet the current-vs.-voltage specifications for PCI. EPX880-10 and EPX8160-10 devices also offer a predictable, 10-ns pin-to-pin propagation delay, a 6-ns clock-to-signal valid delay, and a 6.5-ns synchronous setup time to meet the timing demands of PCI applications. To support bidirectional PCI signals, two output enable product terms are provided in each LAB, for a total of 16 product terms for EPX880 devices and 32 product terms for EPX8160 devices.

Go to *Application Note 41 (PCI Bus Applications in Altera Devices)* for more information on using EPX8160 devices in PCI applications.

JTAG Operation

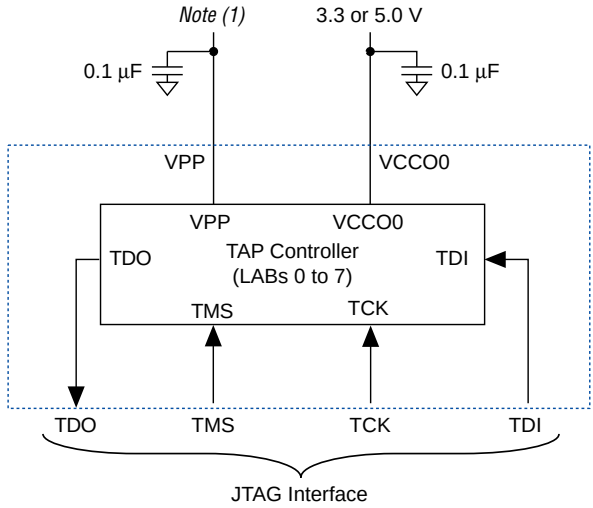
FLASHlogic devices support JTAG IEEE Std. 1149.1-1990 boundary-scan testing (BST). The JTAG BST architecture enables fault-isolation testing of board designs at the device level, enhances production testing and field repair, and is ideal for fault-tolerant applications.

FLASHlogic BST support consists of an instruction register, a data register, scan cells, and associated logic, all of which are accessed through the test access port (TAP). The TAP interface consists of three inputs—test mode select (TMS), test data input (TDI), and test clock input (TCK)—and one output, test data output (TDO).

An EPX880 device contains one JTAG TAP controller. An EPX8160 device contains two JTAG TAP controllers, each of which can operate independently or simultaneously for reconfiguration, reprogramming, and boundary-scan testing. Figure 8 shows the internal connection of the JTAG TAP controllers.

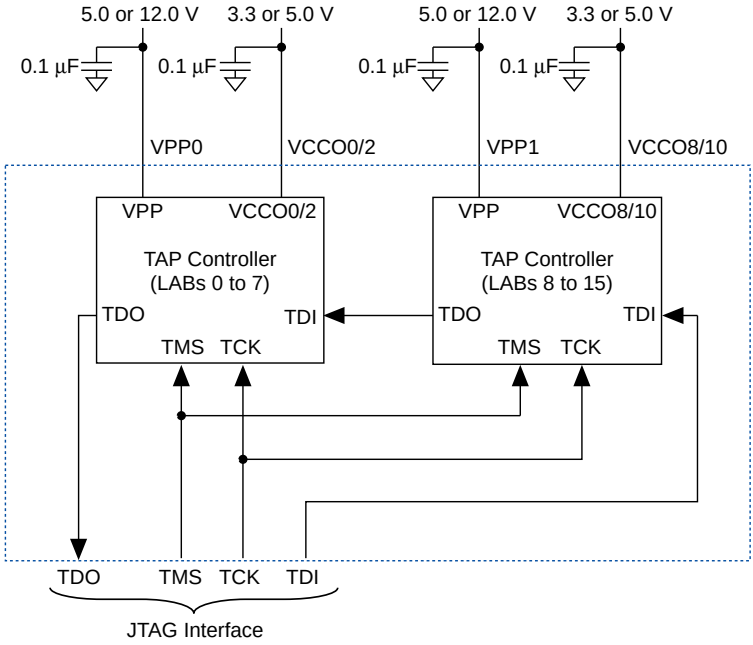
Figure 8. JTAG TAP Controller Connections

EPX880



Note:
(1) 5.0 or 12.0 V for EPX880 devices.

EPX8160



In FLASHlogic devices, the boundary-scan I/O pins are linked to form a shift register chain for all active pins. This chain provides a path that can be used to shift boundary-scan data into and out of the device.

For example, a continuity test can be performed between two JTAG devices on a circuit board by placing a known value on the output buffers of one device and observing the input buffers of the other device. The same technique can also be used to perform in-circuit functional testing of FLASHlogic devices for prototyping new system designs.

The 4-pin JTAG test interface is also used for standard programming, ICR, and ISP.

Boundary-Scan Instructions

The FLASHlogic boundary-scan instruction register (IR) supports the JTAG instructions used for the Program/Verify modes. See Table 5.

Table 5. Boundary-Scan Instructions

Name	Instruction Code (MSB..LSB)	Description
EXTEST	00000	The EXTEST instruction drives the output pins to the values contained in the boundary-scan cells. The instruction tests the external circuitry used for printed circuit board interconnects.
BYPASS	11111	The BYPASS instruction selects the one-bit bypass register (BPR) to be connected to TDI and TDO, which allows BST data to pass synchronously through the selected device to adjacent devices during normal device operation.
SAMPLE/PRELOAD	00001	The SAMPLE/PRELOAD instruction allows a snapshot of the values of the device pins to be captured and examined during normal device operation, and to preload data onto the device pins that are driven to the system circuit board when executing the EXTEST instruction.
IDCODE	00010	The IDCODE instruction selects the ID code register and places it between TDI and TDO, allowing the ID code to be serially shifted out of TDO.
UESCODE	10110	The UESCODE instruction selects the user electronic signature (UES) register and places it between TDI and TDO, allowing the UES register to be serially shifted out of TDO.
HIZ	11101	The HIZ instruction sets all I/O pins to a high-impedance state.

Go to *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices)* for more information about JTAG operation.

ICR & ISP

FLASHlogic devices support in-circuit reconfigurability (ICR). Using the 4-pin JTAG test port, a new configuration can be downloaded to the SRAM by simply shifting the new data into the device. Device reconfiguration can be repeated as many times as desired during prototyping. During ICR, all I/O pins on the device are tri-stated.

Once the design is finalized, it can be programmed into the nonvolatile shadow FLASH cells. FLASHlogic devices support in-system programmability (ISP), allowing devices to be programmed while mounted on a printed circuit board. ISP allows devices to be programmed in-system using the JTAG test port and the programming voltage pins (V_{PP}). FLASH-based devices can be programmed up to 100 times. During ISP, all I/O pins on the device are tri-stated.

During ICR and ISP, the I/O pins of FLASHlogic devices are tri-stated. In addition, the I/O pins for an EPX8160 device have a weak pull-up transistor. Refer to the "Pin Descriptions" on page 298 section of this data sheet for more information.

For more information on ICR and ISP, go to the following documents:

- *Product Information Bulletin 19 (ICR & ISP: In-Circuit Reconfigurability & In-System Programmability)*
- *Application Note 45 (Configuring FLASHlogic Devices)*
- *Application Brief 145 (Designing for In-System Programmability in MAX 7000S Devices)*

Design Security

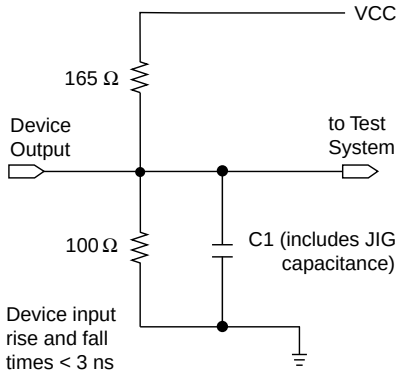
FLASHlogic devices contain a programmable security bit that controls access to the data programmed into the device. Once this security bit is set, the design cannot be read from the nonvolatile cells or the SRAM. The state of the nonvolatile security bit at power-up determines whether data programmed into the device can be accessed and changed by in-circuit reconfiguration.

Generic Testing

FLASHlogic devices are fully functionally tested. Complete testing of each programmable FLASH bit and all internal logic elements ensures 100% programming yield. AC test measurements are taken under conditions equivalent to those shown in Figure 9. Test patterns can be used and erased during early stages of the device production flow.

Figure 9. FLASHlogic AC Test Conditions

Power-supply transients can affect AC measurements. For accurate measurements, avoid simultaneous transitions of multiple outputs. Do not perform threshold tests under AC conditions. Large-amplitude, fast ground-current transients normally occur as the device outputs discharge the load capacitances. When these transients flow through the parasitic inductance between the device ground pin and the test system ground, they can significantly reduce observable noise immunity.



Software Support

FLASHlogic devices are supported by industry-standard PC- and workstation-based EDA tools, including the Altera PLDshell Plus development system and the FLASHlogic Download Cable. In addition, MAX+PLUS II provides programming and configuration support. See the *MAX+PLUS II Programmable Logic Development System & Software Data Sheet* in this data book for more information.

Go to the *PLDshell Plus/PLDasm User's Guide* for information on programming and configuring FLASHlogic devices using PLDshell Plus.

Table 6 lists the third-party vendors that provide software support.

Table 6. Third-Party Software Support

Vendor	Software	Description
Data I/O Corporation	ABEL	Design software that describes and implements logic designs.
	Synario 2.0	Integrated text and graphic design and simulation environment.
Logical Devices, Inc.	CUPL	High-level, universal design software package.
MINC, Inc.	PLDesigner-XL(R)	Design tool for all types of programmable logic with automatic device selection, automatic partitioning, and functional simulation.
OrCAD Systems Corporation	PLD Tools (PLD) and Schematic Design Tool (SDT)	Design tools that Include schematic entry, test vector generation, and multiple forms of input.
	Verification and Simulation Tool (VST)	Series of software tools for performing timing-based simulation of designs.
Viewlogic Systems, Inc.	Workview, PRO Series, and Powerview	Integrated schematic capture and simulation environments.

Simulation models are provided by the following vendors:

- Synopsys Logic Modeling SmartModel—Device model support for behavioral simulation through a variety of simulators.
- Viewlogic ViewSim—Simulation model for Viewlogic verification tools.

Device Programming

FLASHlogic devices can be programmed with MAX+PLUS II software on 486- and Pentium-based PCs using an Altera Logic Programmer card, the Master Programming Unit (MPU), and the appropriate device adapter. The MPU performs continuity checking to ensure adequate electrical contact between the adapter and the device. See the *Altera Programming Hardware Data Sheet* in this data book for more information.

FLASHlogic devices can also be programmed in-system with the MAX+PLUS II software using the BitBlaster serial download cable, and with the PLDshell Plus software using the Altera FLASHlogic Download Cable. Data I/O and other programming hardware manufacturers also provide programming support for FLASHlogic devices. See *Programming Hardware Manufacturers* in this data book for more information.

FLASHlogic Device Absolute Maximum Ratings *Note (1)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage	With respect to GND, *Note (2)*	–2.0	7.0	V
V_{PP}	Programming supply voltage: EPX880 & EPX8160		–2.0	12.6	V
V_I	DC input voltage		–0.5	V_{CC} + 0.5	V
T_{STG}	Storage temperature	No bias	–65	150	° C
T_{AMB}	Ambient temperature	Under bias	–10	85	° C
T_J	Junction temperature	Plastic packages, under bias		135	

FLASHlogic Device Recommended Operating Conditions

Symbol	Parameter	Conditions	Min	Max	Unit
V_{CC}	Supply voltage: 5.0 V		4.75	5.25	V
V_{CCO}	Output supply voltage: 5.0 V		4.75	5.25	V
V_{CCO}	Output supply voltage: 3.3 V		3.0	3.6	V
V_I	Input voltage		0	V_{CC}	V
V_O	Output voltage		0	V_{CCO}	V
T_A	Operating temperature	For commercial use	0	70	° C
T_A	Operating temperature	For industrial use	–40	85	° C
t_R	Input rise time			500	ns
t_F	Input fall time			500	ns

FLASHlogic Device DC Operating Conditions *Note (3)*

Symbol	Parameter	Conditions	Min	Max	Unit
V_{IH}	High-level input voltage		2.0	V_{CC} + 0.3	V
V_{IL}	Low-level input voltage		–0.3	0.8	V
V_{OH}	5.0-V TTL high-level output current	EPX880 & EPX8160: I_{OH} = –16.0 mA DC, V_{CCO} = min., *Note (4)*	2.4		V
	5.0-V CMOS high-level output current	EPX880 & EPX8160: I_{OH} = –100 µA DC, V_{CCO} = min., *Note (4)*	V_{CCO} – 0.2		V
	3.3-V high-level output current	EPX880 & EPX8160: I_{OH} = –100 µA DC, V_{CCO} = min., *Note (4)*	V_{CCO} – 0.2		V
V_{OL}	5.0-V low-level output current	EPX880 & EPX8160: I_{OL} = 24 mA DC, V_{CCO} = min., *Note (4)*		0.45	V
	3.3-V low-level output current	EPX880 & EPX8160: I_{OL} = 12 mA DC, V_{CCO} = min., *Note (4)*		0.2	V
I_I	Input leakage current	V_{CCO} = max., GND < V_{IN} < V_{CCO}, *Note (5)*	–10	10	µA
I_{OZ}	Output leakage current	EPX880 & EPX8160: V_{CCO} = max., V_{OUT} = V_{CCO}	–50	50	µA
		EPX880 & EPX8160: V_{CCO} = max., V_{OUT} = GND	–100	100	µA
I_{SC}	Output short circuit current, *Note (6)*	V_{CCO} = max., V_{OUT} = 0.5 V	–30	–120	mA

FLASHlogic Device Programming Conditions *Notes (3), (7)*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{PP}	Programming voltage: EPX880 & EPX8160		11.4	12	12.6	V
I_{PP1}	V_{PP} read current, IC current, or standby current	$V_{PP} > V_{CC}$		90	200	µA
		$V_{PP} \leq V_{CC}$		15	40	µA
I_{PP2}	V_{PP} programming or program verify current: EPX880 & EPX8160	$V_{PP} = V_{PPH}$ Programming in progress		30	60	mA
I_{PP3}	V_{PP} erase and erase verify current	$V_{PP} = V_{PPH}$		30	60	mA
E_{CNT}	Erase and reprogram count limit				100	–

FLASHlogic Device Capacitance *Notes (8), (9)*

Symbol	Parameter	Conditions	Typ	Max	Unit
C_{IN}	Input pin capacitance	V_{IN} = 2 V, f = 1.0 MHz	10	12	pF
$C_{I/O}$	I/O pin capacitance	V_{OUT} = 2 V, f = 1.0 MHz	12	15	pF
C_{CLK}	Clock pin capacitance	V_{OUT} = 2 V, f = 1.0 MHz	15	18	pF
C_{VPP}	V_{PP} pin capacitance	f = 1.0 MHz	12	15	pF

FLASHlogic Device I_{CC} Supply Current Values *Note (8)*

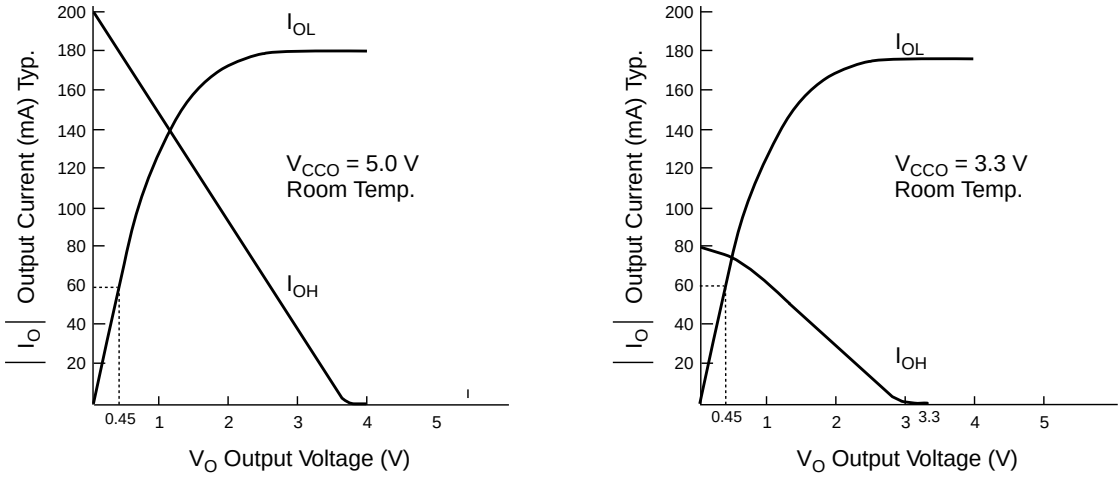
Symbol	Parameter	Conditions	EPX880	EPX8160	Unit
I_{CC1}	V_{CC} supply current (standby, typical)	V_{CC} = max., $V_{IN} = V_{CC}$ or GND, standby mode, *Note (10)*	1	1	mA
I_{CC}	V_{CC} supply current (active, typical)	$V_{IN} = V_{CC}$ or GND, no load, *Note (10)*	1.5	2.5	mA/ MHz

Notes to tables:

(1) See *Operating Requirements for Altera Devices Data Sheet* in this data book.
(2) The minimum DC input is –0.5 V. During transitions, the inputs may undershoot to –2.0 V or overshoot to 7.0 V for periods of less than 20 ns under no-load conditions.
(3) Operating conditions: T_A = 0° C to 70° C, V_{CC} = 5.0 V ± 5% for commercial use.
T_A = –40° C to 85° C, V_{CC} = 5.0 V ± 5% for industrial use.
(4) The I_{OH} parameter refers to high-level TTL output current. The I_{OL} parameter refers to low-level TTL output current.
(5) Input leakage current on JTAG pins is tested at ± 20 µA.
(6) No more than 1 output should be tested at a time. The duration of the test should not exceed 1 second.
(7) Typical values are for T_A = 25° C, V_{CC} = 5.0 V, V_{PP} = 12.0 V.
(8) Typical values are for T_A = 25° C, V_{CC} = 5.0 V.
(9) Capacitance is measured at 25° C, and is sample-tested only.
(10) Measured with a 20-bit, loadable, enabled, up/down counter programmed into each LAB pair.

Figure 10 shows the typical output drive characteristics for FLASHlogic devices.

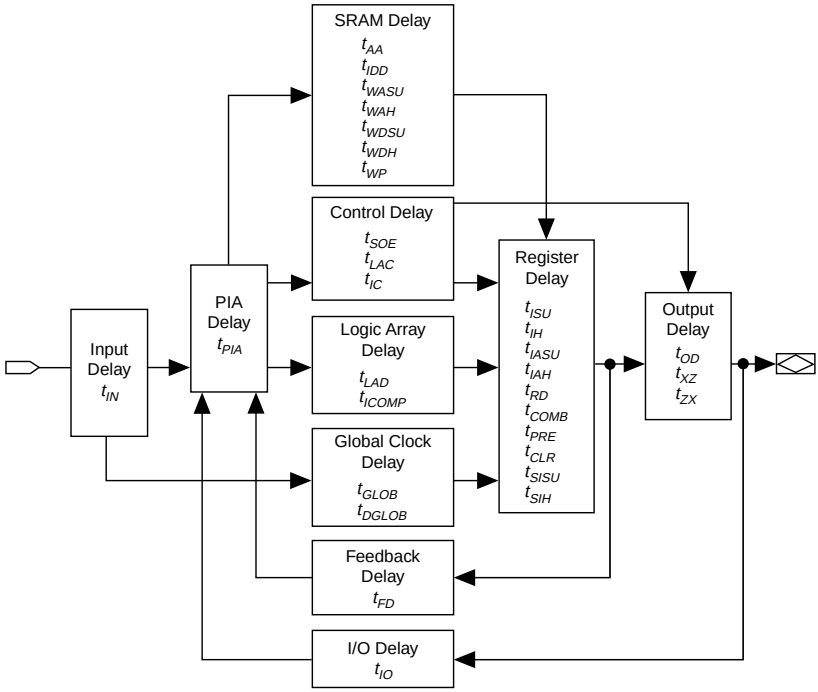
Figure 10. Output Drive Characteristics of FLASHlogic Devices



Timing Model

FLASHlogic devices have fixed internal delays that allow the user to determine the worst-case timing for any design. Device timing can be analyzed with a variety of industry-standard EDA simulators and timing analyzers, or with the timing model shown in Figure 11.

Figure 11. FLASHlogic Timing Model



Industry-standard EDA tools provide timing simulation, point-to-point delay prediction, and detailed analysis for system-level performance evaluation. External timing parameters represent pin-to-pin timing delays. Switching waveforms for these timing parameters (including SRAM read and SRAM write cycles) are shown in Figure 12.

Go to *Application Note 79 (Understanding FLASHlogic Timing)* for more information on FLASHlogic timing parameters.

Figure 12. Switching Waveforms (Part 1 of 3)

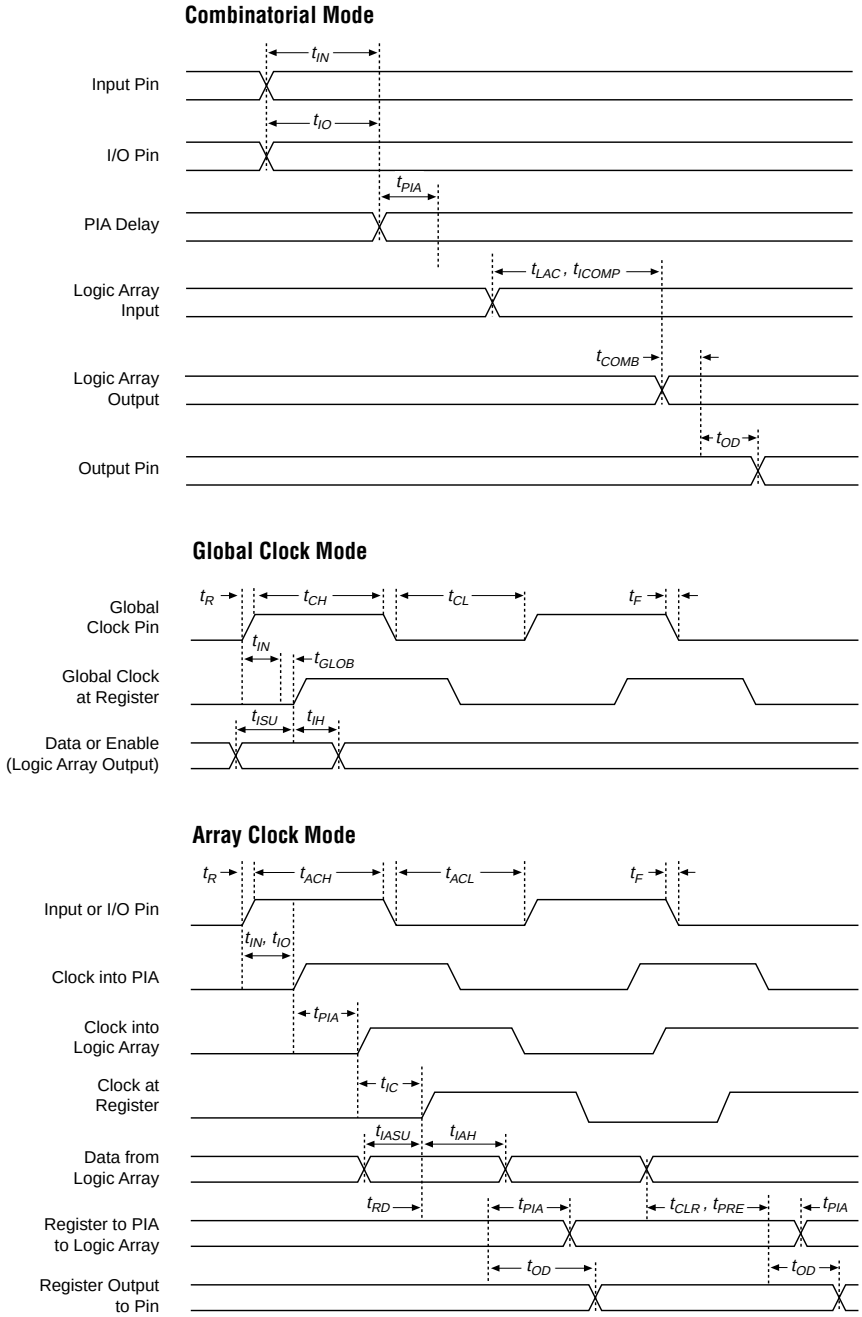


Figure 12. Switching Waveforms (Part 2 of 3)

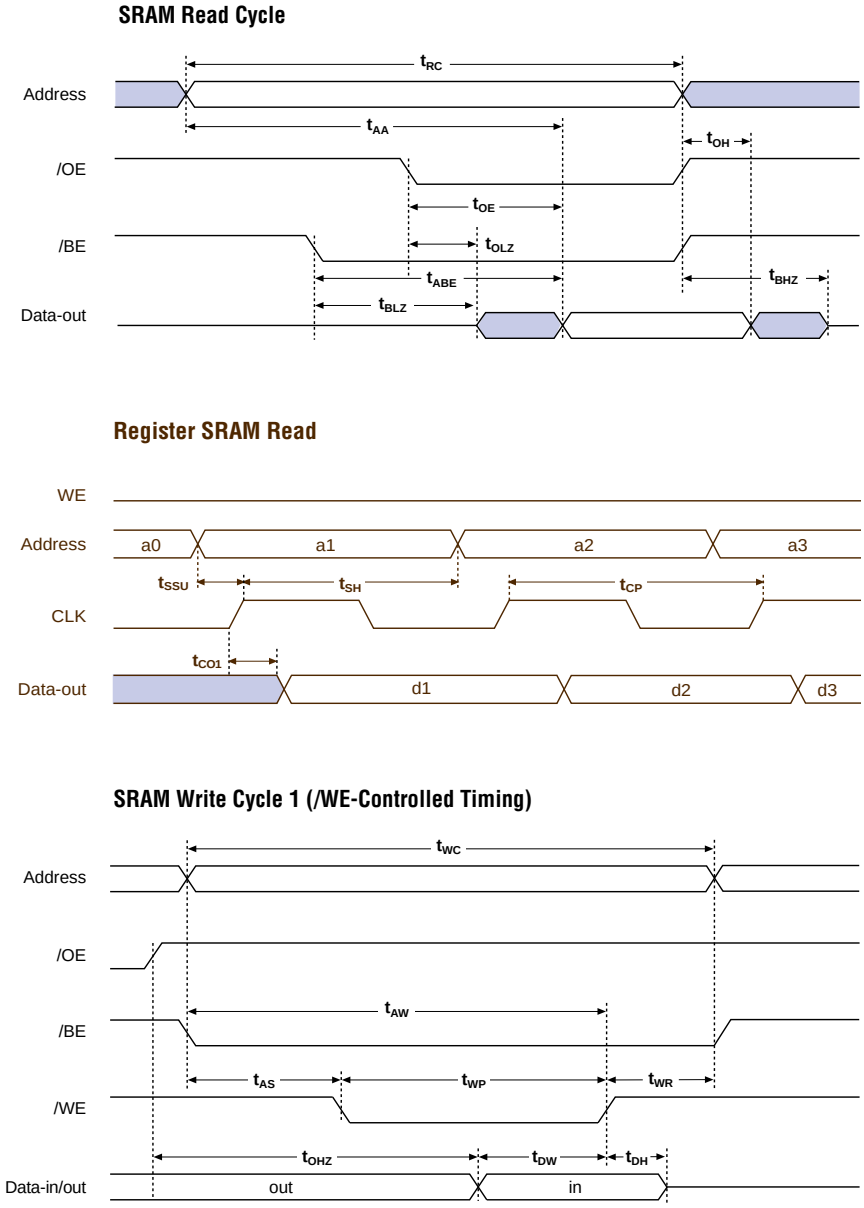
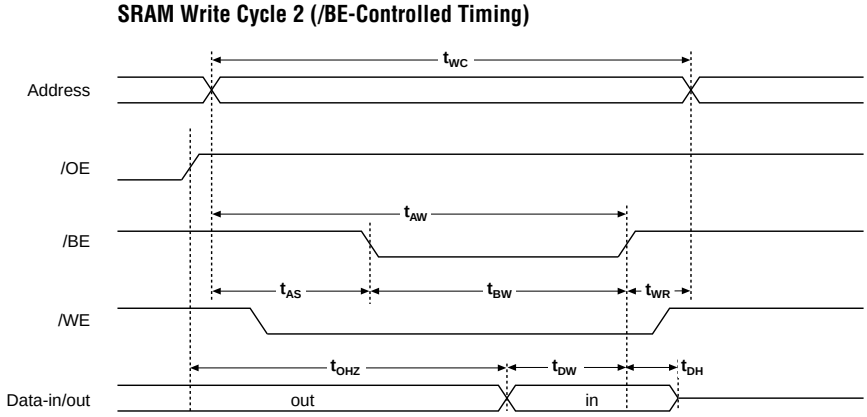


Figure 12. Switching Waveforms (Part 3 of 3)



FLASHlogic Device AC Operating Conditions

External Timing Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
Combinatorial Mode							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{PD1}	Input to nonregistered output	C1 = 35 pF		10		12	ns
t_{PD2}	I/O to nonregistered output	CF = 35 pF		10		12	ns
t_{PZX}	Input or I/O to output enable	C1 = 35 pF		12		14	ns
t_{PXZ}	Input or I/O to output disable	C1 = 5 pF		12		14	ns
t_{CLR}	Array output clear time			15		18	ns
t_{COMP}	Comparator input or I/O feedback to output valid			10		12	ns

External Timing Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
Register Mode—Global Clock							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (1)*	100		83.3		MHz
t_{SU}	Input setup time		6.5		8		ns
t_{H}	Input hold time		0		0		ns
t_{CH}	Clock high time		4.5		5.5		ns
t_{CL}	Clock low time		4.5		5.5		ns
t_{CP}	Clock period		10		12		ns
t_{CO}	Clock-to-output delay	C1 = 35 pF		6		7.5	
t_{ODH}	Output data hold time after clock	C1 = 35 pF *Note (2)*	1		1		ns
t_{CNT}	Minimum clock period			12.5		15.5	
f_{CNT}	Maximum internal frequency	*Note (3)*	80		64.5		MHz

External Timing Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
Register Mode—Delayed Global Clock							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{MAX}	Maximum frequency	*Note (1)*	95.2		80		MHz
t_{DSU}	Input setup time		5		6		ns
t_{DH}	Input hold time		2		2		ns
t_{CH}	Clock high time		4.5		5.5		ns
t_{CL}	Clock low time		4.5		5.5		ns
t_{CP}	Clock period		10.5		12.5		ns
t_{DCO}	Clock-to-output delay	C1 = 35 pF		8		9.5	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *Note (2)*	1		1		ns
t_{DCNT}	Minimum clock period			13		15.5	ns
f_{DCNT}	Maximum internal frequency	*Note (3)*	76.9		64.5		MHz

External Timing Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
Register Mode—Array Clock							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
f_{AMAX}	Maximum frequency	*Note (1)*	80		66.7		MHz
t_{ASU}	Input setup time		2		2.5		ns
t_{AH}	Input hold time		5		6		ns
t_{ACH}	Clock high time		5		5.5		ns
t_{ACL}	Clock low time		5		5.5		ns
t_{ACP}	Clock period		12.5		15		ns
t_{ACO}	Clock-to-output delay	C1 = 35 pF		12		14.5	ns
t_{ODH}	Output data hold time after clock	C1 = 35 pF *Note (2)*	1		1		ns
t_{ACNT}	Minimum clock period			14		17	ns
f_{ACNT}	Maximum internal frequency	*Note (3)*	71.4		58.8		MHz

External TIming Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
SRAM Read *Note (4)*							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{RC}	Read cycle time		15		18		ns
t_{AA}	Address access time			15		18	ns
t_{ABE}	Block enable access time			12		15	ns
t_{OE}	Output enable to output delay	*Note (5)*		12		15	ns
t_{OH}	Output hold from address change		2		3		ns
t_{BLZ}	Block enable to output in low impedance	*Note (5)*	3		4		ns
t_{BHZ}	Block disable to output in high impedance	C1 = 5 pF *Note (5)*		12		15	ns
t_{OLZ}	Output enable to output in low impedance	*Note (5)*	3		4		ns

External Timing Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
Register SRAM Read—Global *Note (4)*							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{SSU}	Input or I/O setup time to clock		11		13		ns
t_{SH}	Input or I/O hold time from clock		0		0		ns
t_{CO1}	Clock-to-output delay			6		7.5	ns
t_{CL}	Clock low time		4.5		5.5		ns
t_{CH}	Clock high time		4.5		5.5		ns
t_{CP}	Clock period		15		17		ns

External Timing Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
Register SRAM Read—Delayed Global *Note (4)*							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{SSU}	Input or I/O setup time to clock		10		11		ns
t_{SH}	Input or I/O hold time from clock		2		2		ns
t_{CO1}	Clock-to-output valid			8		9.5	ns
t_{CL}	Clock low time		4.5		5.5		ns
t_{CH}	Clock high time		4.5		5.5		ns
t_{CP}	Clock period		15.5		17.5		ns

External Timing Parameters			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
SRAM Write *Note (4)*							
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{WC}	Write cycle time		15		18		ns
t_{BW}	Block enable to end of write		10		12		ns
t_{AW}	Address valid to end of write		13		15		ns
t_{AS}	Address set-up time		3		4		ns
t_{WP}	Write pulse width		10		12		ns
t_{WR}	Write recovery time		2		3		ns
t_{DW}	Data valid to end of write		10		12		ns
t_{DH}	Data hold time		2		3		ns
t_{OHZ}	Output disable to valid data-in	C1 = 5 pF *Notes (5), (6)*	12		15		ns

Internal Timing Parameters ***Combinatorial & Register Mode***			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{IN}	Input pad & buffer delay			1		1	ns
t_{IO}	I/O input pad & buffer delay			1		1	ns
t_{FD}	Register feedback delay			2		2	ns
t_{LAD}	Logic array delay			6		8	ns
t_{ICOMP}	Identity comparator delay			6		8	ns
t_{LAC}	Logic control array delay			8		10.5	ns
t_{SOE}	SRAM output enable delay			8		11.5	ns
t_{OD}	Output buffer & pad delay			1		1	ns
t_{ZX}	Output buffer enable delay			2		1.5	ns
t_{XZ}	Output buffer disable delay			2		1.5	ns
t_{ISU}	Register setup time, *Note (7)*		2.5 (3)		3.5 (3.5)		ns
t_{IH}	Register hold time, *Note (7)*		5 (4)		4.5 (4.5)		ns
t_{IASU}	Array clock register setup time		4		2.5		ns
t_{IAH}	Array clock register hold time		2.5		6		ns
t_{RD}	Register delay			1		1	ns
t_{COMB}	Combinatorial delay			1		1	ns
t_{GLOB}	Global clock delay			3		4.5	ns
t_{DGLOB}	Delayed global clock delay			5		6.5	ns
t_{IC}	Array clock delay			8		10.5	ns
t_{PRE}	Register preset time			4		4.5	ns
t_{CLR}	Register clear time			4		4.5	ns
t_{PIA}	Programmable interconnect array delay			1		1	ns

Internal Timing Parameters *SRAM Mode*			EPX880-10 EPX8160-10		EPX880-12 EPX8160-12		
Symbol	**Parameter**	**Conditions**	**Min**	**Max**	**Min**	**Max**	**Unit**
t_{AA}	SRAM address access delay			11		14	ns
t_{DD}	SRAM data-in to data-out delay						ns
t_{WASU}	SRAM write address setup time		3		4		ns
t_{WAH}	SRAM write address hold time		2		3		ns
t_{WDSU}	SRAM write data setup time		10		12		ns
t_{WDH}	SRAM write data hold time		2		3		ns
t_{SISU}	SRAM internal register setup time, *Note (7)*		2 (3)		2.5 (2.5)		ns
t_{SIH}	SRAM internal register hold time		9		10.5		ns
t_{WP}	SRAM write pulse width		10		12		ns

Notes to tables:

(1) The $\mathbf{f_{MAX}}$ values represent the highest frequency for pipelined data.
(2) This parameter is a guideline that is sample-tested only and is based on extensive device characterization. This parameter applies for both global and array clocking.
(3) Measured with a 10-bit loadable, enabled, up/down binary counter programmed into each LAB.
(4) Operating conditions: T_A = 0° C to 70° C, V_{CC} = 5.0 V ± 5% for commercial use.
T_A = –40° C to 85° C, V_{CC} = 5.0 V ± 5% for industrial use.
(5) These signals are measured at ± 0.5 V from steady-state voltage as driven by specified output load. Enable values are measured starting from 1.5 V on output.
(6) These specifications do not apply when separate data-in and data-out buses are used.
(7) When using the delay clock, calculate the timing with the values in parentheses.

Power Consumption

Supply power (P) versus frequency ($\mathbf{f_{MAX}}$ in MHz) for FLASHlogic devices is calculated with the following equation:

$$P = P_{INT} + P_{IO}$$

$$P = I_{CCACTIVE} \times V_{CC} + P_{IO}$$

The P_{IO} value, which depends on the device output load characteristics and switching frequency, can be calculated using the guidelines provided in *Application Note 74 (Evaluating Power for Altera Devices)* in this data book.

The $I_{CCACTIVE}$ value depends on the switching frequency and the application logic. The $I_{CCACTIVE}$ value is calculated with the following equation:

$$I_{CCACTIVE} = A \times MC + C \times MC \times \mathbf{f_{MAX}} \times \mathbf{tog_{LC}}$$

The parameters in this equation are as follows:

MC = Number of macrocells used in the design
f_{MAX} = Highest clock frequency to the device
tog_{LC} = Average ratio of logic cells toggling at each clock (typically 0.125)
A, C = Constants, shown in Table 7

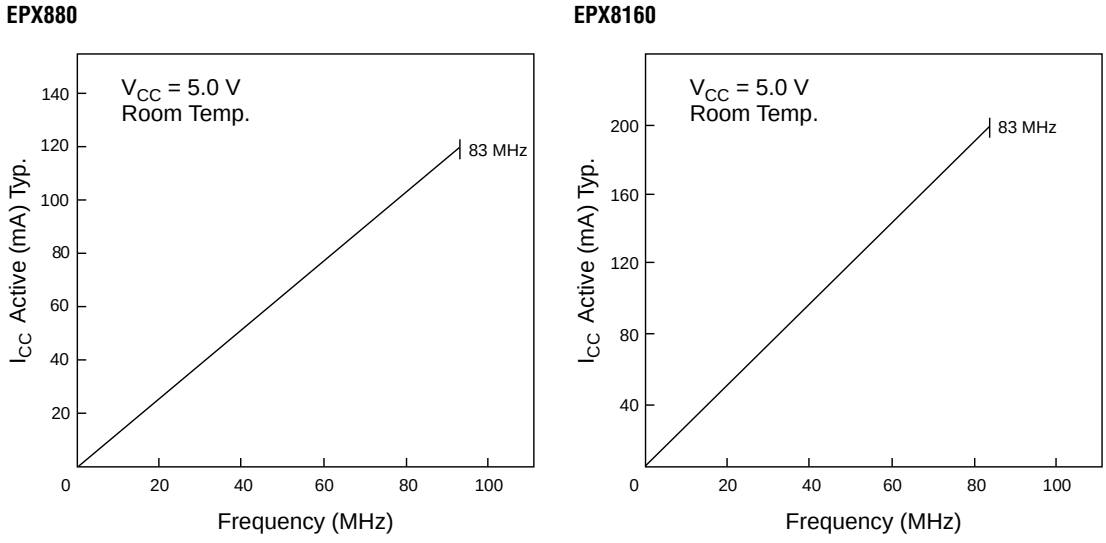
Table 7. FLASHlogic I_{CC} Equation Constants

Device	Constant A	Constant C
EPX880	0.0125	0.150
EPX8160	0.0062	0.125

The formula for calculating $I_{CCACTIVE}$ provides an estimate based on typical conditions using a typical pattern of a 20-bit, loadable, enabled, up/down binary counter with no output load in each pair of LABs. Actual I_{CC} values should be verified during operation because this measurement is sensitive to the actual pattern in the device and the environmental operating conditions.

Figure 13 shows typical I_{CC} supply current versus frequency curves for FLASHlogic devices.

Figure 13. I_{CC} vs. Frequency for FLASHlogic Devices



Power-Up Cycle

Because V_{CC} rise times can vary significantly from one application to another, the device power-up cycle time varies. For a monotonic V_{CC} rise (1 ms/V minimum), the power-up cycle begins when V_{CC} reaches its minimum value and ends 100 µs after V_{CC} reaches the minimum value.

Internal power-up reset circuits ensure that all flipflops are reset to a logic low after the device has powered up. Also, the JTAG TAP controller is put into the test-logic-reset state. During power-up, EPX880 I/O pins are tri-stated; EPX8160 I/O pins are held high by an active-weak pull-up resistor. Upon completion of the power-up cycle, the outputs on an unprogrammed EPX880 device are placed in a high-impedance state. The outputs on an unprogrammed EPX8160 device are placed in a high-impedance state if V_{PP} is held below 2.0 V; the outputs are tri-stated if V_{PP} is held above 2.0 V.

Power-On Reset (POR)

FLASHlogic device configuration data can be reloaded from FLASH memory at any time by issuing a JTAG RESET instruction. For EPX880 and EPX8160 devices, the device configuration data from FLASH memory can also be reloaded by holding V_{PP} at a logic low (0.8 V maximum) for a minimum of 300 ns. By holding V_{PP} low during power-up, the power-up cycle can be delayed. The power-up cycle is completed within a delay of t_{RESET} after V_{PP} reaches 2.0 V (see Table 8). During normal operation, V_{PP} must be held at a logic high (2.4 V minimum) or tied to the V_{PP} supply (12.0 V) for EPX8160 devices.

Table 8. Reset Characteristics

Symbol	Parameter	Value	Conditions
t_{RESET}	JTAG reset time	150 µs maximum	Software control $V_{PP} \geq 2.0$ V

During reconfiguration or reprogramming, the JTAG RESET instruction is automatically issued by the PENGN or JED2JTAG software utilities provided with PLDshell Plus. It is not necessary to pull V_{PP} low for a reconfiguration or reprogram cycle.

For more information on configuring or programming FLASHlogic devices using the JTAG interface, go to the following documents:

- *Application Note 45 (Configuring FLASHlogic Devices)*
- *Application Note 39 (JTAG Boundary-Scan Testing in Altera Devices*

Pin Descriptions

Table 9 describes the pin names and descriptions for FLASHlogic devices.

Table 9. Pins Descriptions

Pin Name	Description
VCC, *Note (1)*	Supply voltage. Must be connected to 5.0 V.
GND	Ground connection.
VPP, *Note (1)*	Programming voltage. When programming FLASHlogic devices, 12.0 V must be supplied to this pin. When the EPX880 and EPX8160 devices are not in programming mode, VPP must be connected to VCC or VPP. The EPX880 and EPX8160 devices will reset themselves if VPP is held below 0.8 V for a minimum of 300 ns.
IN*n*	Input-only pins. These pins are not available in all packages. Unused inputs should be connected to VCC or GND.
TDI	Test data input. This pin is the boundary-scan serial data input to FLASHlogic devices. JTAG instructions and data are shifted into FLASHlogic devices on the TDI input pin on the rising edge of TCK. TDI can be left floating if unused.
TDO	Test data output. This is the boundary-scan serial data output from FLASHlogic devices. JTAG instructions and data are shifted out of FLASHlogic devices on the TDO output pin on the falling edge of TCK.
TCK	Test clock input. This input provides the boundary-scan clock for FLASHlogic devices. TCK clocks shift information and data into and out of the FLASHlogic devices during boundary-scan or programming modes. The maximum operating frequency of the BST clock is 8 MHz. TCK can be left floating if unused.
TMS	Test control input. This input provides the BST mode select for FLASHlogic devices. TMS can be left floating if unused.
VCCIO*n*, *Note (1)*	Supply voltage for the outputs of the LABs. Connecting these pins to 5.0 V causes the LAB to output 5.0-V signals. Connecting these pins to 3.3 V causes the LAB to output 3.3-V signals. These pins must always be connected to the desired output drive voltage.
CLK*n*	Global clock signals.
I/O*n*	Pins configurable as inputs or outputs. Unused I/O pins should be connected as shown in the Report File. The reserved pins must be left unconnected. During ICR and ISP, the I/O pins of FLASHlogic devices are tri-stated. In addition, the I/O pins for an EPX8160 device has a weak pull-up transistor.

Note:

(1) Proper power decoupling is required on all power pins. A 0.1-µF decoupling capacitor is recommended between each power pin and ground.

Device Pin-Outs

Tables 10 through 13 show the pin names and numbers for the pins in each device FLASHlogic device package.

Table 10. EPX880 Pin-Outs

Pin Name	84-Pin PLCC	132-Pin PQFP
CLK1	3	118
CLK2	45	52
TDI	11	132
TDO	10	131
TMS	52	65
TCK	53	66
VPP	4	119
VCCIO0	25	117
VCCIO1	2	116
VCCIO2	24	19
VCCIO3	67	86
VCCIO4	25	20
VCCIO5	66	85
VCCIO6	44	50
VCCIO7	67	51
VCCINT	26, 68	21, 87
GND	17, 23, 29, 38, 46, 59, 65, 71, 80	11, 17, 18, 27, 44, 53, 59, 77, 83, 84, 93, 110, 125
Dedicated Inputs	–	1, 2, 3, 4, 5, 33, 34, 35, 36, 37, 38, 67, 68, 69, 70, 71, 99, 100, 101, 102, 103, 104

Table 11. EPX880 I/O Pin-Outs (Part 1 of 2) *Note (1)*

LAB	MC	84-Pin J-Lead	132-Pin PQFP	LAB	MC	84-Pin J-Lead	132-Pin PQFP
0	0	5	120	1	10	1	115
0	1	–	121	1	11	84	114
0	2	–	122	1	12	83	113
0	3	6	123	1	13	82	112
0	4	–	124	1	14	81	111
0	5	7	126	1	15	79	109
0	6	–	127	1	16	78	108
0	7	8	128	1	17	77	107
0	8	–	129	1	18	76	106
0	9	9	130	1	19	75	105
2	20	22	16	3	30	69	88
2	21	21	15	3	31	–	89
2	22	20	14	3	32	–	90
2	23	19	13	3	33	70	91
2	24	18	12	3	34	–	92
2	25	16	10	3	35	72	94
2	26	15	9	3	36	–	95
2	27	14	8	3	37	73	96
2	28	13	7	3	38	–	97
2	29	12	6	3	39	74	98

Table 11. EPX880 I/O Pin-Outs (Part 2 of 2) *Note (1)*

LAB	MC	84-Pin J-Lead	132-Pin PQFP	LAB	MC	84-Pin J-Lead	132-Pin PQFP
4	40	27	22	5	50	64	82
4	41	–	23	5	51	63	81
4	42	–	24	5	52	62	80
4	43	28	25	5	53	61	79
4	44	–	26	5	54	60	78
4	45	30	28	5	55	58	76
4	46	–	29	5	56	57	75
4	47	31	30	5	57	56	74
4	48	–	31	5	58	55	73
4	49	32	32	5	59	54	72
6	60	43	49	7	70	47	54
6	61	42	48	7	71	–	55
6	62	41	47	7	72	–	56
6	63	40	46	7	73	48	57
6	64	39	45	7	74	–	58
6	65	37	43	7	75	49	60
6	66	36	42	7	76	–	61
6	67	35	41	7	77	50	62
6	68	34	40	7	78	–	63
6	69	33	39	7	79	51	64

Note:
(1) A dash (–) indicates that the macrocell is buried.

Table 12. EPX8160 Pin-Outs

Pin Name	208-Pin PQFP
CLK1	184
CLK2	181
CLK3	77
CLK4	80
TDI	1
TDO	208
TMS	105
TCK	104
VPP0	182
VPP1	79
VCCIO0/VCCIO2	204
VCCIO1/VCCIO3	161
VCCIO4/VCCIO6	13
VCCIO5/VCCIO7	144
VCCIO8/VCCIO10	57
VCCIO9/VCCIO11	100
VCCIO12/VCCIO14	40
VCCIO13/VCCIO15	117
VCCINT	14, 39, 118, 143
GND	7, 15, 21, 32, 38, 46, 67, 78, 90, 111, 119, 125, 136, 142, 150, 171,183, 194
Dedicated Inputs	52, 53, 54, 55, 56, 59, 61, 63, 65, 69, 71, 73, 75, 82, 84, 86, 88, 92, 94, 96, 98, 101, 102, 103, 156, 157, 158, 159, 160, 163, 165, 167, 169, 173, 175, 177, 179, 186, 188, 190, 192, 196, 198, 200, 202, 205, 206, 207

Table 13. EPX8160 I/O Pin-Outs (Part 1 of 3) *Note (1)*

LAB	MC	208-Pin PQFP	LAB	MC	208-Pin PQFP
0	0	185	1	10	180
0	1	187	1	11	178
0	2	189	1	12	176
0	3	191	1	13	174
0	4	193	1	14	172
0	5	195	1	15	170
0	6	197	1	16	168
0	7	199	1	17	166
0	8	201	1	18	164
0	9	203	1	19	162
2	20	6	3	30	151
2	21	–	3	31	–
2	22	–	3	32	–
2	23	5	3	33	152
2	24	–	3	34	–
2	25	4	3	35	153
2	26	–	3	36	–
2	27	3	3	37	154
2	28	–	3	38	–
2	29	2	3	39	155
4	40	8	5	50	149
4	41	9	5	51	148
4	42	10	5	52	147
4	43	11	5	53	146
4	44	12	5	54	145
4	45	16	5	55	141
4	46	17	5	56	140
4	47	18	5	57	139
4	48	19	5	58	138
4	49	20	5	59	137

Table 13. EPX8160 I/O Pin-Outs (Part 2 of 3) *Note (1)*

LAB	MC	208-Pin PQFP	LAB	MC	208-Pin PQFP
6	60	26	7	70	131
6	61	–	7	71	–
6	62	–	7	72	–
6	63	25	7	73	132
6	64	–	7	74	–
6	65	24	7	75	133
6	66	–	7	76	–
6	67	23	7	77	134
6	68	–	7	78	–
6	69	22	7	79	135
8	80	76	9	90	81
8	81	74	9	91	83
8	82	72	9	92	85
8	83	70	9	93	87
8	84	68	9	94	89
8	85	66	9	95	91
8	86	64	9	96	93
8	87	62	9	97	95
8	88	60	9	98	97
8	89	58	9	99	99
10	100	47	11	110	110
10	101	–	11	111	–
10	102	–	11	112	–
10	103	48	11	113	109
10	104	–	11	114	–
10	105	49	11	115	108
10	106	–	11	116	–
10	107	50	11	117	107
10	108	–	11	118	–
10	109	51	11	119	106

Table 13. EPX8160 I/O Pin-Outs (Part 3 of 3) *Note (1)*

LAB	MC	208-Pin PQFP	LAB	MC	208-Pin PQFP
12	120	45	13	130	112
12	121	44	13	131	113
12	122	43	13	132	114
12	123	42	13	133	115
12	124	41	13	134	116
12	125	37	13	135	120
12	126	36	13	136	121
12	127	35	13	137	122
12	128	34	13	138	123
12	129	33	13	139	124
14	140	27	15	150	130
14	141	–	15	151	–
14	142	–	15	152	–
14	143	28	15	153	129
14	144	–	15	154	–
14	145	29	15	155	128
14	146	–	15	156	–
14	147	30	15	157	127
14	148	–	15	158	–
14	149	31	15	159	126

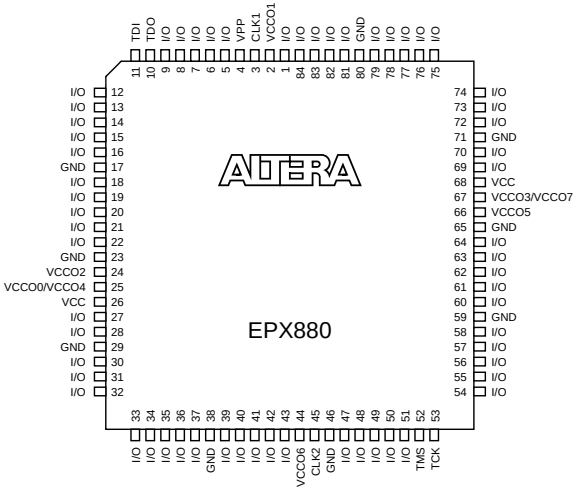
Note:
(1) A dash (–) indicates that the macrocell is buried.

Pin-Out Diagrams

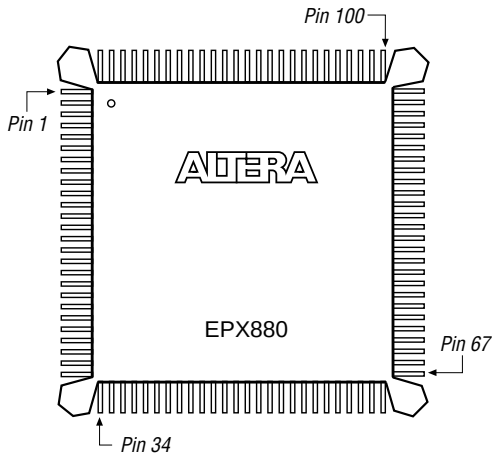
Figures 14 and 15 show the package pin-out diagrams for FLASHlogic devices.

Figure 14. EPX880 Package Pin-Out Diagram

Package outlines not drawn to scale. See Tables 10 and 11 for pin-out information.



84-Pin J-Lead



132-Pin PQFP

Figure 15. EPX8160 Package Pin-Out Diagram

Package outline not drawn to scale. See Tables 12 and 13 for pin-out information.