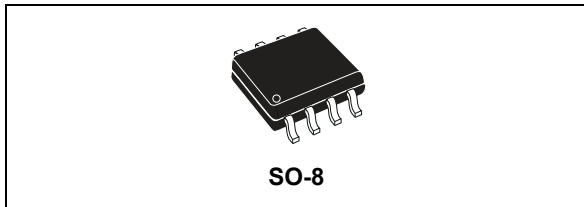


## High voltage high- and low-side driver for automotive applications

Datasheet - production data



### Features

- High voltage rail up to 550 V
- $dV/dt$  immunity  $\pm 50$  V/nsec in full temperature range
- Driver current capability
  - 400 mA source
  - 650 mA sink
- Switching times 50/30 nsec rise/fall with 1 nF load
- CMOS/TTL Schmitt-trigger inputs with hysteresis and pull down
- Internal bootstrap diode

- Outputs in phase with inputs
- Interlocking function
- AECQ100 automotive qualified

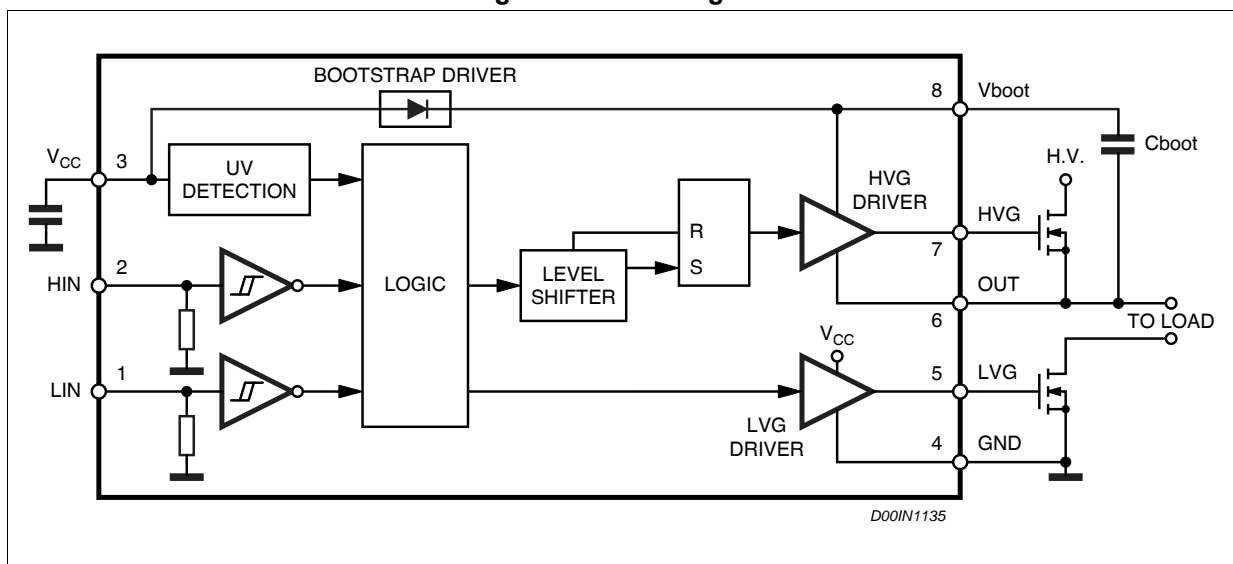
### Applications

- Drive inverters for HEV and EV
- HID ballasts, power supply units
- Motion driver for home appliances, factory automation, industrial drives

### Description

The A6387 is a high voltage device, manufactured with the BCD™ “offline” technology. It is a single chip half-bridge gate driver for N-channel Power MOSFETs or IGBTs. The high-side (floating) section is designed to stand a voltage rail of up to 550 V. The logic inputs are CMOS/TTL compatible for easy interfacing of the microcontroller or DSP.

Figure 1. Block diagram



# Contents

- 1      Electrical data ..... 3**
  - 1.1    Absolute maximum ratings ..... 3
  - 1.2    Thermal data ..... 3
  - 1.3    Recommended operating conditions ..... 3
  
- 2      Pin connection ..... 4**
  
- 3      Electrical characteristics ..... 5**
  - 3.1    AC operation ..... 5
  - 3.2    DC operation ..... 6
  
- 4      Input logic ..... 7**
  
- 5      Bootstrap driver ..... 8**
  - $C_{BOOT}$  selection and charging ..... 8
  
- 6      Typical characteristic ..... 10**
  
- 7      Package information ..... 11**
  
- 8      Ordering information ..... 13**
  
- 9      Revision history ..... 13**

# 1 Electrical data

## 1.1 Absolute maximum ratings

Table 1. Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
$V_{CC}$	Supply voltage	- 0.3	18	V
$V_{out}$	Output voltage	$V_{boot} - 18$	$V_{boot} + 0.3$	V
$V_{boot}$	Bootstrap voltage	- 0.3	568	V
$V_{hvg}$	High-side gate output voltage	$V_{out} - 0.3$	$V_{boot} + 0.3$	V
$V_{lvg}$	Low-side gate output voltage	- 0.3	$V_{CC} + 0.3$	V
$V_i$	Logic input voltage	- 0.3	$V_{CC} + 0.3$	V
$dV_{out}/dt$	Allowed output slew rate		50	V/ns
$P_{tot}$	Total power dissipation ( $T_A = 85\text{ °C}$ )		750	mW
$T_j$	Junction temperature		150	°C
$T_{stg}$	Storage temperature	-50	150	°C
ESD	Human Body Model	2		kV

## 1.2 Thermal data

Table 2. Thermal data

Symbol	Parameter	Value	Unit
$R_{th(JA)}$	Thermal resistance junction to ambient	150	°C/W

## 1.3 Recommended operating conditions

Table 3. Recommended operating conditions

Symbol	Pin	Parameter	Test condition	Min.	Max.	Unit
$V_{CC}$	3	Supply voltage		6.3	17	V
$V_{BO}^{(1)}$	8 - 6	Floating supply voltage			17	V
$V_{out}$	7	Output voltage		-6 <sup>(2)</sup>	530	V
$f_{sw}$		Switching frequency	HVG, LVG load $C_L = 1\text{ nF}$		400	kHz
$T_j$		Junction temperature		-40	125	°C

1.  $V_{BO} = V_{boot} - V_{out}$ .

2. LVG off.  $V_{CC} = 12\text{ V}$ .

## 2 Pin connection

Figure 2. Pin connection (top view)

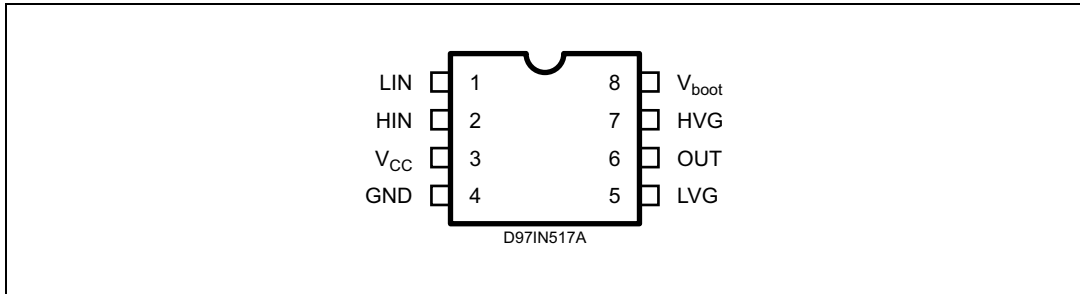


Table 4. Pin description

No.	Pin	Type	Function
1	LIN	I	Low-side driver logic input
2	HIN	I	High-side driver logic input
3	V <sub>CC</sub>	P	Low voltage power supply
4	GND	P	Ground
5	LVG <sup>(1)</sup>	O	Low-side driver output
6	OUT	P	High-side driver floating reference
7	HVG <sup>(1)</sup>	O	High-side driver output
8	V <sub>boot</sub>	P	Bootstrap supply voltage

1. The circuit provides less than 1 V on the LVG and HVG pins (at I<sub>sink</sub> = 10 mA). This allows the omitting of the “bleeder” resistor connected between the gate and the source of the external MOSFET normally used to hold the pin low.

### 3 Electrical characteristics

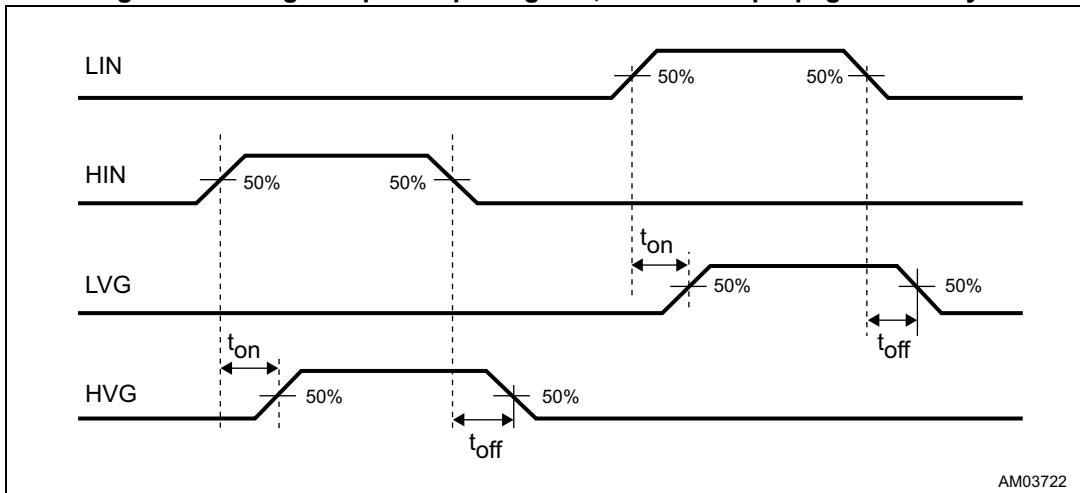
#### 3.1 AC operation

$V_{CC} = 15\text{ V}$ ;  $T_J = -40\text{ }^\circ\text{C} \div 125\text{ }^\circ\text{C}$ , unless otherwise specified.

**Table 5. AC operation electrical characteristics**

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
$t_{on}$	1 vs. 5 2 vs. 7	High/low-side driver turn-on propagation delay	$V_{out} = 0\text{ V}$ $V_{boot} = V_{CC}$ $C_L = 1\text{ nF}$	40	120	240	ns
$t_{off}$	1 vs. 5 2 vs. 7	High/low-side driver turn-off propagation delay		40	110	210	ns
$t_r$	5, 7	Rise time	$C_L = 1\text{ nF}$		50	100	ns
$t_f$	5, 7	Fall time			30	80	ns

**Figure 3. Timing of input/output signals; turn-on/off propagation delays**



### 3.2 DC operation

$V_{CC} = 15\text{ V}$ ;  $T_J = -40\text{ }^\circ\text{C} \div 125\text{ }^\circ\text{C}$ , unless otherwise specified

**Table 6. DC operation electrical characteristics**

Symbol	Pin	Parameter	Test condition	Min.	Typ.	Max.	Unit
<b>Low supply voltage section</b>							
$V_{CC\_thON}$	3	$V_{CC}$ UV turn-on threshold		5.5	6	6.3	V
$V_{CC\_thOFF}$		$V_{CC}$ UV turn-off threshold		5	5.5	6	V
$V_{CC\_hys}$		$V_{CC}$ UV hysteresis		0.3	0.5	0.7	V
$I_{qccu}$		Undervoltage quiescent supply current	$V_{CC} \leq 5\text{ V}$		150	220	$\mu\text{A}$
$I_{qcc}$		Quiescent current			250	320	$\mu\text{A}$
$R_{DSon}$		Bootstrap driver on resistance <sup>(1)</sup>	LVG ON		125		$\Omega$
<b>Bootstrapped supply voltage section <sup>(2)</sup></b>							
$I_{QBO}$	8	$V_{BO}$ quiescent current	HVG ON			100	$\mu\text{A}$
$I_{LK}$		High voltage leakage current	$V_{hvg} = V_{out} = V_{boot} = 550\text{ V}$			10	$\mu\text{A}$
<b>High/low-side driver</b>							
$I_{so}$	5, 7	High/low-side source short-circuit current	$V_{IN} = V_{ih}$ ( $t_p < 10\ \mu\text{s}$ )	300	400		mA
$I_{si}$		High/low-side sink short-circuit current	$V_{IN} = V_{il}$ ( $t_p < 10\ \mu\text{s}$ )	450	650		mA
<b>Logic inputs</b>							
$V_{il}$	1,2	Low level logic threshold voltage				1.4	V
$V_{ih}$		High level logic threshold voltage		3.2			V
$I_{ih}$		High level logic input current	$V_{IN} = 15\text{ V}$	8	20	40	$\mu\text{A}$
$I_{il}$		Low level logic input current	$V_{IN} = 0\text{ V}$			1	$\mu\text{A}$

1.  $R_{DS(on)}$  is tested in the following way:

$$R_{DS(on)} = \frac{(V_{CC} - V_{BOOT1}) - (V_{CC} - V_{BOOT2})}{I_1(V_{CC}, V_{BOOT1}) - I_2(V_{CC}, V_{BOOT2})}$$

where  $I_1$  is pin 8 current when  $V_{BOOT} = V_{BOOT1}$ ,  $I_2$  when  $V_{BOOT} = V_{BOOT2}$ .

2.  $V_{BO} = V_{boot} - V_{out}$ .

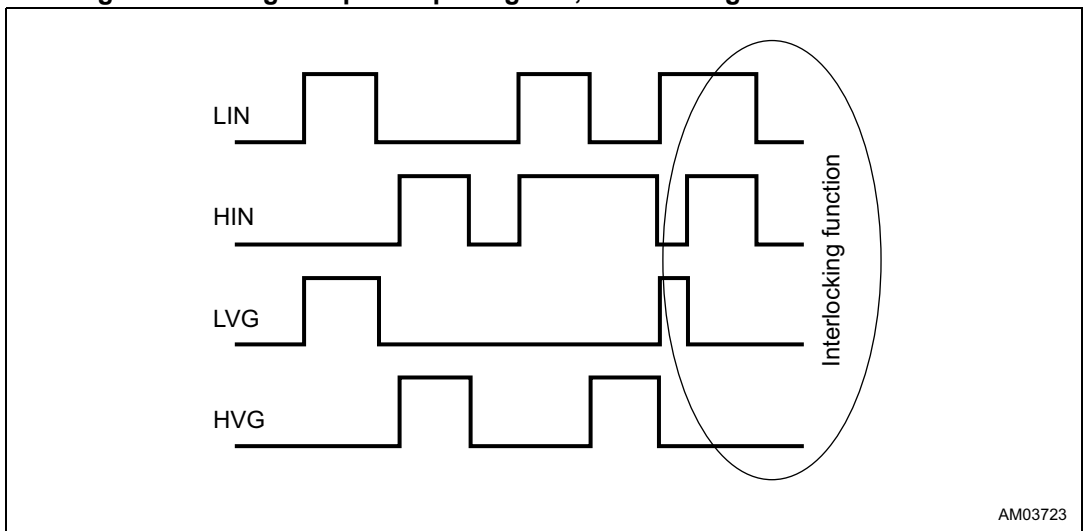
## 4 Input logic

The A6387 input logic is  $V_{CC}$  (17 V) compatible. An interlocking feature is offered (see [Table 7](#)) to avoid undesired simultaneous turn-on of both power switches driven.

**Table 7. Input logic**

Input		Output	
HIN	LIN	HVG	LVG
0	0	0	0
0	1	0	1
1	0	1	0
1	1	0	0

**Figure 4. Timing of input/output signals; interlocking waveforms definition**



AM03723

## 5 Bootstrap driver

A bootstrap circuitry is needed to supply the high voltage section. This function is normally accomplished by a high voltage fast recovery diode (*Figure 5 a*). In the A6387 device a patented integrated structure replaces the external diode. It is realized by a high voltage DMOS, driven synchronously with the low-side driver (LVG), with a diode in series, as shown in *Figure 5 b*. An internal charge pump (*Figure 5 b*) provides the DMOS driving voltage.

### C<sub>BOOT</sub> selection and charging

To choose the proper C<sub>BOOT</sub> value the external MOS can be seen as an equivalent capacitor. This capacitor C<sub>EXT</sub> is related to the MOS total gate charge:

#### Equation 1

$$C_{EXT} = \frac{Q_{gate}}{V_{gate}}$$

The ratio between the capacitors C<sub>EXT</sub> and C<sub>BOOT</sub> is proportional to the cyclical voltage loss. It must be:

$$C_{BOOT} \gg C_{EXT}$$

For example: if Q<sub>gate</sub> is 30 nC and V<sub>gate</sub> is 10 V, C<sub>EXT</sub> is 3 nF. With C<sub>BOOT</sub> = 100 nF the drop would be 300 mV.

If HVG must be supplied for a long period, the C<sub>BOOT</sub> selection must take into account also the leakage and quiescent losses.

For example: HVG steady-state consumption is lower than 100 μA, therefore, if HVG T<sub>ON</sub> is 5 ms, C<sub>BOOT</sub> must supply 0.5 μC to C<sub>EXT</sub>. This charge on a 1 μF capacitor means a voltage drop of 0.5 V.

The internal bootstrap driver offers a big advantage: the external fast recovery diode can be avoided (it usually has very high leakage current).

This structure can work only if V<sub>OUT</sub> is close to GND (or lower) and, in the meantime, the LVG is on. The charging time (T<sub>charge</sub>) of the C<sub>BOOT</sub> is the time in which both conditions are fulfilled and it must be long enough to charge the capacitor.

The bootstrap driver introduces a voltage drop due to the DMOS R<sub>DSon</sub> (typical value: 125 Ω). This drop can be neglected at low switching frequency, but it should be taken into account when operating at high switching frequency.

*Equation 2* is useful to compute the drop on the bootstrap DMOS:

#### Equation 2

$$V_{drop} = I_{charge} R_{dson} \rightarrow V_{drop} = \frac{Q_{gate}}{T_{charge}} R_{dson}$$

where Q<sub>gate</sub> is the gate charge of the external power MOS, R<sub>DSon</sub> is the ON-resistance of the bootstrap DMOS, and T<sub>charge</sub> is the charging time of the bootstrap capacitor.



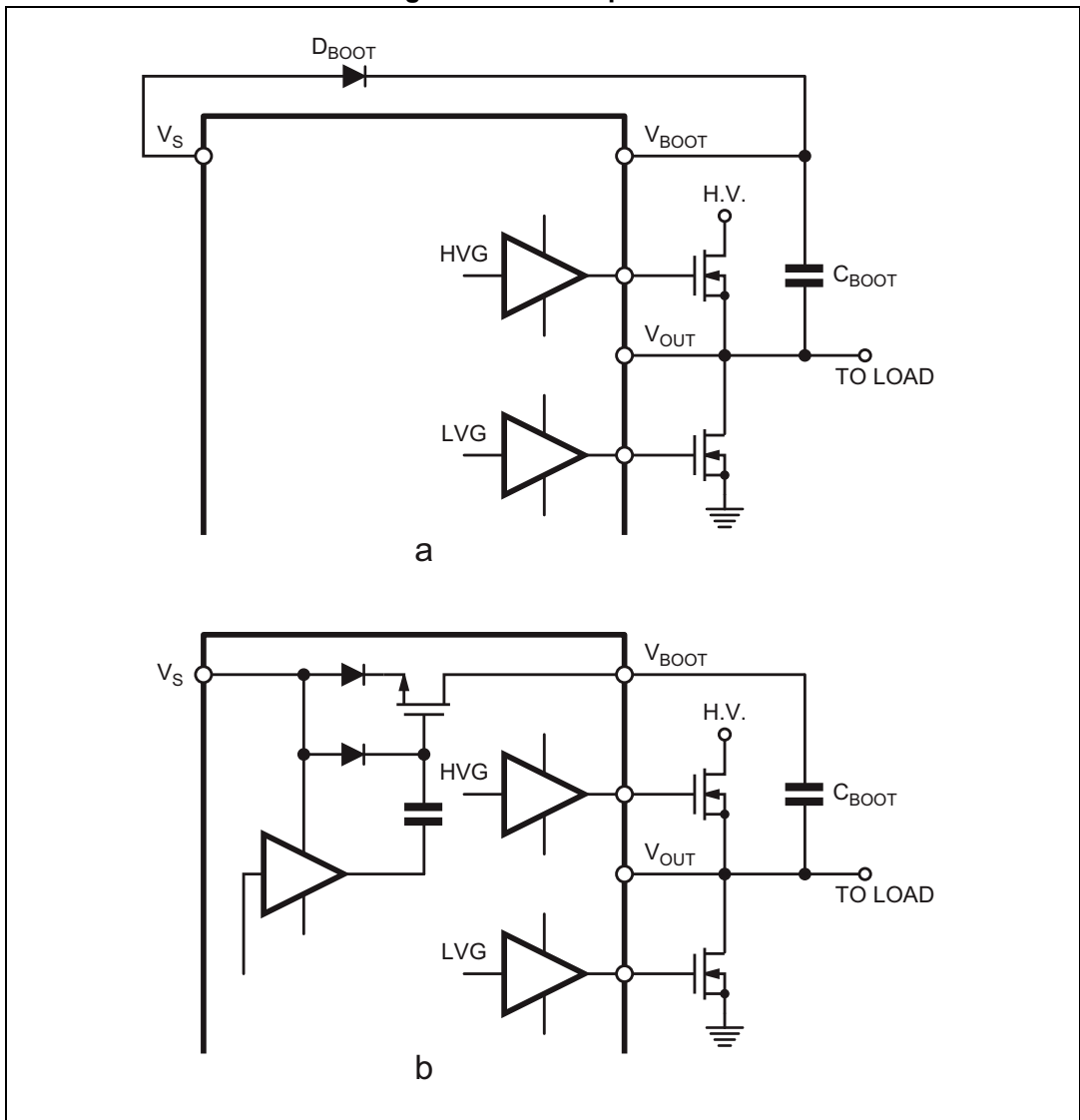
For example: using a power MOS with a total gate charge of 30 nC, the drop on the bootstrap DMOS is about 1 V, if the  $T_{charge}$  is 5  $\mu s$ . In fact:

**Equation 3**

$$V_{drop} = \frac{30nC}{5\mu s} \cdot 125\Omega \sim 0.8V$$

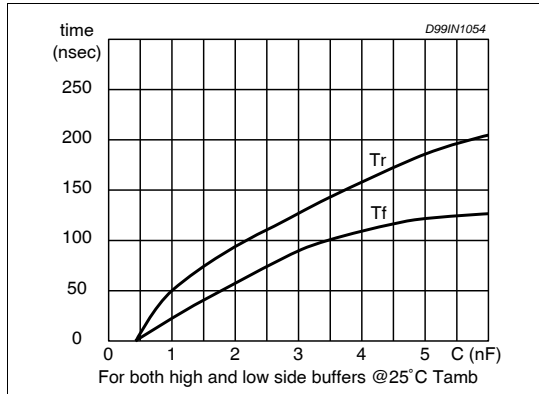
$V_{drop}$  should be taken into account when the voltage drop on  $C_{BOOT}$  is calculated: if this drop is too high, or the circuit topology doesn't allow a sufficient charging time, an external diode can be used.

**Figure 5. Bootstrap driver**

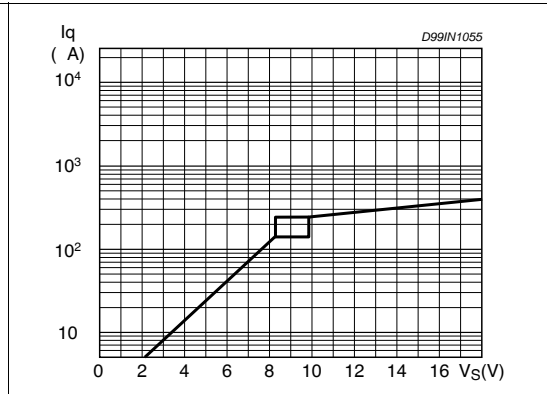


# 6 Typical characteristic

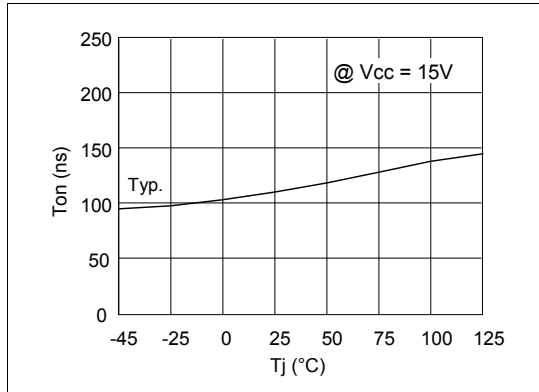
**Figure 6. Typical rise and fall times vs. load capacitance**



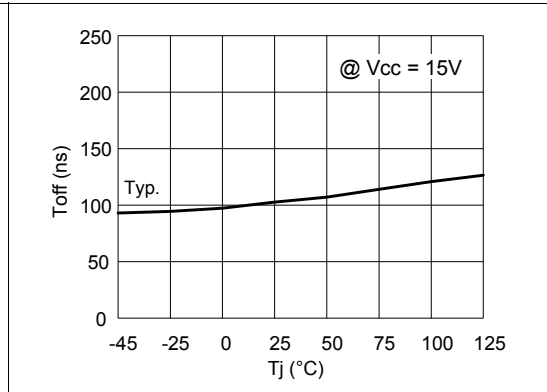
**Figure 7. Quiescent current vs. supply voltage**



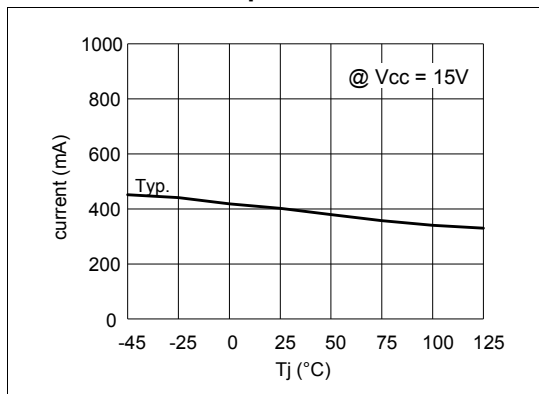
**Figure 8. Turn-on time vs. temperature**



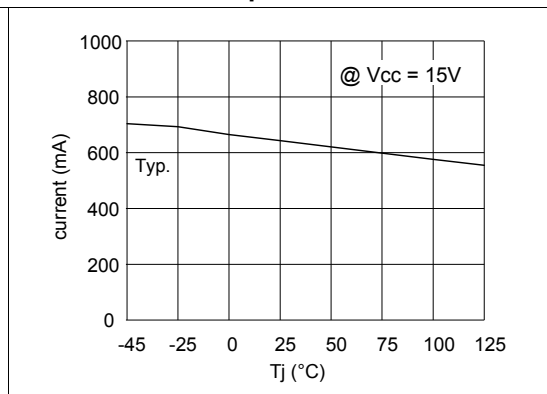
**Figure 9. Turn-off time vs. temperature**



**Figure 10. Output source current vs. temperature**



**Figure 11. Output sink current vs. temperature**



# 7 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Figure 12. SO-8 package outline

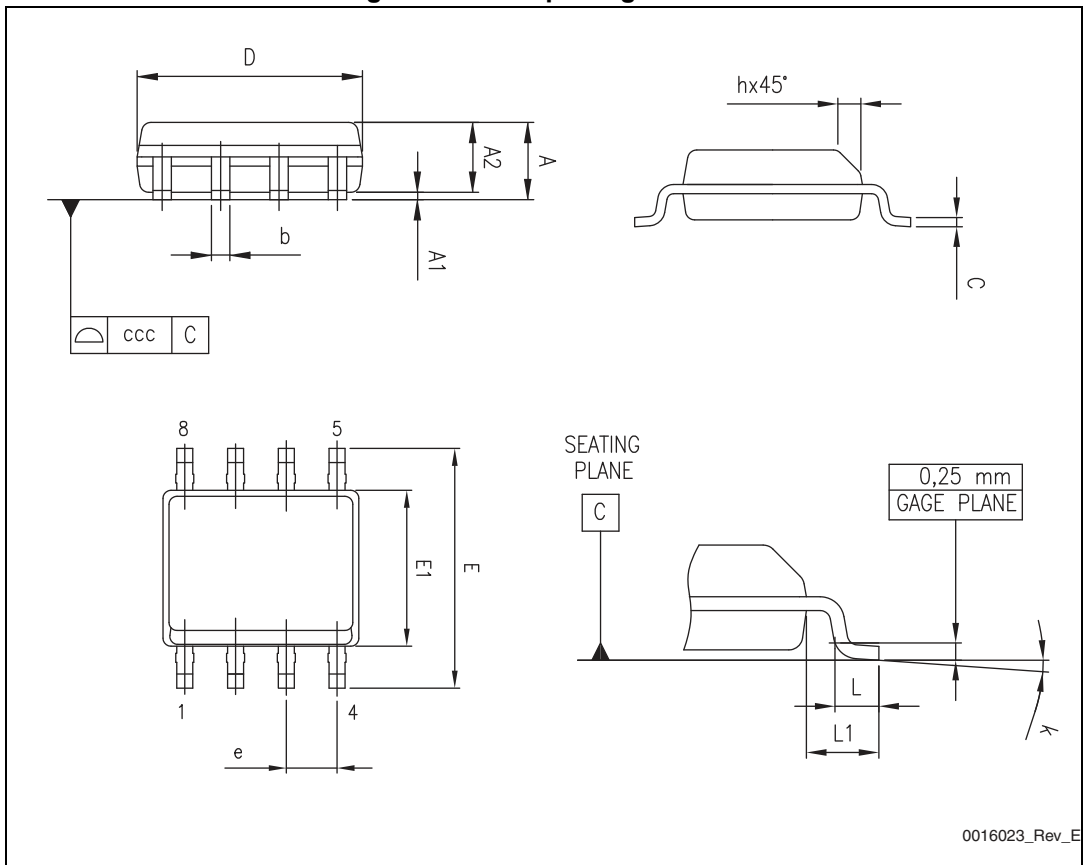


Table 8. SO-8 package mechanical data

Symbol	Dimensions (mm)		
	Min.	Typ.	Max.
A			1.75
A1	0.10		0.25
A2	1.25		
b	0.28		0.48
c	0.17		0.23
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e		1.27	
h	0.25		0.50
L	0.40		1.27
L1		1.04	
k	0°		8°
ccc			0.10

## 8 Ordering information

**Table 9. Ordering information**

Order code	Package	Packaging
A6387D	SO-8	Tube
A6387DTR	SO-8	Tape and reel

## 9 Revision history

**Table 10. Document revision history**

Date	Revision	Changes
05-Jul-2012	1	First release
10-Oct-2013	2	Updated: <a href="#">Section : Features on page 1</a> (added "AECQ100 compliant"). <a href="#">Section : Applications on page 1</a> added: – Drive inverters for HEV and EV, – HID ballasts, power supply units, – Motion driver for home appliances, factory automation, industrial drives. <a href="#">Table 1 on page 3</a> (removed note below <a href="#">Table 1</a> ). Minor corrections throughout document.
22-Oct-2013	3	Updated <a href="#">Section : Features on page 1</a> ("replaced AECQ100 compliant" by "AECQ100 automotive qualified").
14-Apr-2014	4	Updated <a href="#">Section 3.1: AC operation on page 5</a> (added <a href="#">Figure 3</a> ). Updated <a href="#">Section 4: Input logic on page 7</a> (added <a href="#">Figure 4</a> ).
04-Feb-2015	5	Updated <a href="#">Table 1</a> (added <i>Human Body Model</i> parameter). Updated minimum supply voltage in <a href="#">Table 3</a> and maximum $V_{CC}$ UV turn-on threshold voltage in <a href="#">Table 6</a> . Corrected typo in $R_{DS(on)}$ testing equation in footnote of <a href="#">Table 6</a> . Updated <a href="#">Figure 5: Bootstrap driver</a> .

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries (“ST”) reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST’s terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers’ products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved