QorIQ Multicore Processor Development

QorIQ T1040 Reference Design Board

The QorIQ T1040 Reference Design Board (T1040RDB) is a high-performance computing evaluation, development and test platform supporting the QorIQ T1040/20, T1042/22 and T2081 processors built on Power Architecture® technology.

OVERVIEW

The board, with its 1.5 GHz T1040 processor and rich I/O mix, is intended for evaluation of the QorIQ T1 family of processors in networking and Ethernet-centric applications, such as mixed control and data plane in fixed routers, switches, Internet access devices, firewall and other packet filtering applications, as well as general-purpose embedded computing.

The QorIQ T1040RDB can help shorten your time to market. The board, which exercises most capabilities of the device, can serve as a reference for customers' own hardware development. It can also be used as a debug tool to check behaviors on the board compared to behaviors seen on customer boards. It can be used for software development and performance evaluation prior to the customers' own board being ready. The T1040RDB additionally provides support for the pin-compatible superset device, the T2081 processor.

The T1040RDB supports one PCI Express® slot, two mini-PCI Express connectors, an SD/MMC connector interface and two USB 2.0 receptacles. These components, integrated with the T1040 processor, provide an application-specific platform that can help you get a jump start on your next design. The T1040RDB also supports 8 GB of DDR4 at 1600 MHz, 128 MB of NOR flash, a 1 GB NAND flash and a SATA interface.

QorIQ T1040RDB is loaded with the Linux® Software Development Kit (SDK) for QorIQ Processors. The SDK includes a 64-bit SMP Linux kernel, hugetlbfs for applications with a large memory footprint, user space DPAA for high-performance packet handling, u-Boot, the GCC tool chain, virtualization support and many other features.

TARGET APPLICATIONS

- Enterprise equipment:
  - Fixed routers
  - Ethernet switches
  - UTM equipment
- Service provider:
  - Edge routers
  - Mobile backhaul
- Aerospace, defense and government:
  - Ruggedized network
  - appliances
- Industrial computing:
  - Single board computers
  - Factory automation
  - Smart grid

QorIQ T1040RDB BOARD FEATURES

Processor

- QorIQ T1040, 1.5 GHz core with 1600 MT/s DDR4 data rate
- Multiple SysClk inputs for generating various device frequencies

Memory

- 8 GB unbuffered DDR4 SDRAM UDIMM/
- 128 MB NOR flash, 16-bit
- 1 GB SLC NAND flash
- SD connector to interface
- SATA interface

PCI Express

- One x4 PCIe slot
- Two Mini-PCIe connectors

USB 2.0

- Dual USB slot, connected to USB PHY

Ethernet

- One on-board SGMII 10/100/1G Ethernet Port
- Two on-board RGMII 10/100/1G Ethernet ports (T1040 only)
- Two on-board QSGMII 10/100/1G PHYs For 8 GE ports (T1040 only)
- One on-board XFI 10G EDC for 10G SFP+ Port (T2081 only)

UART

- Two UART ports at up to 115200 bps

TDM

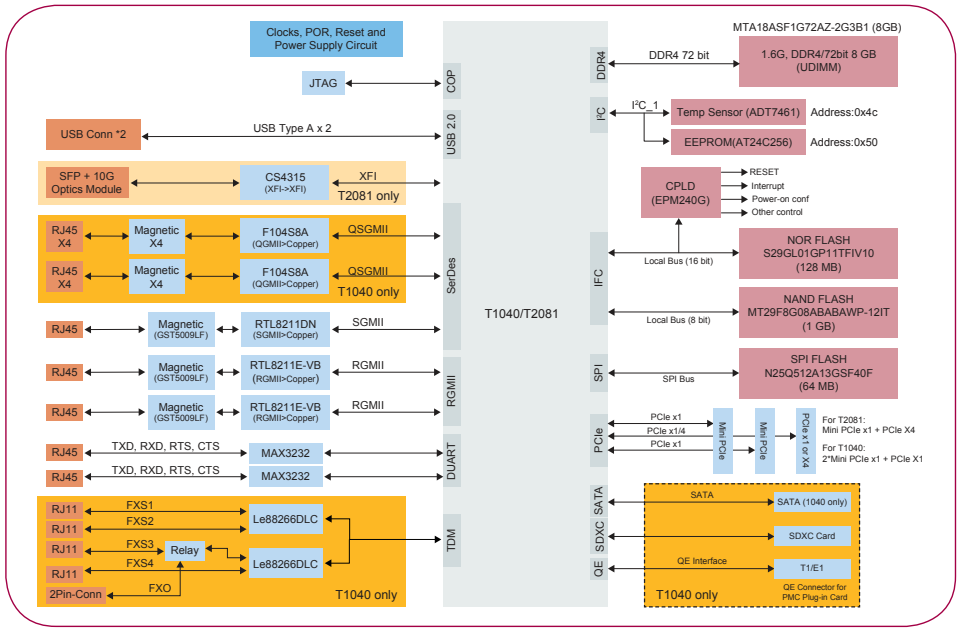
- JTAG/COP for debug
- Thermal Monitor

ABOUT THE QorIQ T1 FAMILY

The QorIQ T1 family is based on the 64-bit e5500 core, built on Power architecture technology, offering speeds of up to 1500 MHz. It has a three-level cache hierarchy with 32 KB of instruction and data cache per core, 256 KB of low-latency backside L2 cache per core, and a 256 KB shared platform cache. This scalable, pin-compatible family also features the industry's first 64-bit embedded processor with an integrated Gigabit Ethernet switch, which simplifies hardware design, reduces power and overall system cost. The processor's I/O includes 8 SerDes lanes running at up to 5 Gb/s multiplexed across four PCI Express controllers, up to five Gigabit Ethernet interfaces, an 8-port Gigabit Ethernet switch (T1040 and T1020 only) and two SATA 2.0 interfaces.

The QorIQ T1 family of communications processors also supports a 64-bit DDR3L and DDR4 SDRAM memory controller with ECC running at up to 1600 MT/s data rate. It includes two highspeed USB2.0 controllers (with integrated PHY), four UARTs, an SD/MMC interface, an integrated flash controller supporting NAN and NOR flash memory, four I²C and SPI. Also included are the accelerator blocks, collectively known as the Data Path Acceleration Architecture, that offload various tasks from the core, including routine packet handling, security algorithm calculation and pattern matching. In addition, the T1 family of processors integrates a QUICC Engine module offering support for legacy protocols such as TDM, HDLC, UART and ISDN; and includes support for hardware-assisted virtualization.

QorIQ T1040 REFERENCE DESIGN BLOCK DIAGRAM



www.nxp.com/QorIQ

Document Number:
T1040RDBFS REV 2

BUILT ON Power