Click here for production status of specific part numbers.

MAX77501

110V_{PK-PK} High-Efficiency Piezo Haptic Actuator Boost Driver

General Description

The MAX77501 is a high-efficiency controller driver for piezo haptic actuators and is optimized for driving up to 2µF piezo elements. It can generate a single-ended haptic waveform of up to 110V_{PK-PK} amplitude from a 2.8V to 5.5V input power supply or a single cell Li+ battery. Memory playback and haptic waveforms real-time streaming modes are supported.

A 25MHz SPI interface provides full system access and control, including fault reporting and monitoring. This allows for a rapid 600µs playback start-up time from shutdown. The on-board memory can be dynamically allocated as multiple waveforms storage or as a FIFO buffer. The IC also implements an ultra-low power boost architecture providing the lowest power consumption solution for a haptic actuator driver.

Built-in undervoltage lockout (UVLO), cycle-by-cycle overcurrent limit, overvoltage and thermal shutdown protections ensure safe operation under abnormal operating conditions.

The MAX77501 is available in a 30-bump, 0.4mm pitch, wafer-level package (WLP).

Applications

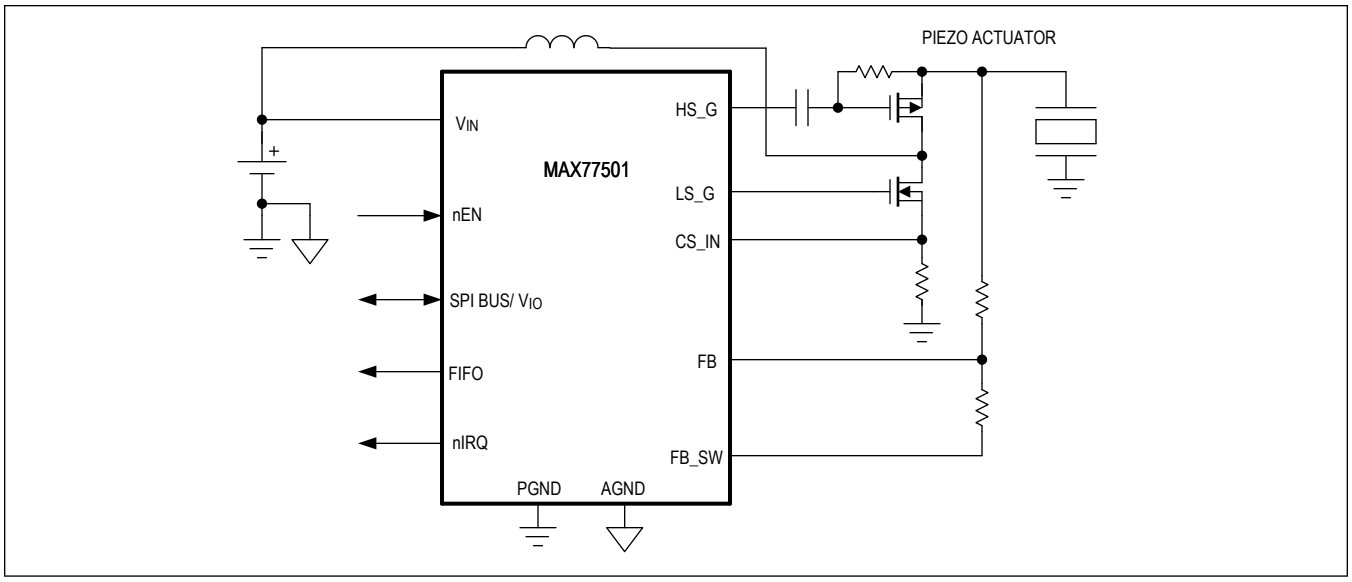
- Smartphones, Tablets/E-readers, Game Consoles
- Keyboard, Mice, Remote Controls, and Peripherals
- Haptic/Tactile Feedback Enabled Equipment

Benefits and Features

- 110V_{PK-PK} Haptic Waveforms Generation
- Optimized for up to 2µF Haptic Piezo Actuator
- 2.8V to 5.5V Input Supply Range
- 600µs Start-Up Time to Haptic Playback
- High-Efficiency, Low I_Q Extends Battery Life
  - 75µA Standby Current/1µA Shutdown Current
  - Maxim Patented Ultra-Low Power Boost Architecture
- 12-Bit Haptic Waveform Playback DAC
- Real-Time Streaming and RAM Playback Modes
  - 9k FIFO Buffer with FIFO Ready Status Signal
  - 8k RAM Buffer for Waveforms Storage
- 25MHz SPI Interface
  - SPI Ready, Warning and Fault Conditions Interrupt
- Protection Features
  - Programmable Cycle-by-Cycle Overcurrent Limit, 130V Overvoltage, UVLO, and Thermal Protections
- Small Size and Low Profile
  - 2.42mm x 2.02mm, 30 Bump WLP

***Ordering Information* appears at end of data sheet.**

Simplified Application Circuit



19-100584; Rev 1; 8/19

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CF2P to PGND ..... V_5 - 0.1V to V_{DD_H} + 0.1V
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V_{SS_H} to PGND ..... -0.3V to V_{DD_H} + 0.3V
Continuous Power Dissipation (Multilayer Board) (T_A = +70°C, derate 40°C/W above +70°C) 240mW
Storage Temperature Range ..... -40°C to +150°C
Junction Temperature ..... +150°C
Soldering Temperature (reflow) ..... +260°C
Operation Junction Temperature ..... -40°C to +125°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Package Information

WLP

Package Code	W302M2+1
Outline Number	21-100276
Land Pattern Number	Refer to *Application Note 1891*
Thermal Resistance, Four-Layer Board:	
Junction to Ambient (θ_{JA})	49.38°C/W

For the latest package outline information and land patterns (footprints), go to *www.maximintegrated.com/packages*. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to *www.maximintegrated.com/thermal-tutorial*.

Electrical Characteristics—Top Level

(V_{IN} = 3.6V, T_A = +25°C, limits are 100% tested at T_A = +25°C, unless otherwise noted. Min and Max limits are guaranteed by design and characterization from T_A = T_J = -40°C to +125°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
GENERAL OPERATING CONDITIONS							
Input Supply Range	V_{IN}			2.8	3.6	5.5	V
Shutdown Supply Current	I_{SHDN}	V_{IN} = 5.5V, nEN = V_{IN}	T_A = +25°C	-1	0.1	+1	µA
			T_A = +85°C		150		nA
			T_A = +125°C		750		
Standby Current	I_Q	nEN = 0V, STANDBY STATE			75	150	µA
Shutdown to Standby State Time Delay	$SHDN\_STDBY_{DLY}$				250		µs
Standby to Play Ready Time Delay	$STDBY\_PLAY_{DLY}$				350		µs
Maximum V_{OUT}	V_{OUT_MAX}	High Range: FULL_SCALE = 1			120		V
		Low Range: FULL_SCALE = 0			70		

Electrical Characteristics—Top Level (continued)

(V_{IN} = 3.6V, T_A = +25°C, limits are 100% tested at T_A = +25°C, unless otherwise noted. Min and Max limits are guaranteed by design and characterization from T_A = T_J = -40°C to +125°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Minimum V_{OUT}	V_{OUT_MIN}				10		V
Operating Current	I_{IN}	C_{PIEZO} = 330nF, frequency = 130Hz, V_{OUT} = 60Vpp			60		mA
		C_{PIEZO} = 680nF, frequency = 130Hz, V_{OUT} = 60Vpp			80		
		C_{PIEZO} =1µF, frequency = 130Hz, V_{OUT} = 60Vpp			90		
Inductor Peak Current Limit	I_{LIM}	nEN = 0V R_{SENSE} = 100mΩ	I_{LIM_SEL}<1:0> = (0, 0)		1		A
			I_{LIM_SEL}<1:0> = (0, 1)		2		
			I_{LIM_SEL}<1:0> = (1, 0)		3		
			I_{LIM_SEL}<1:0> = (1, 1)		4		
Haptic Sample Rate	FSR_{SEL}	SMP_RATE <1:0> = (0,0)		7.6	8	8.4	kHz
		SMP_RATE <1:0> = (0,1)		30.4	32	33.6	
		SMP_RATE <1:0> = (1,0)		45.6	48	50.4	
Undervoltage Lockout	UVLO	Rising V_{IN}		2.646	2.7	2.754	V
		Falling V_{IN}		2.548	2.6	2.652	
Undervoltage-Lockout Hysteresis	$UVLO_{HYST}$	UVLO hysteresis			100		mV
Thermal Shutdown	$THERM_{SHDN}$	nEN = 0V			165		°C
Thermal-Shutdown Hysteresis	$THERM_{HYST}$	nEN = 0V			21		°C
Total Harmonic Distortion + Noise	THD+N	C_{PIEZO} = 680nF, frequency = 130Hz, V_{OUT} = 80Vpp			1		%
V_{DD} Output Voltage	V_{DD}	V_{IN} = 3.8V, nEN = 0V, no load			1.8		V
V_{DD} Output Voltage Accuracy	V_{DDACC}			-5		+5	%
V_{CC} Supply Range	V_{CC}	Haptic playback mode		4.75	5	5.25	V
V_{CC} Load Current (Internal)	I_{LDVCC}	V_{CC} = 5V, haptic playback mode			105		µA
V_{OUT} Overvoltage Regulation	V_{OUTOVP}	FULL_SCALE = 1			130		V
		FULL_SCALE = 0			80		
DAC							
DAC Resolution	DAC_{RES}				12		bit
DAC Linearity	DAC_{DNL}	No compression		-2		+2	LSB
DAC FS Gain Accuracy	DAC_{FS_ACC}	No compression		-2		+2	%
DAC Output Resistance	DAC_{RO}				1.2		MΩ

Electrical Characteristics—Top Level (continued)

(V_{IN} = 3.6V, T_A = +25°C, limits are 100% tested at T_A = +25°C, unless otherwise noted. Min and Max limits are guaranteed by design and characterization from T_A = T_J = -40°C to +125°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Full-Scale DAC Output Voltage	DAC_{FS}			1.2275	1.25	1.2725	V
CHARGE-PUMPS							
5V Charge-Pump Overall Accuracy	CP_{V5_ACC}	2.8V < V_{IN} < 5.5V and I_{LOAD} < 7mA			±10		%
9V Charge-Pump Overall Accuracy	$CP1_{VDDH\_ACC}$	2.8V < V_{IN} < 5.5V and I_{LOAD} < 7mA			±10		%
V_{DD_H} Charge-Pump Switching Frequency	CP_{VDDH_FSW}			0.95	1	1.05	MHz
5V Charge-Pump Start-Up Time	CP_{V5_TSU}	C_{F1} = 150nF, C_{V5} = 1µF	0 to 95% of final V_5 output		200		µs
V_{DD_H} Charge-Pump Start-Up Time	CP_{VDDH_TSU}	C_{F2} = 150nF, C_{VDD_H} = 1µF	0 to 95% of final V_{DD_H} output		300		µs
V_{SS_H} Accuracy	V_{SSHACC}	V_{IN} = 3.6V, C_{VSS_H} = 2.2nF		V_{DD_H} - 1.9V	V_{DD_H} - 1.8V	V_{DD_H} - 1.7V	V
5V Charge-Pump Active Discharge Resistance	CP_{V5_RPD}	STANDBY state			200		Ω
V_{DD_H} Charge-Pump Active Discharge Resistance	CP_{VDDH_RPD}				200		Ω
5V Charge-Pump VOK Threshold	$CP_{V5\_VOK\_TH\_R}$	5V VOK comparator rising threshold		4.35	4.5	4.65	V
	$CP_{V5\_VOK\_TH\_F}$	5V VOK comparator falling threshold		3.85	4	4.17	
V_{DD_H} Charge-Pump VOK Threshold	$CP_{VDDH\_VOK\_TH\_R}$	10V VOK comparator rising threshold		6.7	7	7.2	V
	$CP_{VDDH\_VOK\_TH\_F}$	10V VOK comparator falling threshold		5.63	5.9	6.09	
V_{DD_H} Charge-Pump Enable Threshold	$CP_{VDDH\_EN\_TH}$	10V Enable comparator rising threshold		3.35	3.5	3.65	V
		10V Enable comparator falling threshold		2.95	3.1	3.25	
V_{DD_H} Charge-Pump Enable Hysteresis	$CP_{VDDH\_EN\_HYS}$	10V Enable comparator hysteresis			0.4		V
FIFO STATUS PIN							
FIFO Status VOL	VOL_{FIFO}	I_{SINK} = 2mA				0.4	V
FIFO Status Falling Edge Time	t_{FALL_FIFO}	C_{LOAD} = 25pF			2		ns
FIFO Leakage Current	$FIFO_{LKG}$	V_{IN} = V_{FIFO} = 5.5V	T_A = +25°C	-1		+1	µA
			T_A = +85°C		±0.01		
			T_A = +125°C		±0.01		

Electrical Characteristics—Top Level (continued)

(V_{IN} = 3.6V, T_A = +25°C, limits are 100% tested at T_A = +25°C, unless otherwise noted. Min and Max limits are guaranteed by design and characterization from T_A = T_J = -40°C to +125°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
ENABLE INPUT (nEN)							
nEN Input Leakage Current	I_{nEN_LKG}	V_{IN} = V_{nEN} = 5.5V	T_A = +25°C	-1		+1	µA
			T_A = +85°C		±0.01		
			T_A = +125°C		±0.01		
nEN Input Falling Threshold	$V_{TH\_nEN\_F}$	nEN falling				1	V
nEN Input Rising Threshold	$V_{TH\_nEN\_R}$	nEN rising		V_{IN} - 1			V
OPEN-DRAIN INTERRUPT OUTPUT (nIRQ)							
nIRQ VOL	VOL_{nIRQ}	I_{SINK} = 2mA				0.4	V
nIRQ Falling Edge Time	t_{FALL_nIRQ}	C_{nIRQ} = 25pF			2		ns
nIRQ Leakage Current	I_{nIRQ_LKG}	V_{IN} = V_{nIRQ} = 5.5V	T_A = +25°C	-1		+1	µA
			T_A = +85°C		±0.01		
			T_A = +125°C		±0.01		
ILIM Flag Count	$ILIM_{FLG\_CNT}$	ILIM Interrupt Flags	ILIM_FLAG<1,0> = (0,0)		128		
			ILIM_FLAG<1,0> = (0,1)		256		
			ILIM_FLAG<1,0> = (1,0)		1024		
			ILIM_FLAG<1,0> = (1,1)		2048		

Electrical Characteristics—Boost Controller

(V_{IN} = 3.6V, T_A = +25°C, limits are 100% tested at T_A = +25°C, unless otherwise noted. Min and Max limits are guaranteed by design and characterization from T_A = T_J = -40°C to +125°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
GMAMP						
GMAMP Transconductance	$GMAMP_{GM}$		25	30	33	µS
Input Common Mode Range	$GMAMP_{CMR}$		0.23		3.4	V
GMAMP Output Swing	GM_{VO}	No load	0.1		V_{CC} - 0.1	V
GMAMP Maximum Output Current	$GMAMP_{IO}$		7			µA
PREAMPLIFIER						
Preamplifier Gain	AV_{PA}			2.818		V/V
Preamplifier Gain Accuracy	AV_{PA_ACC}		-2		+2	%

Electrical Characteristics—Boost Controller (continued)

(V_{IN} = 3.6V, T_A = +25°C, limits are 100% tested at T_A = +25°C, unless otherwise noted. Min and Max limits are guaranteed by design and characterization from T_A = T_J = -40°C to +125°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
SLP COMPARATOR							
SLP Comparator Level Shift	SLP_{CMP_LS}	SLP rising threshold when LX switches low to high			V_{COMP} - 0.4		V
SLP Rising Threshold Propagation Delay	CMP_{TPD}	Rising input slew rate = 1V/µs			10		ns
SLP Discharge Resistance	SLP_{DSCHG}				8		Ω
SLP Leakage	SLP_{LKG}	V_{SLP} = 5V	T_A = +25°C	-1		+1	µA
			T_A = +85°C		±50		nA
			T_A = +125°C		±250		
COT COMPARATOR							
COT Comparator Threshold	COT_{CMP_TH}	COT rising threshold when LX switches high to low			V_{IN}/10		V
COT Rising Threshold Propagation Delay	COT_{TPD_R}	Rising input slew rate = 1V/µs			10		ns
COT Discharge Resistance	COT_{DSCHG}				8		Ω
COT Leakage	COT_{LKG}	V_{COT} = 5V	T_A = +25°C	-1		+1	µA
			T_A = +85°C		±50		nA
			T_A = +125°C		±250		
ILIM COMPARATOR							
ILIM Comparator Threshold	$ILIM_{CMP\_TH}$	ILIM_SEL<1,0> = (0,0)		90	100	110	mV
		ILIM_SEL <1:0> = (0,1)		190	200	210	
		ILIM_SEL<1,0> = (1,0)		285	300	315	
		ILIM_SEL<1,0> = (1,1)		380	400	420	
ILIM Rising Theshold Propagation Delay	$t_{PD\_ILIM\_CMP}$	Rising input slew rate = 1V/µs			10		ns
OVP COMPARATOR							
OVP Comparator Threshold	OVP_{CMP_TH}	OVP rising threshold when LX switches low to high		3.336	3.512	3.688	V
OVP Rising Threshold Propagation Delay	OVP_{CMP_TPD}	Rising input slew rate = 1V/µs			10		ns
GATE DRIVER							
HS_G Gate Driver Pullup Strength	HSG_{P_RON}			0.5	1	2	Ω
HS_G Gate Driver Pulldown Strength	HSG_{N_RON}			21	33	52	Ω
LS_G Gate Driver Pulldown Strength	LSG_{N_RON}			0.25	0.5	1	Ω
LS_G Gate Driver Pullup Strength	LSG_{P_RON}			21	30	49	Ω

Electrical Characteristics—Boost Controller (continued)

(V_{IN} = 3.6V, T_A = +25°C, limits are 100% tested at T_A = +25°C, unless otherwise noted. Min and Max limits are guaranteed by design and characterization from T_A = T_J = -40°C to +125°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
T_{ON} AND T_{OFF} CONTROLLER							
Maximum T_{ON}	TON_{MAX}	Maximum on time low-side NFET		2	3.6	7	µs
Maximum T_{OFF}	$TOFF_{MAX}$	Maximum on time high-side PFET		1	2	4	µs
Minimum T_{ON}	TON_{MIN}	Minimum on time low-side NFET			50		ns
Minimum T_{OFF}	$TOFF_{MIN}$	Minimum on time high-side PFET			10		ns
FB_SW PIN							
FB_SW Input Resistance	FB_SW_{IR}				54		Ω
FB_SW Leakage	FB_SW_{LKG}	V_{FB_SW} = 5V	T_A = +25°C	-1		+1	µA
			T_A = +85°C		±50		nA
			T_A = +125°C		±250		
CS_IN LEAKAGE							
CS_IN Leakage Current		nEN = 0V, SSB = V_{IO}	T_A = +25°C	-1		+1	µA
			T_A = +85°C		±0.01		
			T_A = +125°C		±0.01		

Electrical Characteristics—SPI Communication Controller

(V_{IN} = 3.6V, T_A = +25°C, limits are 100% tested at T_A = +25°C, unless otherwise noted. Min and Max limits are guaranteed by design and characterization from T_A = T_J = -40°C to +125°C.) (Note 1)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI						
V_{IO} Supply Voltage	V_{IO}		1.62	1.8	1.98	V
Input Leakage Current (SSB, SCLK, MOSI)	$LEAK_{SPI}$	T_A = +25°C	-1	0.1	+1	µA
		T_A = +85°C		±10		nA
		T_A = +125°C		±250		
Input Capacitance (SSB, SCLK, MOSI)	C_IN_{SPI}			10		pF
SPI Input Logic Low Voltage (SSB, SCLK, MOSI)	VIL_{SPI}				0.4	V
SPI Input Logic High Voltage (SSB, SCLK, MOSI)	VIH_{SPI}		1.4			V
SPI Input Logic Hysteresis	VI_{HYST}			275		mV
SPI Logic VOH	VOH_{MISO}	IOH_{MISO} = 2mA	V_{IO}-0.4			V
SPI Logic VOL	VOL_{MISO}	IOL_{MISO} = 2mA			0.4	V
MISO Leakage Current	$MISO_{LKG}$	SSB = V_{IO}, T_A = +25°C	-1		+1	µA
		SSB = V_{IO}, T_A = +125°C		0.1		

Electrical Characteristics—SPI Communication Controller (continued)

(V_{IN} = 3.6V, T_A = +25°C, limits are 100% tested at T_A = +25°C, unless otherwise noted. Min and Max limits are guaranteed by design and characterization from T_A = T_J = -40°C to +125°C.) (Note 1)

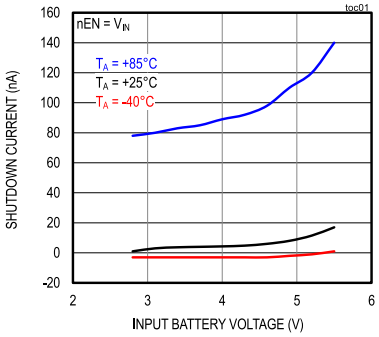
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SPI INTERFACE TIMING						
SPI Operating Frequency	f_{SPI}	V_{IO} = 1.8V		25		MHz
MOSI Input Valid to SCLK Rising Edge	t_{SU_MOSI}	V_{IO} = 1.8V	10			ns
MOSI Input Valid from SCLK Rising Edge	t_{HD_MOSI}	V_{IO} = 1.8V	10			ns
MISO Output Valid from SCLK Falling Edge	t_{D_MISO}	V_{IO} = 1.8V, C_L = 50pF			19	ns
MISO Rising/Falling Time	t_R, t_F	V_{IO} = 1.8V, C_L = 20pF			10	ns
SSB Setup Time Before SCLK	t_{SU_SSB}	V_{IO} = 1.8V	20			ns
SSB Hold Time After SCLK	t_{HD_SSB}	V_{IO} = 1.8V	20			ns
Minimum SSB HIGH Pulse Width	$t_{SSB\_H(MIN)}$	V_{IO} = 1.8V	50			ns

Note 1: See the *Typical Applications Circuit*.

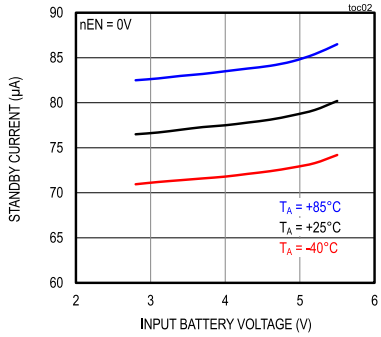
Typical Operating Characteristics

(Typical Applications Circuit, V_{IN} = 3.7V, V_{IO} = 1.8V, L = 10µH, T_A = +25°C, unless otherwise noted. See Table 13 for the components chosen for specific piezo capacitance values (C_{PIEZO}) listed.)

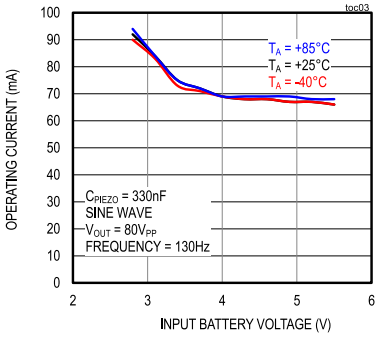
SHUTDOWN CURRENT vs. INPUT BATTERY VOLTAGE



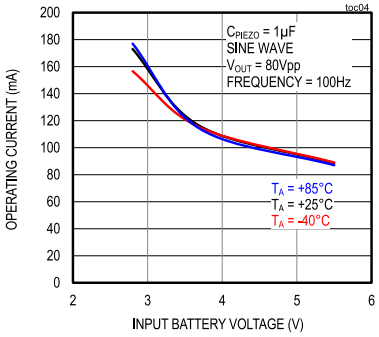
STANDBY CURRENT vs. INPUT BATTERY VOLTAGE



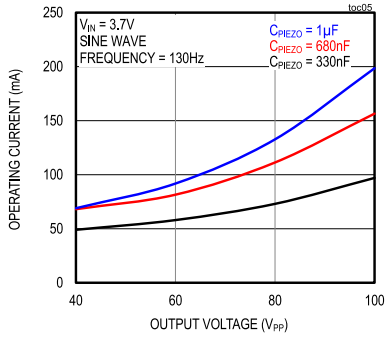
OPERATING CURRENT vs. INPUT BATTERY VOLTAGE



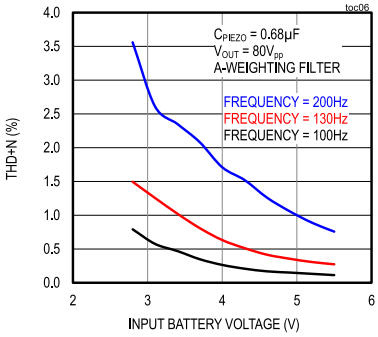
OPERATING CURRENT vs. INPUT BATTERY VOLTAGE



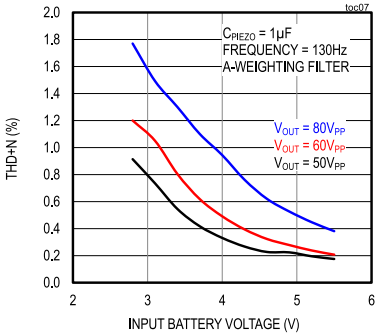
OPERATING CURRENT vs. PEAK-TO-PEAK OUTPUT VOLTAGE



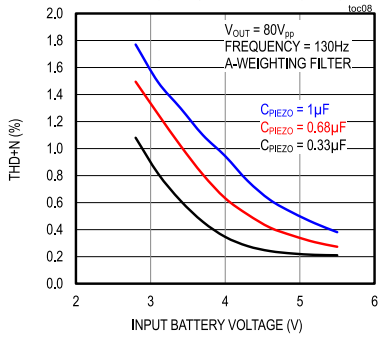
THD+N vs. INPUT BATTERY VOLTAGE



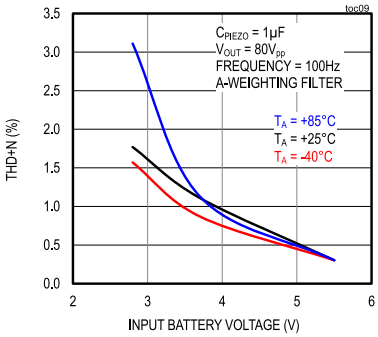
THD+N vs. INPUT BATTERY VOLTAGE



THD+N vs. INPUT BATTERY VOLTAGE



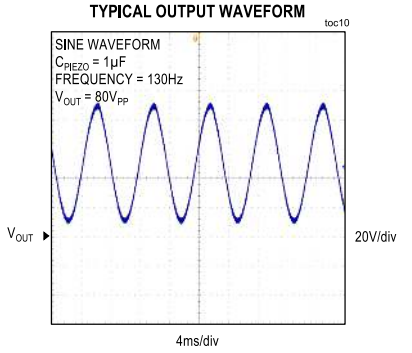
THD+N vs. INPUT BATTERY VOLTAGE



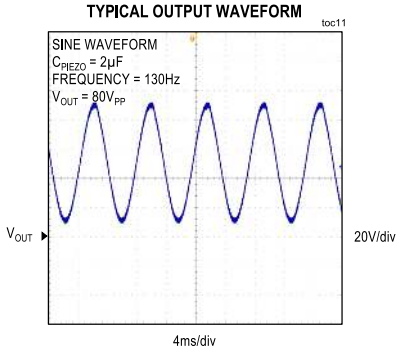
Typical Operating Characteristics (continued)

(Typical Applications Circuit, V_{IN} = 3.7V, V_{IO} = 1.8V, L = 10µH, T_A = +25°C, unless otherwise noted. See Table 13 for the components chosen for specific piezo capacitance values (C_{PIEZO}) listed.)

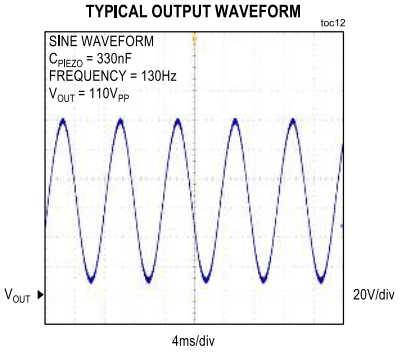
TYPICAL OUTPUT WAVEFORM



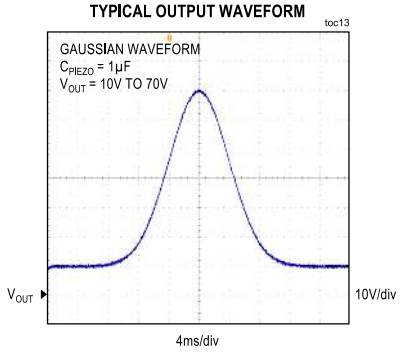
TYPICAL OUTPUT WAVEFORM



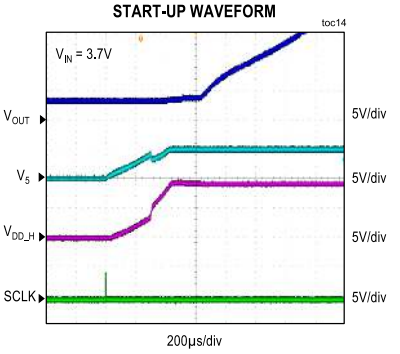
TYPICAL OUTPUT WAVEFORM



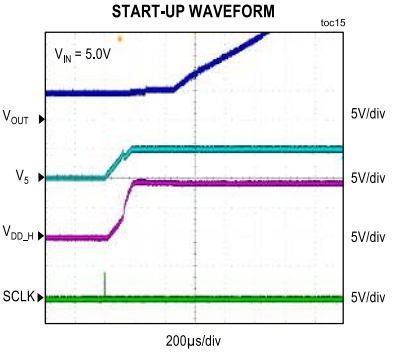
TYPICAL OUTPUT WAVEFORM



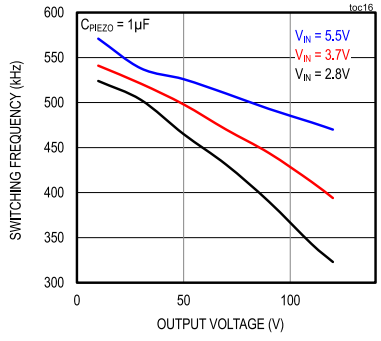
HAPTIC PLAYBACK START-UP WAVEFORM



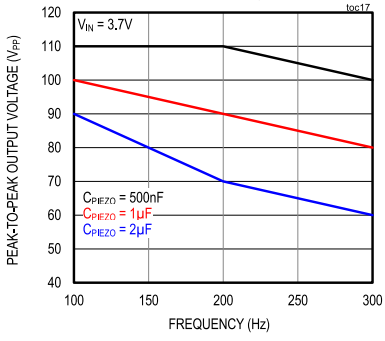
HAPTIC PLAYBACK START-UP WAVEFORM



SWITCHING FREQUENCY vs. OUTPUT VOLTAGE

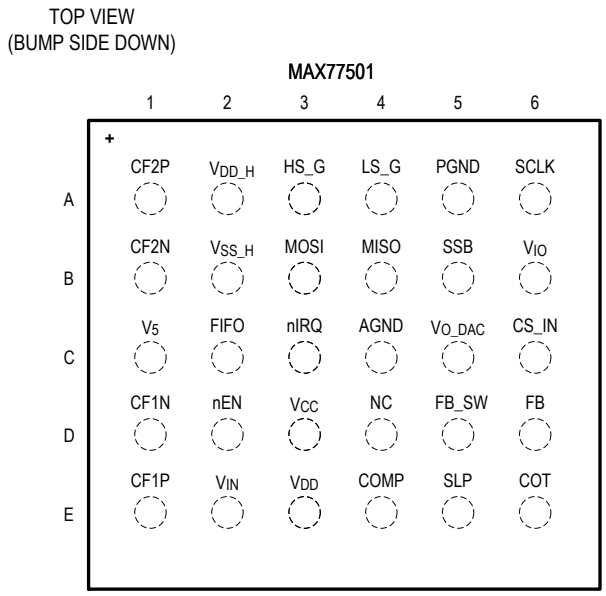


MAXIMUM PEAK-TO-PEAK OUTPUT VOLTAGE vs. SINE WAVE FREQUENCY



Bump Configurations

30 WLP



30 WLP
(2.02mm x 2.42mm x 0.70mm)

Bump Descriptions

PIN	NAME	FUNCTION
A5	PGND	Power Ground. Connect the PGND pin to the PCB ground plane. Refer to the *PCB Layout Guidelines* section for more information.
C4	AGND	Analog Ground. The AGND pin must be connected to PGND, preferably close to the PGND pin. See the *PCB Layout Guidelines* section for more information.
E2	V_{IN}	Voltage Input Supply Pin. Bypass to AGND with a 1µF ceramic capacitor close to the IC. There should be two separate supply paths from the input power supply, a high-current path to the inductor and a separate, low-current path to V_{IN}. See the *Typical Application Circuit* for more information.
B2	V_{SS_H}	High-Side Voltage Reference. Connect a 2.2nF decoupling capacitor for the high-side gate driver from V_{SS_H} to the V_{DD_H} pin.
A2	V_{DD_H}	Gate Driver Supply Voltage Output. Bypass this pin with a 1µF capacitor to PGND. This pin is the output of the second charge pump and is approximately 9V.
E3	V_{DD}	Internal Logic Supply Voltage Output. 1.8V output from internal bias block, powered from V_{IN}. Bypass with 1µF to AGND. Do not use for external loads.
C1	V_5	5 Volt Internal Charge Pump Output. V_5 is a regulated charge pump output voltage powered by V_{IN}. Bypass with 1µF to PGND. Do not use for external loads.
D3	V_{CC}	Low Noise Analog Supply Input. Connect a 2.2µF capacitor from this pin to AGND close to the IC. Connect a low value resistor (typically 1Ω) from V_5 to this pin.
B6	V_{IO}	SPI Logic I/O Supply Input. Bypass with a 1µF capacitor to AGND.
B5	SSB	SPI Chip Select Logic Input. Active-low.

Bump Descriptions (continued)

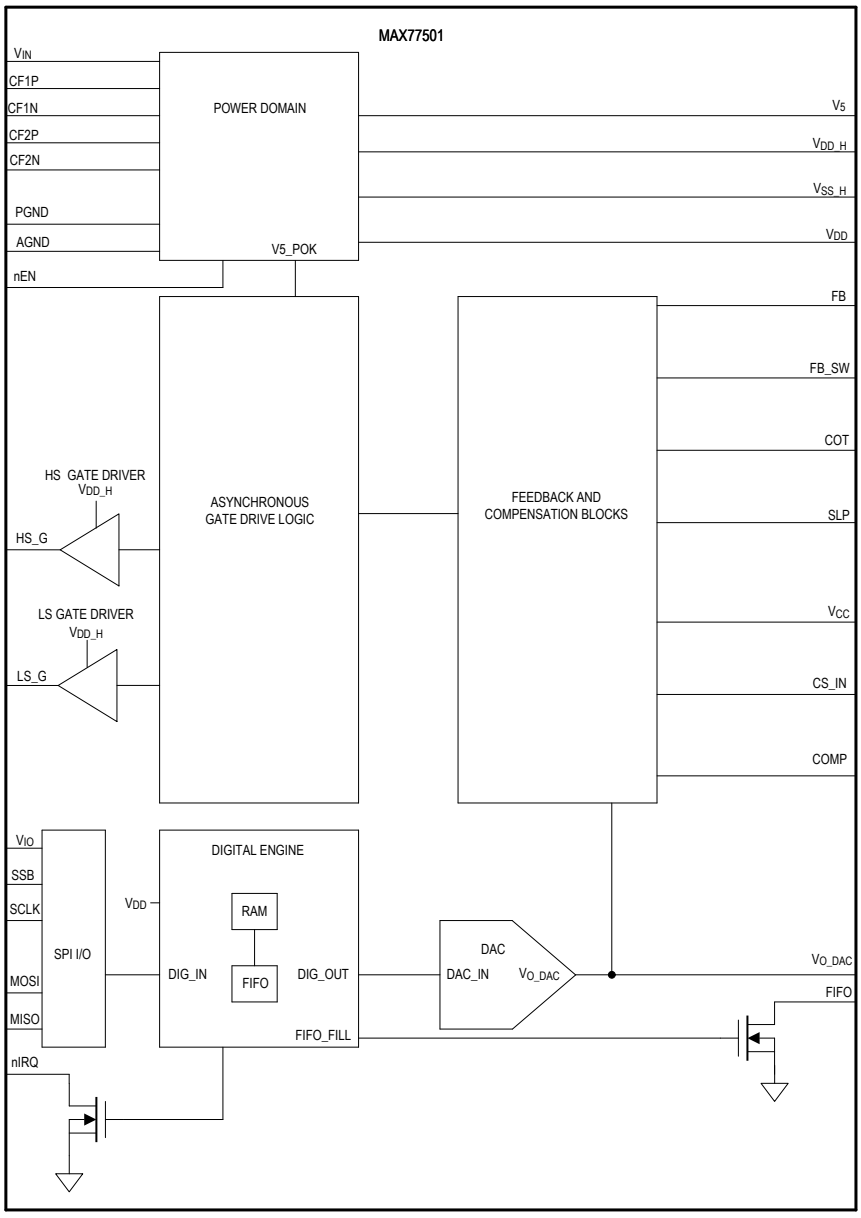
PIN	NAME	FUNCTION
B3	MOSI	SPI Serial Data Input (Master Output Slave Input).
B4	MISO	SPI Serial Data Output (Master Input Slave Output). MISO is high-Z with SSB = V_{IO}.
A6	SCLK	SPI Serial Clock Input.
E1	CF1P	5V Charge Pump Fly Cap, Positive Pin. Connect a 150nF capacitor from this pin to CF1N.
D1	CF1N	5V Charge Pump Fly Cap, Negative Pin. Connect a 150nF capacitor from this pin to CF1P.
A1	CF2P	9V Charge Pump Fly Cap, Positive Pin. Connect a 150nF capacitor from this pin to CF2N.
B1	CF2N	9V Charge Pump Fly Cap, Negative Pin. Connect a 150nF capacitor from this pin to CF2P.
A3	HS_G	High-Side Gate Driver Output. Connect a 10nF capacitor (150V minimum rating) from this pin to the gate of the external P-Channel power FET (see the *High Side PFET Drive applications information* section).
A4	LS_G	Low-Side Gate Driver Output. Connect this pin to the gate of the external power NFET.
D6	FB	Voltage Feedback Input. Connect a resistor from V_{OUT} to this pin and another resistor from this pin to either AGND or to the FB_SW pin. The two resistors form a resistor divider to set the closed-loop gain of the system. Route the resistor divider close to the IC and away from clock, logic or other digital signals. The FB_SW pin is off (high-Z) when the part is in shutdown or standby modes reducing leakage current from V_{OUT} if desired. See the *Full-Scale Options* section for more information on selecting resistor values.
C5	V_{O_DAC}	DAC Output. Connect a 39pF filter capacitor from this pin to AGND to provide a LPF function to the DAC output signal. The LPF reduces clock and sampling frequency energy at the DAC output (i.e., anti-aliasing) before driving the boost converter.
E4	COMP	Compensation Network Input. Connect the external compensation components from this pin to AGND as shown in the *External Component Selection Guide* section. Place these components as close to the COMP pin as possible.
C6	CS_IN	Current Sense Input. Connect this pin to a 390pF capacitor to AGND and to the slope-compensation capacitor (see the Slope Compensation section). Additionally, connect a 100Ω from this pin to the current sense resistor thereby forming a low-pass filter between the current sense resistor and the CS_IN pin.
D2	nEN	Active-Low Enable Input. Driving nEN low causes the IC to enter STANDBY mode. Connect a pullup resistor from this pin to V_{IN} for shutdown. If nEN is driven from a source (e.g., a µP) that is not 6V tolerant, then an external FET can be used as a level shift. See the *Turn-On Sequence* section for details on the nEN functionality.
C2	FIFO	Open-Drain FIFO Status Flag Output. The FIFO pin is active-low and indicates the fill status (see the *FIFO Full, Empty, and Almost Empty* section for more information). An external pullup resistor to V_{IO} is required to use this pin function. Leave this pin unconnected if not used.
D4	NC	Leave this pin unconnected.
E6	COT	Computed Off-Time Input. Connect a resistor from V_{OUT} to this pin and a capacitor from this pin to AGND to form a Low-Pass Filter from V_{OUT}. The time constant of this filter partly determines the switching frequency of the boost converter (typically ~ 20µs for 500kHz switching frequency). See the *Switching Frequency and COT Timer Operation* section for more information.
E5	SLP	Slope-Compensation Input Pin. Connect a resistor from V_{OUT} to this pin, a resistor from V_5 to this pin, and a capacitor from this pin to the CS_IN pin. See the *Slope Compensation* section for more details.
D5	FB_SW	Feedback Resistor Termination Input. Connect the low-side feedback resistor (from FB) to this pin to reduce resistive load on V_{OUT} during SHUTDOWN. Leave this pin unconnected if not used. See the *Feedback Switch Functionality* section for more details.

Bump Descriptions (continued)

PIN	NAME	FUNCTION
C3	nIRQ	Active-Low Interrupt Request Output. An external pullup resistor to V_{IO} (e.g., 100kΩ) is required to use this pin function. The nIRQ is an active-LOW signal and is used to indicate a number of internal interrupt and fault conditions. See the nIRQ description in the *Interrupts and Fault Conditions* section.

Functional Diagrams

Simplified Block Diagram



Detailed Description—Top Level

The MAX77501 is a highly-efficient piezo driver specifically developed for haptic, audio, or other transducer applications. The IC converts a stored or streamed digital input signal into a high voltage drive waveform up to 110Vpp (i.e., 10V minimum to 120V maximum V_{OUT}). A proprietary, highly-efficient DC-to-AC, single-ended wave-shaping conversion process drives a piezo element, while consuming minimum input power.

An internal charge pump generates a regulated 5V (V_5), which then drives a second, voltage-doubling charge pump to generate a 9V (V_{DD_H}) voltage rail used by the gate drivers to drive the external power FETs. The high-side gate drive (HS_G) is AC coupled to level-shift the gate drive to V_{OUT} and drives the high-side PFET. An external, 10V Zener diode and a parallel 20kΩ resistor resets the PFET gate charge to turn it off when HS_G goes high. In this way, the PFET gate logic signal follows V_{OUT} at about one diode voltage above V_{OUT} to about 9V below V_{OUT} during each off time.

State Diagram

The MAX77501 has three primary modes of operation:

- A low current SHUTDOWN mode where all of the internal blocks are off.
- A STANDBY mode where a minimal set of circuits are active to receive SPI commands.
- A fully enabled HAPTIC PLAYBACK mode.

Figure 1 describes this state diagram and how to move between each of the three states as well as other, intermediary states.

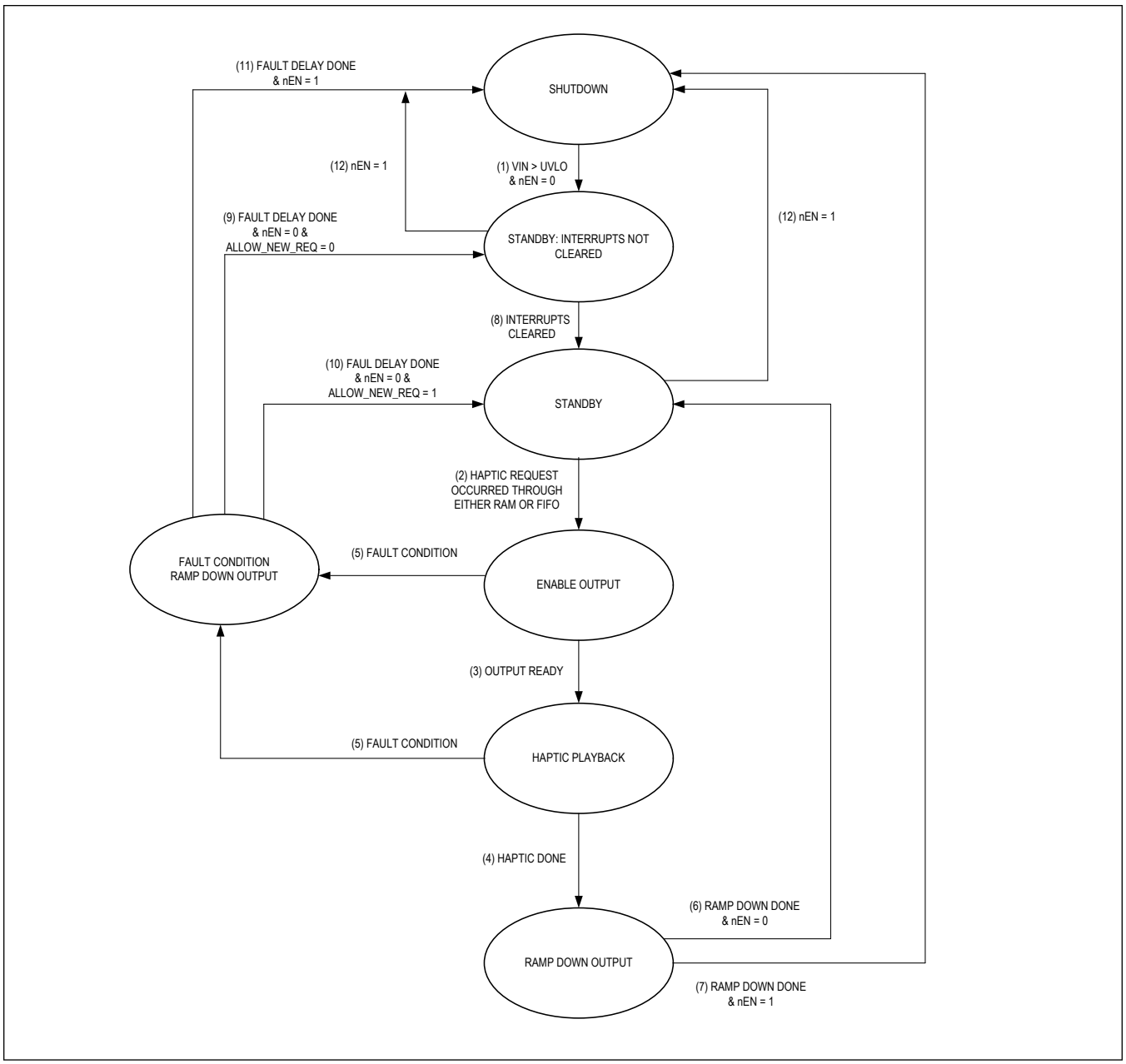


Figure 1. State Diagram

Table 1. State Diagram Description

STATE/ TRANSITION	DESCRIPTION
SHUTDOWN	The IC is in SHUTDOWN mode with low shutdown current. All functionality is off and the SPI communication bus does not function.
(1) V_{IN} > UVLO and nEN = 0	When the power supply is present and nEN is pulled low, the part enables the internal oscillator and bias circuitry. Once this is complete, the part transitions into the STANDBY: INTERRUPTS NOT CLEARED state. The SPI Ready interrupt occurs and the ISR_SPI_RDY register needs to be read and cleared before moving to the STANDBY state.
STANDBY: INTERRUPTS NOT CLEARED	After the output is disabled due to a fault condition, the IC transitions back into the STANDBY: INTERRUPTS NOT CLEARED state. HAPTIC PLAYBACK mode cannot occur until the interrupts are cleared. Read the ISR register in order to clear the interrupts and transition into the STANDBY state. The IC also transitions into this state when nEN is pulled low due to the SPI Ready Interrupt. This state is the same as the STANDBY state, except haptic playback cannot be enabled.
STANDBY	STANDBY mode is a low-power state where the output is disabled and the system awaits a haptic playback request from the user. The SPI bus is working and the registers and RAM can be written to and read from in order to prepare for a haptic request.
(2) Haptic Request Occurred through RAM or FIFO	A haptic request can occur either by programming the RAM and enabling the RAM_PLAY register or by writing to the FIFO_WRITE_PORT register. This enables haptic playback.
ENABLE OUTPUT	Prior to performing the haptic request, the part enables the charge pumps and all of the analog blocks and ramps the DAC up to its minimum voltage so that the output of the converter is 10V at the beginning of HAPTIC PLAYBACK.
(3) Output Ready	When the output reaches 10V, the part transitions into HAPTIC PLAYBACK.
HAPTIC PLAYBACK	The converter is enabled and playing the haptic signal sent through the RAM or FIFO.
(4) Haptic Done	Once the haptic event is done, the part proceeds to the RAMP DOWN OUTPUT state.
RAMP DOWN OUTPUT	The IC ramps the DAC down to all 0's, disables the output, and disables the charge pumps.
(5) Fault Condition	If a fault condition occurs, the system ramps the output down to 10V and then disables the converter. The system transitions to either the STANDBY state, the STANDBY: INTERRUPTS NOT CLEARED state, or the SHUTDOWN state depending on the status of nEN. See the *Interrupts and Fault Protection* section for more information.
FAULT CONDITION RAMP DOWN OUTPUT	After a fault condition occurs, the output is ramped down to 10V. There is a delay after the fault condition happens that allows time for the output to ramp down to 10V. The default value is 2ms and can be set by the FAULT_DLY register. After the delay has finished, the IC disables the charge pumps.
(6) RAMP DOWN DONE & nEN = 0	If nEN is still low after the output has been disabled, the system proceeds to the STANDBY state.
(7) RAMP DOWN DONE & nEN = 1	If nEN is high after the output has been disabled, the system transitions to the SHUTDOWN state.
(8) Interrupts Cleared	Read the ISR register to transition from the STANDBY STATE: INTERRUPTS NOT CLEARED to the STANDBY STATE so that HAPTIC PLAYBACK can be enabled.
(9) FAULT DELAY DONE & nEN = 0 & ALLOW_NEW_REQ = 0	After a fault condition, the DAC ramps down to its minimum value, there is a FAULT DELAY (default 2ms) that allows the output to ramp down safely. After the fault delay is finished, the IC transitions into the STANDBY: INTERRUPTS NOT CLEARED state. The interrupts need to be cleared to move into the STANDBY state where a haptic request can occur.
(10) nEN = 0 & ALLOW_NEW_REQ = 1	After a fault condition, the DAC ramps down to its minimum value, there is a FAULT DELAY (default 2ms) that allows the output to ramp down safely. If the ALLOW_NEW_REQ register is set to 1, then the interrupts do not need to be cleared after a fault condition occurs. After the FAULT DELAY has finished, the part transitions immediately to the STANDBY state and haptic requests are allowed.

Table 1. State Diagram Description (continued)

STATE/ TRANSITION	DESCRIPTION
(11) FAULT DELAY DONE & nEN = 1	After a fault condition, the DAC ramps down to its minimum value, there is a FAULT DELAY (default 2ms) that allows the output to ramp down safely. If nEN is high, the IC transitions to the SHUTDOWN state after the FAULT DELAY has finished.
(12) nEN = 1	If nEN is pulled high in either the STANDBY state or the STANDBY: INTERRUPTS NOT CLEARED state, then the IC transitions to the SHUTDOWN state.

Turn-On Sequence

The MAX77501 is typically turned on by pulling the nEN (active-low enable) pin low. Optionally, the nEN pin can be connected directly to ground to enable the IC any time power is applied at V_{IN} and V_{IO}.

Before the nEN is pulled low, the IC remains in SHUTDOWN, a low-power mode that consumes less than 1µA of supply current. Be aware that all internal memory (registers, RAM, and FIFO) is cleared in SHUTDOWN.

After nEN transitions low, the IC enters the STANDBY: INTERRUPTS NOT CLEARED state within 1ms and the supply current rises to 75µA. After entering STANDBY: INTERRUPTS NOT CLEARED from SHUTDOWN, an SPI Ready Interrupt is issued by the IC to alert the system that SPI communication is now enabled. This interrupt is cleared by reading the ISR register, which transitions the part to STANDBY mode. All settings must be restored through the SPI interface every time the part transitions from SHUTDOWN to STANDBY because all of the registers are cleared during SHUTDOWN.

Digital Configuration

The SPI interface communicates with the MAX77501 through a set of 16-bit registers. Typically, the SPI master configures the IC immediately after transitioning from the SHUTDOWN to the STANDBY state in preparation for subsequent waveform output events.

In most applications, only the *CONFIGURATION* register is set before sending waveform data. The other registers can be left unmodified at their default values. The two analog levels it configures are the peak current limit threshold and the output voltage FULL SCALE range. For a given application, it is rare to alter the values stored in the CONFIGURATION register after a design is complete, but because the internal memory is cleared whenever the power is cycled or SHUTDOWN is entered, it is important to reload the CONFIGURATION register after these events.

The *CONFIGURATION* register also configures the DAC sample rate. The 32kHz DAC sample rate is preferred when SPI traffic is not a concern. Otherwise, the 8kHz option can be used to reduce the amount of SPI traffic required to transmit a waveform. In addition, the 8kHz sample rate also allows longer duration waveforms to be stored in the RAM.

Besides the current limit threshold, output voltage range, and DAC sample rate, the *CONFIGURATION* register also sets the FIFO Almost Empty Level (FIFO_AE_LEVEL). Depending on the FIFO_AE_LEVEL, the FIFO pin transitions low 125µs, 250µs, 500µs, or 2ms before the FIFO runs empty to assist the SPI master in FIFO data flow control.

Digital Engine Overview

The digital engine is responsible for providing waveform data to the DAC. An SPI bus is available as an interface. Waveform data can be streamed into the FIFO for immediate playback (FIFO mode) or stored in the memory for future playback (RAM playback mode). Besides the SPI interface and some analog control signals, the digital block has only one functional output, which is a 12-bit bus representing the waveform data and is connected to the input of the DAC.

The digital block consists of the following major blocks, as shown in Figure 2.

1. SPI Slave
2. Registers
3. FIFO/RAM
4. Control Logic

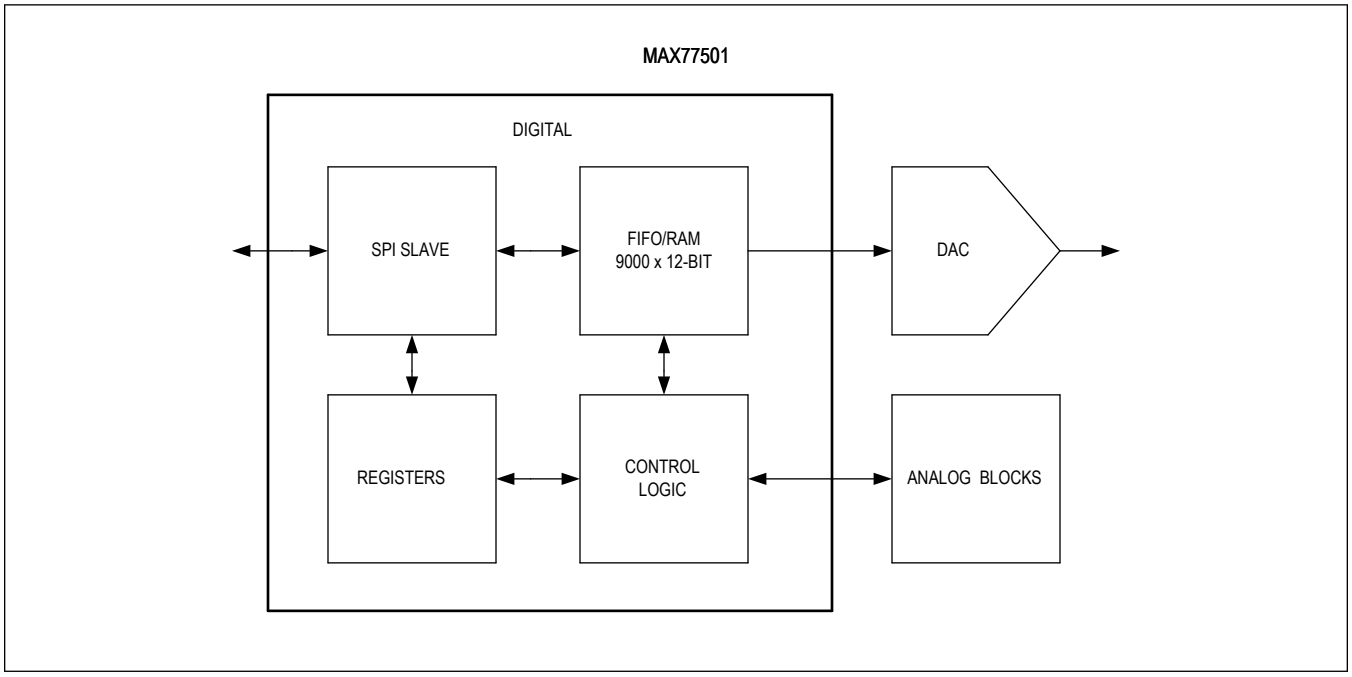


Figure 2. Digital Engine Block Diagram

Modes of Playback

There are two ways to create the waveform: Real-time FIFO and RAM Playback.

Table 2. Waveform Modes of Playback

MODE	DESCRIPTION
Real-time FIFO	Raw waveform data is supplied directly through the SPI bus. Data is taken out at a constant rate of either 8kHz, 32kHz, or 48kHz.
RAM Playback	Raw waveform data is stored in a 8192 x 12-bit RAM. Data is taken out at a constant rate of either 8kHz, 32kHz, or 48kHz. 8192 RAM can provide a total of 1.024s of playback at 8kHz, 256ms of playback at 32kHz, and 170ms of playback at 48kHz.

Waveform Input—FIFO

The simplest way to drive the output waveform is through the ICs FIFO. When data is written to the FIFO_WRITE_PORT register, the lower 12 bits is automatically loaded into the First-In First-Out FIFO's queue. Subsequent writes continue to

be loaded into the FIFO as described in the *SPI Burst Write Diagram* section.

As soon as a value is loaded into the FIFO, the IC prepares to drive the output waveform. First, it powers up the internal charge pumps (2ms max allowable start-up time). Then, it ramps up the output to 10V. When that is complete, the FIFO begins to send data to the DAC, and the corresponding waveform is produced at the output. The DAC is clocked at 8kHz, 32kHz, or 48kHz, as determined by the SMP_RATE register. After the last value has been transferred from the FIFO, the IC transitions back to the low power STANDBY state after a delay.

If the FIFO is full, the IC ignores further attempts to write to the FIFO. (Be aware that when waveforms are stored in RAM, the available FIFO memory is reduced by an equivalent amount.) To assist in FIFO handling, the FIFO pin signals when the queue reaches an almost empty level, as determined by the FIFO_AE_LEVEL register. Upon reaching this level, the FIFO pin is driven low to notify the system that the FIFO will soon run empty unless more data is loaded.

FIFO Size

The system includes RAM with 9216 12-bit words that are shared between the FIFO mode and the RAM Playback mode. 1024 of the 9216 RAM entries are reserved exclusively for the FIFO. Therefore, at most 8192 entries are available for RAM Playback mode. Table 3 demonstrates how the RAM is shared between the FIFO and the stored RAM playback waveforms.

Table 3. FIFO Total Size Example

<table>
<tr><th>EXAMPLE 1</th><th></th><th>EXAMPLE 2</th><th></th><th>EXAMPLE 3</th><th></th></tr>
<tr><th>Address</th><th>No RAM Playback Content</th><th>Address</th><th>Some RAM Playback Content</th><th>Address</th><th>Full RAM Playback Content</th></tr>
<tr><td>0x43FF</td><td rowspan="3">Reserved for FIFO (1024 words)</td><td>0x43FF</td><td rowspan="3">Reserved for FIFO (1024 words)</td><td>0x43FF</td><td rowspan="3">Reserved for FIFO (1024 words)</td></tr>
<tr><td>…</td><td>…</td><td>…</td></tr>
<tr><td>0x4000</td><td>0x4000</td><td>0x4000</td></tr>
<tr><td>0x3FFF</td><td rowspan="11">Extra for FIFO (8192 words)</td><td>0x3FFF</td><td rowspan="8">Extra for FIFO (5192 words)</td><td>0x3FFF</td><td rowspan="11">Used by RAM Playback (8192 words)</td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td></td><td></td><td></td></tr>
<tr><td></td><td>0x2BB8</td><td rowspan="3">Used by RAM Playback (3000 words)</td><td>0x2BB8</td></tr>
<tr><td></td><td></td><td></td></tr>
<tr><td>0x2000</td><td>0x2000</td><td>0x2000</td></tr>
</table>

If no data is stored for RAM Playback mode, then all 9216 entries in the RAM are available for FIFO use. On the other hand, if the host has already stored some data for RAM Playback mode, the amount of space for FIFO reduces by the number of entries stored in the RAM. For example, if the host has stored two waveform effects for RAM Playback mode, with first effect occupying 1000 entries and the second 2000, then the total available size for FIFO is 9216 - 3000 = 6216 entries. The number of entries available in the FIFO can be read in the FIFO_TOTAL_DEPTH register. This is the maximum number of entries that the host processor can write to the FIFO at one time.

If the available space for the FIFO is large enough to fit all data the host processor would like to play, it can write everything in just one burst write transaction and no more attention is required from the host. However, if the host wants to play more data than the FIFO can take, it needs to break the data into multiple SPI transactions and wait between the transactions. In order to free the host from periodically polling the FIFO status register to check whether it should start a new SPI transaction, the FIFO is designed such that when it reaches a certain level of emptiness, the IC pulls the FIFO pin low to indicate to the host that it can start sending in more data. The level of emptiness is programmable through the FIFO_AE_LEVEL register.

FIFO Full, Empty, and Almost Empty

The FIFO_EMPTY_DEPTH register contains the amount of data that can be written to the FIFO. The FIFO_EMPTY_DEPTH register reads as zero if the FIFO is full. If the FIFO is empty, the FIFO_EMPTY_DEPTH register reads the same as the FIFO_TOTAL_DEPTH register.

The FIFO_AE_LEVEL register determines how many entries are left in the FIFO when the FIFO pin pulls low. The register determines the length of time before all of the data in the FIFO is processed. This length of time can be set to 125µs, 250µs, 500µs, or 2ms. The number of samples left in the FIFO is the FIFO_AE_LEVEL multiplied by the sample rate.

The amount of samples left in the FIFO for a given sample rate and FIFO Almost Empty Level can be determined using Table 4.

Table 4. Number of FIFO Samples Left for a Given FIFO_AE_LEVEL and Sample Rate

	FIFO_AE_LEVEL = 125µs	FIFO_AE_LEVEL = 250µs	FIFO_AE_LEVEL = 500µs	FIFO_AE_LEVEL = 2ms
Sample Rate = 8kHz	1	2	4	16
Sample Rate = 32kHz	4	8	16	64
Sample Rate = 48kHz	6	12	24	98

Using the FIFO Mode

To use the FIFO, the host should follow these steps:

1. Program the FIFO Almost Empty register, which is discussed in more details in the *FIFO Full, Empty, and Almost Empty* section. The number of entries left in the FIFO is the amount of time programmable by the FIFO_AE_LEVEL register multiplied by the sample rate.
2. Determine the number of entries currently available for FIFO mode. This can be done by simply reading the FIFO_EMPTY_DEPTH register.
3. Start a burst write of data up to the amount in the FIFO_EMPTY_DEPTH register.
4. If the FIFO is large enough to hold all of the data, the operation is done.
5. If not, wait for the FIFO pin to go low before sending in more data.

Figure 3 shows an example of this procedure.

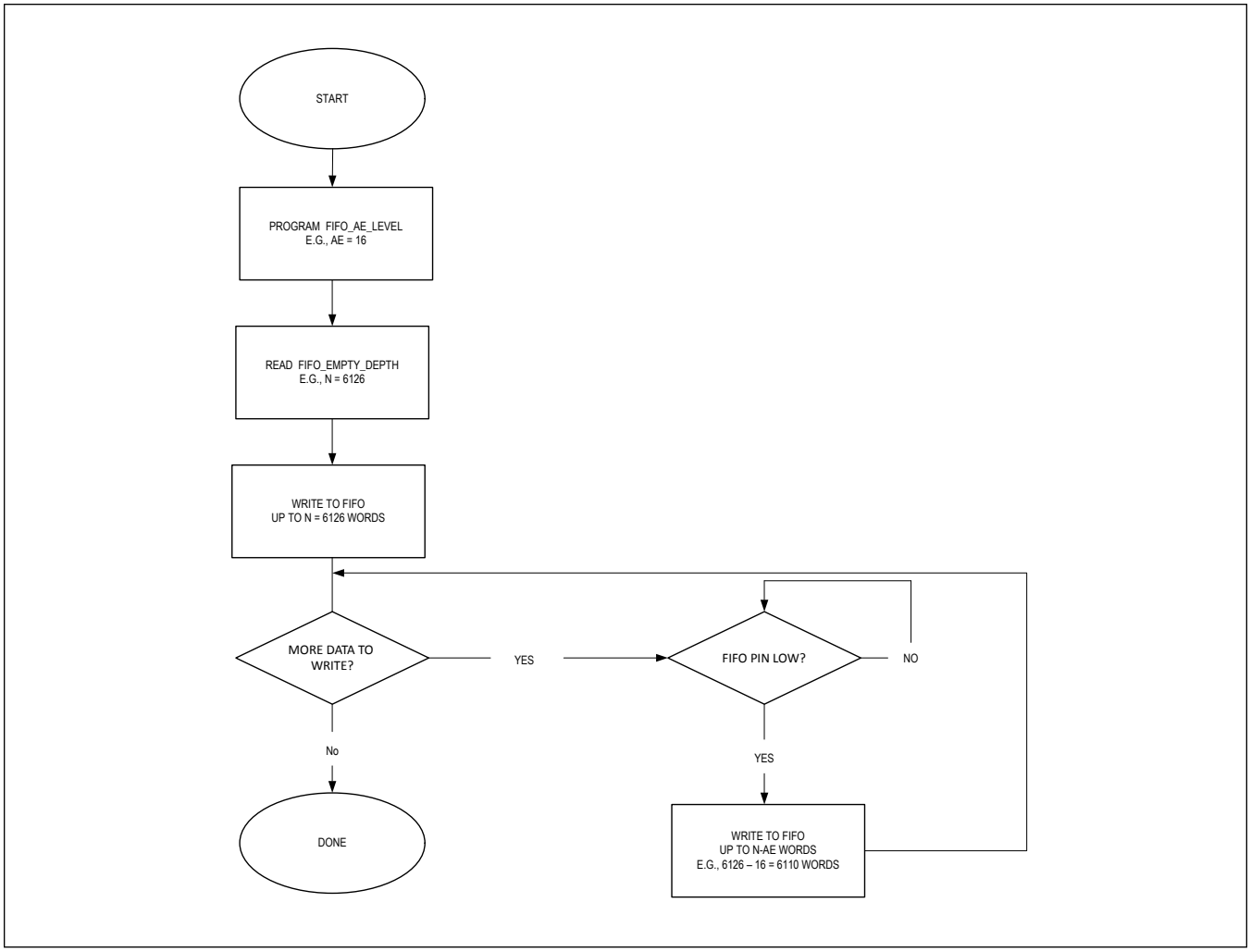


Figure 3. FIFO Write Flow Chart

Waveform Input—RAM

In addition to FIFO real-time control of the output, waveforms can be stored in RAM for playback on demand. Up to 16 waveforms can be stored and repeated in any order in multiples of up to 255. The repeat count registers are 8-bit with a default value of 1, which means that a given waveform is played once. If that register is set to 0, then the waveform is played indefinitely. As with the FIFO mode described above, the IC remains in a low-power-standby mode unless a waveform is being played. It automatically enables and disables the charge pumps, MOSFET gate drive, and output voltage as necessary to enter and exit the STANDBY state. The RAM_PLAY bit is used to start haptic playback. Setting the RAM_PLAY bit to 1 starts haptic playback. The RAM_PLAY bit self-clears after haptic playback has finished. As soon as the RAM_PLAY bit is set to 1, the IC prepares to drive the output waveform. First, it powers up the internal charge pumps (2ms max). Then, it ramps up the output from the initial V_{IN} voltage (where the output voltage sits in STANDBY) to 10V. When that is complete, the RAM begins to send data to the DAC and the corresponding waveform is produced at the output.

The RAM contains a total of 8192 entries. Every entry stored in the RAM reduces the number of entries that can be stored in the FIFO at the same time.

Address Space for RAM and Registers

The address spaces for the RAM and the registers are shown in Table 5.

Table 5. RAM/Register Address Space

ADDRESS	CONTENT
0x0000 to 0x00FF	Register
0x2000 to 0x3FFF	RAM

Note that the RAM actually has a depth of 9216 not 8192, but the higher 1024 entries are reserved for FIFO and are not directly accessible by the host processor.

RAM Content Organization

Waveforms are stored as one continuous block of data in the RAM. The host should store each waveform in the RAM continuously, starting at address 0x2000 and without any gap between each waveform in the memory addresses. That means the first word of the first waveform (Waveform 0) is always stored at 0x2000, followed by the second word at address 0x2001, etc. The second waveform (Waveform 1), if needed, should immediately follow the last word of Waveform 0. See Table 6 for an example of how data is organized in the RAM. Data can be stored in the RAM by writing to the RAM address with an SPI write command.

Table 6. RAM Content Organization Example

ADDRESS	RAM CONTENT
0x3FFF	Empty
…	
…	
…	
0x2901	
0x2900	Data for Waveform 3
…	
…	
0x2601	
0x2600	Data for Waveform 2
…	
0x2501	
0x2500	Data for Waveform 1
…	
…	
…	
…	
…	
…	
…	
…	
0x2101	
0x2100	Data for Waveform 0
…	
0x2000	

Waveform Ending Address Registers

Up to sixteen waveforms can be stored in the RAM for playback. All waveforms are stored continuously in the RAM, so the system needs additional information from the host in order to locate each waveform. This is done through the "ending address" registers. There are sixteen ending address registers, with one register corresponding to each waveform stored in the RAM. WAVEFORM_0_EA corresponds to Waveform 0, which is the first waveform stored in the RAM. WAVEFORM_1_EA corresponds to the ending address of Waveform 1, which is the next waveform stored in the RAM. No starting addresses are necessary. The starting address of Waveform 0 is always 0x2000, the first RAM register address. The starting address of every subsequent waveform is the address after the ending address programmed for the previous waveform.

Number of Waveforms Stored in the RAM

The host needs to program the number of distinct waveforms stored in the RAM into the NUM_WAVEFORMS_STORED register. The number of waveforms stored in the RAM and the ending address of the last stored waveform determines the amount of space available for FIFO operation. The FIFO_TOTAL_DEPTH contains the number of entries available for the FIFO. If the NUM_WAVEFORMS_STORED register is set to 0, the entire RAM is available for the FIFO.

Playlist Registers

The register map contains registers that allow a playlist to be programmed. The playlist determines the number of times each waveform is played and in what order. The NUM_WAVEFORMS_PLAY register determines how many waveforms should be played when the RAM_PLAY register is set to 1. Each waveform to be played has a corresponding play ID. PLAY_0_ID contains the waveform number of the first waveform to be played. Similarly, the PLAY_1_ID register contains the ID of the second waveform to be played. If PLAY_0_ID is programmed to 0x4, then Waveform 4 stored in the RAM is the first waveform played. Table 7 contains an example playlist that can be programmed through these registers.

Table 7. Example Playlist

REGISTER	VALUE	MEANING
NUM_WAVEFORMS_PLAY	0x4	Number of Waveforms to Play: 4
PLAY_0_ID	0x2	1st waveform to play: Waveform 2
PLAY_1_ID	0x3	2nd waveform to play: Waveform 3
PLAY_2_ID	0x1	3rd waveform to play: Waveform 1
PLAY_3_ID	0x2	4th waveform to play: Waveform 2

Repeat Count Register

A repeat count register is available for each item in the playlist. The host can choose to play any waveform in the playlist multiple times before the playback continues to the next waveform. The repeat count registers are 8-bits wide. A value of 1, which is the default, means the waveform is played once. A value of 2, means the waveform is played twice. When a repeat count register is set to 0, that waveform is played indefinitely until the RAM_PLAY register bit is set to 0. Table 8 shows how to program the registers to play Waveform 2 once, then Waveform 3 three times, then Waveform 1 twice, and Waveform 2 again 16 times.

Table 8. Repeat Count Example

REGISTER	VALUE	MEANING
NUM_WAVEFORMS_PLAY	0x4	Number of waveforms to play: 4
PLAY_0_ID	0x2	1st waveform to play: Waveform 2
PLAY_0_REPEAT	0x01	Play waveform 2 one time
PLAY_1_ID	0x3	2nd waveform to play: Waveform 3
PLAY_1_REPEAT	0x03	Play waveform 3 three times
PLAY_2_ID	0x1	3rd waveform to play: Waveform 1
PLAY_2_REPEAT	0x02	Play waveform 1 two times

Table 8. Repeat Count Example (continued)

REGISTER	VALUE	MEANING
PLAY_3_ID	0x2	4th waveform to play: Waveform 2
PLAY_3_REPEAT	0x10	Play waveform 2 sixteen times

Example Configuration

In Table 9, four waveforms are stored in the RAM.

Table 9. RAM Storage Example

ADDRESS	RAM CONTENT
0x3FFF	Empty
…	
…	
…	
0x2901	
0x2900	Data for Waveform 3
…	
…	
0x2601	
0x2600	Data for Waveform 2
…	
0x2501	
0x2500	Data for Waveform 1
…	
…	
…	
…	
…	
…	
…	
…	
0x2101	
0x2100	Data for Waveform 0
…	
0x2000	

Table 10 shows how the NUM_WAVEFORMS_STORED and the ending address registers should be programmed for such a RAM setup.

Table 10. RAM Waveform Storage Example

REGISTER	VALUE
NUM_WAVEFORMS_STORED	0x0004
WAVEFORM_0_EA	0x2100
WAVEFORM_1_EA	0x2500
WAVEFORM_2_EA	0x2600

Table 10. RAM Waveform Storage Example (continued)

REGISTER	VALUE
WAVEFORM_3_EA	0x2900

The host can then create a playlist in the register by writing to the registers shown in Table 11. In Table 11, three out of four stored waveforms are programmed to be played in this order, Waveform 2 for 5 times, Waveform 0 for 8 times, Waveform 3 for 10 times.

Table 11. RAM Playlist Example

REGISTER	VALUE
NUM_WAVEFORMS_PLAY	0x0003
PLAY_0_ID	0x0002
PLAY_0_REPEAT	0x0005
PLAY_1_ID	0x0000
PLAY_1_REPEAT	0x0008
PLAY_2_ID	0x0003
PLAY_2_REPEAT	0x000A

Using the RAM Playback Mode

In summary, to use RAM playback follow these steps:

1. Store the waveform data in the RAM (keep in mind when accessing the RAM through SPI an offset of 0x2000 is needed, so addresses range from 0x2000 to 0x3FFF).
2. Program the ending address registers (WAVEFORM_0_EA, WAVEFORM_1_EA, etc.).
3. Program the NUM_WAVEFORMS_STORED register.
4. Program the waveform ID registers for the playlist (PLAY_0_ID, PLAY_1_ID, etc.).
5. Program the repeat count registers (PLAY_0_REPEAT, PLAY_1_REPEAT, etc.). They default to 1.
6. Program the NUM_WAVEFORMS_PLAY register.
7. Start the playback by writing 1 to the RAM_PLAY register.

Reading the RAM

In order to read from the RAM, write the RAM register address to the RAM_READ_ADDR register. The RAM_READ_DATA register contains the contents of the RAM address written to the RAM_READ_ADDR register. If a burst read is used on this register, the part supplies the data contents for each subsequent RAM register. So to read addresses 0x2000 through 0x2004, the user must write 0x2000 to the RAM_READ_ADDR register and then perform a burst read on the RAM_READ_DATA register for five words.

Overlapping Playback Requests

If the IC receives a new haptic request through the RAM or FIFO while another haptic operation is in progress, it postpones the new request until the current operation is finished.

DAC Code to Output Voltage Conversion

In order to produce the correct haptic waveforms at the output of the converter, the correct DAC codes have to be programmed to the RAM or written to the FIFO. The DAC code goes through a compression algorithm so that the correct voltage appears on the ouput of the DAC for a given DAC Code. This output voltage is the input to a preamplifier, the output of which is used as the reference voltage for the error amplifier.

The equation for converting the DAC code to the intended output voltage for FULL_SCALE set to 60Vpp is as follows:

V_{OUT} = (DAC_CODE(decimal) × 0.875 + 508) × (DAC_FS ⁄ DAC_HIGH) × AV_{PA} × ((RFB1 + RFB2) ⁄ RFB2)

where AV_{PA} = 2.818V/V, DAC_FS = 1.25V, DAC_HIGH = 4095, and RFB1 is the feedback resistor attached to V_{OUT}

and RFB2 is the feedback resistor tied to GND.

The equation for converting the DAC code to the intended output voltage for FULL_SCALE set to 120Vpp is as follows:

V_{OUT} = (DAC_CODE(decimal) × 0.923 + 315) × (DAC_FS ⎪ DAC_HIGH) × AV_{PA} × ((RFB1 + RFB2) ⎪ RFB2)

where AV_{PA} = 2.818V/V, DAC_FS = 1.25V, DAC_HIGH = 4095, and RFB1 is the feedback resistor attached to V_{OUT} and RFB2 is the feedback resistor tied to GND.

Note that a certain amount of error is expected due to the error from the DAC, the preamplifier, and the amplifier offsets. See the *Full-Scale Settings* section for selecting RFB1 and RFB2.

DAC Output Sampling Rate

The part provides three sample rates at which the DAC samples data out of the FIFO and RAM. These sample rates can be set to either 8kHz, 32kHz, or 48kHz depending on the setting of the SMP_RATE register. The sample rate chosen affects the length of the waveforms stored in the RAM. For example, with the default 32kHz sample rate, 256ms of data can be stored in 8192 RAM addresses. With the 8kHz option, 1.024s of data can be stored in 8192 RAM addresses and with a 48kHz sampling rate, 170ms of data can be stored in 8192 RAM addresses. In addition, the sample rate must be taken into account when building waveforms of the correct length and frequency.

Interrupts and Fault Protection

Several status, interrupt, and interrupt mask registers monitor key information which asserts the nIRQ pin (nIRQ = 0) when an interrupt event has occurred. The nIRQ pin is an active-low, open-drain output which requires a pullup resistor to V_{IO}. All interrupts are unmasked by default. The interrupt function allows the host processor to poll the nIRQ pin to determine if a system interrupt has occurred. If the nIRQ pin is low, the host processor can access the interrupt registers through the SPI bus to determine what interrupt has occurred. After an interrupt has occurred, the host processor must read the ISR register to clear the interrupt register before haptic playback can be re-enabled. Interrupts that are reported include FIFO and RAM playback errors, current limit warnings and fault conditions, charge pump time-out, charge pump not okay, UVLO, temperature fault condition, bias not okay, and nEN fault. See the *Register Map* section of the data sheet for more information on the various interrupts and fault conditions.

nEN Interrupt and Fault Condition

An nEN interrupt is generated if the nEN pin is pulled high during a haptic playback event. This generates an interrupt on the nIRQ pin. In addition, the device ramps down the output to a safe level of 10V prior to entering the SHUTDOWN state, as shown in the *State Diagram*.

Undervoltage Lockout (UVLO) Fault Protection

A UVLO interrupt and fault condition is generated if V_{IN} dips below the falling UVLO threshold (2.6V). If the UVLO condition occurs during the HAPTIC PLAYBACK state, the output voltage safely ramps down to 10V prior to transitioning to the STANDBY: INTERRUPTS NOT CLEARED state. V_{IN} needs to rise above the UVLO rising threshold (2.7V), and the UVLO interrupt register needs to be read and cleared to release nIRQ and this fault.

Charge Pump Time Out Fault Protection

A Charge Pump Time Out fault condition is generated if either the V_5 or V_{DD_H} charge pump voltages are unable to reach their respective VOK thresholds within 2ms of entering the ENABLE OUTPUT state. Once the Charge Pump Time Out Fault Flag is generated, both charge pumps are disabled and the IC transitions back to the STANDBY: INTERRUPTS NOT CLEARED state. The ISR_CPOK_TO register needs to be read and cleared to release nIRQ and this fault.

Charge Pump Not Okay Fault Protection

A Charge Pump Not OK fault condition is generated if either the V_5 or V_{DD_H} charge pump voltages dip below their respective VOK thresholds in the ENABLE OUTPUT or HAPTIC PLAYBACK states.

In the ENABLE OUTPUT state, once the Charge Pump Not OK fault is generated, both charge pumps are disabled and the IC returns to the STANDBY: INTERRUPTS NOT CLEARED state. The ISR_CPOK register needs to be read and cleared to release nIRQ and this fault.

In the HAPTIC PLAYBACK state, once the Charge Pump Not OK fault is generated, the IC output voltage safely ramps down to 10V, both charge pumps are disabled, and the IC transitions to the STANDBY: INTERRUPTS NOT CLEARED state. The ISR_CPOK register needs to be read and cleared to release nIRQ and this fault.

ILIM Warning Interrupt and Fault Protection

An ILIM Warning interrupt is generated if the inductor current exceeds the ILIM threshold for the programmed number of consecutive inductor switching cycles. The programmed number of consective inductor switching cycles is set by the ILIM_WARN register. If there is a switching cycle without the ILIM threshold being reached, the ILIM Warning counter is reset. The ISR_ILIM_WARN register needs to be read and cleared to release the nIRQ and this interrupt.

An ILIM Fault interrupt is generated if the programmed number of consecutive ILIM_WARN flags is reached. The programmed number of ILIM_WARN flags is set by the ILIM_FAULT register. If there is an inductor switching cycle without the ILIM threshold being reached, the ILIM_FLAG counter is reset. Once the ILIM fault has been detected, the output voltage safely ramps down to 10V, the charge pump is disabled, and the IC transitions to the STANDBY: INTERRUPTS NOT CLEARED state. The ISR_ILIM_FAULT register needs to be read and cleared to release nIRQ and this fault.

As mentioned, consecutive inductor switching cycles are required to trigger the ILIM warning or fault condition. However, the NUM_NO_ILIM register allows the ILIM condition to skip a programmed number of inductor switching cycles and still allow the triggering of the ILIM Warning interrupt or Fault condition.

Invalid RAM Address Interrupt and Fault Protection

An Invalid Address and fault condition is generated if RAM playback is attempted while the NUM_WAVEFORM_PLAY register is set to 0 or there is a conflict in the ending address registers. For example, if the WAVEFORM_0_EA register is set to 0x2030 and the WAVEFORM_1_EA register is set to 0x2020, meaning the Waveform 1 ending address is before the Waveform 0 ending address, the fault condition is generated. All waveforms must be stored in order in the RAM (0, 1, 2, etc.), so the ending addresses must also be programmed in this order. The ISR_INVALID_ADDR register needs to be read and cleared to release nIRQ and this fault.

Empty RAM Interrupt and Fault Condition

An Empty RAM interrupt and fault condition is generated if RAM playback is attempted while the NUM_WAVEFORMS_STORED register is set to 0, which means that the RAM is empty. The ISR_EMPTY_RAM register needs to be read and cleared to release nIRQ and this fault.

RAM Address Overflow Interrupt and Fault Condition

A RAM Address Overflow interrupt and fault condition is generated if the RAM address overflows during a burst read or write operation, which means that the processor attempted to read from or write to an address that is greater than 0x3FFF. The ISR_ADDR_OVERFLOW register needs to be read and cleared to release nIRQ and this fault.

FIFO Overflow Interrupt and Fault Condition

A FIFO Overflow interrupt and fault condition is generated when a FIFO write is attempted while the FIFO is full. The IC ignores any FIFO writes while the FIFO is full. The ISR_FIFO_OVERFLOW register needs to be read and cleared to release nIRQ and this fault.

Thermal Interrupt and Fault Protection

A Thermal interrupt is generated if the ICs internal die temperature exceeds 165°C.

In the ENABLE OUTPUT state, once the Thermal interrupt is generated, both charge pumps are disabled and the IC returns to the STANDBY: INTERRUPT NOT CLEARED state. The ISR_TOK register needs to be read and cleared to release nIRQ and this fault. The ICs die temperature must drop below 144°C before re-entering the ENABLE OUTPUT and HAPTIC PLAYBACK states.

In the HAPTIC PLAYBACK state, once the Thermal interrupt is generated, the output voltage safely ramps down to 10V, both charge pumps are disabled and the IC returns to the STANDBY: INTERRUPT NOT CLEARED state. The ISR_TOK register needs to be read and cleared to release nIRQ and this fault. The ICs die temperature must drop below 144°C before re-entering the ENABLE OUTPUT and HAPTIC PLAYBACK states.

Bias NOT OK Fault Protection

A Bias Not OK interrupt is generated if the ICs internal biasing monitors are below their Bias OK (BOK) thresholds. These include internal biasing current generators and the V_{DD} output voltage.

In the ENABLE OUTPUT state, once the BIAS NOT OK interrupt is generated, both charge pumps are disabled and the IC returns to the STANDBY: INTERRUPTS NOT CLEARED state. The ISR_BOK needs to be read and cleared to release nIRQ and this fault. The internal biasing must be restored before re-entering the ENABLE OUTPUT and HAPTIC PLAYBACK states.

In the HAPTIC PLAYBACK state, once the BIAS NOT OKAY interrupt is generated, the IC output voltage safely ramps down to 10V, both charge pumps are disabled, and the IC transitions to the STANDBY: INTERRUPTS NOT CLEARED state. The ISR_BOK needs to be read and cleared to release nIRQ and this fault. The internal biasing must be restored before re-entering the ENABLE OUTPUT and HAPTIC PLAYBACK states.

SPI Ready Interrupt

An SPI Ready Interrupt is generated when the ICs digital engine is ready to receive SPI commands when the IC is enabled (nEN = 0V). The ISR_SPI_RDY register needs to be read and cleared to release the nIRQ and this interrupt before issuing any haptic playback SPI requests from the STANDBY state. The SPI Ready interrupt occurs about 320µs after entering the STANDBY: INTERRUPTS NOT CLEARED state from the SHUTDOWN state by bringing nEN to 0V from V_{IN}.

Detailed Description—Boost Controller

Description of Modulator Operation

The ICs modulator operation is a peak current-mode controlled, forced PWM modulator using a COT (i.e., Computed-OFF-Time) frequency controller and adaptive-controlled slope compensation. This configuration provides for stable operation over a wide range of output voltage swing to input voltage operation.

Switching Frequency and COT Timer Operation

The switching frequency of the boost controller is set by a COT (Computed-Off-Time) controller. An external RC (R_{COT},

C_{COT}) time constant sets the frequency based on V_{IN} and V_{OUT}.

Slope Compensation

Slope compensation is added to the current control loop by creating an external time constant with R_{SLP} and C_{SLP}. Connecting C_{SLP} to the CS_IN pin adds the feed-forward slope-compensation signal to the current sense feedback.

Small Signal Frequency Compensation

The IC is typically compensated with a simple type-II compensation network as shown in Figure 4. An additional pole is intrinsically created by parasitic capacitance at the COMP node. Therefore, it is important to keep the compensation components very close to the COMP pin in order to minimize excess lag in the loop caused by this pole.

See the following chart in the *External Component Selection Guide* to choose compensation components appropriate for your application requirements.

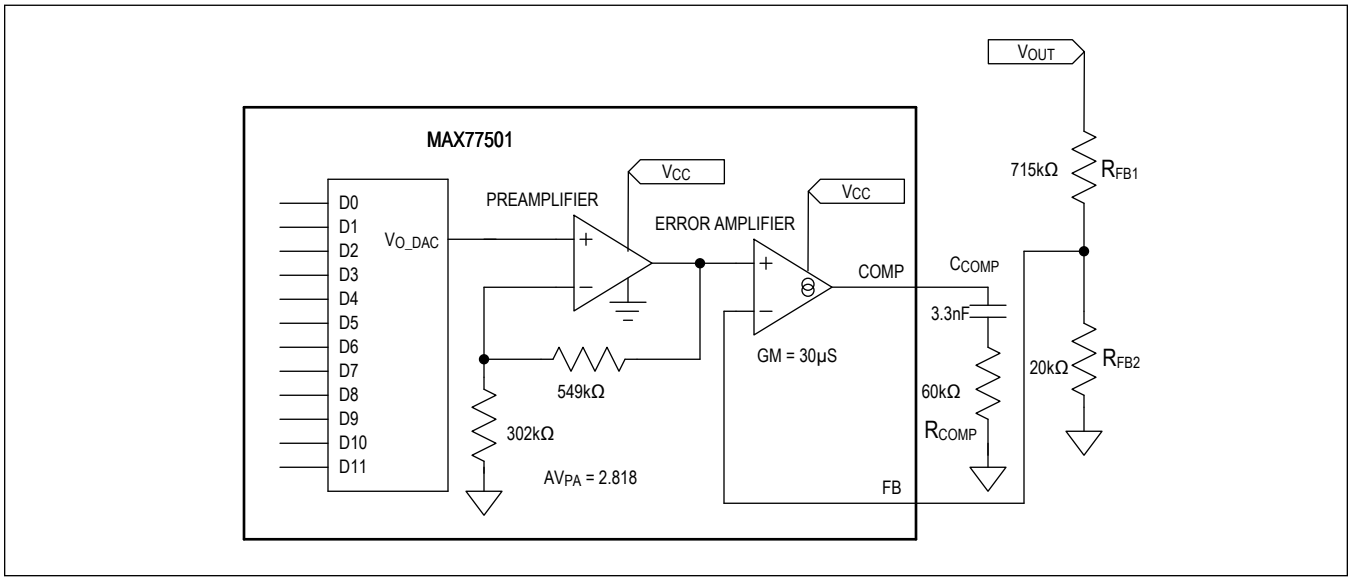


Figure 4. Error Amplifier Block Diagram

Current Limit Protection

The IC has a programmable cycle-by-cycle peak current limit set by the ILIM_SEL register. The ILIM_SEL register provides four programmable threshold voltages (0.1V, 0.2V, 0.3V, and 0.4V). The peak inductor current limit is the programmed threshold level divided by the external sense resistor that is connected between the CS_IN and PGND pins. Since the sense resistor has a typical recommended value of 100mΩ, the programmable current limits would result in 1A, 2A, 3A, and 4A, respectively.

Overvoltage Protection

The IC has a cycle-by-cycle peak overvoltage protection achieved by monitoring the FB pin voltage. If the FB voltage exceeds 3.5V, the external low-side NFET turns off, limiting the inductor energy available for driving the output voltage. The output voltage therefore clamps to 3.5V x ((R_{FB1} + R_{FB2})/R_{FB2}) during an overvoltage condition.

Detailed Description—SPI Communication Controller

The IC includes an SPI slave controller that allows for communication between the host micro-processor and the ICs control registers. The IC features a 4-pin SPI interface that can run up to 25MHz and supports full duplex communication. The SPI interface operates in mode 0, which means that data is launched at the falling edge of the SCLK and captured

at the rising edge of the SCLK. The SPI interface features an active-low chip-select pin called SSB. When the SSB pin is pulled high, the MISO pin is placed in a high-impedance mode to allow for communication from other ICs on the SPI bus. However, the data rate of the SPI can be affected by the extra capacitance provided by multiple slave connections. Figure 5 shows the interface timing specifications for the SPI Bus.

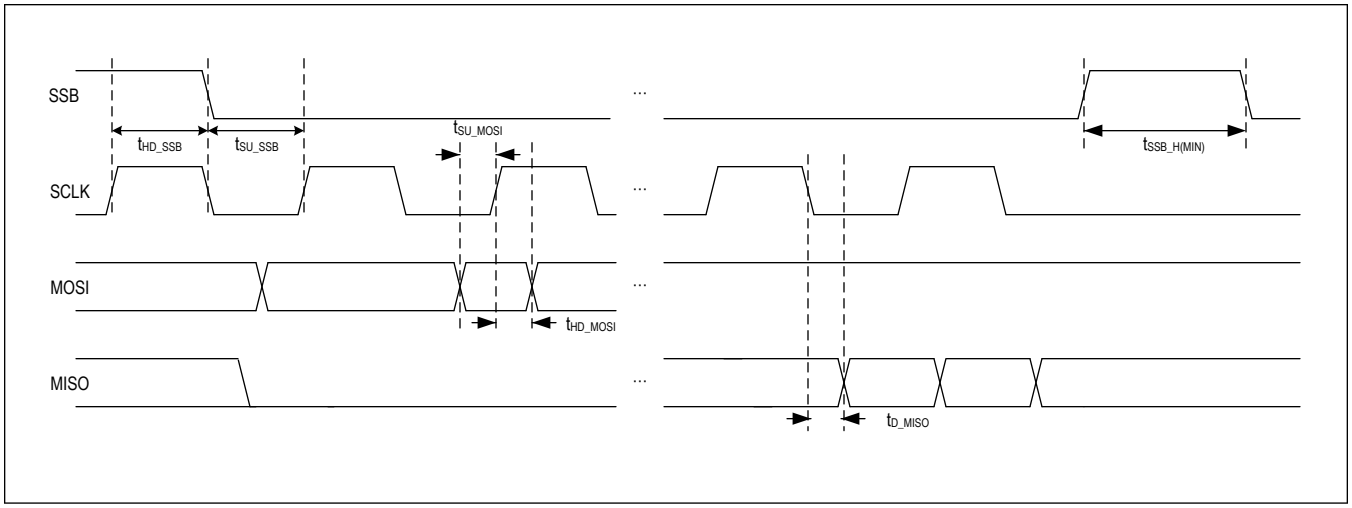


Figure 5. SPI Interface Timing Diagram

Features

The SPI slave controller has the following features:

- Slave Only
- Single Read/Write Support
- Burst Read/Write Support
- Up to 25MHz Operating Frequency

Frame Structure

Figure 6 shows the frame structure for writing to and reading from a register of the IC.

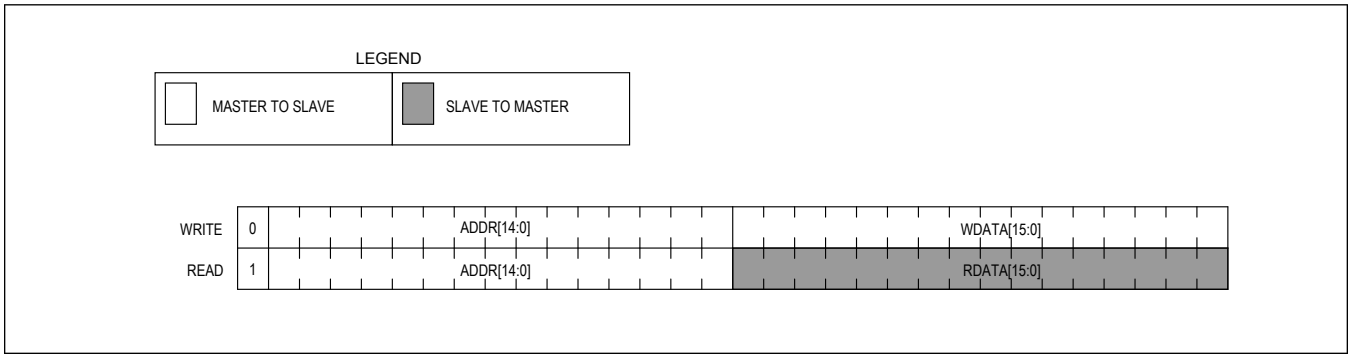


Figure 6. SPI Single Read/Write Frame Structure

Read/Write Bits

The first bit indicates either read (1) or write (0) frame.

Address Bits (ADDR[14:0])

After the Read/Write bit, the SPI master controller loads 15 address bits on MOSI that correspond to the address of the register in the IC register map.

Data Bits (RDATA[15:0]/WDATA[15:0])

The SPI slave controller has a 16-bit data bus. For a write command, the SPI master controller loads 16 data bits on MOSI to be written to the register. For a read command, the slave controller loads data onto the MISO which represent the data contained in the register being read.

SPI Write Frame Diagram

As shown in Figure 7, the SPI Write Frame is 32-bits long. It involves a write bit (0), followed by a 15-bit register address, followed by 16-bits of register data.

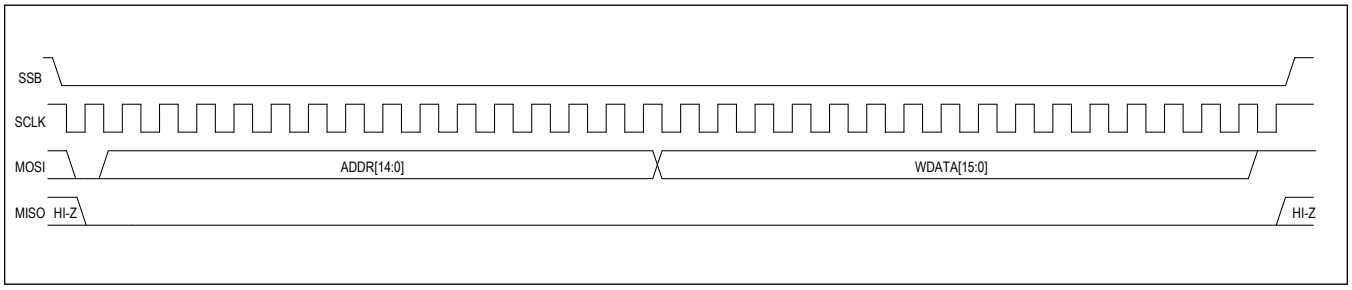


Figure 7. SPI Write Frame

SPI Read Frame Diagram

As shown in Figure 8, the SPI Write Frame is 32-bits long. It involves a write bit (1), followed by a 15-bit register address. The IC responds with 16-bits of data on the MISO line.

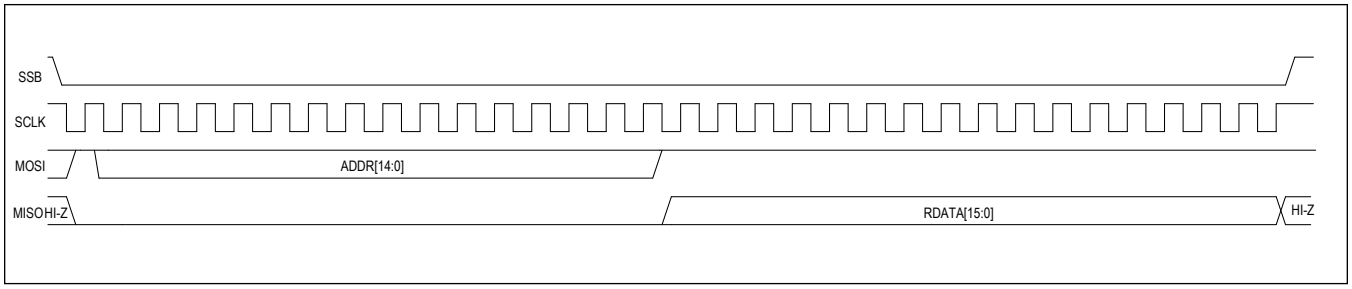


Figure 8. SPI Read Frame

SPI Burst Write Diagram

The IC supports a Burst Write capability. As shown in Figure 9, the host processor sends a write bit (0), followed by a 15-bit address. Afterwards, the host processor can continue to send 16-bits of data to the IC, which auto-increments the register address and writes the data to subsequent register addresses. The exception to this is the FIFO_WRITE_PORT register. For this register, the purpose is to continuously write data to the FIFO, so the auto-increment feature is disabled when burst writing to this register.

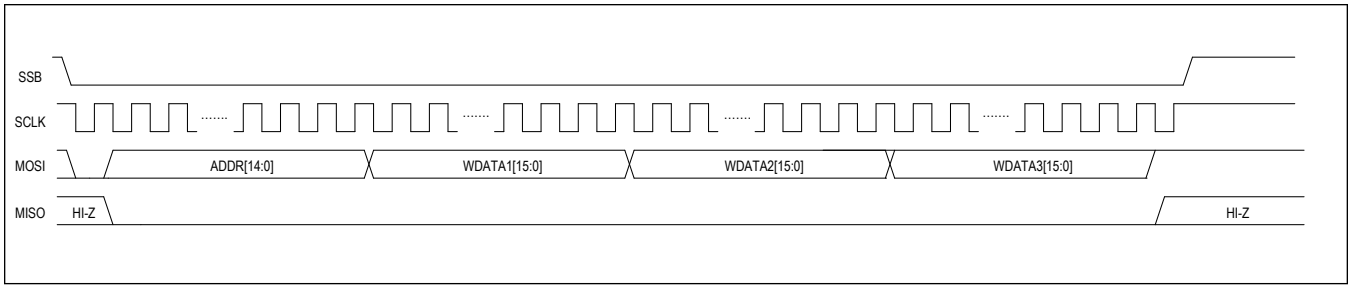


Figure 9. SPI Burst Write Diagram

SPI Burst Read Diagram

The IC supports a Burst Read capability. As shown in Figure 10, the host processor sends a write bit (1), followed by a 15-bit address. Afterwards, the host processor can continue to send a read bit (1) and a 15-bit address. The IC responds with 16-bits of data on the MISO for each register address that is sent during the burst read.

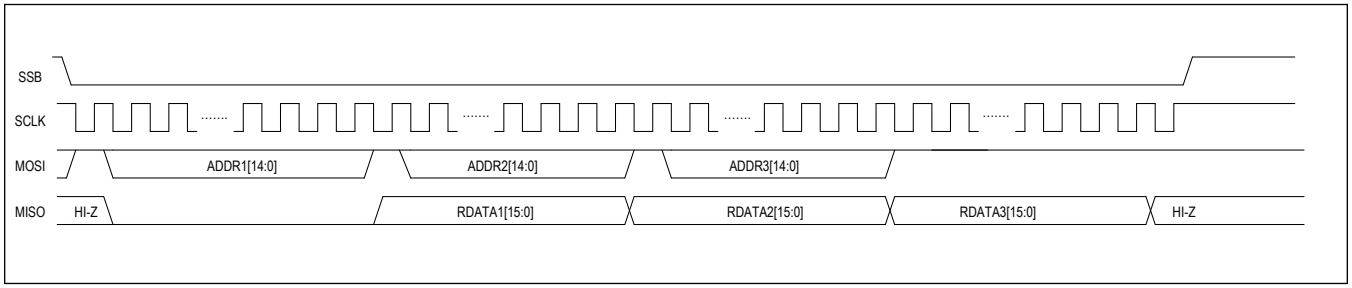


Figure 10. SPI Burst Read Diagram

Register Map

MAX77501

ADDRESS	NAME	MSB							LSB
DIGITAL									
0x00	SOFT_RESET[15:8]	–	–	–	–	–	–	–	–
	SOFT_RESET[7:0]	–	–	–	–	–	–	–	DIGITAL_SOFT_RESET
0x01	STATUS[15:8]	–	–	–	–	–	–	–	–
	STATUS[7:0]	–	FIFO_ALMOST_EMPTY	FIFO_FULL	FIFO_EMPTY	CPOK	UVLO_STATUS	TOK	BOK
0x02	RAM_PLAY[15:8]	–	–	–	–	–	–	–	–
	RAM_PLAY[7:0]	–	–	–	–	–	–	ABORT_FIFO	RAM_PLAY
0x03	CONFIGURATION[15:8]	–	–	–	–	–	–	–	–
	CONFIGURATION[7:0]	–	FIFO_AE_LEVEL[1:0]		SMP_RATE[1:0]		ILIM_SEL[1:0]		FULL_SCALE
0x04	FAULT_CTRL[15:8]	–	ALLOW_NEW_REQ	–	–	–	–	–	–
	FAULT_CTRL[7:0]	–	NUM_NO_ILIM[1:0]		ILIM_FAULT[2:0]			ILIM_WARN[1:0]	
0x05	FAULT_PROTECT[15:8]	–	–	–	–	–	–	–	–
	FAULT_PROTECT[7:0]	–	–	–	FP_CPOK	FP_UVLO	FP_TOK	FP_BOK	FP_nEN
0x06	ISR[15:8]	–	ISR_SPI_RDY	ISR_INVALID_ADDR	ISR_EMPTY_RAM	ISR_ADDR_OVERFLOW	ISR_FIFO_OVERFLOW	–	–
	ISR[7:0]	ISR_ILIM_FAULT	ISR_ILIM_WARN	ISR_CPOK_TO	ISR_CPOK	ISR_UVLO	ISR_TOK	ISR_BOK	ISR_nEN
0x07	IMR[15:8]	–	IMR_SPI_RDY	IMR_INVALID_ADDR	IMR_EMPTY_RAM	IMR_ADDR_OVERFLOW	IMR_FIFO_OVERFLOW	–	–
	IMR[7:0]	IMR_ILIM_FAULT	IMR_ILIM_WARN	IMR_CPOK_TO	IMR_CPOK	IMR_UVLO	IMR_TOK	IMR_BOK	IMR_nEN
0x08	FIFO_TOTAL_DEPTH[15:8]	–	–	FIFO_TOTAL_DEPTH[13:8]					
	FIFO_TOTAL_DEPTH[7:0]	FIFO_TOTAL_DEPTH[7:0]							
0x09	FIFO_EMPTY_DEPTH[15:8]	–	–	FIFO_EMPTY_DEPTH[13:8]					
	FIFO_EMPTY_DEPTH[7:0]	FIFO_EMPTY_DEPTH[7:0]							

ADDRESS	NAME	MSB							LSB
0x0A	FIFO_WRITE_PORT[15:8]	–	–	–	–	FIFO_WRITE_PORT[11:8]			
	FIFO_WRITE_PORT[7:0]	FIFO_WRITE_PORT[7:0]							
0x0B	RAM_READ_ADDR[15:8]	–	–	RAM_READ_ADDR[13:8]					
	RAM_READ_ADDR[7:0]	RAM_READ_ADDR[7:0]							
0x0C	RAM_READ_DATA[15:8]	–	–	–	–	RAM_READ_DATA[11:8]			
	RAM_READ_DATA[7:0]	RAM_READ_DATA[7:0]							
0x0D	NUM_WAVEFORMS[15:8]	–	–	–	NUM_WAVEFORMS_PLAY[4:0]				
	NUM_WAVEFORMS[7:0]	–	–	–	NUM_WAVEFORMS_STORED[4:0]				
0x0E	WAVEFORM_0_EA[15:8]	–	–	WAVEFORM_0_EA[13:8]					
	WAVEFORM_0_EA[7:0]	WAVEFORM_0_EA[7:0]							
0x0F	WAVEFORM_1_EA[15:8]	–	–	WAVEFORM_1_EA[13:8]					
	WAVEFORM_1_EA[7:0]	WAVEFORM_1_EA[7:0]							
0x10	WAVEFORM_2_EA[15:8]	–	–	WAVEFORM_2_EA[13:8]					
	WAVEFORM_2_EA[7:0]	WAVEFORM_2_EA[7:0]							
0x11	WAVEFORM_3_EA[15:8]	–	–	WAVEFORM_3_EA[13:8]					
	WAVEFORM_3_EA[7:0]	WAVEFORM_3_EA[7:0]							
0x12	WAVEFORM_4_EA[15:8]	–	–	WAVEFORM_4_EA[13:8]					
	WAVEFORM_4_EA[7:0]	WAVEFORM_4_EA[7:0]							
0x13	WAVEFORM_5_EA[15:8]	–	–	WAVEFORM_5_EA[13:8]					
	WAVEFORM_5_EA[7:0]	WAVEFORM_5_EA[7:0]							
0x14	WAVEFORM_6_EA[15:8]	–	–	WAVEFORM_6_EA[13:8]					
	WAVEFORM_6_EA[7:0]	WAVEFORM_6_EA[7:0]							
0x15	WAVEFORM_7_EA[15:8]	–	–	WAVEFORM_7_EA[13:8]					
	WAVEFORM_7_EA[7:0]	WAVEFORM_7_EA[7:0]							
0x16	WAVEFORM_8_EA[15:8]	–	–	WAVEFORM_8_EA[13:8]					
	WAVEFORM_8_EA[7:0]	WAVEFORM_8_EA[7:0]							
0x17	WAVEFORM_9_EA[15:8]	–	–	WAVEFORM_9_EA[13:8]					
	WAVEFORM_9_EA[7:0]	WAVEFORM_9_EA[7:0]							

ADDRESS	NAME	MSB							LSB
0x18	WAVEFORM_10_EA[15:8]	–	–	WAVEFORM_10_EA[13:8]					
	WAVEFORM_10_EA[7:0]	WAVEFORM_10_EA[7:0]							
0x19	WAVEFORM_11_EA[15:8]	–	–	WAVEFORM_11_EA[13:8]					
	WAVEFORM_11_EA[7:0]	WAVEFORM_11_EA[7:0]							
0x1A	WAVEFORM_12_EA[15:8]	–	–	WAVEFORM_12_EA[13:8]					
	WAVEFORM_12_EA[7:0]	WAVEFORM_12_EA[7:0]							
0x1B	WAVEFORM_13_EA[15:8]	–	–	WAVEFORM_13_EA[13:8]					
	WAVEFORM_13_EA[7:0]	WAVEFORM_13_EA[7:0]							
0x1C	WAVEFORM_14_EA[15:8]	–	–	WAVEFORM_14_EA[13:8]					
	WAVEFORM_14_EA[7:0]	WAVEFORM_14_EA[7:0]							
0x1D	WAVEFORM_15_EA[15:8]	–	–	WAVEFORM_15_EA[13:8]					
	WAVEFORM_15_EA[7:0]	WAVEFORM_15_EA[7:0]							
0x1E	PLAY_0[15:8]	PLAY_0_REPEAT[7:0]							
	PLAY_0[7:0]	–	–	–	–	PLAY_0_ID[3:0]			
0x1F	PLAY_1[15:8]	PLAY_1_REPEAT[7:0]							
	PLAY_1[7:0]	–	–	–	–	PLAY_1_ID[3:0]			
0x20	PLAY_2[15:8]	PLAY_2_REPEAT[7:0]							
	PLAY_2[7:0]	–	–	–	–	PLAY_2_ID[3:0]			
0x21	PLAY_3[15:8]	PLAY_3_REPEAT[7:0]							
	PLAY_3[7:0]	–	–	–	–	PLAY_3_ID[3:0]			
0x22	PLAY_4[15:8]	PLAY_4_REPEAT[7:0]							
	PLAY_4[7:0]	–	–	–	–	PLAY_4_ID[3:0]			
0x23	PLAY_5[15:8]	PLAY_5_REPEAT[7:0]							
	PLAY_5[7:0]	–	–	–	–	PLAY_5_ID[3:0]			
0x24	PLAY_6[15:8]	PLAY_6_REPEAT[7:0]							
	PLAY_6[7:0]	–	–	–	–	PLAY_6_ID[3:0]			
0x25	PLAY_7[15:8]	PLAY_7_REPEAT[7:0]							
	PLAY_7[7:0]	–	–	–	–	PLAY_7_ID[3:0]			
0x26	PLAY_8[15:8]	PLAY_8_REPEAT[7:0]							
	PLAY_8[7:0]	–	–	–	–	PLAY_8_ID[3:0]			
0x27	PLAY_9[15:8]	PLAY_9_REPEAT[7:0]							
	PLAY_9[7:0]	–	–	–	–	PLAY_9_ID[3:0]			

ADDRESS	NAME	MSB							LSB
0x28	PLAY_10[15:8]	PLAY_10_REPEAT[7:0]							
	PLAY_10[7:0]	–	–	–	–	PLAY_10_ID[3:0]			
0x29	PLAY_11[15:8]	PLAY_11_REPEAT[7:0]							
	PLAY_11[7:0]	–	–	–	–	PLAY_11_ID[3:0]			
0x2A	PLAY_12[15:8]	PLAY_12_REPEAT[7:0]							
	PLAY_12[7:0]	–	–	–	–	PLAY_12_ID[3:0]			
0x2B	PLAY_13[15:8]	PLAY_13_REPEAT[7:0]							
	PLAY_13[7:0]	–	–	–	–	PLAY_13_ID[3:0]			
0x2C	PLAY_14[15:8]	PLAY_14_REPEAT[7:0]							
	PLAY_14[7:0]	–	–	–	–	PLAY_14_ID[3:0]			
0x2D	PLAY_15[15:8]	PLAY_15_REPEAT[7:0]							
	PLAY_15[7:0]	–	–	–	–	PLAY_15_ID[3:0]			
0x2E	MISC[15:8]	–	–	–	–	–	–	–	–
	MISC[7:0]	–	–	–	FAULT_DLY[1:0]		SLEW_RATE[2:0]		

Register Details

SOFT_RESET (0x0)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	–	DIGITAL_SOFT_RESET
Reset	–	–	–	–	–	–	–	0x0
Access Type	–	–	–	–	–	–	–	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
DIGITAL_SOFT_RESET	0	Self-Cleared Digital Soft Reset	0x0: No action 0x1: Resets the digital block except the SPI interface and self-clears this register bit.

STATUS (0x1)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	FIFO_ALMOST_EMPTY	FIFO_FULL	FIFO_EMPTY	CPOK	UVLO_STATUS	TOK	BOK
Reset	–	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	–	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only	Read Only

BITFIELD	BITS	DESCRIPTION	DECODE
FIFO_ALMOST_EMPTY	6	FIFO Almost Empty. The threshold of this register is controlled by the FIFO_AE_LEVEL register.	0x0: FIFO is not almost empty. 0x1: FIFO is almost empty.
FIFO_FULL	5	FIFO Full Status	0x0: FIFO is not full. 0x1: FIFO is full.
FIFO_EMPTY	4	FIFO Empty Status	0x0: FIFO is not empty. 0x1: FIFO is empty.
CPOK	3	CPOK Status	0x0: The charge pump voltages are below the charge pump VOK. 0x1: The charge pump voltages are above the charge pump VOK.
UVLO_STATUS	2	UVLO Status	0x0: The V_{IN} voltage is below UVLO. 0x1: The V_{IN} voltage is above UVLO.
TOK	1	Temperature Okay Status	0x0: The junction temperature of the part has exceeded 165°C. 0x1: The junction temperature of the part is below 165°C.
BOK	0	BIAS Okay Status	0x0: The bias circuitry has failed. 0x1: The bias circuitry is operating as expected.

RAM_PLAY (0x2)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	–	–	ABORT_FIFO	RAM_PLAY
Reset	–	–	–	–	–	–	0x0	0x0
Access Type	–	–	–	–	–	–	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
ABORT_FIFO	1	Abort FIFO playback and flush all data in FIFO.	0x0: Do not abort FIFO playback. 0x1: Abort FIFO playback and flush all data in FIFO.

BITFIELD	BITS	DESCRIPTION	DECODE
RAM_PLAY	0	Start prestored RAM Playback Mode. Write 1 to start RAM Playback Mode. This bit is automatically set to 0 when playback is done. Writing 0 to this bit stops any ongoing playback.	0x0: Stop RAM Playback mode. 0x1: Start RAM Playback mode.

CONFIGURATION (0x3)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	FIFO_AE_LEVEL[1:0]		SMP_RATE[1:0]		ILIM_SEL[1:0]		FULL_SCALE
Reset	–	0x2		0x1		0x2		0x1
Access Type	–	Write, Read		Write, Read		Write, Read		Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FIFO_AE_LEVEL	6:5	FIFO Almost Empty Level. When the FIFO emptiness reaches the level specified in this register, the IC asserts the FIFO pin by pulling it low to indicate that it's time to refill the FIFO.	0x0: At least 125µs until empty. 0x1: At least 250µs until empty. 0x2: At least 500µs until emtpy. 0x3: At least 2ms until empty.
SMP_RATE	4:3	DAC Output Sampling Rate. Sets the sampling rate that the DAC samples the FIFO and RAM.	0x0: 8kHz 0x1: 32kHz 0x2: 48kHz 0x3: Reserved
ILIM_SEL	2:1	Current Limit Select. Sets the current limit of the part. The value assumes that a 100mΩ sense resistor is being used.	0x0: ILIM = 1A 0x1: ILIM = 2A 0x2: ILIM = 3A 0x3: ILIM = 4A
FULL_SCALE	0	Selects the Full-Scale Haptic Output Level of the Converter	0x0: Full-Scale Output = 60Vpp 0x1: Full-Scale Output = 110Vpp

FAULT_CTRL (0x4)

BIT	15	14	13	12	11	10	9	8
Field	–	ALLOW_NEW_REQ	–	–	–	–	–	–
Reset	–	0x0	–	–	–	–	–	–
Access Type	–	Write, Read	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	NUM_NO_ILIM[1:0]		ILIM_FAULT[2:0]			ILIM_WARN[1:0]	
Reset	–	0x0		0x0			0x1	
Access Type	–	Write, Read		Write, Read			Write, Read	

BITFIELD	BITS	DESCRIPTION	DECODE
ALLOW_NEW_REQ	14	Allow new waveform playback request even if fault interrupts are not cleared.	0x0: No playback request accepted until fault interrupts cleared. 0x1: Continue accepting playback requests even if fault interrupts are not cleared.
NUM_NO_ILIM	6:5	Number of boost-converter on-time cycles without ILIM pulses required to reset the ILIM pulse counter that determines the ILIM Warning and Fault conditions.	0x0: 2 cycles 0x1: 8 cycles 0x2: 16 cycles 0x3: 64 cycles
ILIM_FAULT	4:2	Number of ILIM warnings required to trigger an ILIM fault and auto-fault protection.	0x0: 4 warnings 0x1: 8 warnings 0x2: 16 warnings 0x3: 32 warnings 0x4: 64 warnings 0x5: 128 warnings 0x6: 256 warnings 0x7: No ILIM auto protection
ILIM_WARN	1:0	Number of consecutive ILIM pulses required to trigger an ILIM Warning.	0x0: 128 consecutive pulses 0x1: 256 consecutive pulses 0x2: 512 consecutive pulses 0x3: 1024 consecutive pulses

FAULT_PROTECT (0x5)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FP_CPOK	FP_UVLO	FP_TOK	FP_BOK	FP_nEN
Reset	–	–	–	0x1	0x1	0x1	0x1	0x1
Access Type	–	–	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
FP_CPOK	4	Auto Fault Protection for CPOK	0x0: Disable auto protection. 0x1: Enable auto protection.
FP_UVLO	3	Auto Fault Protection for UVLO	0x0: Disable auto protection. 0x1: Enable auto protection.
FP_TOK	2	Auto Fault Protection for TOK	0x0: Disable auto protection. 0x1: Enable auto protection.
FP_BOK	1	Auto Fault Protection for BOK	0x0: Disable auto protection. 0x1: Enable auto protection.
FP_nEN	0	Auto Fault Protection for nEN	0x0: Disable auto protection. 0x1: Enable auto protection.

ISR (0x6)

BIT	15	14	13	12	11	10	9	8
Field	–	ISR_SPI_RDY	ISR_INVALID_ADDR	ISR_EMPTY_RAM	ISR_ADDR_OVERFLOW	ISR_FIFO_OVERFLOW	–	–
Reset	–	0x0	0x0	0x0	0x0	0x0	–	–
Access Type	–	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	–	–

BIT	7	6	5	4	3	2	1	0
Field	ISR_ILIM_FAULT	ISR_ILIM_WARN	ISR_CPOK_TO	ISR_CPOK	ISR_UVLO	ISR_TOK	ISR_BOK	ISR_nEN
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All	Read Clears All

BITFIELD	BITS	DESCRIPTION	DECODE
ISR_SPI_RDY	14	SPI ready signal indicating when the SPI slave is ready to receive commands.	0x0: Condition not detected. 0x1: Condition detected.
ISR_INVALID_ADDR	13	RAM Playback attempted while NUM_WAVEFORMS_PLAY is 0 or there were conflicts in the ending address registers.	0x0: Condition not detected. 0x1: Condition detected.
ISR_EMPTY_RAM	12	RAM Playback attempted while the RAM was empty (i.e., the NUM_WAVEFORMS_STORED register was 0).	0x0: Condition not detected. 0x1: Condition detected.
ISR_ADDR_OVERFLOW	11	RAM address overflow detected during auto-increment for burst read/write operation, i.e., it went over 0x3FFF.	0x0: Condition not detected. 0x1: Condition detected.
ISR_FIFO_OVERFLOW	10	FIFO write attempted while FIFO was full	0x0: Condition not detected. 0x1: Condition detected.
ISR_ILIM_FAULT	7	ILIM Fault Interrupt	0x0: Condition not detected 0x1: The number of ILIM Warnings set by the ILIM_FAULT register have occurred creating a fault condition.
ISR_ILIM_WARN	6	ILIM warning interrupt	0x0: Condition not detected 0x1: The number of ILIM pulses set by the ILIM_WARN register have been counted to cause a warning.
ISR_CPOK_TO	5	CPOK not detected for 2ms after the haptic request has occurred.	0x0: Condition not detected. 0x1: The charge pump voltages have not come above the V_5 charge pump VOK and V_{DD_H} charge pump VOK levels within 2ms of the haptic request.
ISR_CPOK	4	CPOK is no longer valid	0x0: CPOK is still valid. 0x1: The charge pump output voltages have fallen below the V_5 VOK level or the V_{DD_H} VOK level.
ISR_UVLO	3	Undervoltage-Lockout Interrupt Status	0x0: V_{IN} has not fallen below the UVLO voltage level. 0x1: V_{IN} voltage has fallen below the UVLO voltage level.

BITFIELD	BITS	DESCRIPTION	DECODE
ISR_TOK	2	Temperature Okay Interrupt Status Register	0x0: A temperature okay fault condition has not occurred. 0x1: The junction temperature of the part is below 165°C.
ISR_BOK	1	Bias Circuitry Failure Interrupt	0x0: Bias circuitry has not failed. 0x1: Bias circuitry has failed.
ISR_nEN	0	Rising Edge of nEN Detected	0x0: nEN has not gone high. 0x1: nEN has gone high during haptic operation.

IMR (0x7)

BIT	15	14	13	12	11	10	9	8
Field	–	IMR_SPI_RDY	IMR_INVALID_ADDR	IMR_EMPTY_RAM	IMR_ADDR_OVERFLOW	IMR_FIFO_OVERFLOW	–	–
Reset	–	0x0	0x0	0x0	0x0	0x0	–	–
Access Type	–	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	–	–

BIT	7	6	5	4	3	2	1	0
Field	IMR_ILIM_FAULT	IMR_ILIM_WARN	IMR_CPOK_TO	IMR_CPOK	IMR_UVLO	IMR_TOK	IMR_BOK	IMR_nEN
Reset	0x0	0x0	0x0	0x0	0x0	0x0	0x0	0x0
Access Type	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read	Write, Read

BITFIELD	BITS	DESCRIPTION	DECODE
IMR_SPI_RDY	14	Interrupt Mask for SPI Ready	0x0: Enable the interrupt. 0x1: Mask the interrupt.
IMR_INVALID_ADDR	13	Interrupt Mask for INVALID_ADDR	0x0: Enable the interrupt. 0x1: Mask the interrupt.
IMR_EMPTY_RAM	12	Interrupt Mask for EMPTY_RAM	0x0: Enable the interrupt. 0x1: Mask the interrupt.
IMR_ADDR_OVERFLOW	11	Interrupt Mask for ADDR_OVERFLOW	0x0: Enable the interrupt. 0x1: Mask the interrupt.
IMR_FIFO_OVERFLOW	10	Interrupt Mask for FIFO_OVERFLOW	0x0: Enable the interrupt. 0x1: Mask the interrupt.
IMR_ILIM_FAULT	7	Interrupt Mask for ILIM Fault	0x0: Enable the interrupt. 0x1: Mask the interrupt.
IMR_ILIM_WARN	6	Interrupt Mask for ILIM Warning	0x0: Enable the interrupt. 0x1: Mask the interrupt.
IMR_CPOK_TO	5	Interrupt Mask for CPOK_TO	0x0: Enable the interrupt. 0x1: Mask the interrupt.
IMR_CPOK	4	Interrupt Mask for CPOK	0x0: Enable the interrupt. 0x1: Mask the interrupt.
IMR_UVLO	3	Interrupt Mask for UVLO	0x0: Enable the interrupt. 0x1: Mask the interrupt.
IMR_TOK	2	Interrupt Mask for TOK	0x0: Enable the interrupt. 0x1: Mask the interrupt.

BITFIELD	BITS	DESCRIPTION	DECODE
IMR_BOK	1	Interrupt Mask for BOK	0x0: Enable the interrupt. 0x1: Mask the interrupt.
IMR_nEN	0	Interrupt Mask for nEN	0x0: Enable the interrupt. 0x1: Mask the interrupt.

FIFO_TOTAL_DEPTH (0x8)

BIT	15	14	13	12	11	10	9	8
Field	–	–	FIFO_TOTAL_DEPTH[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Read Only					

BIT	7	6	5	4	3	2	1	0
Field	FIFO_TOTAL_DEPTH[7:0]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FIFO_TOTAL_DEPTH	13:0	Indicates the total available size for FIFO. This is the total size of the RAM minus the size of the data currently stored for RAM Playback mode.

FIFO_EMPTY_DEPTH (0x9)

BIT	15	14	13	12	11	10	9	8
Field	–	–	FIFO_EMPTY_DEPTH[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Read Only					

BIT	7	6	5	4	3	2	1	0
Field	FIFO_EMPTY_DEPTH[7:0]							
Reset	0x0000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
FIFO_EMPTY_DEPTH	13:0	Indicates the number of entries that can currently be written to the FIFO.

FIFO_WRITE_PORT (0xA)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	FIFO_WRITE_PORT[11:8]			
Reset	–	–	–	–	0x000			
Access Type	–	–	–	–	Write Only			

BIT	7	6	5	4	3	2	1	0
Field	FIFO_WRITE_PORT[7:0]							
Reset	0x000							
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
FIFO_WRITE_PORT	11:0	FIFO write port. Every write to this register is placed in the FIFO queue.

RAM_READ_ADDR (0xB)

BIT	15	14	13	12	11	10	9	8
Field	–	–	RAM_READ_ADDR[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write Only					

BIT	7	6	5	4	3	2	1	0
Field	RAM_READ_ADDR[7:0]							
Reset	0x0000							
Access Type	Write Only							

BITFIELD	BITS	DESCRIPTION
RAM_READ_ADDR	13:0	RAM read address. Write the starting address to be read from the RAM here.

RAM_READ_DATA (0xC)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	RAM_READ_DATA[11:8]			
Reset	–	–	–	–	0x000			
Access Type	–	–	–	–	Read Only			

BIT	7	6	5	4	3	2	1	0
Field	RAM_READ_DATA[7:0]							
Reset	0x000							
Access Type	Read Only							

BITFIELD	BITS	DESCRIPTION
RAM_READ_DATA	11:0	RAM Read Data. After writing to RAM_READ_ADDR, the IC stores the data stored at that RAM address in this register so that it can be read using an SPI Read command.

NUM_WAVEFORMS (0xD)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	NUM_WAVEFORMS_PLAY[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Write, Read				

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	NUM_WAVEFORMS_STORED[4:0]				
Reset	–	–	–	0x00				
Access Type	–	–	–	Write, Read				

BITFIELD	BITS	DESCRIPTION
NUM_WAVEFORMS_PLAY	12:8	Number of Waveforms to Play. This has to be set before RAM_PLAY bit is programmed. The device plays this many waveforms stored in the waveform playlist.
NUM_WAVEFORMS_STORED	4:0	Number of Waveforms Stored in the RAM. Program this register to the number of waveforms that have been programmed for playback.

WAVEFORM_0_EA (0xE)

BIT	15	14	13	12	11	10	9	8
Field	–	–	WAVEFORM_0_EA[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	WAVEFORM_0_EA[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAVEFORM_0_EA	13:0	Ending address for Waveform 0.

WAVEFORM_1_EA (0xF)

BIT	15	14	13	12	11	10	9	8
Field	–	–	WAVEFORM_1_EA[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	WAVEFORM_1_EA[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAVEFORM_1_EA	13:0	Ending address for Waveform 1.

WAVEFORM_2_EA (0x10)

BIT	15	14	13	12	11	10	9	8
Field	–	–	WAVEFORM_2_EA[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	WAVEFORM_2_EA[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAVEFORM_2_EA	13:0	Ending address for Waveform 2.

WAVEFORM_3_EA (0x11)

BIT	15	14	13	12	11	10	9	8
Field	–	–	WAVEFORM_3_EA[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	WAVEFORM_3_EA[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAVEFORM_3_EA	13:0	Ending address for Waveform 3.

WAVEFORM_4_EA (0x12)

BIT	15	14	13	12	11	10	9	8
Field	–	–	WAVEFORM_4_EA[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	WAVEFORM_4_EA[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAVEFORM_4_EA	13:0	Ending address for Waveform 4.

WAVEFORM_5_EA (0x13)

BIT	15	14	13	12	11	10	9	8
Field	–	–	WAVEFORM_5_EA[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	WAVEFORM_5_EA[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAVEFORM_5_EA	13:0	Ending address for Waveform 5.

WAVEFORM_6_EA (0x14)

BIT	15	14	13	12	11	10	9	8
Field	–	–	WAVEFORM_6_EA[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	WAVEFORM_6_EA[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAVEFORM_6_EA	13:0	Ending address for Waveform 6.

WAVEFORM_7_EA (0x15)

BIT	15	14	13	12	11	10	9	8
Field	–	–	WAVEFORM_7_EA[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	WAVEFORM_7_EA[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAVEFORM_7_EA	13:0	Ending address for Waveform 7.

WAVEFORM_8_EA (0x16)

BIT	15	14	13	12	11	10	9	8
Field	–	–	WAVEFORM_8_EA[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	WAVEFORM_8_EA[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAVEFORM_8_EA	13:0	Ending address for Waveform 8.

WAVEFORM_9_EA (0x17)

BIT	15	14	13	12	11	10	9	8
Field	–	–	WAVEFORM_9_EA[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	WAVEFORM_9_EA[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAVEFORM_9_EA	13:0	Ending address for Waveform 9.

WAVEFORM_10_EA (0x18)

BIT	15	14	13	12	11	10	9	8
Field	–	–	WAVEFORM_10_EA[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	WAVEFORM_10_EA[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAVEFORM_10_EA	13:0	Ending address for Waveform 10.

WAVEFORM_11_EA (0x19)

BIT	15	14	13	12	11	10	9	8
Field	–	–	WAVEFORM_11_EA[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	WAVEFORM_11_EA[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAVEFORM_11_EA	13:0	Ending address for Waveform 11.

WAVEFORM_12_EA (0x1A)

BIT	15	14	13	12	11	10	9	8
Field	–	–	WAVEFORM_12_EA[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	WAVEFORM_12_EA[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAVEFORM_12_EA	13:0	Ending address for Waveform 12.

WAVEFORM_13_EA (0x1B)

BIT	15	14	13	12	11	10	9	8
Field	–	–	WAVEFORM_13_EA[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	WAVEFORM_13_EA[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAVEFORM_13_EA	13:0	Ending address for Waveform 13.

WAVEFORM_14_EA (0x1C)

BIT	15	14	13	12	11	10	9	8
Field	–	–	WAVEFORM_14_EA[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	WAVEFORM_14_EA[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAVEFORM_14_EA	13:0	Ending address for Waveform 14.

WAVEFORM_15_EA (0x1D)

BIT	15	14	13	12	11	10	9	8
Field	–	–	WAVEFORM_15_EA[13:8]					
Reset	–	–	0x0000					
Access Type	–	–	Write, Read					

BIT	7	6	5	4	3	2	1	0
Field	WAVEFORM_15_EA[7:0]							
Reset	0x0000							
Access Type	Write, Read							

BITFIELD	BITS	DESCRIPTION
WAVEFORM_15_EA	13:0	Ending address for Waveform 15.

PLAY_0 (0x1E)

BIT	15	14	13	12	11	10	9	8
Field	PLAY_0_REPEAT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PLAY_0_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
PLAY_0_REPEAT	15:8	Number of times the corresponding waveform should be played. If set to 0, the waveform plays infinitely until the RAM_PLAY bit is set to 0.
PLAY_0_ID	3:0	Waveform ID of the first waveform to be played.

PLAY_1 (0x1F)

BIT	15	14	13	12	11	10	9	8
Field	PLAY_1_REPEAT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PLAY_1_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
PLAY_1_REPEAT	15:8	Number of times the corresponding waveform should be played. If set to 0, the waveform plays infinitely until the RAM_PLAY bit is set to 0.
PLAY_1_ID	3:0	Waveform ID of the second waveform to be played.

PLAY_2 (0x20)

BIT	15	14	13	12	11	10	9	8
Field	PLAY_2_REPEAT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PLAY_2_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
PLAY_2_REPEAT	15:8	Number of times the corresponding waveform should be played. If set to 0, the waveform plays infinitely until the RAM_PLAY bit is set to 0.
PLAY_2_ID	3:0	Waveform ID of the third waveform to be played.

PLAY_3 (0x21)

BIT	15	14	13	12	11	10	9	8
Field	PLAY_3_REPEAT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PLAY_3_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
PLAY_3_REPEAT	15:8	Number of times the corresponding waveform should be played. If set to 0, the waveform plays infinitely until the RAM_PLAY bit is set to 0.
PLAY_3_ID	3:0	Waveform ID of the fourth waveform to be played.

PLAY_4 (0x22)

BIT	15	14	13	12	11	10	9	8
Field	PLAY_4_REPEAT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PLAY_4_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
PLAY_4_REPEAT	15:8	Number of times the corresponding waveform should be played. If set to 0, the waveform plays infinitely until the RAM_PLAY bit is set to 0.
PLAY_4_ID	3:0	Waveform ID of the fifth waveform to be played.

PLAY_5 (0x23)

BIT	15	14	13	12	11	10	9	8
Field	PLAY_5_REPEAT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PLAY_5_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
PLAY_5_REPEAT	15:8	Number of times the corresponding waveform should be played. If set to 0, the waveform plays infinitely until the RAM_PLAY bit is set to 0.
PLAY_5_ID	3:0	Waveform ID of the sixth waveform to be played.

PLAY_6 (0x24)

BIT	15	14	13	12	11	10	9	8
Field	PLAY_6_REPEAT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PLAY_6_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
PLAY_6_REPEAT	15:8	Number of times the corresponding waveform should be played. If set to 0, the waveform plays infinitely until the RAM_PLAY bit is set to 0.
PLAY_6_ID	3:0	Waveform ID of the seventh waveform to be played.

PLAY_7 (0x25)

BIT	15	14	13	12	11	10	9	8
Field	PLAY_7_REPEAT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PLAY_7_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
PLAY_7_REPEAT	15:8	Number of times the corresponding waveform should be played. If set to 0, the waveform plays infinitely until the RAM_PLAY bit is set to 0.
PLAY_7_ID	3:0	Waveform ID of the eighth waveform to be played.

PLAY_8 (0x26)

BIT	15	14	13	12	11	10	9	8
Field	PLAY_8_REPEAT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PLAY_8_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
PLAY_8_REPEAT	15:8	Number of times the corresponding waveform should be played. If set to 0, the waveform plays infinitely until the RAM_PLAY bit is set to 0.
PLAY_8_ID	3:0	Waveform ID of the nineth waveform to be played.

PLAY_9 (0x27)

BIT	15	14	13	12	11	10	9	8
Field	PLAY_9_REPEAT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PLAY_9_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
PLAY_9_REPEAT	15:8	Number of times the corresponding waveform should be played. If set to 0, the waveform plays infinitely until the RAM_PLAY bit is set to 0.
PLAY_9_ID	3:0	Waveform ID of the 10th waveform to be played.

PLAY_10 (0x28)

BIT	15	14	13	12	11	10	9	8
Field	PLAY_10_REPEAT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PLAY_10_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
PLAY_10_REPEAT	15:8	Number of times the corresponding waveform should be played. If set to 0, the waveform plays infinitely until the RAM_PLAY bit is set to 0.
PLAY_10_ID	3:0	Waveform ID of the 11th waveform to be played.

PLAY_11 (0x29)

BIT	15	14	13	12	11	10	9	8
Field	PLAY_11_REPEAT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PLAY_11_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
PLAY_11_REPEAT	15:8	Number of times the corresponding waveform should be played. If set to 0, the waveform plays infinitely until the RAM_PLAY bit is set to 0.
PLAY_11_ID	3:0	Waveform ID of the 12th waveform to be played.

PLAY_12 (0x2A)

BIT	15	14	13	12	11	10	9	8
Field	PLAY_12_REPEAT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PLAY_12_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
PLAY_12_REPEAT	15:8	Number of times the corresponding waveform should be played. If set to 0, the waveform plays infinitely until the RAM_PLAY bit is set to 0.
PLAY_12_ID	3:0	Waveform ID of the 13th waveform to be played.

PLAY_13 (0x2B)

BIT	15	14	13	12	11	10	9	8
Field	PLAY_13_REPEAT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PLAY_13_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
PLAY_13_REPEAT	15:8	Number of times the corresponding waveform should be played. If set to 0, the waveform plays infinitely until the RAM_PLAY bit is set to 0.
PLAY_13_ID	3:0	Waveform ID of the 14th waveform to be played.

PLAY_14 (0x2C)

BIT	15	14	13	12	11	10	9	8
Field	PLAY_14_REPEAT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PLAY_14_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
PLAY_14_REPEAT	15:8	Number of times the corresponding waveform should be played. If set to 0, the waveform plays infinitely until the RAM_PLAY bit is set to 0.
PLAY_14_ID	3:0	Waveform ID of the 15th waveform to be played.

PLAY_15 (0x2D)

BIT	15	14	13	12	11	10	9	8
Field	PLAY_15_REPEAT[7:0]							
Reset	0x01							
Access Type	Write, Read							

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	–	PLAY_15_ID[3:0]			
Reset	–	–	–	–	0x0			
Access Type	–	–	–	–	Write, Read			

BITFIELD	BITS	DESCRIPTION
PLAY_15_REPEAT	15:8	Number of times the corresponding waveform should be played. If set to 0, the waveform plays infinitely until the RAM_PLAY bit is set to 0.
PLAY_15_ID	3:0	Waveform ID of the 16th waveform to be played.

MISC (0x2E)

BIT	15	14	13	12	11	10	9	8
Field	–	–	–	–	–	–	–	–
Reset	–	–	–	–	–	–	–	–
Access Type	–	–	–	–	–	–	–	–

BIT	7	6	5	4	3	2	1	0
Field	–	–	–	FAULT_DLY[1:0]		SLEW_RATE[2:0]		
Reset	–	–	–	0x2		0x0		
Access Type	–	–	–	Write, Read		Write, Read		

BITFIELD	BITS	DESCRIPTION	DECODE
FAULT_DLY	4:3	Delay time to allow enough time for converter to slew down to 10V output after a fault condition occurs prior to entering STANDBY or OFF states.	0x0: 0s 0x1: 1ms 0x2: 2ms 0x3: 4ms

BITFIELD	BITS	DESCRIPTION	DECODE
SLEW_RATE	2:0	Slew Rate Control. DAC value ramps up prior to a haptic waveform and ramps down after a haptic waveform to the minimum DAC value at this rate.	0x0: No slew rate control 0x1: 4µs per LSB 0x2: 2µs per LSB 0x3: 1µs per LSB 0x4: 500ns per LSB 0x5: 250ns per LSB 0x6: 125ns per LSB 0x7: 62.5ns per LSB

Applications Information

nEN Enable Input

nEN is an active-low, digital input that typically comes from the application processor. The purpose of this input is to wake up the IC and enter the STANDBY: INTERRUPTS NOT CLEARED state. Bringing nEN below 1V enables the V_{DD} regulator and the clock generator cells, thus allowing communication through the SPI interface. The SPI I/O block is powered by V_{IO}. As shown in the *State Diagram*, once the STANDBY state is achieved and the SPI Ready Interrupt has been cleared, a haptic signal playback can commence, either from stored RAM data or SPI streaming.

Bringing nEN back above V_{IN} - 1V puts the IC into a SHUTDOWN state (I_{SHDN} < 0.1µA), and all stored RAM and register data is lost. Because the nEN pin is relative to V_{IN}, most processors needs a level shifting FET to pull nEN high and disable the part. A recommended FET is listed in the *External Component Selection Guide* section.

Charge Pumps

Two charge pumps are included in the IC to create internal voltage domains. Charge pump #1 is a regulating charge pump configured to generate 5V (i.e., V_5). It has an external fly capacitor, CF1 and a bypass capacitor to PGND. This voltage is externally filtered to generate V_{CC}, which is used as an internal analog supply. The second charge pump is a non-regulating, voltage doubling charge pump and generates V_{DD_H} which is approximately equal to 9V. The input to this charge pump is V_5. V_{DD_H} is used to power the gate driver cells. A second, external fly capacitor is used by the charge pump and is bypassed to PGND.

As shown in the *State Diagram*, when a playback command is issued the charge pumps are enabled and a CPOK signal is generated when V_{DD_H} is above the V_{DD_H} VOK threshold of 7V. Once CPOK is asserted, the boost converter is allowed to start-up and V_{OUT} follows the playback waveform. After the haptic playback waveform is completed, the boost converter and charge pumps are shutdown and the system returns to STANDBY mode. The charge pump outputs are discharged internally to GND with 200Ω active-discharge resistors to ground.

Piezo Suppliers

Table 12. Piezo Suppliers

PIEZO SUPPLIERS	ADDRESS	EMAIL
MIDE	200 Boston Ave, Ste. 1000, Medford, MA 02155	www.mide.com
Piezo Systems	65 Tower Office Park, Woburn, MA 01801	www.piezo.com
Tokin (Kemet)	2560 N. First St. Ste. 100, San Jose, CA 95131	www.tokin.com
APC	213 Duck Run Rd., PO Box 180, Mackeyville, PA 17750	www.americanpiezo.com

Applications Information—Boost Controller

External Component Selection Guide

Table 13 contains recommended inductor and FETs based on C_{PIEZO}. See the Typical Operating Characteristics for a graph showing the maximum V_{OUT} peak-to-peak swing that can be achieved for each condition for a given sine wave frequency. The data was taken at three frequencies (100Hz, 200Hz, and 300Hz) and represents the maximum V_{OUT} peak-to-peak swing before the signal becomes too distorted.

Table 13. Recommended Inductors and FETs

C_{PIEZO}	INDUCTOR (L)	PFET (Q2)	NFET (Q1)	HIGH SIDE GATE DRIVE LEVEL SHIFT CAPACITOR (C_{HS_G})
30nF to 500nF	Coilcraft LPS6225-103MRB (10µH)	ON Semiconductor FDMC8097AC (N + P Channel)	ON Semiconductor FDMC8097AC (N + P Channel)	2.2nF, 200V
500nF to 2µF	Coilcraft XEL5050-103ME (10µH)	Siliconix SI7317DN-T1-GE3	Siliconix SI7818DN-T1-E3	10nF, 200V

Table 14 contains a list of passive resistors and components used in the *Typical Applications Circuit*.

Table 14. Recommended External Components

COMPONENT	DESCRIPTION	VALUE	RATING
C_L	Inductor Path Input Capacitor	100µF	10V
C_{IN}	IC Input Capacitor	10µF	10V
C_{VDD_H}	9V Charge Pump Output Capacitor	1µF	16V
C_{VSS_H}	V_{SS_H} Decoupling Capacitor	2.2nF	16V
C_{F1}	5V Charge Pump Fly Capacitor	150nF	16V
C_{F2}	9V Charge Pump Fly Capacitor	150nF	16V
R_{FILT_V5}	Filter Resistor from V_5 to V_{CC}	1Ω	1/16W
C_{VCC}	V_{CC} Output Capacitor	2.2µF	10V
C_{V5}	V_5 Output Capacitor	1µF	10V
R_{COT}	Computed Off-Time Resistor	200kΩ	150V, 1/16W
C_{COT}	Computed Off-Time Capacitor	68pF	10V
R_{HS_G}	High-Side Gate Drive Level-Shift Resistor	20kΩ	1/16W
C_{OUT1}	Output Decoupling Capacitor*	100nF	200V
C_{OUT2}	Output Decoupling Capacitor*	10nF	200V
R_{FILT}	Current Sense Filter Resistor	100Ω	1/16W
C_{FILT}	Current Sense Filter Capacitor	390pF	10V
R_{SENSE}	Current Sense Resistor**	100mΩ	(**)
R_{nIRQ}	nIRQ Pullup Resistor	100kΩ	1/16W
R_{FIFO}	FIFO Pullup Resistor	100kΩ	1/16W
R_{nEN}	nEN Pullup Resistor	1MΩ	1/16W
C_{VO_DAC}	DAC Output Capacitor	47pF	10V
C_{VIO}	V_{IO} Decoupling Capacitor	1µF	10V
C_{VDD}	V_{DD} Output Capacitor	1µF	10V

Table 14. Recommended External Components (continued)

COMPONENT	DESCRIPTION	VALUE	RATING
R_{COMP}	Compensation Resistor	60.4kΩ	1/16W
C_{COMP}	Compensation Capacitor	3.3nF	16V
R_{SLP}	Output Slope Compensation Resistor	1MΩ	150V, 1/16W
C_{SLP}	Slope Compensation Capacitor	390pF	16V
R_{SLPV5}	V_5 Slope Compensation Capacitor	200kΩ	1/16W

*C_{OUT} is a ceramic decoupling capacitor at V_{OUT} in parallel with C_{PIEZO}.

**R_{SENSE} requires a 2/3W rating for a 4A ILIM, a 1/2W rating for a 3A ILIM, a 1/4W rating for a 2A ILIM and a 1/10W rating for a 1A ILIM.

Table 15 contains the recommended active components used in the *Typical Applications Circuit*.

Table 15. Recommended Active Components

COMPONENT	DESCRIPTION	RATINGS	PART NUMBER
DZ1	10V Zener Diode for High-Side Gate Drive Level Shift	10V, 350mW	Fairchild BZX84C
Q3	Input Battery Voltage Blocking FET	V_{TH} = 0.8V, I_{DS} = 11A	Diodes Incorporated DMN1019UFDE
Q4	nEN Level Shift FET	V_{TH} = 0.75V, V_{DS} = 20V	Nexperia PMZB290UNE

Depending on the Full-Scale-Output Setting, Table 16 is the selection guide for the feedback resistors.

Table 16. Feedback Resistor Selection Table

FULL SCALE SETTING	R_{FB1}	R_{FB2}
60Vpp	442kΩ	20kΩ
110Vpp	715kΩ	20kΩ

Note that R_{FB1} requires a 1/16W, 150V rating and R_{FB2} requires a 1/16W rating.

FET Selection Guide

The output power FET selection depends on the requirements of the piezo drive application. Table 13 has recommended FET types for typical applications based on piezo capacitance that are used in the MAX77501 evaluation kit. However, it is possible to use alternative FET part numbers if the FET parameters adhere to the following guidelines. These guidelines refer to both the high-side PFET and the low-side NFET.

1. **BVDSS**: Choose a FET breakdown voltage rating that exceeds the desired maximum output voltage, plus some headroom. Generally, add about 10V to maximum V_{OUT}. For example, for a 110Vpp output swing (10V to 120V swing), the minimum BVDSS should be at least 130V (typically a 150V rating is chosen).
2. **ID Rating**: Choose a FET current rating that is > 5A for the NFET and > 1A for the PFET. Discrete FETs have a DC and a pulsed current rating. In a switching regulator like the MAX77501, both ratings apply and the pulsed rating is generally higher than the DC rating. Since the MAX77501 is operated as a boost converter with high duty-cycle, the NFET requires a larger current rating than the PFET.
3. **RDS_{ON}**: Choose RDS_{ON} for the NFET < 150mΩ and < 2Ω for the PFET. FET on-resistance affects power transfer efficiency and generally lower is better. However, there is usually a trade off between RDS_{ON} and Q_G. ID rating requirements are similar to RDS_{ON} requirements in that they are different for the PFET than for the NFET due to high duty cycle operation. Also, both rating requirements are dependent on output power delivery. All else being equal, P_{OUT} is proportional to C_{PIEZO} (i.e., doubling C_{PIEZO}, doubles P_{OUT}).
4. **Gate Drive Voltage (V_{GS})**: Choose FETs that are fully ON with V_{GS_ON} values between 6V and 9V and have a maximum V_{GS} rating of > 10V. Lower V_{GS_ON} ratings are better since, once the FET is fully enhanced, gate charge

requirements are reduced and efficiency is improved.

5. **Gate Charge (Q_G)**: Choose Q_G < 20nC for the NFET and < 5nC for the PFET. As with all switching regulators, efficiency is affected by gate charge. FET Q_G is proportional to it's parameters: BVDSS, ID, V_{GS}, and RDS_{ON}. Choose FETs with the lowest Q_G possible. Additionally, the AC coupling capacitor (C_{HS_G}) forms a voltage divider with gate capacitance ($Q_G = C_G \times V_{GS}$), reducing the gate drive voltage and possibly not turning the FET on sufficiently. Therefore, increased Q_G requires a larger C_{HS_G} capacitor value. Always make sure that the PFET gate drive is greater than the minimum V_{GS_ON} specification in operation.
6. **Gate Series Resistance (R_G)**: Choose R_G < 5Ω. Series gate resistance can cause shoot-through current during LX node transitions, however, some shoot-through current is inevitable. Excessive shoot-through current causes significant energy loss and creates large ground bounces and current sense glitches. Choose the lowest R_G possible. If a FET selection shows significant shoot-through current problems (e.g., loss of output swing or higher input current), then the gate drive strength and/or non-overlap time needs to be modified.
7. **Shoot-Through Current**: As described above, shoot-through current is very problematic and must be minimized. Some FET selections, even with proper parameter selection, still show evidence of shoot-through current. The only sure way to determine if a particular FET selection has shoot-through current problems is to build a test evaluation PCB. The most common evidence of shoot-through current is unexpectedly low output voltage (clipping) and significantly increased input current at clipping. High shoot-through current spikes can also be observed at the CS node. However, since the voltage at CS is a sum of shoot-through current spikes + NFET gate charge-injection, separating the shoot-through spike is difficult. Shoot-through currents are generally larger at high output voltage values, whereas gate-charge injection is generally constant. Therefore, during high output voltage values, excessive shoot-through current spikes become more apparent.
8. **Separate vs. Dual FET Options**: There are two options for the power FET selection, separate FETs or a complementary pair (dual). Both options are listed in Table 13. The dual FET has a smaller footprint but is limited in parameter selection options.

High-Side PFET Drive

As shown in Figure 11, to properly drive the high-side PFET (Q2), an AC coupling capacitor is required from the HS_G pin to the gate of the power PFET. This capacitor level shifts the HS_G drive logic signal from the V_{DD_H} power domain (~9V) to the piezo driver output voltage (V_{OUT}). The gate drive of the PFET follows V_{OUT}. During a power conversion cycle OFF time, the PFET device is turned ON, requiring the gate to be driven to at least V_{OUT} - 8V (to fully enhance the PFET). The 10V Zener diode is in the circuit to catch the negative gate-drive swing and clamp it. Once the OFF time cycle is complete, the PFET gate drive swings positive and the Zener diode is forward biased as the gate is driven above V_{OUT} by a forward diode voltage. At this point, the forward biased Zener diode discharges the stored gate charge in the PFET and turns OFF. There is a voltage division between the AC coupling capacitor (C_{HS_G}) and the gate capacitance of Q2, thereby reducing the effective gate-drive voltage. If the gate capacitance exceeds 10% of C_{HS_G}, then C_{HS_G} should be increased appropriately. However, larger values of C_{HS_G} increase the power consumption of the gate driver and reduces the efficiency. It is important to choose Q2 with a minimum gate charge in order to minimize the value of C_{HS_G}. The resistor (R_{HS_G}) in parallel with the Zener diode is used to discharge any residual stored gate or Zener diode charge before the beginning of the next TOFF time cycle.

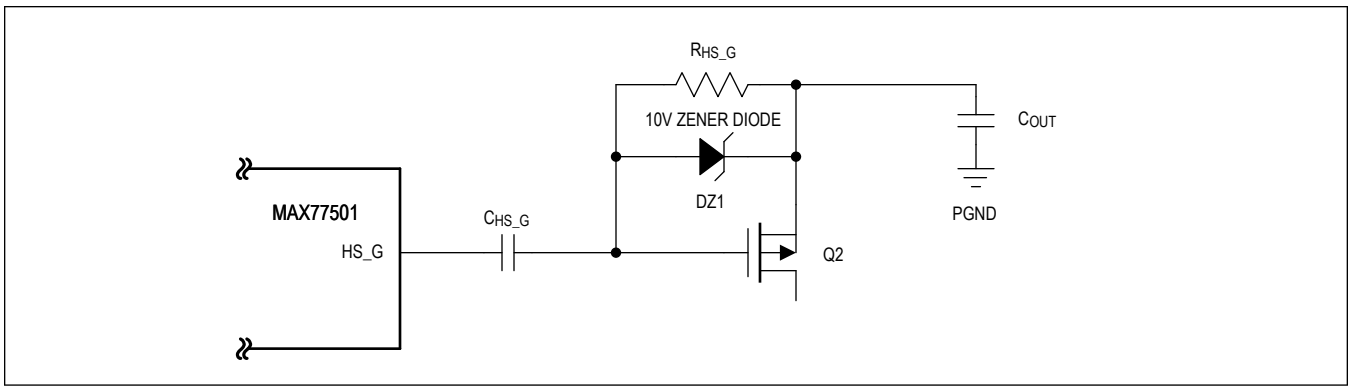


Figure 11. High-Side PFET Gate Drive

Slew Rate Control

Piezo actuators can exhibit an audible 'click' with fast output voltage slew rates. Fast output slew rates can occur prior to and at the end of a haptic waveform when the output voltage ramps up or down to the 10V minimum output voltage. The IC has a slew rate control option to reduce this audible 'click' prior to the first haptic waveform and at the end of all haptic waveforms. In order to provide slew rate control, the host processor must write to the SLEW_RATE control register in the STANDBY state prior to the first haptic playback. The slower the slew rate programmed, the lower the audible 'click'. Therefore, it is recommended that the user begins and ends every haptic waveform at a DAC code of all 0's to eliminate these delays. A DAC code of all 0's corresponds to the 10V minimum output voltage.

Input Battery Voltage Blocking FET

In normal operation during STANDBY or SHUTDOWN mode, the output voltage of the system sits at the battery voltage minus the body diode voltage of the high-side PFET (Q2). In some applications, it may be desirable to have the output voltage sit at 0V while the part is in STANDBY or SHUTDOWN mode. This can be achieved by adding an NFET (Q3) between the input voltage and the inductor, as shown in Figure 12. The gate of Q3 can be attached to V_{DD_H} so that Q3 only turns on after V_{DD_H} is enabled during a haptic request. When the part transitions to STANDBY or SHUTDOWN mode, the output voltage on the piezo is drained to 0V through the feedback resistors to ground. For this to work, the feedback resistors must be tied directly to ground, rather than to the FB_SW pin. Since FB_SW disconnects the feedback resistors from ground during the SHUTDOWN or STANDBY states, the output voltage has no way to discharge to 0V. A suitable FET for Q3 is the DMN1019UFDE from Diodes Incorporated.

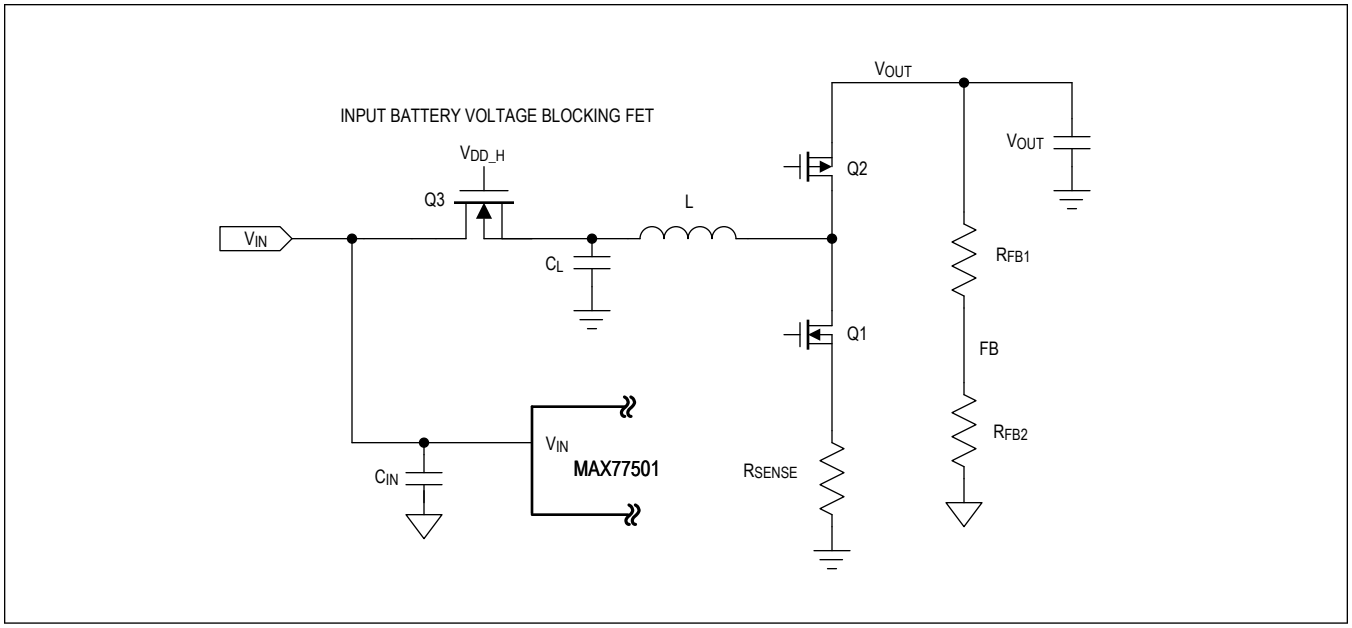


Figure 12. Input Battery Voltage Blocking FET Diagram

Feedback Switch Functionality

If it is desirable to remove the load on V_{OUT} during STANDBY or SHUTDOWN mode, an option exists in the part to connect the feedback resistors to the FB_SW pin, as shown in Figure 13. In STANDBY and SHUTDOWN mode, the output voltage of the part sits at V_{IN} minus the body diode voltage of the high-side PFET. Since the FB_SW pin disconnects the feedback resistors from ground during the SHUTDOWN or STANDBY states, the output voltage has no path to discharge to the battery voltage. If this is a concern, the output feedback resistors should be tied directly to ground and the FB_SW pin should be left open. This pin should not be used in conjunction with an *Input Battery Voltage Blocking FET*.

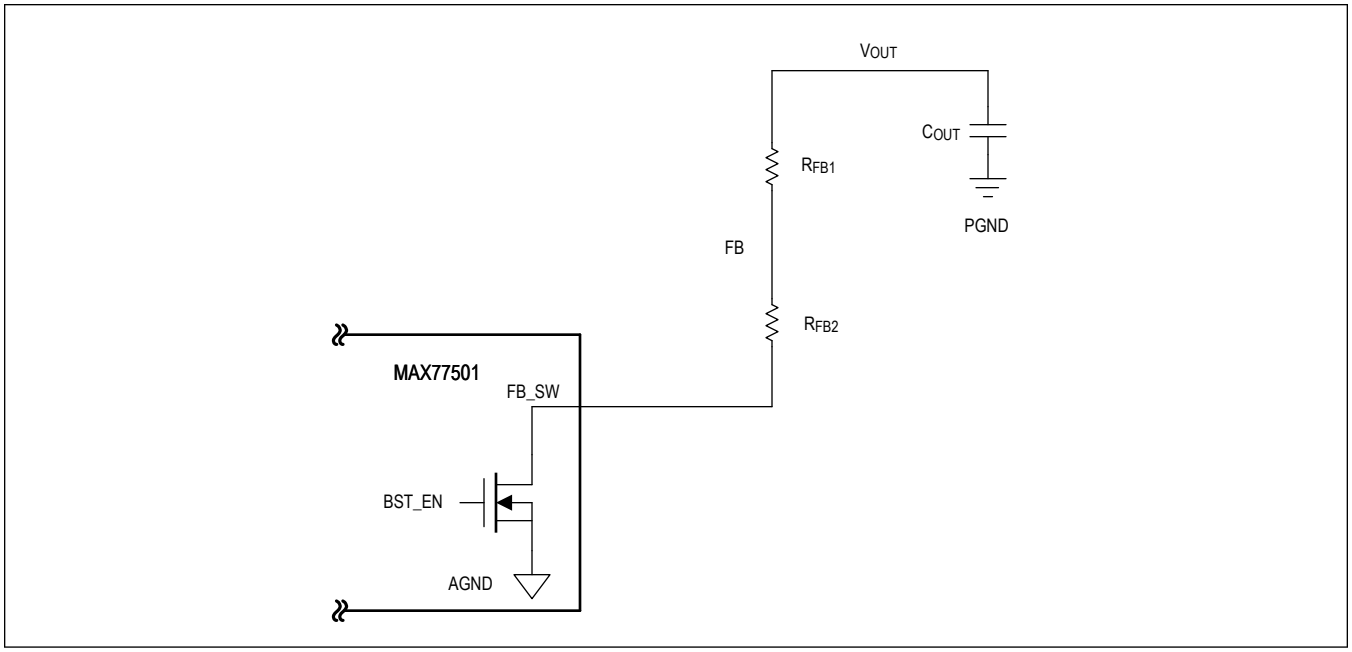


Figure 13. Feedback Switch Diagram

Full-Scale Settings

The device supports two full-scale settings, a 60Vpp setting and a 110Vpp setting. The 60Vpp setting is for haptic waveforms that range from 10V to 70V, and the 110Vpp setting is for haptic waveforms that range from 10V to 120V. To select the correct setting for your application, the processor must write to the FULL_SCALE register prior to any haptic request. In addition, to select the correct gain of the system for each setup, RFB1 should be set to 442kΩ for the 60Vpp setting and to 715kΩ for the 110Vpp setting. RFB2 should be set to 20kΩ in both cases.

PCB Layout Guidelines

Use the MAX77501 evaluation kit as a PCB layout reference. Good printed circuit board (PCB) layout is necessary to achieve optimal performance. The evaluation kit (EV kit) provides an example layout that optimizes its performance. PCB layouts must:

1. Refer to the EV kit data sheet for component locations as well as for layout routing and grounding recommendations.
2. Place the V_{IN} capacitor (C_{IN}) as close to the V_{IN} pin as possible.
3. Place the input capacitors (C_L) close to the inductor and the R_{SENSE} ground connection as possible.
4. Place the inductor (L) very close to the common drain of the power FET's (Q1, Q2) with wide metal.
5. Route the feedback connection from the feedback resistors (R_{FB1}, R_{FB2}) away from noise sources (i.e., clock and data lines) and keep the connection as short as possible to the FB pin.
6. Place the charge pump fly caps (C_{F1}, C_{F2}) as close to their respective pins as possible (CF1P and CF1N, CF2P and CF2N).
7. Place the decoupling capacitors for V_{CC}, V_{O_DAC}, V_{IO}, V_{DD}, V_5, V_{DD_H}, and V_{SS_H} (C_{VCC}, C_{VO_DAC}, C_{VIO}, C_{VDD}, C_{V5}, C_{VDD_H} and C_{VSS_H} respectively) as close to their respective pins as possible.
8. The compensation components (R_{COMP}, C_{COMP}) must be placed close to the COMP pin.
9. Keep the COMP pin and compensation components as isolated as possible.
10. Place C_{COT} and R_{COT} as close to the COT pin as possible.
11. Place C_{SLP} and R_{SLP} as close to the SLP pin as possible.
12. Place C_{FILT} as close to the CS_IN pin as possible.
13. Place R_{SENSE} very close to the source of the N-channel power FET with wide metal.
14. Keep the input power loop (V_{IN} through the inductor to the low side NFET) as short as possible with wide metal

traces.

15. Keep the output power loop (V_{IN} through the inductor, high-side PFET to V_{OUT}) as short as possible.
16. Keep the high dV/dt loop (LX through the high-side PFET, $C_{OUT1,2}$ to the source of the low-side NFET) as short as possible.
17. Return the ground side of the V_{OUT} decoupling capacitors ($C_{OUT1,2}$) close to the R_{SENSE} ground connection.
18. **Note:** the R_{SENSE} ground return is the center point of the V_{IN} power loop (V_{IN}, C_{IN}, inductor, N-channel power FET) and the V_{OUT} power loop (V_{IN}, inductor, P-channel power FET and V_{OUT} decoupling capacitors). Both loops should be short and use wide metal traces to reduce parasitic resistance and inductance.

See Figure 14 for an example of a PCB layout for the inductor power path.

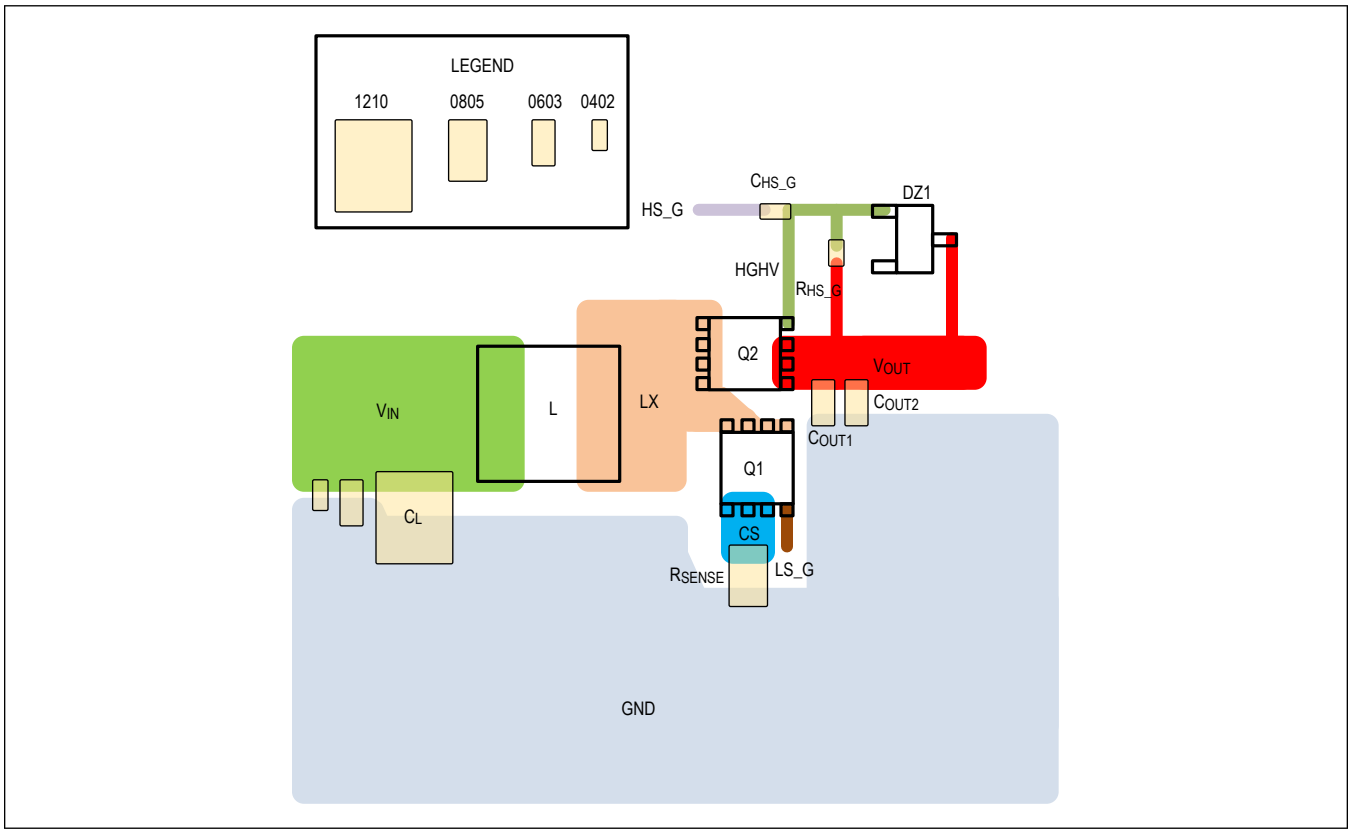


Figure 14. Inductor Power Path Layout Example

See Figure 15 for an example of a PCB layout for the IC and its external components.

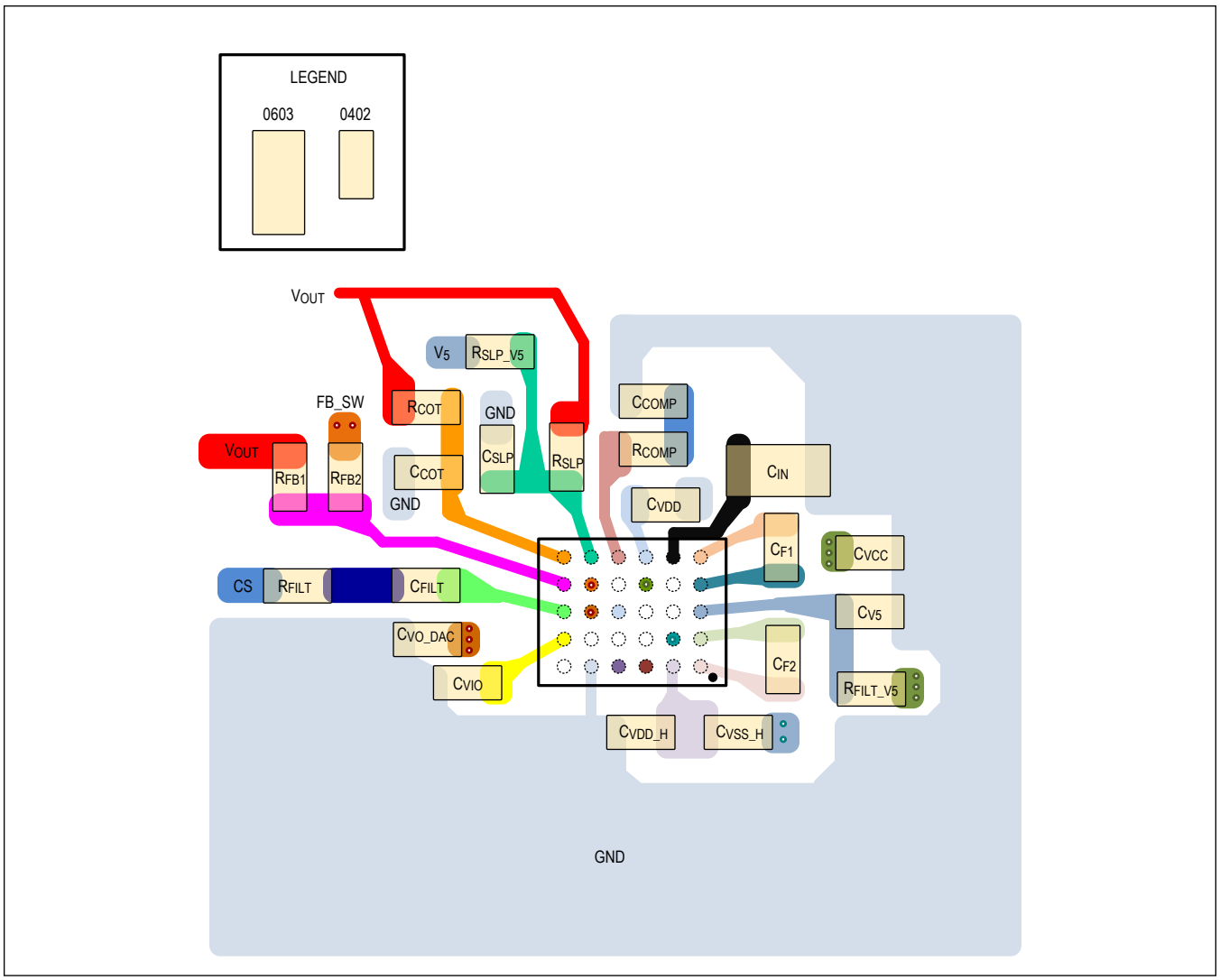
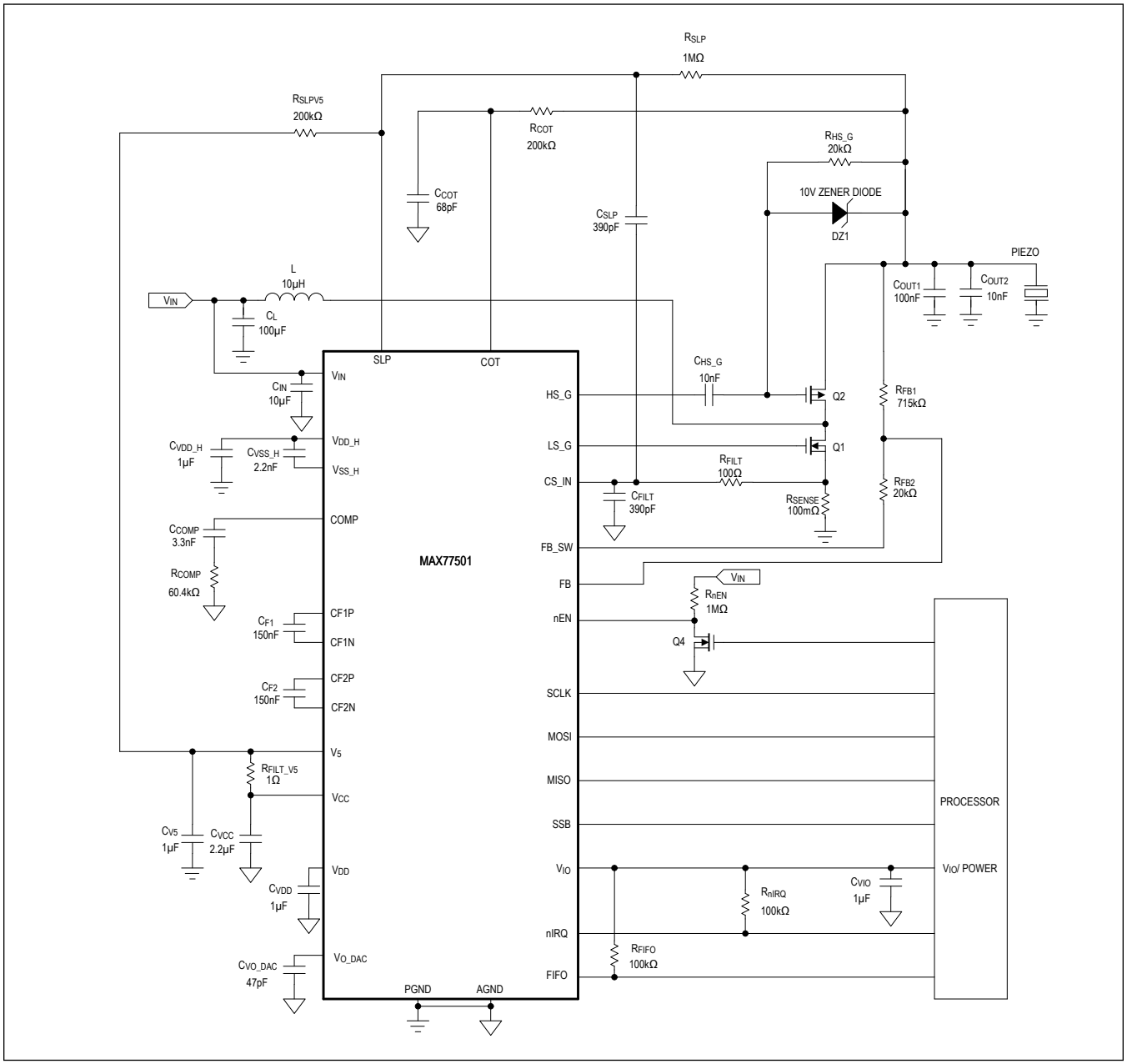


Figure 15. IC Controller Layout

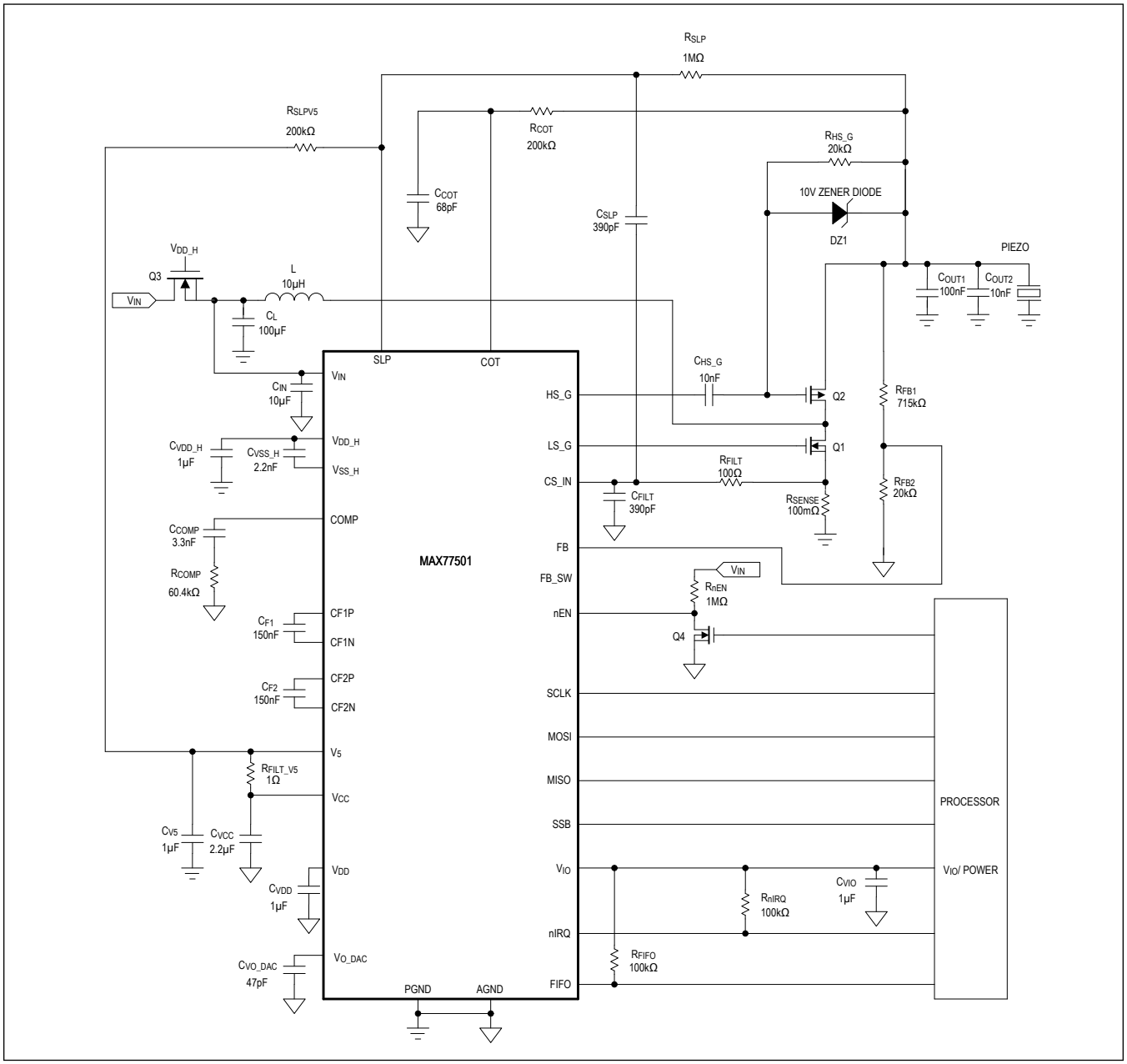
Typical Application Circuits

Current Mode Configuration with Feedback Switch Functionality



Typical Application Circuits (continued)

Current Mode Configuration with Input Battery Voltage Blocking FET



Ordering Information

PART NUMBER	TEMP RANGE	PIN-PACKAGE
MAX77501EWV+T	-40°C to +125°C	30 WLP

+Denotes a lead(Pb)-free/RoHS-compliant package.

T = Tape and reel.

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	6/19	Initial release	—
1	8/19	Updated the *Benefits and Features* section, *Typical Operating Characteristics*, and the *Bump Configurations* diagram	1, 14, 16