

User's Guide

LMR54410EVM User's Guide



ABSTRACT

The Texas Instruments LMR54410EVM evaluation module (EVM) helps designers evaluate the operation and performance of the LMR54410 wide-input synchronous buck regulator. This document describes the following:

- Setup
- Input/output connections of the EVM
- Board layout
- Schematic
- Bill of materials

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1 Introduction

The Texas Instruments LMR54410EVM evaluation module (EVM) helps designers evaluate the operation and performance of the LMR54410 wide-input buck regulator.

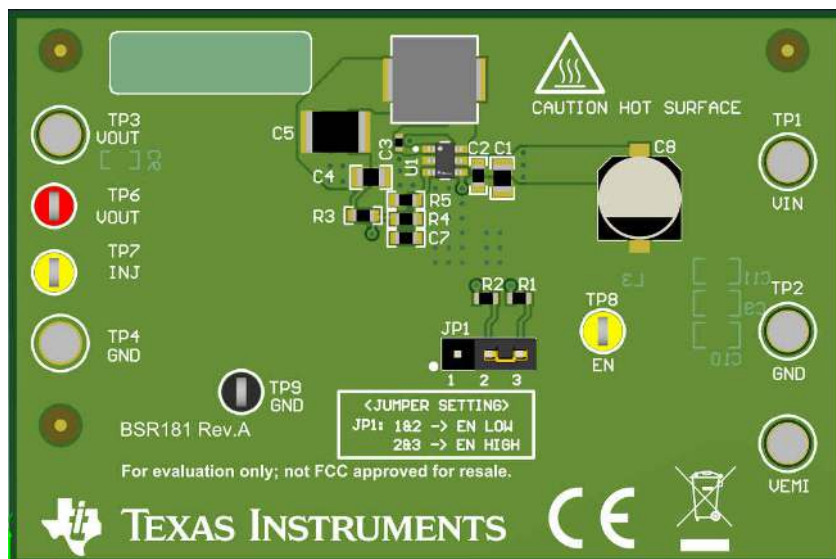


Figure 1-1. LMR54410EVM Board

EVM Features

- 4-V to 36-V input voltage range
- Default 3.3-V output
- Up to 1-A output current
- 1100-kHz switching frequency
- Hiccup mode short current protection
- Internal compensation

The EVM contains one DC/DC converter (see [Table 1-1](#)).

Table 1-1. Device and Package Configurations

CONVERTER	EVM	DEVICE	PACKAGE
U1	LMR54410EVM	LMR54410	SOT23-6

2 Setup

This section describes the jumpers and connectors on the EVM and how to properly connect, set up, and use the LMR54410EVM.

2.1 Input/Output Connector Description

VIN — Terminal TP1 – Power input terminal for the converter. Adjacent to it is the GND reference ground. Use this terminal to attach the EVM to a cable harness.

VOUT — Terminal TP3 – Regulated output voltage for the converter. Adjacent to it is the GND reference ground.

GND — Terminal TP2, TP4 – Ground reference for the converter. Use these terminals to attach the EVM to a cable harness.

ENABLE SETTING — Jumper JP1 – Used to enable the switch-mode converter. The device will be enabled when the EN pin is high, and disabled when low.

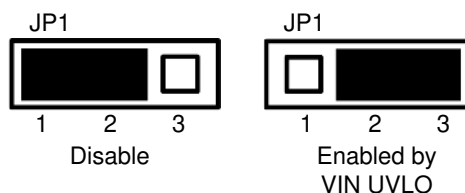


Figure 2-1. Enable Jumper Setting

Testpoint — TP7, TP6, TP9 – Test points used for loop response measurements

2.2 Adjusting the Output Voltage

If other outputs need to be configured, leave jumper J1 unconnected and adjust the feedback resistors using the [Equation 1](#).

$$V_{OUT} = V_{REF} \times (1 + (R4 / R5)) \quad (1)$$

where

- V_{REF} is 0.8 V.

3 LMR54410EVM Schematic

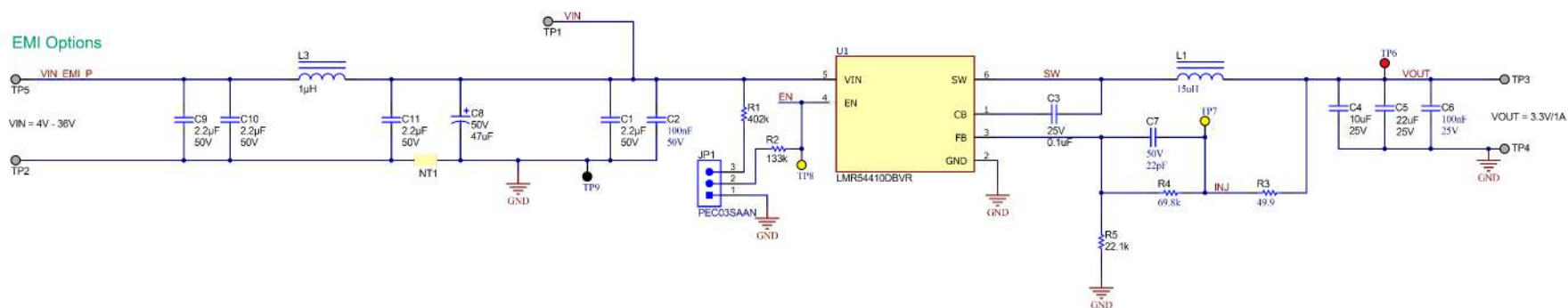


Figure 3-1. LMR54410EVM Schematic

4 Board Layout

Figure 4-1 and Figure 4-4 show the board layout for the LMR54410EVM. The PCB consists of a 4-layer design. The board size is 46-mm × 69-mm, 2-oz copper planes are applied on top and bottom layers, 1-oz copper planes are applied on middle layers.

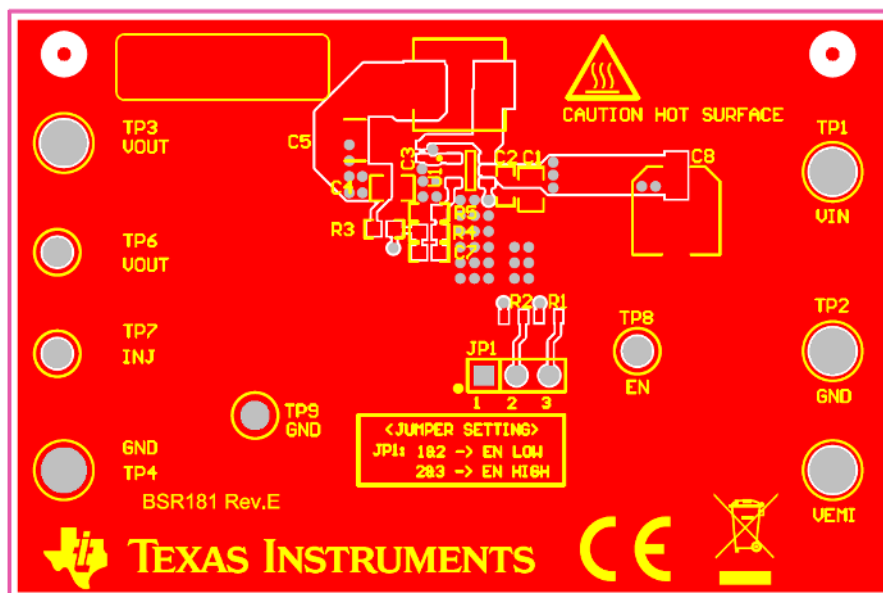


Figure 4-1. Top Layer

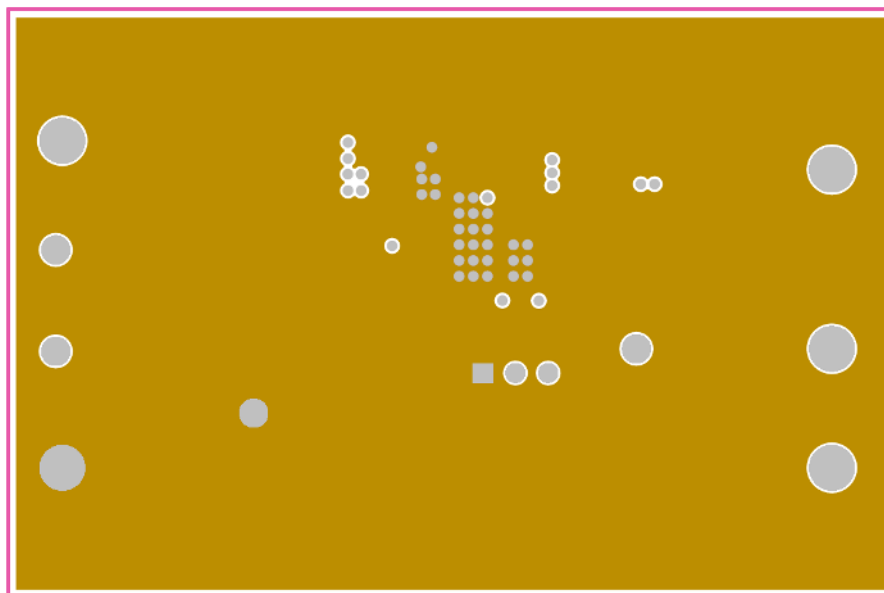


Figure 4-2. Middle Layer One

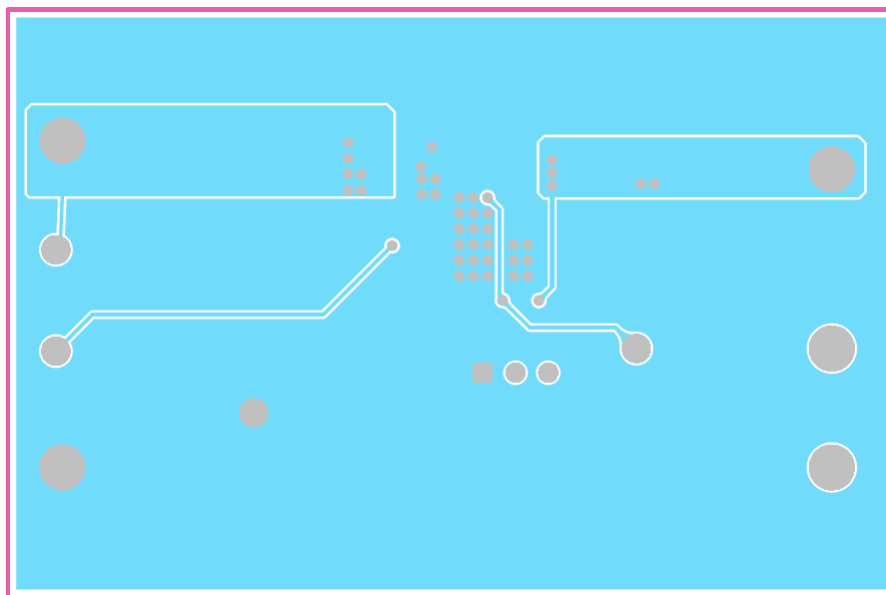


Figure 4-3. Middle Layer Two

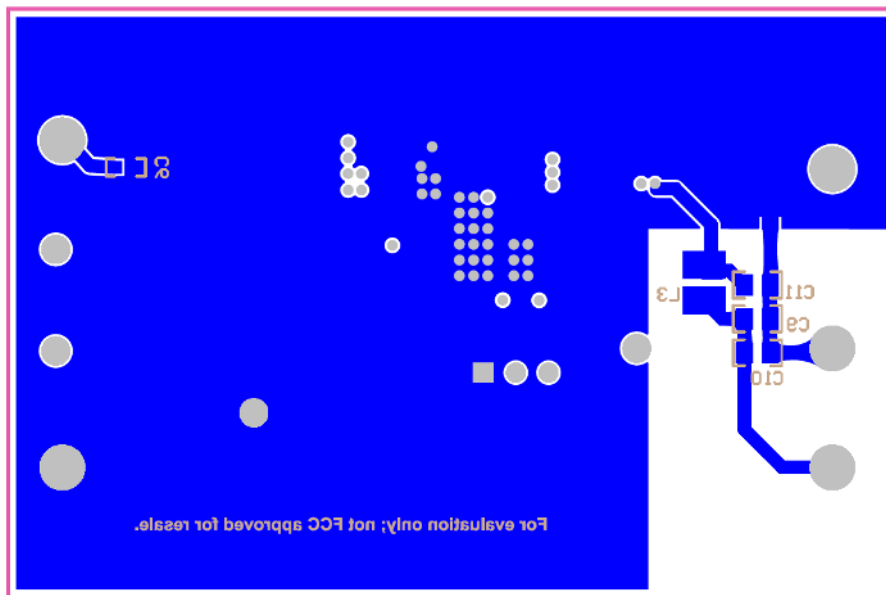


Figure 4-4. Bottom Layer

5 Bill of Materials

Table 5-1. LMR54410EVM Bill of Materials

DESIGNATOR	QUANTITY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
C1	1	2.2 μ F	CAP, CERM, 2.2 μ F, 50 V, $\pm 10\%$, X7R, AEC-Q200 Grade 1, 0805	0805		
C2	1	0.1 μ F	CAP, CERM, 0.1 μ F, 50 V, $\pm 10\%$, X7R, 0603	0603		
C3	1	0.1 μ F	CAP, CERM, 0.1 μ F, 25 V, $\pm 10\%$, X7R, 0402	0402		
C4	1	10 μ F	CAP, CERM, 10 μ F, 25 V, $\pm 10\%$, X7R, 0805	0805		
C6	1	0.1 μ F	CAP, CERM, 0.1 μ F, 25 V, $\pm 10\%$, X7R, 0603	0603		
JP1	1		Header, 100 mil, 3 $\times$ 1, Tin, TH	Header, 3 PIN, 100 mil, Tin		
L1	1	15 μ H	Inductor, Shielded Drum Core, Powdered Iron, 15 μ H, 2.75 A, 0.092 Ω , SMD	7.30 $\times$ 4.80 $\times$ 6.60 mm	74437349150	Würth Electronics
R1	1	402 k	RES, 402 k, 1%, 0.1 W, 0603	0603		
R2	1	133 k	RES, 133 k, 1%, 0.1 W, 0603	0603		
R3	1	49.9	RES, 49.9, 1%, 0.1 W, 0603	0603		
R4	1	69.8k	RES, 69.8 k, 1%, 0.1 W, 0603	0603		
R5	1	22.1 k	RES, 22.1 k, 1%, 0.1 W, 0603	0603		
SH-J1	1	1x2	Shunt, 100 mil, Gold plated, Black	Shunt		
TP1, TP2, TP3, TP4	4		Terminal, Turret, TH, Double	Keystone1502-2		
TP6	1		Test Point, Multipurpose, Red, TH	Red Multipurpose Testpoint		
TP7, TP8	2		Test Point, Multipurpose, Yellow, TH	Yellow Multipurpose Testpoint		
TP9	1		Test Point, Multipurpose, Black, TH	Black Multipurpose Testpoint		
U1	1		LMR54410YQDBVRQ1, DBV0006A (SOT-23-6)	DBV0006A	LMR54410YQDBVRQ1	Texas Instruments
C5	0	22 μ F	CAP, CERM, 22 μ F, 25 V, $\pm 20\%$, X7R, AEC-Q200 Grade 1,		CGA8P1X7R1E226M25 0KC	TDK
C7	0	22 pF	CAP, CERM, 22 pF, 50 V, $\pm 5\%$, C0G/NP0, 0603	0603		
C8	0	47 μ F	CAP, AL, 47 μ F, 50 V, $\pm 20\%$, 0.6 Ω , SMD	F80		
C9, C10, C11	0	2.2 μ F	CAP, CERM, 2.2 μ F, 50 V, $\pm 10\%$, X7R, AEC-Q200 Grade 1, 0805	0805		
L3	0	1 μ H	Inductor, Shielded, Metal Composite, 1 μ H, 2.9 A, 0.048 Ω , SMD	2 $\times$ 1.6 mm	DfE201612E-1R0M	MuRata
TP5	0		Terminal, Turret, TH, Double	Keystone1502-2		

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