SC2434
TriPhase Current Mode Controller with Power Good

Description

The SC2434, a tri-phase, current mode controller is designed to work with Semtech smart synchronous drivers, such as the SC1205, SC1206, and SC1207 to provide the DC/DC converter solution for the most demanding Microprocessor applications. Input current sensing is used to guarantee precision phase to phase current matching using a single sense resistor on the input power line. This topology reduces the power loss and complexity associated with output current sense methods. Multi phase operation allows significant reduction in input/output ripple while enhancing transient response. Two or three phase operation is selectable. The DAC step size and range are programmable with external components thus allowing compliance with new and emerging VID ranges. A novel approach implements active droop to minimize output capacitors during load transients.

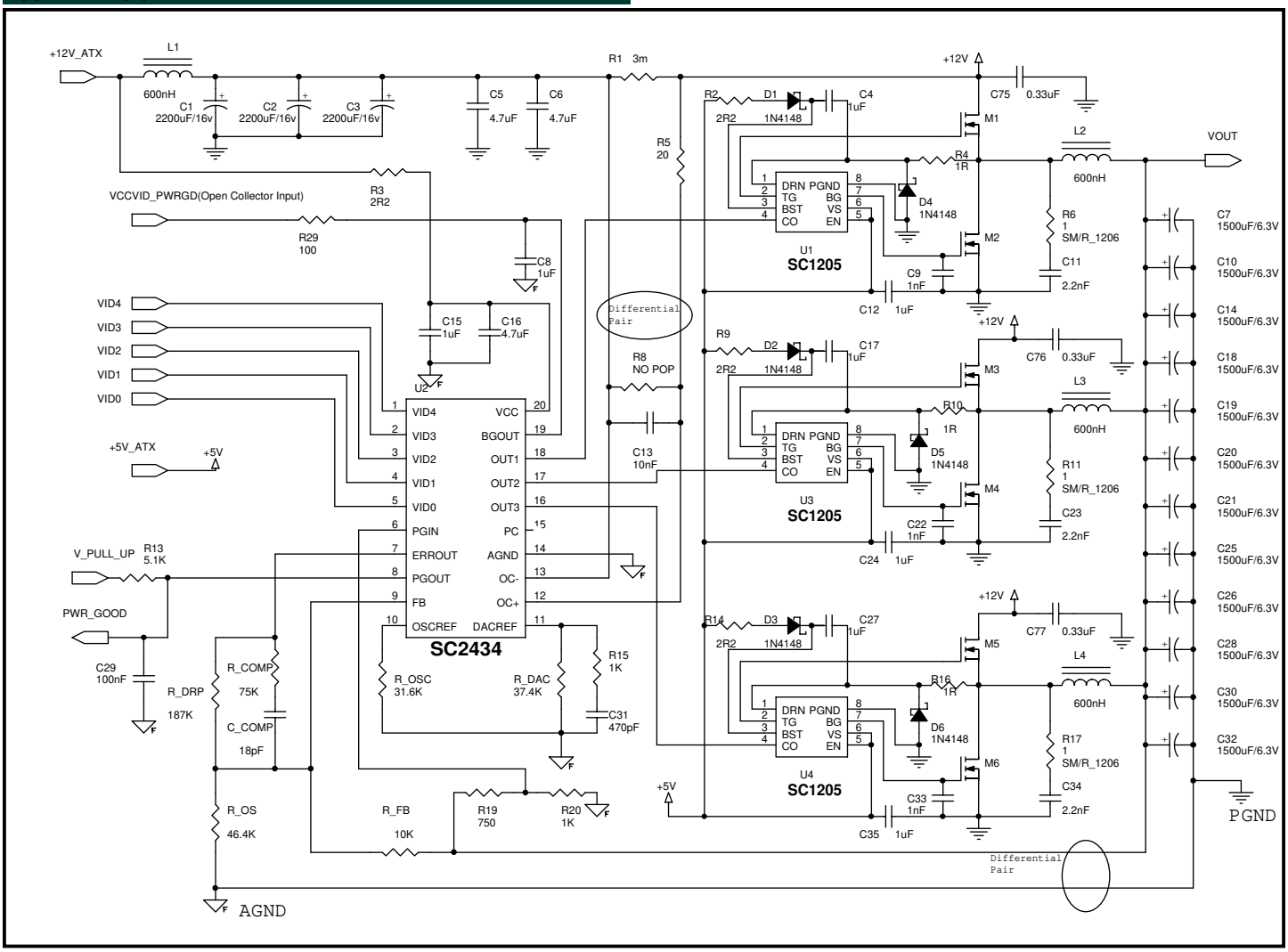
Features

- 12V input
- Input sensing current mode control
- Selectable 2 or 3 phase operation
- Precision, pulse by pulse phase current matching
- Active drooping allows for best transient response
- Programmable internal oscillator to 1.5 MHz
- Programmable DAC step size/offset allows compliance with VRM9.0 and VRM9.2
- VID 11111 Inhibit (No CPU)
- Externally programmable soft-start
- 0% minimum duty cycle improves transient response
- Cycle by cycle current limiting plus hiccup
- Power good signal

Applications

- Intel Pentium-4 microprocessors
- High performance desktop systems

Typical Application Circuit



Absolute Maximum Ratings

Exceeding the specifications below may result in permanent damage to the device, or device malfunction. Operation outside of the parameters specified in the Electrical Characteristics section is not implied.

Parameter	Symbol	Maximum	Units
Input DC Rail Voltage to GND	V_{IN}	18	V
Ambient Temperature Range	T_A	0 to 70	°C
Junction Temperature	T_J	0 to 125	°C
Thermal Resistance Junction to Case	θ_{JC}	20	°C/W
Thermal Resistance Junction to Ambient	θ_{JA}	60	°C/W
Storage Temperature Range	T_{STG}	-65 to +150	°C
Lead Temperature (Soldering) 10 Sec.	T_{LEAD}	300	°C

Electrical Characteristics

Unless specified: V_{CC} = +12V, T_{AMB} = 25°C, R_{DAC} = 37.4kΩ, R_{OSC} = 28.5kΩ. See Typical Application Circuit

Parameter	Conditions	Min	Typ	Max	Unit
Chip_Supply					
IC Supply Voltage		10	12	14	V
IC Supply Current	V_{CC} = 12.0V		10	15	mA
Reference Section					
Bandgap Output	C_{BG} = 4.7nF		1.5		V
Source Impedance			6		kΩ
Supply Rejection	V_{CC} = 10.0V ~ 14.0V		.5		mV/V
VID Step	R_{FB} = 10kΩ, R_{DAC} = 37.4kΩ		25		mV
Temperature Stability	0°C < T_{AMB} < 70°C		0.5		%
Voltage Accuracy	0°C < T_{AMB} < 70°C	-0.8		+0.8	%
Oscillator Section					
Frequency Range		300		1500	kHz
Frequency Accuracy	V_{IN} = 12.0V	675	750	825	kHz
Temperature Stability	0°C < T_{AMB} < 70°C		±5		%
Voltage Error Amplifier					
Input Offset Voltage			±5		mV
Input Offset Current			0.1		µA
Open Loop Gain	1V < V_{ERROUT} < 4V		90		dB
PSRR	V_{CC} = 9 - 14V		80		dB
Output Sink Current	V_{ERROUT} = 1V		2.5		mA
Output Source Current	V_{ERROUT} = 4V		2		mA
Unity Gain Bandwidth	I_O < 100µA		1.6		MHz
Slew Rate	I_O < 100µA		10		V/µS

Electrical Characteristics (Cont.)

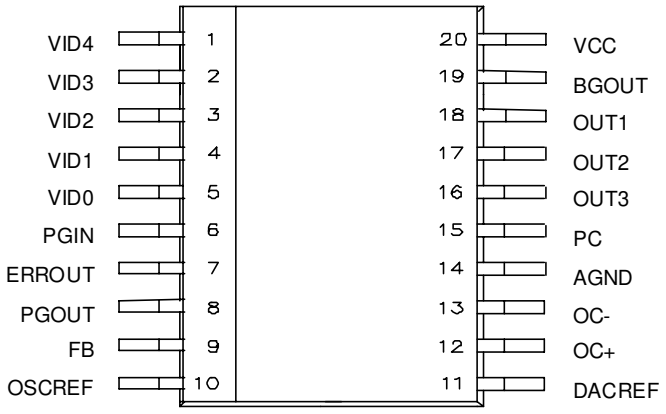
Unless specified: V_{CC} = +12V, T_{AMB} = 25°C, R_{DAC} = 37.4kΩ, R_{OSC} = 28.5kΩ. See Typical Application Circuit

Parameter	Test Conditions	Min	Typ	Max	Unit
Current Sense Amplifier					
Amplifier Gain	(V_{OC-} - V_{OC+}) < 120mV	18.9	19.3	19.7	V/V
Input Offset Voltage, Input Referred	(V_{OC-} - V_{OC+}) < 120mV		4		mV
CMRR	V_{ICM} = 9 ~ 14V @ DC		80		dB
PSRR	V_{CC} = 9 ~ 14V @ DC		80		dB
Input Common Mode Range			V_{CC} ±0.3		V
Max Differential Signal/Current Limit Threshold	V_{OC-} - V_{OC+}		120		mV
I-Limit Delay	Current limit activation to OUT1, OUT2 & OUT3 switching off		60		ns
Vcc UVLO					
Ramp-up Threshold			7.5		V
Ramp-down Threshold			7.25		V
Outputs (OUT1, OUT2, OUT3)					
Max Duty Cycle Per Phase	F_{OSC} = 500kHz, PC pin floating		31		%
	F_{OSC} = 500kHz, PC pin grounded		47		%
Output Voltage	R_L = 10kΩ , high		2.5		V
	R_L = 10kΩ , low		0.8		
	R_L = 100kΩ , high		3.3		V
	R_L = 100kΩ , low		0.2		
Logic Input					
VID Logic Threshold (1) (2)		0.8		2	V
VID Logic Impedance	Internal pull-up = 2.5V		25		kΩ
Phase Control					
Logic Threshold (2)		0.8		2	V
Internal Pull-up	PC pin open circuit		2.5		V
Internal Pull-up Impedance			25		kΩ
Power Good Signal					
Off Leakage Current	PWRGOOD = Logic high			2	µA
Power Good Max Sink Current	PWRGOOD < 0.8V	4			mA
Power Good Threshold			0.8		V

Notes:
1. If VIDs are left open, no external pull-up is required. When external pull-up is needed, use 3.3V.
2. Max logic input is recommended to be less than 5.5V.

Pin Configuration

Top View



(20-Pin SOIC or TSSOP)

Ordering Information

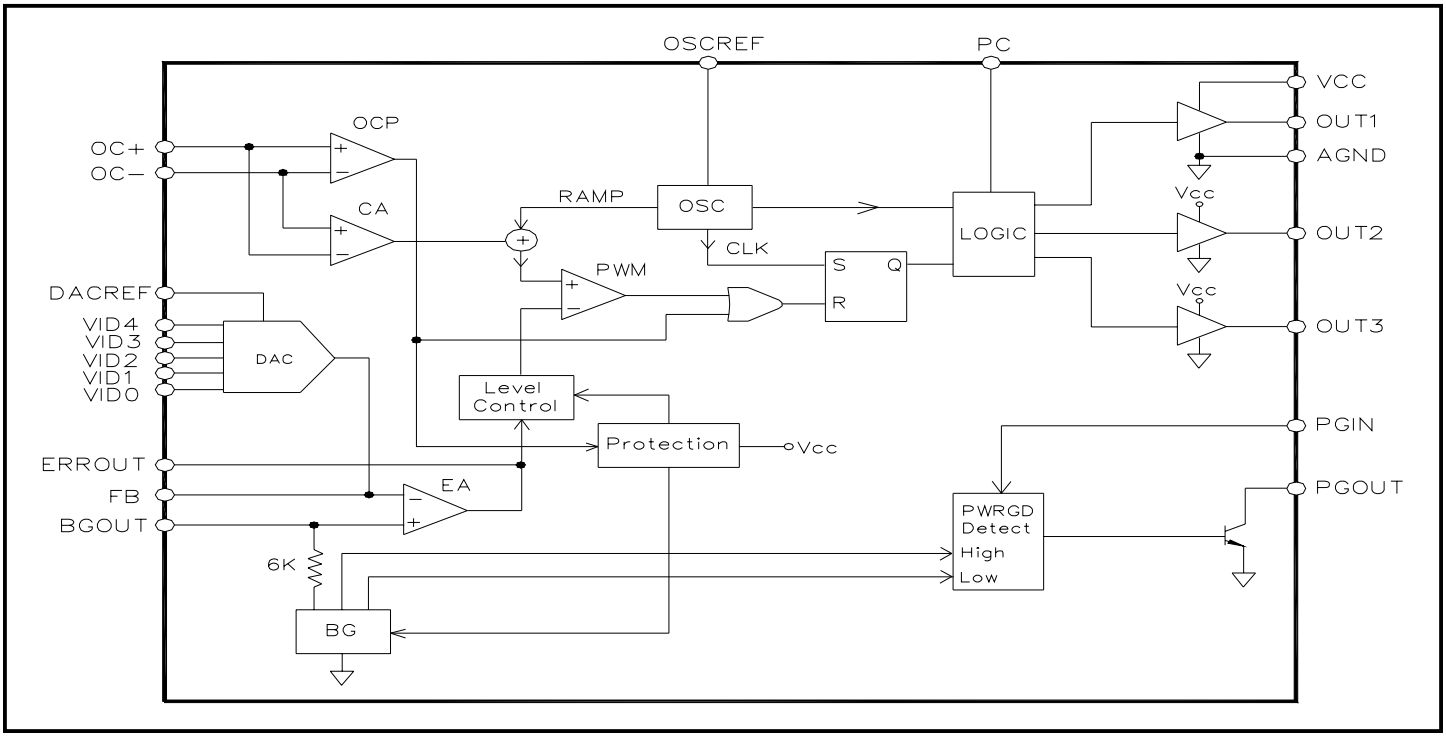
Device	Package	Temp. Range (T_A)
SC2434SWTR (1)	SOIC-20	0 - 70°C
SC2434TSTR (1)	TSSOP-20	0 - 70°C
SC2434SWTRT (1,2)	SOIC-20	0 - 70°C
SC2434TSTRT (1,2)	TSSOP-20	0 - 70°C
SC2434EVB (3)	Evaluation Board	

Note:
(1) Only available in tape and reel packaging. A reel contains 1000 devices for the SOIC-20 and 2500 devices for the TSSOP-20 package.
(2) Lead free package. Devices are fully WEEE and RoHS compliant.
(3) Specify SOIC-20 or TSSOP-20 package.

Pin Descriptions

Pin#	Pin Name	Pin Function
1	VID4	MSB
2	VID3	
3	VID2	
4	VID1	
5	VID0	LSB
6	PGIN	Power good input. Connect this pin to regulator output through a resistor divider.
7	ERROUT	Error-amplifier output.
8	PGOUT	Power good output signal (open collector).
9	FB	Error-amplifier inverting input.
10	OSCREF	Oscillator frequency setting.
11	DACREF	DAC current setting.
12	OC+	Supply input current sense, positive input.
13	OC-	Supply input current sense, negative input.
14	AGND	Analog ground pin.
15	PC	Phase control. Leave it floating or high for 3 phase operaton. Ground it for 2 phase operation.
16	OUT3	PWM output for phase 3. When PC pin is grounded OUT3 is disabled.
17	OUT2	PWM output for phase 2.
18	OUT1	PWM output for phase 1.
19	BGOUT	Bandgap reference.
20	VCC	Chip positive supply.

Block Diagram



Applications Information- Output Voltage

Output Voltage

Unless specified: 0 = GND; 1 = High (or Floating). T_A = 25°C, V_{CC} = 12V, 3-Phase operation .

VID4	VID3	VID2	VID1	VID0	V_{CCCORE} (VDC)
1	1	1	1	1	Output Off
1	1	1	1	0	1.1
1	1	1	0	1	1.125
1	1	1	0	0	1.15
1	1	0	1	1	1.175
1	1	0	1	0	1.2
1	1	0	0	1	1.225
1	1	0	0	0	1.25
1	0	1	1	1	1.275
1	0	1	1	0	1.3
1	0	1	0	1	1.325
1	0	1	0	0	1.35
1	0	0	1	1	1.375
1	0	0	1	0	1.4
1	0	0	0	1	1.425
1	0	0	0	0	1.45
0	1	1	1	1	1.475
0	1	1	1	0	1.5
0	1	1	0	1	1.525
0	1	1	0	0	1.55
0	1	0	1	1	1.575
0	1	0	1	0	1.6
0	1	0	0	1	1.625
0	1	0	0	0	1.65
0	0	1	1	1	1.675
0	0	1	1	0	1.7
0	0	1	0	1	1.725
0	0	1	0	0	1.75
0	0	0	1	1	1.775
0	0	0	1	0	1.8
0	0	0	0	1	1.825
0	0	0	0	0	1.85

Applications Information

Theory of Operation

The simplified voltage regulator (VR) based on SC2434 is depicted in Fig. 1. The key timing chart is also shown in the same picture. The 12V input power passes through the input filter establishing the input power rail. The current sensing resistor located at positive input rail monitors the top FET currents of all the phases. An internal differential amplifier amplifies the voltage across the current sensing resistor. The output of the current amplifier and an internally generated saw tooth ramp signal are added together to be the PWM carrier signal. This signal meets the output of the error amplifier at the pulse width modulator (PWM). The output of the PWM is then divided into three phases alternately to be the inputs of the synchronous drivers.

Feedback and Regulation

The feedback circuitry reads the regulator output voltage and compares it with an accurately trimmed bandgap voltage reference, which is 1.5V with less then 0.8% tolerance. The compensation network allows optimization of the control-loop for system stability and fast transient responses.

Flexible VID

The VID circuitry reads the 5 bit digital command and converts it into a current flowing into the inverting input pin of the error amplifier. The output current of the DAC produces a voltage offset on the feedback resistor, R_{FB} (see Fig. 1), which changes the set point of the converter output voltage for different VID combinations.

Active Voltage Positioning

By programming the gain of the error amplifier, one can easily and accurately implement adaptive output voltage positioning. This is equivalent to programming the VR output impedance in an active manner. The advantage of allowing the VR certain output impedance (typically 1~3 mOhm) is that one can use a minimum amount of high quality output bulk capacitors to meet the voltage regulation requirement. Hence, the cost and the size of the VR solution can be significantly reduced.

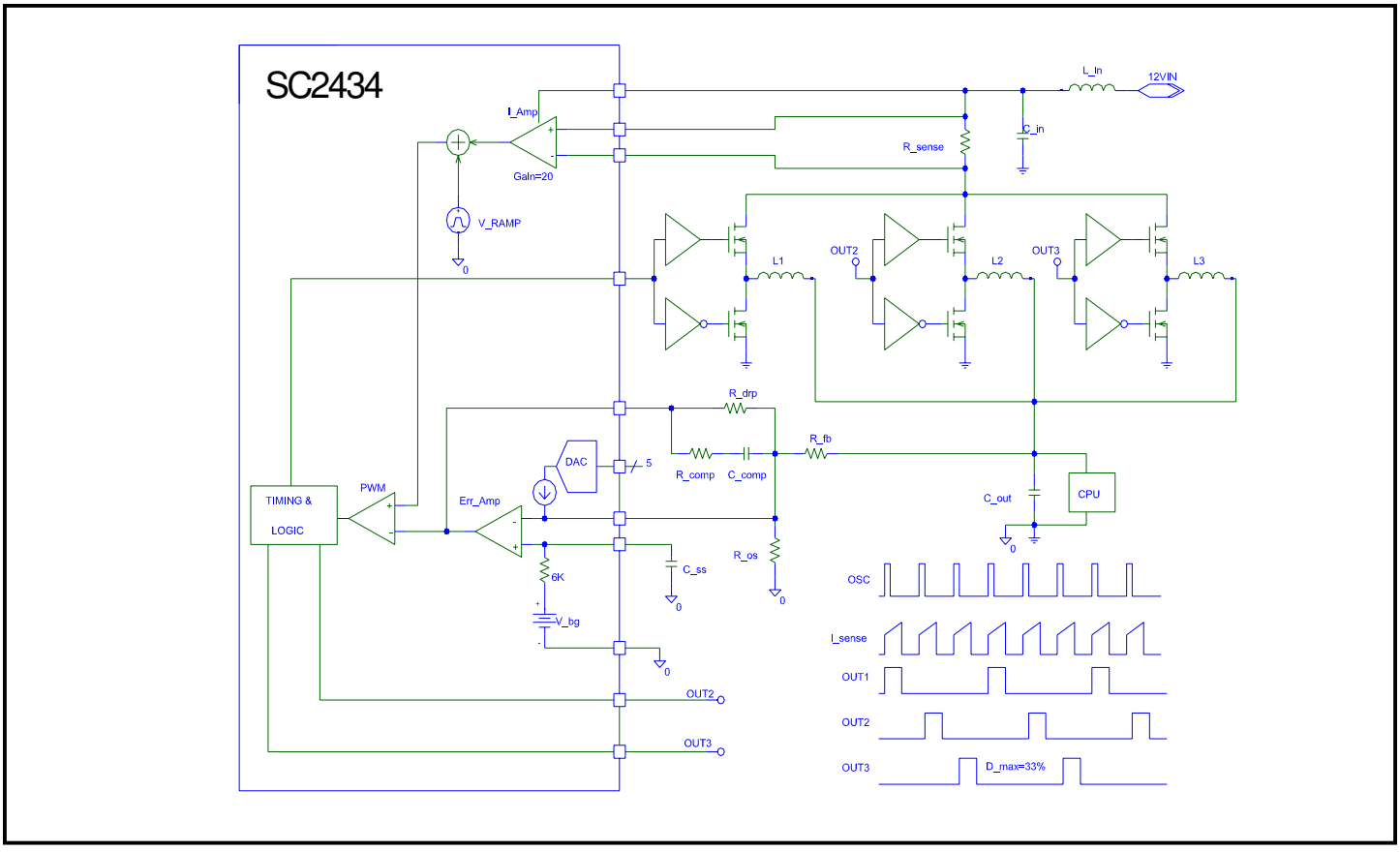


Fig.1 - The simplified voltage regulator based on SC2434.

Applications Information (Cont.)

Phase Current Balance

One of the fundamental challenges for multi-phase solutions is to balance the phase currents to achieve the best possible electrical and thermal performance. It is quite easy to use the SC2434 control topology to achieve very good phase current balance. Since the current of all the phases passes through the same current sensing component and the same current current of all the phases are well balanced on pulse by pulse basis. This control results in small and even output voltage ripple and evenly distributed thermal load. Additional advantages of using input current mode are less sensing circuitry, less IC pins, and less power loss on the sensing resistor comparing sensing inductor current on the output side. Fig. 2 shows the waveform of inductor currents under heavy load conditions, which clearly demonstrates the excellent performance of SC2434 on balancing the phase current.

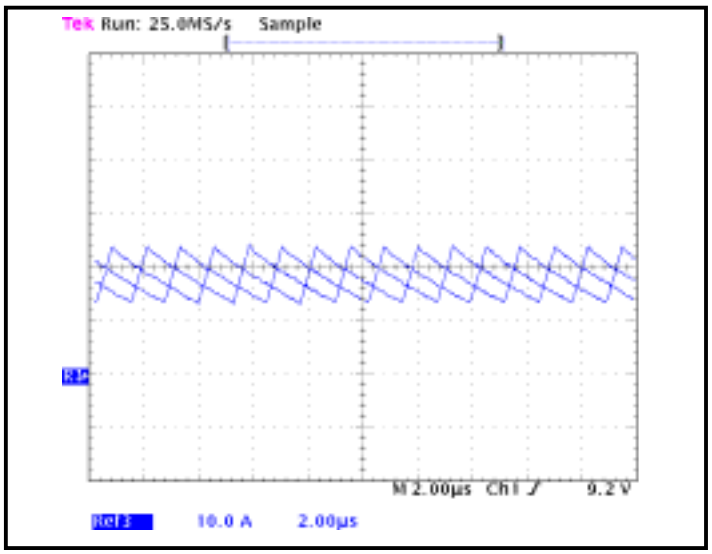


Fig. 2 - Measured inductor currents of SC2434 3-phase VR under heavy load condition.

Under Voltage Lockout (UVLO)

During power up, when UVLO circuitry detects the chip supply (Vcc) be bigger than 7.5V (typical value with proper hysteresis), the bandgap voltage reference starts to charge the external soft start capacitor through a 6 Kohm internal resistor. When soft start capacitor voltage reaches 0.5V, the output voltage starts to build up which follows the exponential voltage profile of the soft start capacitor. The soft start process ensures that the output voltage will have no over shoot. During power down, UVLO will discharge the soft start capacitor to shut of the PWM. The load will absorb the energy in the output filter and no resonance will occur. Hence, the CPU will not see any negative voltage. Fig. 3 shows the measured waveforms of power up and power down.

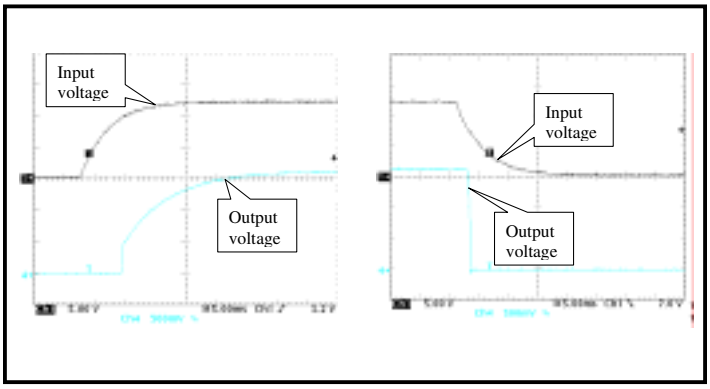


Fig. 3 - Shows the measured waveforms of power up and power down.

Over Current Protection (OCP)

When sensed current signal across the differential input of the current amplifier exceeds 120mV typical value, OCP circuitry will pull down the error amplifier output voltage and also discharge the soft start capacitor. The pull down of the error amplifier will not be released until the soft capacitor is discharged bellow 0.3V. At this point, the PWM outputs are reactivated and the soft start capacitor begins to charge up again through the internal 6 Kohm resistor. The VR will try to bring up the output voltage until the over load or short circuit condition is removed. The hiccup mode OCP can significantly reduce the average output current under overload conditions. The hiccup timing is controlled by the soft start time constant. Please also notice that the OCP threshold has less than 10% tolerance, hence, the onset of the OCP is quite accurate. The advantage is that the VR designer does not need to reserve big thermal headroom to deal with the worst-case operation when load is over 100% but the OCP has yet not been triggered. An RC filter is needed to filter out the leading edge voltage spike across the current sensing resistor to prevent false triggering of the OCP. The time constant should be around 200nS (please see application schematic).

Power Good

SC2434 features a power good input and an open collector power good output. The VR output voltage is scaled down through a resistive divider and this signal is fed into PGIN (power good input) pin. The scaled VR output voltage has to be bigger than 0.8V otherwise the power good output pin is pulled down. A 5 Kohm pull-up resistor and a 0.1uF capacitor to ground are recommended to prevent false trigger during logic transition.

Applications Information (Cont.)

Program The Controller

Please refer to Fig. 1 and the application schematics in this data sheet for the discussion. The resistor from pin 10 to ground, R_{OSC}, programs the switching frequency. The resistor from pin 11 to ground, R_{DAC}, sets the DAC current step size. The resistors, R_{FB}, R_{OS}, and R_{DRP} set the DAC step size, the output voltage set point, and the droop, respectively.

MathCAD programs are available to calculate the required parameters upon request.

Programming The Switching Frequency

The oscillator frequency can be selected first by setting the value of R_{OSC} as given below:

$$R_{OSC} := 28.5 \cdot K\Omega \cdot \frac{750 \cdot KHz}{F_{osc}}$$

The per phase switching frequency is 1/3 of the oscillator frequency in three-phase mode. It is recommended that per phase switching frequency is 200~300KHz for good trade off of efficiency vs. transient responses.

Programming The DAC Step Size

The SC2434 allows programming of the output voltage and the DAC step size by selecting external resistors. The LSB of the DAC current is given by:

$$I_{DAC\_LSB} := \frac{1}{16} \cdot \frac{V_{bg}}{R_{DAC}}$$

where V_{bg} is the trimmed voltage reference (V_{bg} = 1.5V) and R_{DAC} is the resistor from pin 11 to ground. For the given VID step size (25mV for VRM9.0 and VRM9.2 specifications), the feedback resistor can be calculated according to the LSB of DAC current:

$$R_{FB} := \frac{VID_{step}}{I_{DAC\_LSB}}$$

The above two equations are for choosing R_{DAC} and R_{FB} simultaneously. The advantage of this method is that new VID step size can be accommodated by modifying external components while maintaining the required precision.

Choose Current Sensing Resistor According To The Threshold Of OCP

The SC2434 controller has an over current protection (OCP) threshold of 120mV. The normal practice is to let the peak voltage across the sensing resistor corresponding to full-load operation be 75% of the given OCP threshold:

$$R_{sense} := \frac{75\% \cdot 120mV}{I_{peak}}$$

where I_{peak} is the peak current of the output inductor. Since the choice of sensing resistor values are limited, typically 3 mOhm, 4 mOhm, or 5 mOhm, it is recommended to choose the sensing resistor with a bigger value than that was calculated, and to use a resistive divider to get the equivalent R_{sense} value. The two attenuation resistors should have value of 20 Ohm in parallel. A filter capacitor of 10nF is also needed to be across the OC+ and OC- pins of the controller IC. Please refer the application circuit schematic.

Programming The Dynamic (Active) Droop

To optimize transient responses, the SC2434 actively regulates output voltage as a function of output current. At zero current the output is positioned to the upper limit of the regulation window. As the load increases, the output "droops" towards the lower limit. This makes optimum use of the output voltage error band, yielding minimum output capacitor size and cost.

The droop is adjusted by setting the DC gain of the error amplifier. This is done by choosing the resistor from the ERROUT pin to the FB pin (R_{DRP}) of the controller. While the optimum value of R_{DRP} may be derived experimentally, the following equation can provide the first order calculation for given droop slope:

$$R_{drp} := \frac{R_{FB} \cdot R_{sense} \cdot G_{ca}}{\Delta V_{out}} \cdot \frac{\Delta I_{out}}{N_{phase}}$$

where R_{sense} is the current sensing resistance after taken into account of attenuation, and G_{ca} is the gain of the current amplifier while N_{phase} is number of phases being used.

Any output interconnection impedance not within the feedback loop can contribute to additional drooping. This effect has to be taken into account. Usually, when testing the regulation at different CPU pins, the results may vary slightly by same token.

It is important to use surface mount current sensing resistor to minimize the parasitic inductance for accurate correlation between the above equation and the test results. This is because the inductive contribution, which may also

Applications Information (Cont.)

be caused by layout inductances, may alter the PWM comparator trip point. The value of R_{DRP} may have to be adjusted to compensate for such parasitic effects.

It must be noted that the current amplifier gain is quite precise, with greater than 80dB of Common Mode Rejection Ratio (CMRR). Thus the droop accuracy is primarily based upon external components tolerances. By employing 1% current sensing element with very low temperature coefficient, this topology is proved to be the best comparing the schemes of using R_{dson} sensing and using inductor winding resistance sensing. The accurate drooping translates into minimum amount output bulk capacitor needed to meet the voltage regulation specifications and the least system cost.

Programming The DC Level Of The Output Voltage

Kirchoff's current law can be applied to the error amplifier's inverting input (see Fig. 1) to calculate R_{OS}, the DC level setting resistor. For given output voltage set point and VID setting, the resistance can be calculated by:

$$R_{os} := \frac{V_{bg}}{\left(\frac{V_{set} - V_{bg}}{R_{FB}} + \frac{V_{eo} - V_{bg}}{R_{drp}} + N_{DAC\_STEP} I_{DAC\_LSB}\right)}$$

where N_{DAC_STEP} is the number of VID steps down from the highest set point (VID=00000). For example, when VID [4:1]=00100, N_{DAC_STEP} = 4. V_{EO} is the error amplifier output voltage and, as a first approximation, it is equal to 1..7V. Again, V_{BG} = Precision Reference Voltage = 1.5V. The final value of R_{OS} may need to be fine tuned experimentally after the droop resistor has been chosen.

Control Loop Compensation

The current mode control yields a power supply easy to compensate because the power stage has first order (single pole) behavior. The SC2434 provides internal slope compensation to avoid sub harmonic oscillation of the current loop. The added ramp signal has 300mV peak-to-peak amplitude and the ramp frequency is as same as the oscillator frequency.

As depicted in Fig. 4, the gain for the voltage feedback loop can be expressed as a product of the power stage gain and the compensator gain:

$$Loop(s,R) := H_{p\_ccm}(s,R) \cdot H_c(s)$$

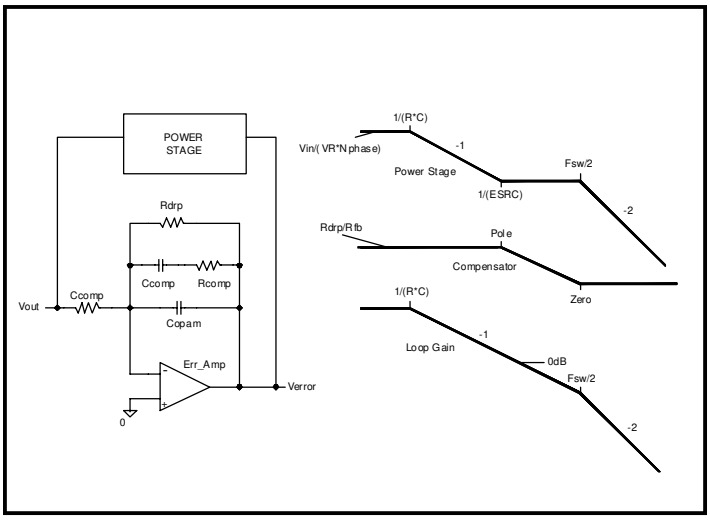


Fig. 4 - Loop gain and compensation of the current mode controller.

where C_{opam} is the equivalent internal capacitor across the error amplifier output and the inverting input with a value of 11pF.

The power stage transfer function under continuous conduction mode can be approximated by:

$$H_{p\_ccm}(s,R) := G_{pwm} \cdot \frac{\left(1 + s \cdot C \cdot R_c\right)}{(1 + s \cdot R \cdot C) \cdot \left[1 + 1.5 \cdot \frac{s}{\pi \cdot F_s} + \left(\frac{s}{\pi \cdot F_s}\right)^2\right]}$$

where G_{PWM} is the low frequency gain of the power stage. The power stage has an ESR zero, a dominant pole at low frequency, and a pair of complex pole located at one half of the switching frequency. The parameter used here are defined as below:

C = output bulk capacitance
R = load resistance
R_C = ESR of output bulk capacitor
F_{SW} = switching frequency

The PWM gain is defined as:

$$G_{pwm} := \frac{R \cdot N_{phase}}{R_{sense} \cdot G_{CA}}$$

Applications Information (Cont.)

The compensator transfer function has two poles and one zero:

$$H_c(s) := \frac{-R_{drp}}{R_{FB}} \cdot \frac{\left(1 + \frac{s}{\omega_z}\right)}{\left(1 + \frac{s}{\omega_{p1}}\right) \cdot \left(1 + \frac{s}{\omega_{p2}}\right)}$$

To optimize the transient responses, it is recommended that:

- To use the first compensator pole to cancel the power stage ESR zero;
- To place the compensator zero at one half of the switching frequency;
- And to place the second compensator pole at high frequency.

The Bode plots based this model and those obtained from experiment are depicted in Fig. 5 and Fig. 6, respectively. It can be seen that the model agrees well with the experiment. The control model provides us physical insight of the loop dynamics and helps the designer to achieve good transient responses and system stability. Here are few comments:

- The loop crossover frequency (0dB frequency) should be lower than one fifth (20%) of the switch frequency to avoid noise pick up and the phase lag introduced by the complex pole located at one half of the switching frequency;
- A >20KHz crossover frequency is adequate to assure good transient response when the VR output impedance, or droop impedance, is programmed to be equal to the output capacitor ESR. The ESR frequency for the output bulk capacitor is usually less than 20KHz, and beyond that frequency the capacitor behaves like a resistor up to few hundred KHz, which is desired for dynamic droop. There is no point to demand the control loop to have much higher crossover frequency beyond the ESR zero frequency.

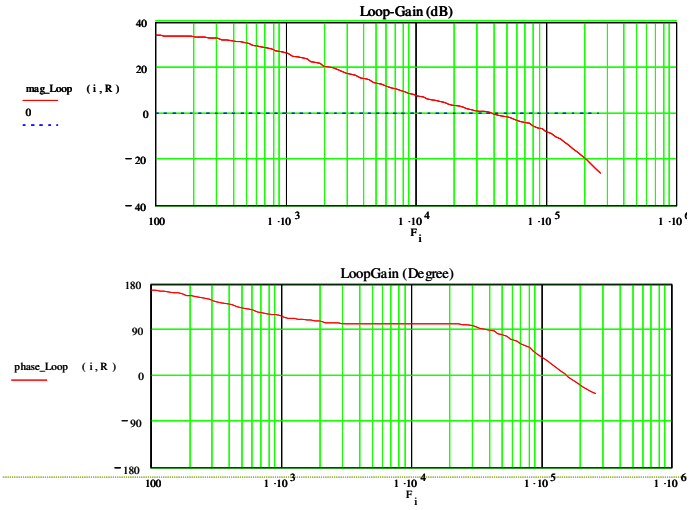


Fig. 5 - Loop gain Bode plot based on control loop model.

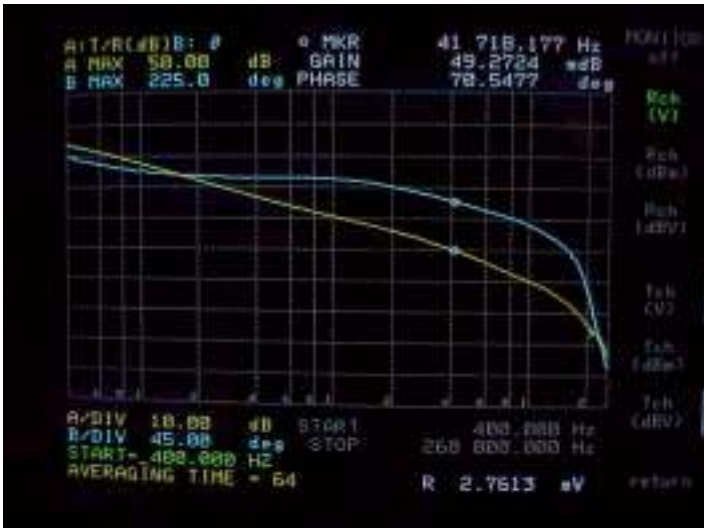


Fig. 6 - Measured loop gain Bode plots.

Applications Information (Cont.)

PCB Layout Consideration

Good layout is necessary for successful implementation of the SC2434 based 3 tri-phase topology. There are few general rules:

- Reserve enough PCB space for the power supply (1.2~1.5 square inch for every 10A of load current);
- Place enough high frequency ceramic capacitors inside and around the CPU socket (please follow CPU manufacture's decoupling guideline);
- Place bulk output capacitors around the CPU socket as uniformly as possible. The connection copper between these capacitors and the CPU socket must be short and wide to minimize inductance and resistance;
- Always place the high power parts first;
- Always use a ground plane or ground planes;
- Always try to minimize the stray inductance of the high pulsating current loop which is formed by input capacitors and the MOSFET half-bridges.

The following layout guideline gives details on how to achieve a good layout:

- Input filter should contain mixed electrolytic capacitors and MLC capacitors. For every 20A of load current, use about 10uF of MLC caps. Put MLC caps close to current sensing resistor;
- Use surface mount current sensing resistor (typically 3~5 mOhm in surface mount package with low temperature coefficient and low package inductance, typically less than 0.3nH);
- Try to minimize the stray inductance from the current sensing resistor to the drains of the top FETs by using wide trace (>0.5" wide and no more than 3" long). This trace can run on inner1 layer, for example, if the inner2 layer is the ground plane, assuming the FETs are on the top layer. This arrangement forms so called strip line structure for the pulsating power current, which yields least amount of stray inductance. The concept is depicted in Fig. 7;
- Keep the layout as electrically symmetrical as possible, as shown in Fig. 8, to avoid very uneven stray inductance from the sensing resistor to the drains of the top FETs;
- Use a pair of closely paralleled traces to pick up the sensing voltage across the sensing resistor. The sensing traces server as differential input to the OC+ and OC- pins of the SC2434 controller. These traces should run on a routing layer (e.g., bottom layer for 4 layer PCB case) to avoid picking up strong AC magnetic field due to power current flow. In this case, the differential sensing traces are shielded by the ground layer. The filter cap across the OC+ and OC- pins should be placed as close as possible to the controller. Pay close attention that never allow power current flowing on or running close by the sensing traces. Please see Fig. 8;
- Separate power ground from analog ground to prevent power current from running over the analog ground plane. The SC2434 controller should be placed on the quite analog ground area. The analog ground should be single-point connected to the PGND near the output capacitor or the CPU socket to provide best possible ground sense. Refer to the application schematics for those components should be connected directly to the AGND (Vcc decoupling caps, cap on BGOUT pin, resistors on OSCREF pin, DACREF pin, FB pin, and PGIN pin).

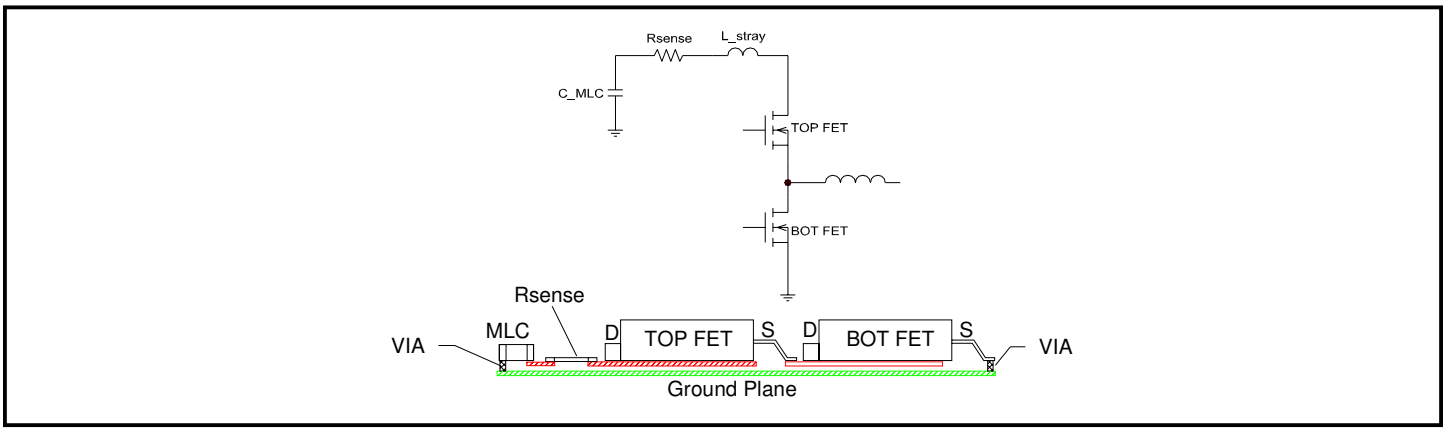


Fig. 7 - Use MLC capacitors and strip line structure to minimize the stray inductance for the switching current loop.

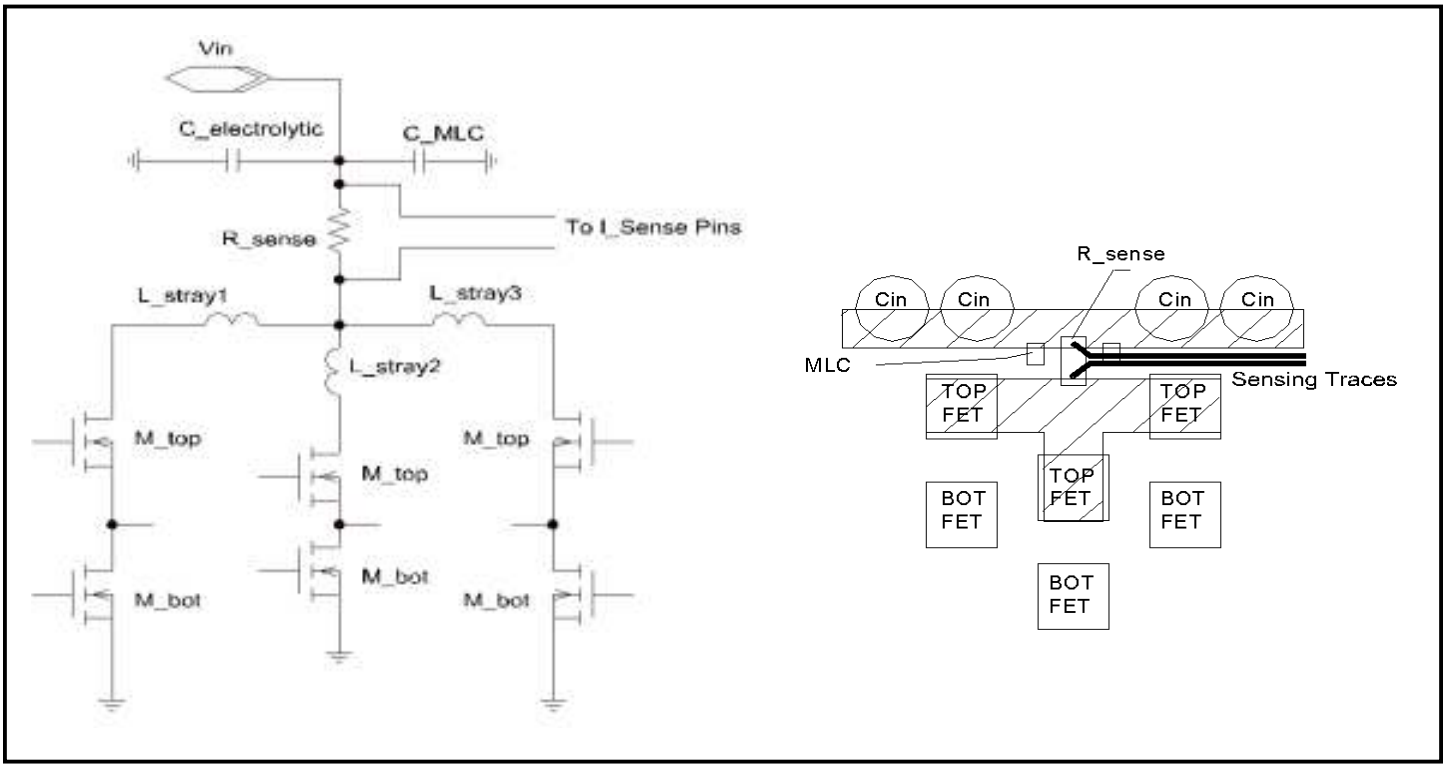


Fig. 8 - Layout concept for input current sensing: (a) use MLC input capacitors; (b) minimize inductance; (c) keep electrical symmetry; and (d) use differential sensing traces.

A Reference Design Example For Intel Pentium IV Processor

Brief specifications of this design are listed below:

- V_{in}=12V
- V_{out}=1.725V +/- 25mV at 0A load
- V_{out} droop slope is 1.5 mOhm
- V_{out} tolerance is +/-25mV for all load conditions
- I_{out} = 60A max
- VID [4:0] = 00100

The schematic is shown on the cover page of this data sheet.

Bill of Materials - Reference Design

Item	Qty.	Reference	Value	Description/Part No.	Package	Vendor
1	1	C_COMP	47pF	10V, X7R,MLCC,VJ603Y470KXXAT	0603	VISHAY
2	1	C1	0.33uF	25V, X7R,MLCC,VJ805Y334KXXAT	0805	VISHAY
3	3	C2,C3,C4	2200uF	15V Al. Elec. cap	CPCYL/D.400/ LS.200/.034	Sanyo
4	8	C5,C9,C13, C15,C18, C26,C30,C38	1uF	16V, Y5V,MLCC,PCC1849CT-ND	0805	Panasonic
5	3	C6,C7,C16	4.7uF	16V, Y5V,MLCC,PCC1900CT-ND	1206	Panasonic
6	12	C8,C10,C14, C19,C20,C22, C23,C27,C28, C31,C33,C35	1500uF	6.3V Al. Cap Rybucon MBZ	CPCYL/D.325/ LS.125/.034	Rubicon
7	3	C11,C24,C36	1nF	16V, X7R,MLCC,VJ603Y102KXXAT	0603	VISHAY
8	3	C12,C25,C37	2.2nF	50V, X7R,MLCC,VJ805Y222KXXAT	0805	VISHAY
9	2	C17,C29	0.33uF	25V, X7R,MLCC,VJ803Y334KXXAT	0805	VISHAY
10	1	C21	10nF	10V, X7R,MLCC,VJ603Y103KXXAT	0603	VISHAY
11	1	C32	100nF	16V, X7R,MLCC,VJ603Y104KXXAT	0603	VISHAY
12	1	C34	470pF	10V, X7R,MLCC,VJ603Y471KXXAT	0603	VISHAY
13	6	D1,D2,D3,D4, D5,D6	3A	30V SM Schottly DL4148MSCT-ND	DO213AC	DIGI-KEY
14	4	L1,L2,L3,L4	638nH	638nH, 20A , Inductor TTIF1305-638	IN/L500/W400/.10	Falco
15	3	M1,M3,M5	FDB6036BL	MOSFET	TO-263AB	Fairchild
16	2	M2,M4	FDB7045L	MOSFET	TO-263AB	Fairchild
17	1	M6	FDP7045L	MOSFET	TO-263AB	Fairchild
18	1	R_COMP	29.4K	SM 1% CRCW06032942F	0603	VISHAY
19	1	R_DAC	37.4K	SM 1% CRCW06033742F	0603	VISHAY
20	1	R_DRP	187K	SM 1% CRCW06031873F	0603	VISHAY
21	1	R_FB	10.0K	SM 1% CRCW06031002F	0603	VISHAY
22	1	R_OS	46.4K	SM 1% CRCW06034642F	0603	VISHAY
23	1	R_OSC	31.6K	SM 1% CRCW06033162F	0603	VISHAY
24	1	R1	3m	SM Sensing R 1% RL7520W	2512	CYNTEC
25	4	R2,R5,R8,R13	2R2	SM 1% CRCW06032R2F	0603	VISHAY
26	1	R3	20	SM 1% CRCW060320R0F	0603	VISHAY
27	3	R4,R10,R15	1R0	SM 1% CRCW060331R0F	0603	VISHAY
28	1	R6	100	SM 1% CRCW06031000F	0603	VISHAY
29	3	R7,R11,R16	1R0	SM 1% CRCW12061R0F	1206	VISHAY

Bill of Materials - Reference Design (Cont.)

Item	Qty.	Reference	Value	Description/Part No.	Package	Vendor
30	1	R9	NO POP	SM 1% CRCW06031R0F	0603	VISHAY
31	1	R12	5.1K	SM 1% CRCW06035111F	0603	VISHAY
32	2	R14,R18	1.0K	SM 1% CRCW06031001F	0603	VISHAY
33	1	R17	750	SM 1% CRCW06037500F	0603	VISHAY
34	3	U1, U3, U4	SC1205	Dual FET Driver	SOIC-8	SEMTECH
35	1	U2	SC2434	Tri-Phase Current Mode Controller w/ Power Good	SOIC-20 or TSSOP-20	SEMTECH

Note 1: Magnetic Cool Mu 77041, 5 turns AWG #16 (800nH@0A, 600nH@25A)

Applications Information (Cont.)

Typical Performance Of The Reference Design

The reference design implemented 1.5mOhm output droop impedance as shown in Fig. 9.

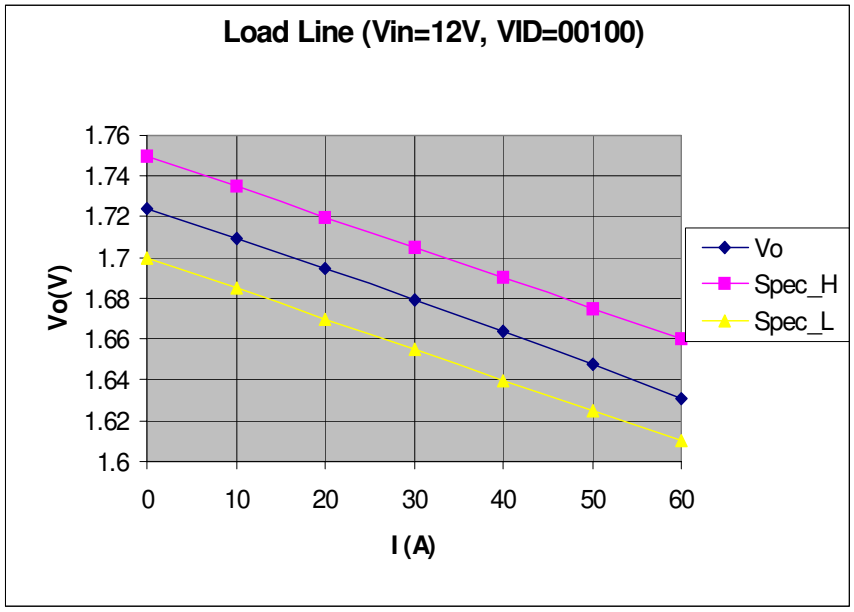


Fig. 9 - Measured output drooping characteristics of the 60A design.

The efficiency of the design is depends on the MOSFET being used and thermal management requirements of controlling the PCB temperature and the MOSFET junction temperature. The following efficiency curve is corresponding to 4mOhm bottom FET, while the top FET has 12 mOhm Rdson.

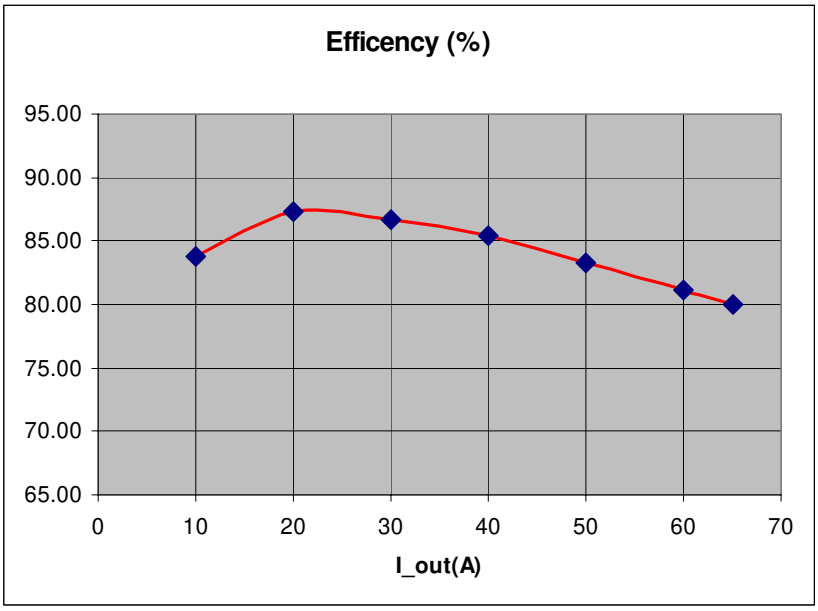


Fig. 10 - Typical efficiency curve for 12 mOhm top FETs and 4 Ohm bottom FETs.

Applications Information (Cont.)

The typical phase node voltage and the output voltage ripple waveform is shown in Fig. 11 under 60A full load operation, where one can see the output ripple is very small and even with a frequency three times of the switching frequency.

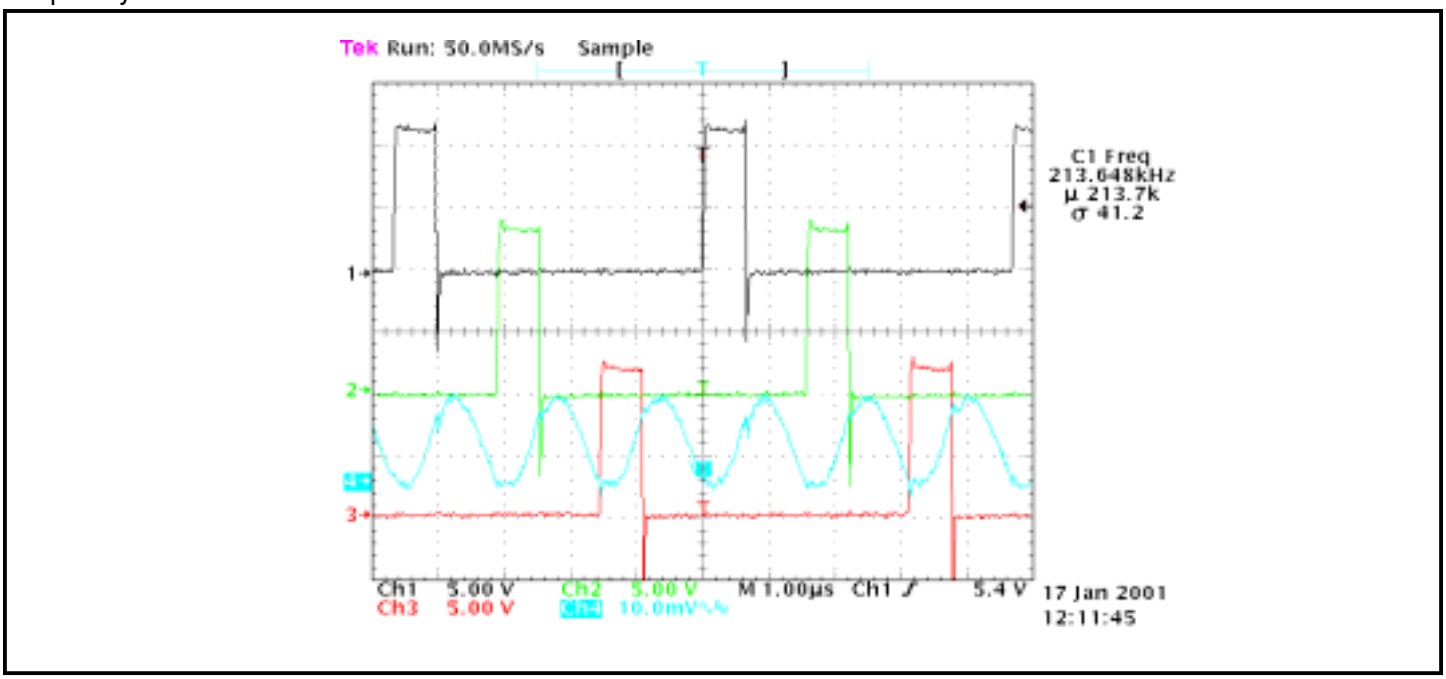


Fig. 11 - The typical phase node voltage and the output voltage ripple waveform under 60A full load operation.

The typical gate waveform for the top and bottom MOSFETs is also shown here, well-controlled dead time is demonstrated which ensures high efficiency operation of the VR.

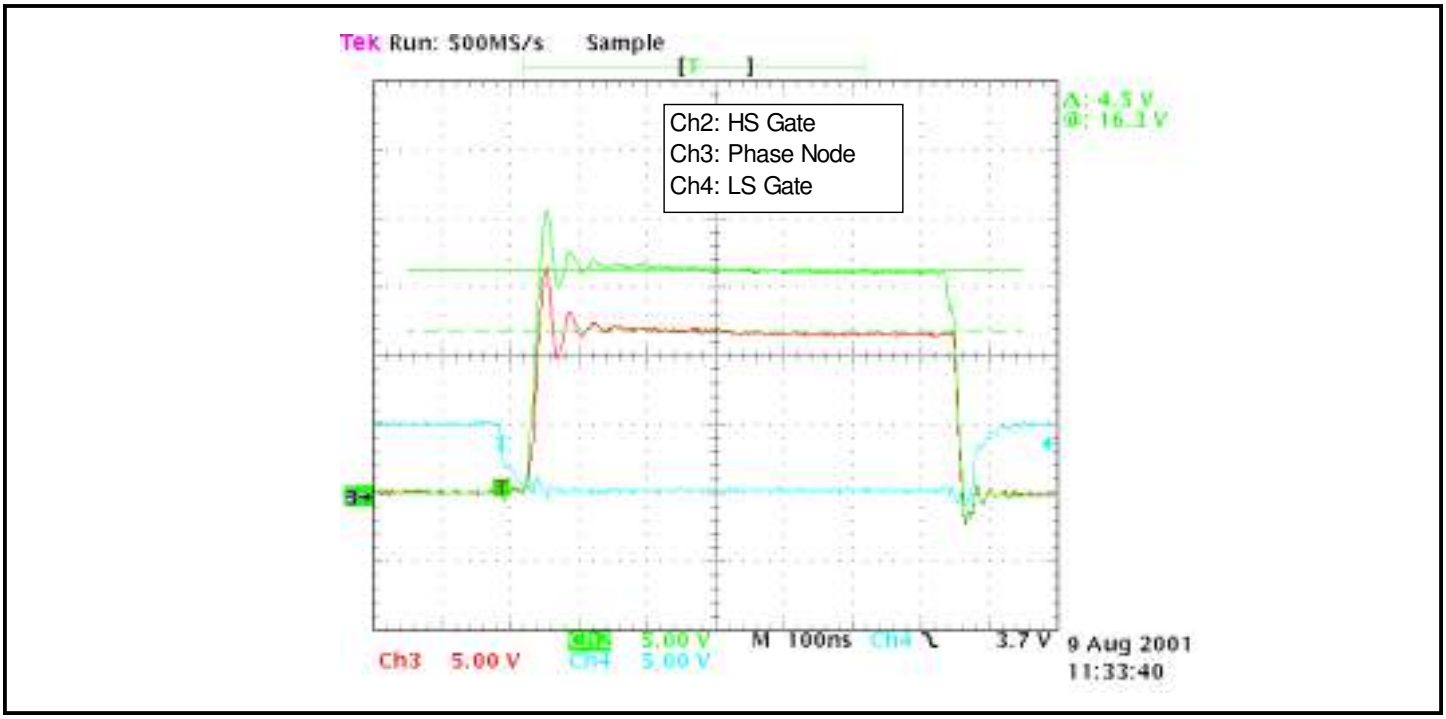


Fig. 12 - The typical gate waveform for the top and bottom MOSFETs.

Applications Information (Cont.)

The transient response for a maximum load step changes (10A to 60A) is shown in Fig. 14, where one can see that accurate drooping will help to reduce the amount of output capacitance needed. Please notice that using more multilayer ceramic capacitors for better high frequency decoupling can reduce the narrow voltage spikes.

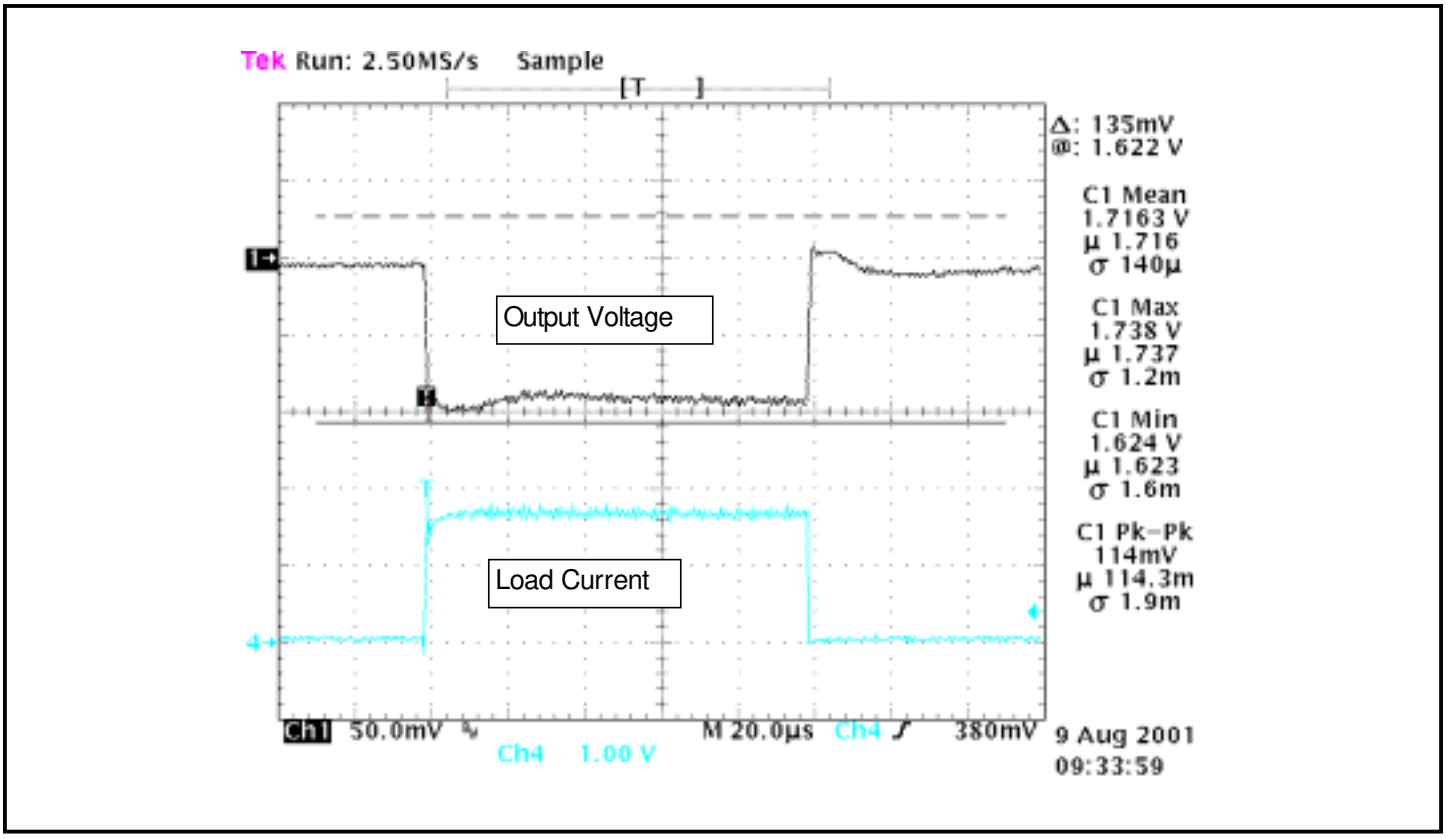
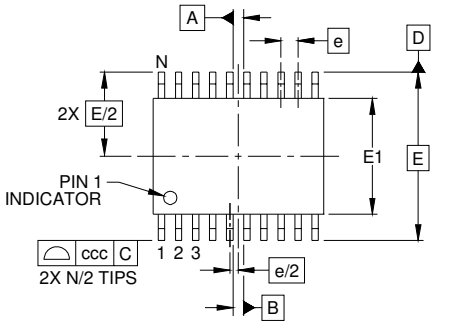
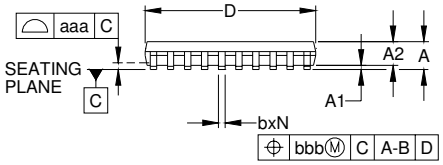
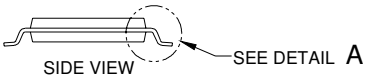


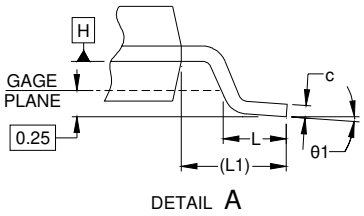
Fig. 13 - Transient response and the test condition:
Step Load from 10A to 60A
Output Capacitors: 14 units of 560uF OSCON caps, 38 units of 10uF ceramic caps
Ch1: Output Voltage
Ch4: Output Current (1A = 27.5mV di/dt = 370A/uS)
Meet Intel P-4 spec

Outline Drawing - TSSOP-20







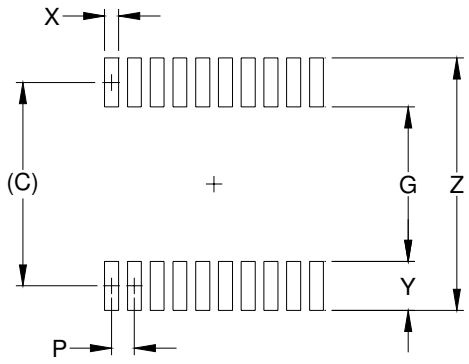


DIM	DIMENSIONS					
	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	-	-	.047	-	-	1.20
A1	.002	-	.006	0.05	-	0.15
A2	.031	-	.042	0.80	-	1.05
b	.007	-	.012	0.19	-	0.30
c	.003	-	.007	0.09	-	0.20
D	.251	.255	.259	6.40	6.50	6.60
E1	.169	.173	.177	4.30	4.40	4.50
E	.252 BSC			6.40 BSC		
e	.026 BSC			0.65 BSC		
L	.018	.024	.030	0.45	0.60	0.75
L1	(.039)			(1.0)		
N	20			20		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.004			0.10		
ccc	.008			0.20		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MO-153, VARIATION AC.

Land Pattern - TSSOP-20

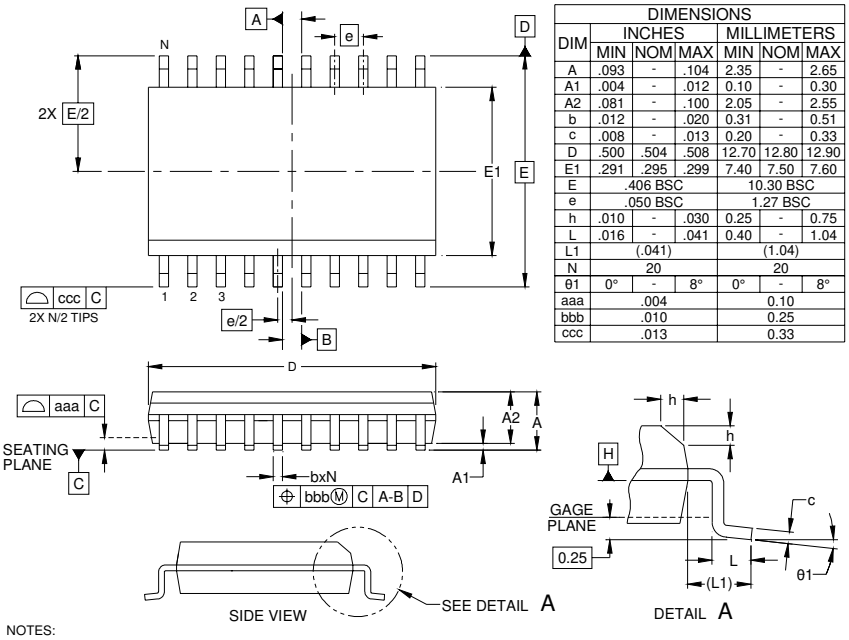


DIMENSIONS		
DIM	INCHES	MILLIMETERS
C	(.222)	(5.65)
G	.161	4.10
P	.026	0.65
X	.016	0.40
Y	.061	1.55
Z	.283	7.20

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.

Outline Drawing - SOIC-20

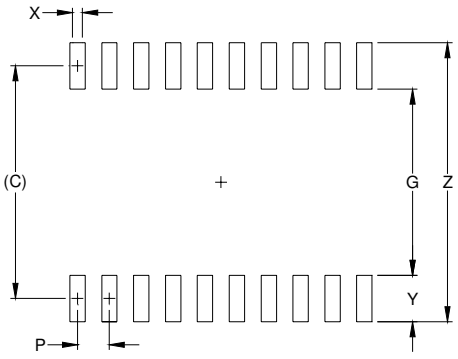


DIM	INCHES			MILLIMETERS		
	MIN	NOM	MAX	MIN	NOM	MAX
A	.093	-	.104	2.35	-	2.65
A1	.004	-	.012	0.10	-	0.30
A2	.081	-	.100	2.05	-	2.55
b	.012	-	.020	0.31	-	0.51
c	.008	-	.013	0.20	-	0.33
D	.500	.504	.508	12.70	12.80	12.90
E1	.291	.295	.299	7.40	7.50	7.60
E	.406 BSC			10.30 BSC		
e	.050 BSC			1.27 BSC		
h	.010	-	.030	0.25	-	0.75
L	.016	-	.041	0.40	-	1.04
L1	(.041)			(1.04)		
N	20			20		
θ1	0°	-	8°	0°	-	8°
aaa	.004			0.10		
bbb	.010			0.25		
ccc	.013			0.33		

NOTES:

1. CONTROLLING DIMENSIONS ARE IN MILLIMETERS (ANGLES IN DEGREES).
2. DATUMS -A- AND -B- TO BE DETERMINED AT DATUM PLANE -H-
3. DIMENSIONS "E1" AND "D" DO NOT INCLUDE MOLD FLASH, PROTRUSIONS OR GATE BURRS.
4. REFERENCE JEDEC STD MS-013, VARIATION AC.

Land Pattern - SOIC-20



DIM	INCHES	MILLIMETERS
C	(.362)	(9.20)
G	.276	7.00
P	.050	1.27
X	.024	0.60
Y	.087	2.20
Z	.449	11.40

NOTES:

1. THIS LAND PATTERN IS FOR REFERENCE PURPOSES ONLY. CONSULT YOUR MANUFACTURING GROUP TO ENSURE YOUR COMPANY'S MANUFACTURING GUIDELINES ARE MET.
2. REFERENCE IPC-SM-782A, RLP NO. 307A.

Contact Information

Semtech Corporation
Power Management Products Division
200 Flynn Road, Camarillo, CA 93012
Phone: (805)498-2111 FAX (805)498-3804