MP86952

16V, 70A, Radiation-Tolerant, Monolithic Half-Bridge Intelli-Phase™ Solution with Internal Power MOSFETs and Gate Drivers

DESCRIPTION

The MP86952 is a radiation-tolerant, monolithic half-bridge IC with built-in internal power MOSFETs and gate drivers. It achieves up to 70A of continuous output current across a wide 3V to 16V input voltage range.

This Intelli-Phase™ solution can drive up to 70A of current per phase. The integrated MOSFETs and drivers achieve high efficiency through optimized dead time (DT) and reduced parasitic inductance. The MP86952 has an operating range of 100kHz to 3MHz.

This device offers many features to simplify system design. It is compatible with tri-state pulse-width modulation (PWM) signal controllers, has Accu-Sense™ current sense to monitor the inductor current (I_L), and has temperature sense to report the junction temperature (T_J).

The MP86952 is ideal for server applications where efficiency and small size are critical. The MP86952 is available in an LGA-41 (5mmx6mm) package.

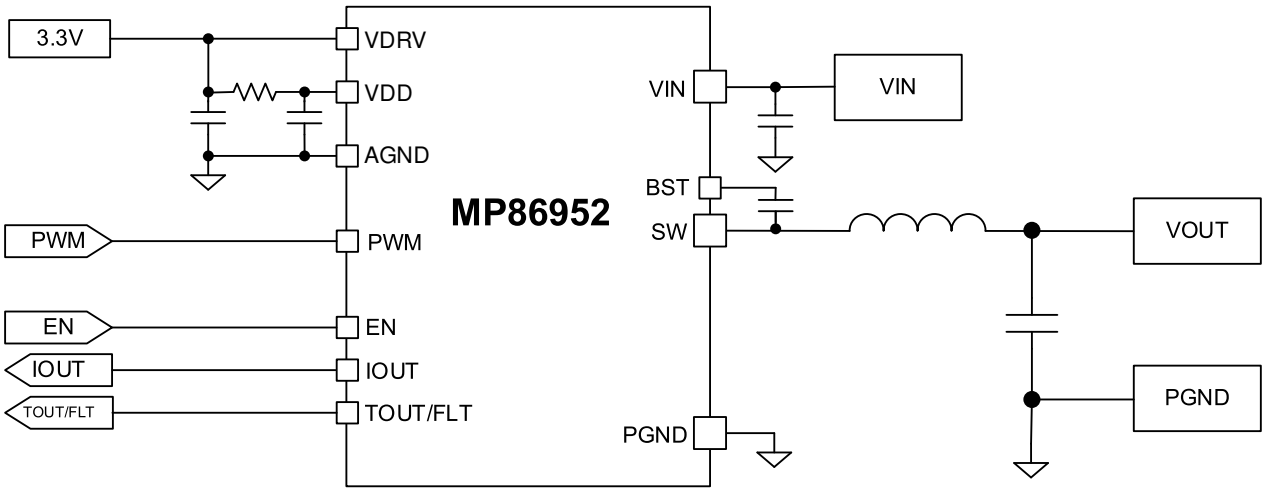
FEATURES

- Wide 3V to 16V Operating Input Range
- Up to 70A Continuous Output Current
- Current Sense with Accu-Sense™
- Temperature Sense
- Tri-State Pulse-Width Modulation (PWM) Signal Compatible
- Current-Limit Protection
- Over-Temperature Protection (OTP)
- Fault Reporting
- Available in an LGA-41 (5mmx6mm) Package

APPLICATIONS

- Server Core Voltages
- Graphic Card Core Regulators
- Power Modules

TYPICAL APPLICATION



ORDERING INFORMATION

Part Number*	Package	Top Marking	MSL Rating
MP86952GMJ	LGA-41 (5mmx6mm)	*See Below*	3

* For Tape & Reel, add suffix -Z (e.g. MP86952GMJ-Z).

TOP MARKING

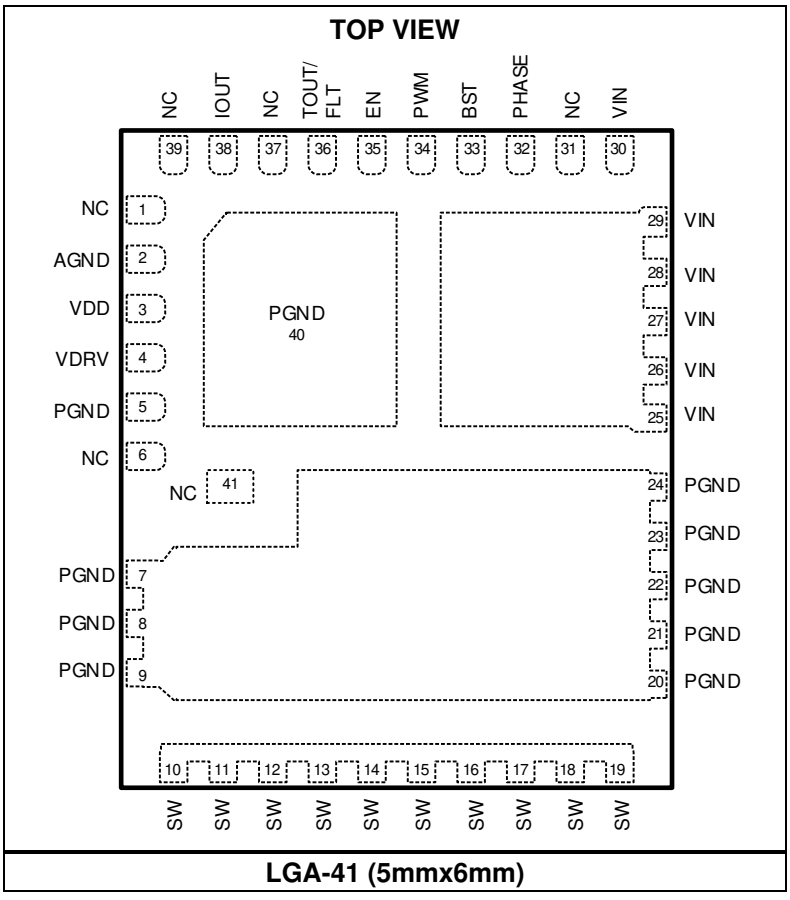
MPSYYWW

MP86952

LLLLLLL

MPS: MPS prefix
YY: Year code
WW: Week code
MP86952: Part number
LLLLLLL: Lot number

PACKAGE REFERENCE



LGA-41 (5mmx6mm)

PIN FUNCTIONS

Pin #	Name	Description
1, 6, 31, 37, 39, 41	NC	**No connection.**
2	AGND	**Analog ground.**
3	VDD	**Supply voltage (3.3V) for the internal circuitry.** Connect the VDD and VDRV pins with a 2.2Ω resistor. Decouple VDD with a 1µF of greater ceramic capacitor connected to AGND. Connect AGND and PGND at the VDD capacitor's ground connection.
4	VDRV	**Driver voltage.** Connect the VDRV pin to the 3.3V supply. Decouple VDRV with a 1µF to 4.7µF ceramic capacitor.
5, 7, 8, 9, 20, 21, 22, 23, 24, 40	PGND	**Power ground.**
10, 11, 12, 13, 14, 15, 16, 17, 18, 19	SW	**Phase node.**
25, 26, 27, 28, 29, 30	VIN	**Input supply voltage.** Place a ceramic input capacitor (C_{IN}) close to the device to support the switching current and minimize parasitic inductance.
32	PHASE	**Switching node for the bootstrap capacitor connection.**
33	BST	**Bootstrap.** The BST pin requires a 0.1µF to 0.22µF capacitor to drive the power MOSFET's gate above the supply voltage. Connect BST to the capacitor between SW and BST to form a floating supply across the MOSFET driver.
34	PWM	**Pulse-width modulation input.** Float the PWM pin or drive PWM to a middle state to put SW in a high-impedance (Hi-Z) state.
35	EN	**Enable.** Pull the EN pin low to disable the device and put SW in a Hi-Z state.
36	TOUT/FLT	**Single-pin temperature sense and fault reporting.** If a fault occurs, the TOUT/FLT pin is pulled up to VDD's voltage level.
38	IOUT	**Current-sense output.** Use an external resistor to adjust the voltage to be proportional to the inductor current (I_L).

ABSOLUTE MAXIMUM RATINGS (1)

Supply voltage (V_{IN}) 18V
V_{IN} to V_{PHASE} (DC) .....-0.3V to +25V
V_{IN} to V_{PHASE} (10ns).....-5V to +32V
V_{SW} to PGND (DC).....-0.3V to V_{IN} + 0.3V
V_{SW} to PGND (25ns) .....-5V to +25V
V_{BST} ..... V_{PHASE} + 4V
V_{DD}, V_{DRV} .....-0.3V to +4V
All other pins .....-0.3V to V_{DD} + 0.3V
Instantaneous current 125A
Junction temperature .....150°C
Lead temperature .....260°C
Storage temperature ..... -65°C to +150°C

ESD Ratings

Human body model (HBM) .....Class 1C
Charged device model (CDM) .....Class C2B

Recommended Operating Conditions (2)

Supply voltage (V_{IN}).....3V to 16V
Driver voltage (V_{DRV}).....3V to 3.6V
Logic voltage (V_{DD}) .....3V to 3.6V
Operating junction temp (T_J)…. -40°C to +125°C

Thermal Resistance (3) (4) θ_{JB} θ_{JC_TOP}

LGA-41 (5mmx6mm) ..... 2.2..... 8.7.... °C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The device is not guaranteed to function outside of its operating conditions.
3) θ_{JB} is the thermal resistance from the junction to the board around the PGND soldering point.
4) θ_{JC_TOP} is the thermal resistance from the junction to the top of the package.

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, V_{DRV} = V_{DD} = V_{EN} = 3.3V, T_A = 25°C for typical values, T_J = -40°C to +125°C for maximum and minimum values, unless otherwise noted.

Parameter	Symbol	Condition	Min	Typ	Max	Units
I_{IN} shutdown current		EN is low		90	180	µA
V_{IN} under-voltage lockout (UVLO) rising threshold				2.5	3	V
V_{IN} UVLO threshold hysteresis				450		mV
I_{VDRV} quiescent current		PWM is low		250	350	µA
I_{VDD} quiescent current		PWM is low		3		mA
VDD UVLO rising threshold				2.75	2.95	V
VDD UVLO threshold hysteresis				300		mV
High-side (HS) current limit (5)	I_{LIM_FLT}	Cycle-by-cycle, up to eight cycles		110		A
Low-side (LS) current limit (5)		Negative cycle-by-cycle current limit, no fault report		-35		A
Negative LS current limit off time (5)				200		ns
HS current limit shutdown counter (5)				8		times
SW dead time (DT) rising (5)				2		ns
SW DT falling (5)		Positive I_L		6		ns
		Negative I_L		28		ns
EN input logic high voltage	V_{EN_HIGH}		2.3			V
EN input logic low voltage	V_{EN_LOW}				0.8	V
PWM high to SW rising delay (5)	t_{RISING}			20		ns
PWM low to SW falling delay (5)	$t_{FALLING}$			20		ns
PWM tri-state to SW Hi-Z delay (5)	t_{LT}			40		ns
	t_{TL}			30		ns
	t_{HT}			40		ns
	t_{TH}			30		ns
Minimum PWM pulse width (5)				30		ns
IOUT sense gain accuracy (5)		20A ≤ I_{SW} ≤ 70A	-2	0	+2	%
IOUT sense gain	G_{IOUT}			5		µA/A
IOUT sense offset		I_{SW} = 0A, V_{IOUT} = 1.2V, T_J = 25°C	-2	0	+2	µA
		PWM is in a Hi-Z state, V_{IOUT} = 1.2V	-1	0	+1	µA
IOUT voltage (5)	V_{IOUT}		0.7		2.1	V
TOUT/FLT sense gain (5)				8		mV/°C
TOUT/FLT sense offset (5)		T_J = 25°C		800		mV
Over-temperature protection (OTP) shutdown and fault flag (5)				160		°C
TOUT/FLT fault (5)			3	3.3		V
PWM resistor		Pull-up resistor, EN is high		6		kΩ
		Pull-down resistor, EN is high		5		kΩ
PWM logic high voltage			2.3			V
PWM tri-state region			1.1		1.8	V
PWM logic low voltage					0.8	V

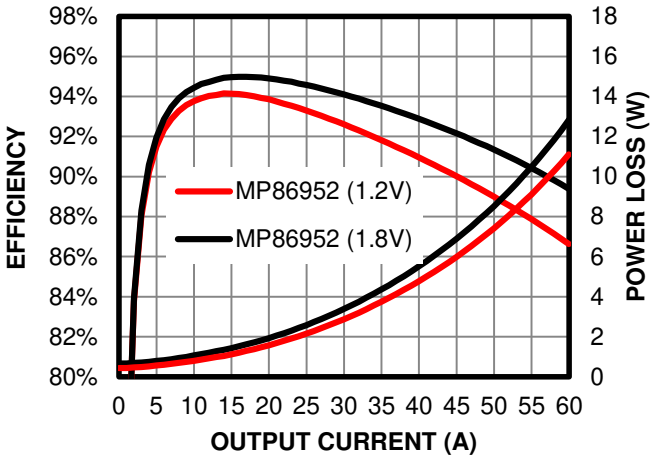
Note:

5) Guaranteed by design or characterization data. Not tested in production.

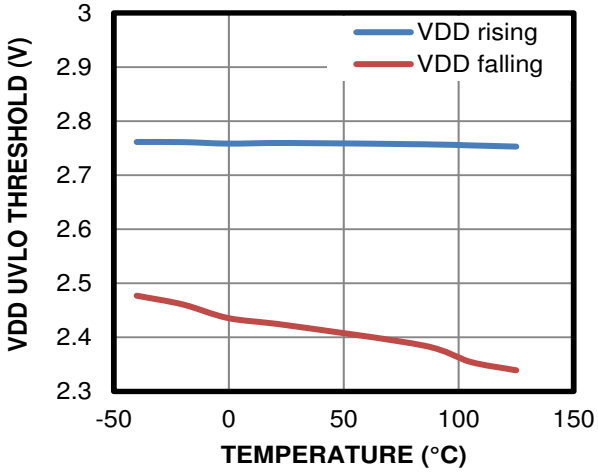
TYPICAL CHARACTERISTICS

Efficiency vs. Output Current vs. Power Loss

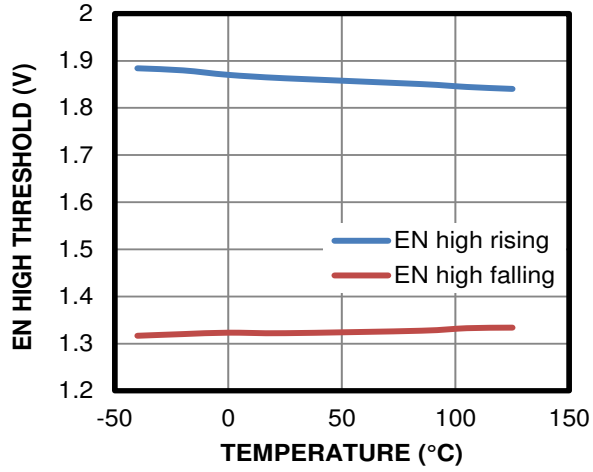
V_{IN} = 12V, L = 150nH, f_{SW} = 500kHz



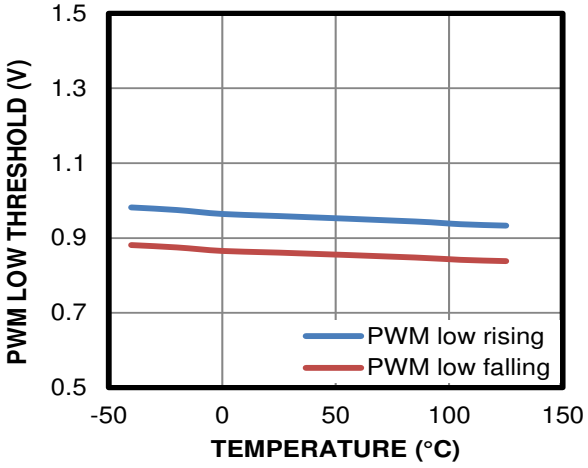
VDD UVLO Threshold vs. Temperature



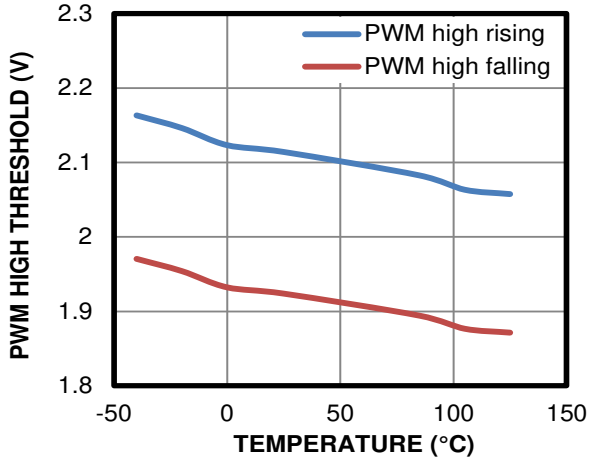
EN High Threshold vs. Temperature



PWM Low Threshold vs. Temperature



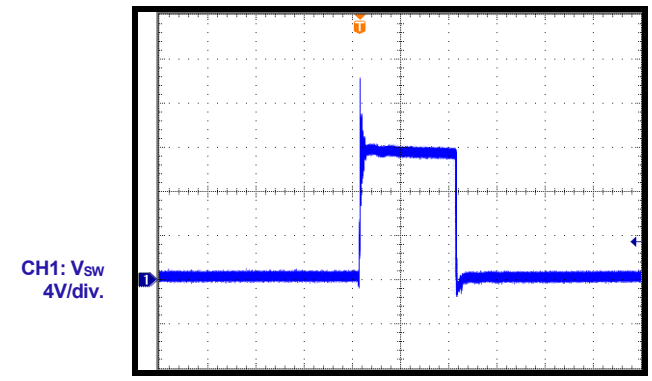
PWM High Threshold vs. Temperature



TYPICAL PERFORMANCE CHARACTERISTICS

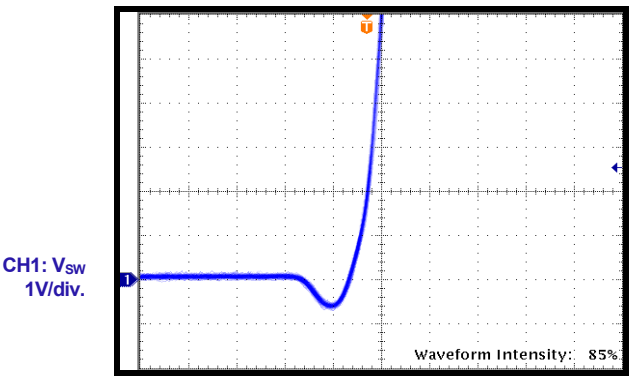
Switching

V_{IN} = 12V, L = 150nH, load = 30A



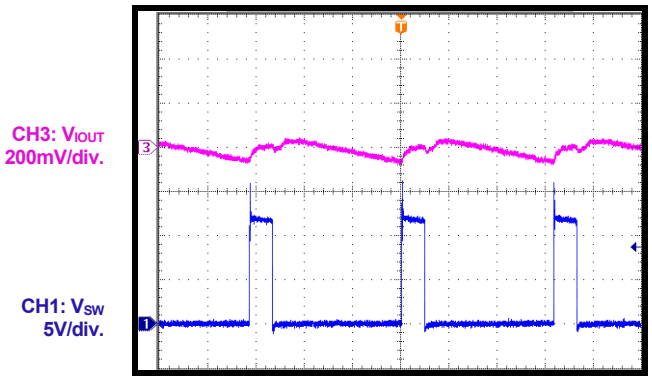
Dead Time at SW Ringing

Load = 30A



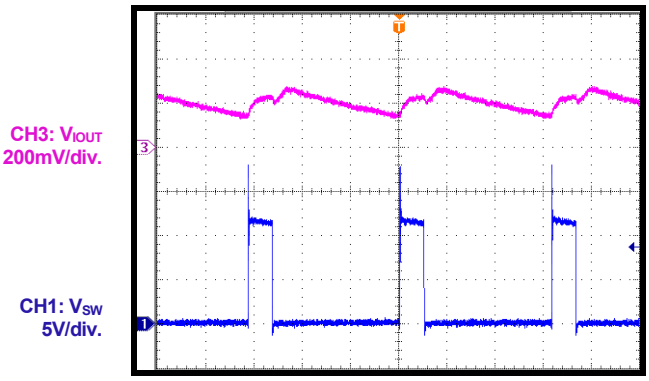
IOUT Output

Load = 0A

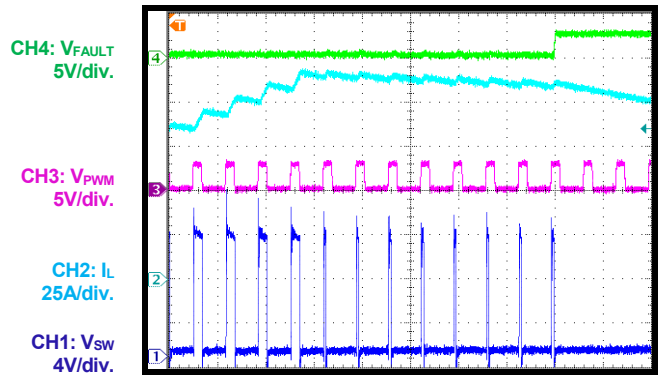


IOUT Output

Load = 30A



HS-FET Current Limit



FUNCTIONAL BLOCK DIAGRAM

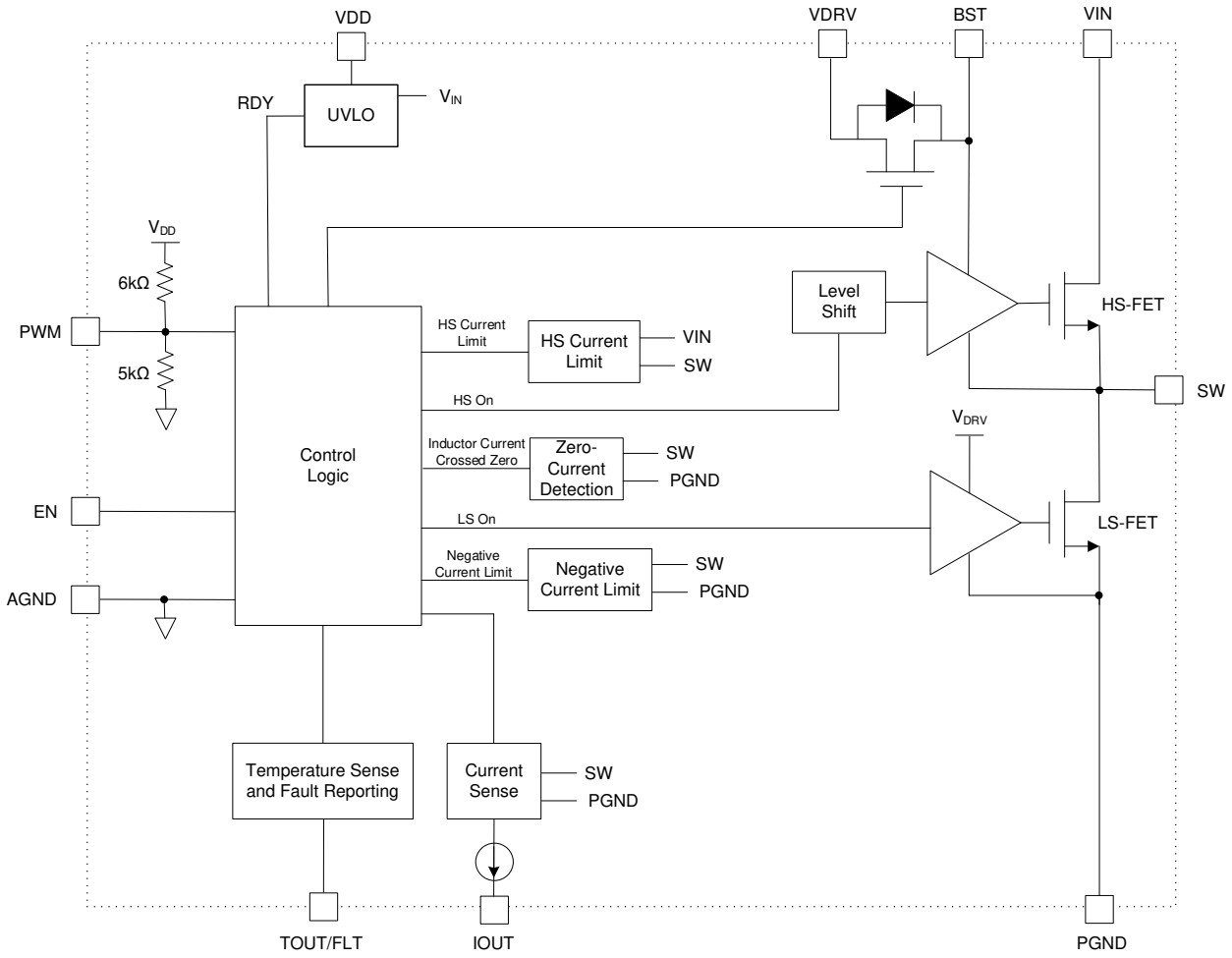


Figure 1: Functional Block Diagram

OPERATION

The MP86952 is a 16V, 70A, monolithic, half-bridge Intelli-Phase™ solution with integrated power MOSFETs and drivers. It is ideal for multi-phase buck regulator applications.

An external 3.3V supply is required to supply both the VDD and VDRV pins. Once the EN, VDD, and VDRV pins transition from low to high, the part starts up.

Pulse-Width Modulation (PWM)

The pulse-width modulation (PWM) input can operate as a tri-state input. If the PWM input signal is within the tri-state threshold window (t_{HT} to t_{LT}) for 50ns, then the high-side MOSFET (HS-FET) turns off and the low-side MOSFET (LS-FET) enters diode emulation mode. The LS-FET remains in diode emulation mode until zero-current detection (ZCD). The tri-state PWM input can come from a forced middle-voltage PWM signal, or can be made by floating the PWM input so that the internal current source charges the signal to a middle voltage. Figure 2 shows the propagation delay definition from PWM to the SW node.

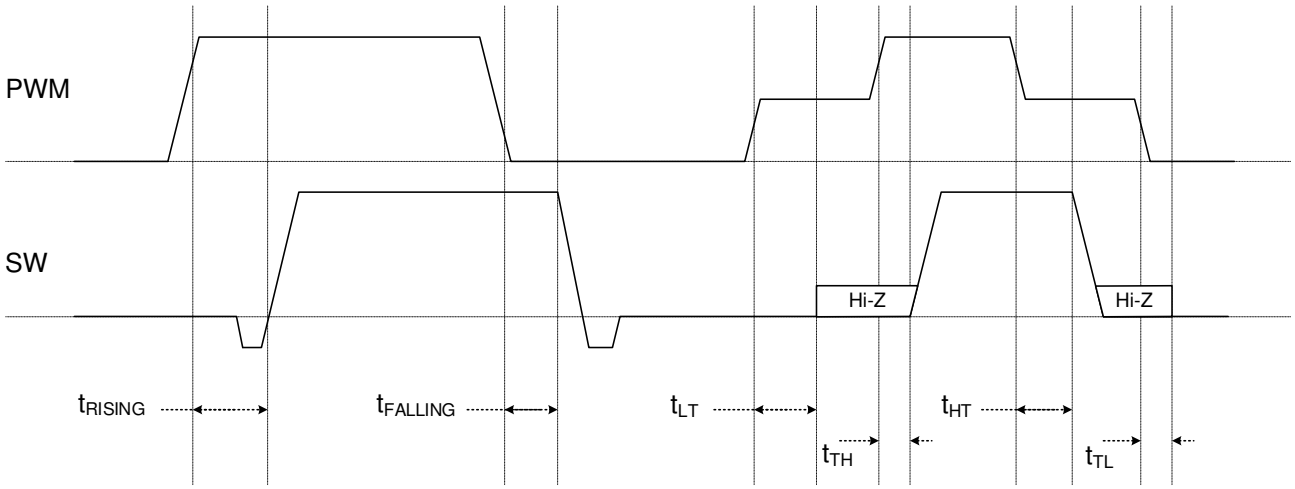


Figure 2: PWM Timing Diagram

Diode Emulation Mode

In diode emulation mode, PWM is low or in a tri-state input. If the inductor current (I_L) is positive, then the LS-FET turns on. If I_L is negative or crosses the ZCD threshold, then the LS-FET turns off. Diode emulation mode can be enabled by driving the PWM pin to a middle state or floating PWM.

Current Sense (CS)

The MP86952's current sense (CS) is a bidirectional current source proportional to I_L. The current-sense gain (G_{CS}) is 5μA/A. A resistor can be used to adjust the voltage gain to be proportional to I_L.

The IOUT pin has two output states (see Table 1). If EN is low (disabled), then the current-sense circuit is disabled and IOUT is in a high-impedance (Hi-Z) state.

Table 1: IOUT Output States

PWM	EN	IOUT
Enabled	High	Active
Disabled	Low	Hi-Z

IOUT requires a 0.7V to 2.1V voltage range to achieve an accurate current output of up to +350μA/-200μA (+70A/-40A). A resistor (R_{IOUT}) from IOUT to an external voltage is typically used to sink small currents and provide the 0.7V to 2.1V voltage level to meet the IOUT operating voltage. The proper reference voltage (V_{CM}) connected to R_{IOUT} can be calculated with Equation (1):

$$0.7V < I_{IOUT} \times R_{IOUT} + V_{CM} < 2.1V \quad (1)$$

The output current (I_{IOUT}) can be calculated with Equation (2):

$$I_{IOUT} = I_{SW} \times G_{IOUT} \quad (2)$$

The Intelli-Phase™ current-sense output is

used by the controller to accurately monitor I_{IOUT}. The cycle-by-cycle current information from IOUT is used for phase-current balancing, over-current protection (OCP), and active voltage positioning (output voltage droop).

Positive and Negative Inductor Current Limits

If an HS-FET over-current (OC) condition is detected, then the HS-FET turns off for one PWM cycle. If an OC condition is detected for eight consecutive cycles, then the HS-FET latches off and the TOUT/FLT pin is pulled high to VDD's voltage level. The LS-FET turns on and remains on until ZCD, then turns off. Recycle the power on VIN or VDD, or toggle EN to release the latch and restart the device.

If a -35A valley current is detected, then the LS-FET turns off and the HS-FET turns on for 200ns to limit the negative current. The LS-FET's negative current limit does not trigger a fault report.

Temperature-Sense Output with Fault Indicator (TOUT/FLT)

The TMON/FLT pin has dual functions. It acts as the device's junction temperature sense and fault detection. These functions are described below.

Junction Temperature Sense

If V_{DD} exceeds its under-voltage lockout (UVLO) threshold and the part is active, then the TOUT/FLT pin voltage output is proportional to the junction temperature (T_J). The gain is 8mV/°C with an 800mV offset at 25°C. For example, TMON/FLT is 0.8V at T_J = 25°C, and 1.6V at T_J = 125°C.

Fault Function

When a fault occurs, TOUT/FLT is pulled to VDD to report the fault event, regardless of T_J. After a 200ns delay, PWM's resistance changes according to the indicated fault event.

Table 2 shows the PWM resistance for each fault event.

Table 2: PWM Resistance for Each Fault Event

Fault Event	PWM Resistance
Over-current (OC) fault	10kΩ to AGND
Over-temperature (OT) fault	20kΩ to AGND
SW to PGND short	1kΩ to VDD

TMON/FLT monitors three different fault events: OC, over-temperature (OT), and SW to PGND short.

1. OC fault: Eight consecutive current limit faults trigger an OC fault. Once a fault occurs, the part latches off to turn off the HS-FET. The LS-FET turns on, then turns off once I_L reaches 0A. The PWM pin uses a 10kΩ resistor connected to AGND to indicate this fault event.
2. OT fault: At T_J > 160°C, the part latches off to turn off the HS-FET. The LS-FET turns on, then turns off once I_L reaches 0A. PWM uses a 20kΩ resistor connected to AGND to indicate this fault event.
3. SW to PGND short: Once this fault occurs, the part latches off to turn off the HS-FET. PWM is pulled high via a 1kΩ resistor connected to VDD to indicate this fault event.

Release a fault latch by toggling EN, or cycling the power on VIN or VDD.

For multi-phase operation, connect the TOUT/FLT pin of each Intelli-Phase™ together (see Figure 3).

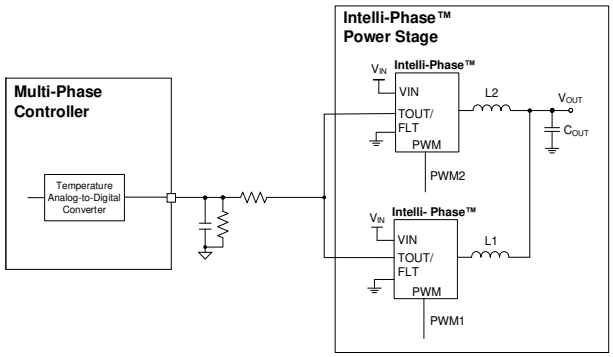


Figure 3: Multi-Phase Temperature Sense

APPLICATION INFORMATION

PCB Layout Guidelines

Efficient PCB layout is critical for stable operation. For the best results, refer to Figure 4 and follow the guidelines below:

1. Place the MLCC input capacitors as close to VIN and PGND as possible.
2. Place the major MLCC capacitors on the same layer as the MP86952.
3. Place as many VIN and PGND vias underneath the package as possible. Place these vias between the VIN and PGND long pads.
4. Place a VIN copper plane on the second inner layer to form the PCB stack (positive/negative/positive) to reduce parasitic impedance from the MLCC input capacitor to the MP86952. Ensure that the copper plane on the inner layer covers the VIN vias and MLCC input capacitors.
5. Place more PGND vias close to the PGND pin/pad to minimize parasitic resistance, parasitic impedance, and thermal resistance.
6. Place the 0.1µF to 1µF BST capacitor and the VDRV capacitor as close to the MP86952's pins as possible.
7. For BST routing, use a trace width greater than 20mils. Avoid placing vias on the BST driving path.
8. Place the VDD decoupling capacitor close to the device.
9. Connect AGND and PGND at the VDD capacitor's ground connection.
10. Keep the IOUT signal trace away from high-current paths, such as SW and PWM.

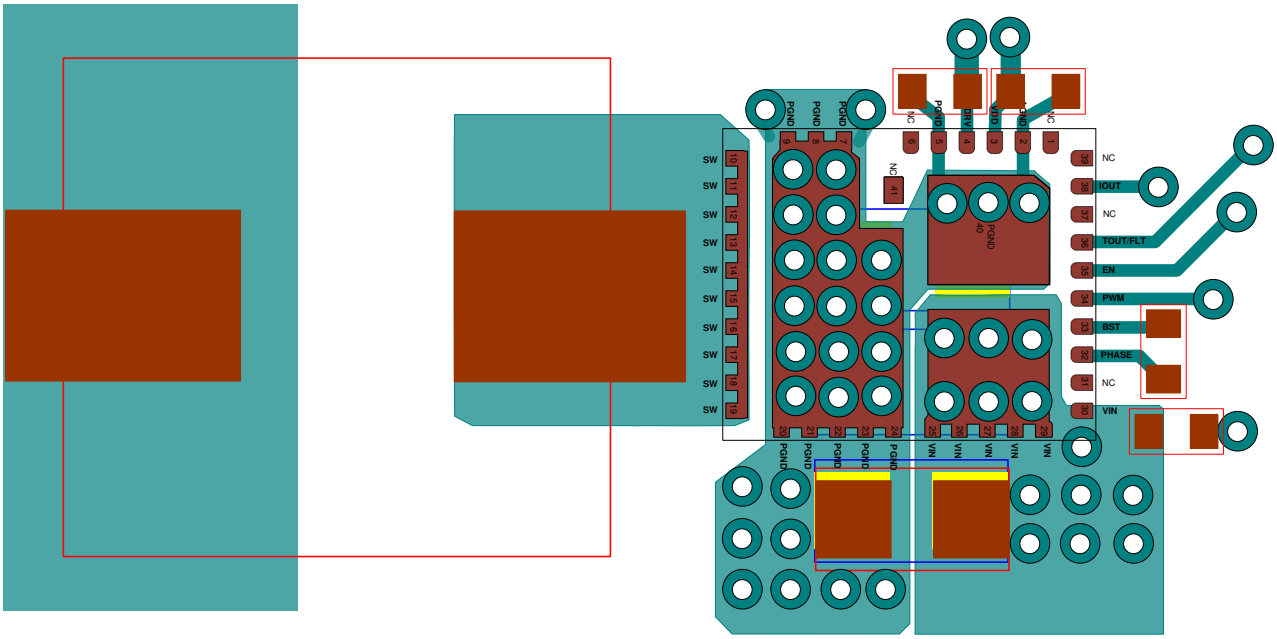


Figure 4: Recommended PCB Layout

Input Capacitor: 0402 Package (Top Side) and 0805 Package (Top Side and Bottom Side)

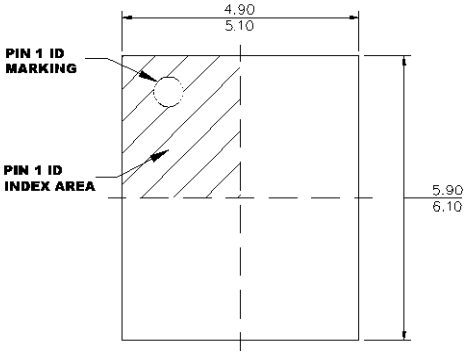
Inductor: 11mmx8mm Package

VDD/BST/VDRV Capacitors: 0402 Package

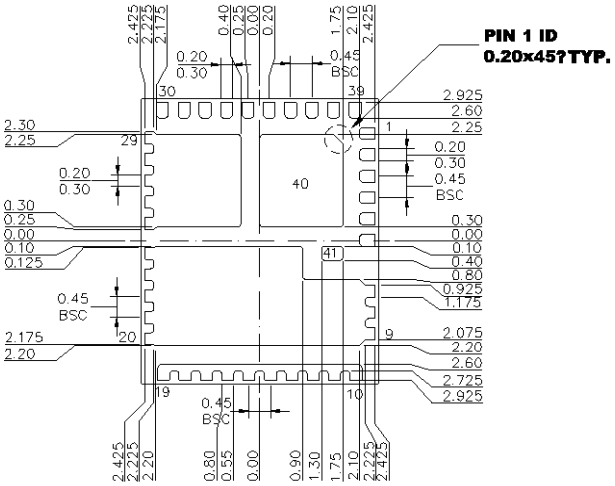
Via Size: 20/10mils

PACKAGE INFORMATION

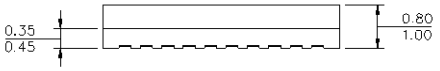
LGA-41 (5mmx6mm)



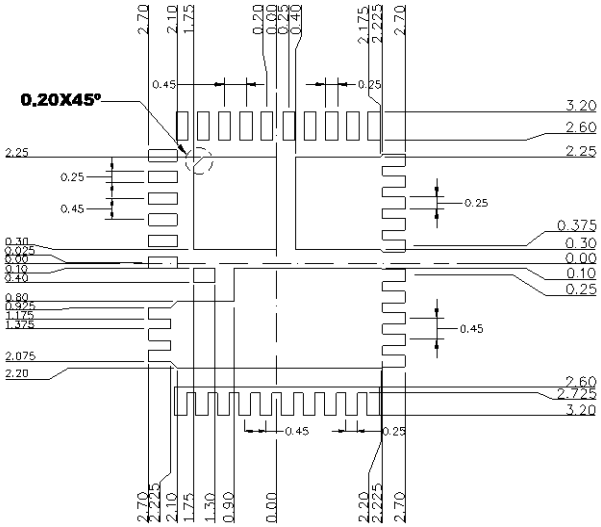
TOP VIEW



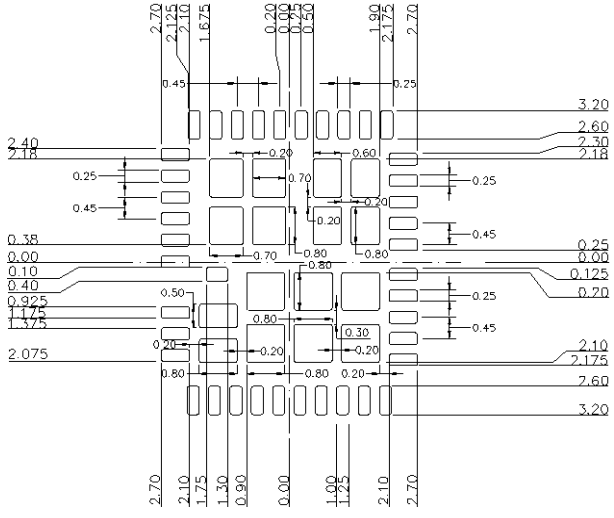
BOTTOM VIEW



SIDE VIEW



RECOMMENDED LAND PATTERN

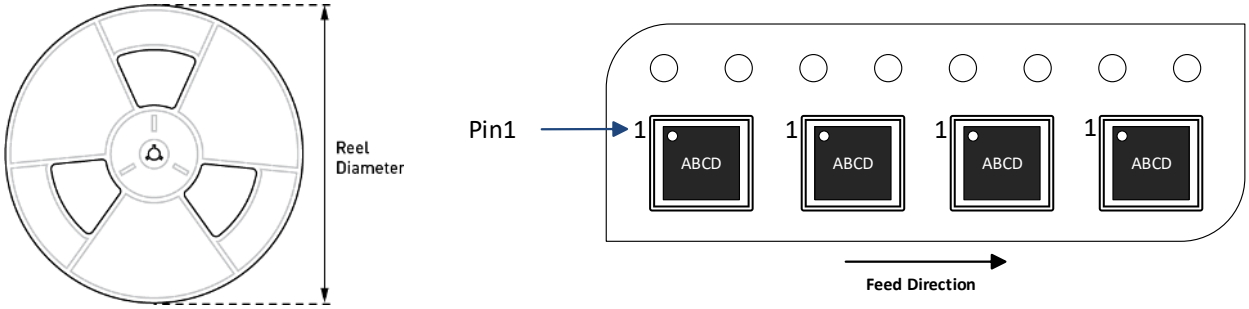


RECOMMENDED STENCIL DESIGN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS.
2) LEAD COPLANARITY SHALL BE 0.10 MILLIMETERS MAX.
3) JEDEC REFERENCE IS MO-303.
4) DRAWING IS NOT TO SCALE.

CARRIER INFORMATION



Part Number	Package Description	Quantity/ Reel	Quantity/ Tube	Quantity/ Tray	Reel Diameter	Carrier Tape Width	Carrier Tape Pitch
MP86952GMJ-Z	LGA-41 (5mmx6mm)	5000	N/A	N/A	13in	12mm	8mm

REVISION HISTORY

Revision #	Revision Date	Description	Pages Updated
1.0	5/13/2021	Initial Release	-