FAIRCHILD SEMICONDUCTOR®

SFR9230B / SFU9230B

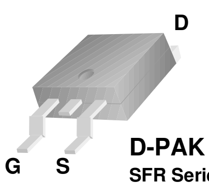
200V P-Channel MOSFET

General Description

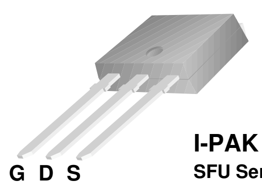
These P-Channel enhancement mode power field effect transistors are produced using Fairchild's proprietary, planar, DMOS technology.
This advanced technology has been especially tailored to minimize on-state resistance, provide superior switching performance, and withstand high energy pulse in the avalanche and commutation mode. These devices are well suited for high efficiency switching DC/DC converters.

Features

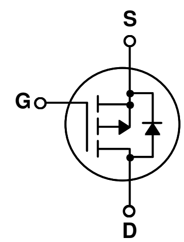
- -5.4A, -200V, $R_{DS(on)}$ = 0.8Ω @V_{GS} = -10 V
- Low gate charge (typical 33 nC)
- Low Crss (typical 45 pF)
- Fast switching
- 100% avalanche tested
- Improved dv/dt capability



D-PAK
SFR Series



I-PAK
SFU Series



Absolute Maximum Ratings

T_C = 25°C unless otherwise noted

Symbol	Parameter		SFR9230B / SFU9230B	Units
V_{DSS}	Drain-Source Voltage		-200	V
I_D	Drain Current - Continuous (T_C = 25°C)		-5.4	A
	- Continuous (T_C = 100°C)		-3.4	A
I_{DM}	Drain Current - Pulsed	(Note 1)	-22	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy	(Note 2)	390	mJ
I_{AR}	Avalanche Current	(Note 1)	-5.4	A
E_{AR}	Repetitive Avalanche Energy	(Note 1)	4.9	mJ
dv/dt	Peak Diode Recovery dv/dt	(Note 3)	-5.5	V/ns
P_D	Power Dissipation (T_A = 25°C) *		2.5	W
	Power Dissipation (T_C = 25°C)		49	W
	- Derate above 25°C		0.39	W/°C
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	°C
T_L	Maximum lead temperature for soldering purposes, 1/8" from case for 5 seconds		300	°C

Thermal Characteristics

Symbol	Parameter	Typ	Max	Units
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case	--	2.55	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient *	--	50	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient	--	110	°C/W

* When mounted on the minimum pad size recommended (PCB Mount)

Electrical Characteristics

T_C = 25°C unless otherwise noted

Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain-Source Breakdown Voltage	V_{GS} = 0 V, I_D = -250 µA	-200	--	--	V
ΔBV_{DSS} / ΔT_J	Breakdown Voltage Temperature Coefficient	I_D = -250 µA, Referenced to 25°C	--	-0.16	--	V/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -200 V, V_{GS} = 0 V	--	--	-1	µA
		V_{DS} = -160 V, T_C = 125°C	--	--	-10	µA
I_{GSSF}	Gate-Body Leakage Current, Forward	V_{GS} = -30 V, V_{DS} = 0 V	--	--	-100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	V_{GS} = 30 V, V_{DS} = 0 V	--	--	100	nA
On Characteristics						
$V_{GS(th)}$	Gate Threshold Voltage	V_{DS} = V_{GS}, I_D = -250 µA	-2.0	--	-4.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	V_{GS} = -10 V, I_D = -2.7 A	--	0.6	0.8	Ω
g_{FS}	Forward Transconductance	V_{DS} = -40 V, I_D = -2.7 A (Note 4)	--	5.9	--	S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -25 V, V_{GS} = 0 V, f = 1.0 MHz	--	775	1000	pF
C_{oss}	Output Capacitance		--	135	175	pF
C_{rss}	Reverse Transfer Capacitance		--	45	60	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -100 V, I_D = -6.5 A, R_G = 25 Ω (Note 4, 5)	--	10	30	ns
t_r	Turn-On Rise Time		--	30	70	ns
$t_{d(off)}$	Turn-Off Delay Time		--	120	250	ns
t_f	Turn-Off Fall Time		--	60	130	ns
Q_g	Total Gate Charge	V_{DS} = -160 V, I_D = -6.5 A, V_{GS} = -10 V (Note 4, 5)	--	33	45	nC
Q_{gs}	Gate-Source Charge		--	4.5	--	nC
Q_{gd}	Gate-Drain Charge		--	14.5	--	nC
Drain-Source Diode Characteristics and Maximum Ratings						
I_S	Maximum Continuous Drain-Source Diode Forward Current		--	--	-5.4	A
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current		--	--	-22	A
V_{SD}	Drain-Source Diode Forward Voltage	V_{GS} = 0 V, I_S = -5.4 A	--	--	-5.0	V
t_{rr}	Reverse Recovery Time	V_{GS} = 0 V, I_S = -6.5 A, dI_F / dt = 100 A/µs (Note 4)	--	160	--	ns
Q_{rr}	Reverse Recovery Charge		--	1.25	--	µC

Notes:
1. Repetitive Rating : Pulse width limited by maximum junction temperature
2. L = 20mH, I_{AS} = -5.4A, V_{DD} = -50V, R_G = 25 Ω, Starting T_J = 25°C
3. I_{SD} ≤ -6.5A, di/dt ≤ 400A/µs, V_{DD} ≤ $BV_{DSS,}$ Starting T_J = 25°C
4. Pulse Test : Pulse width ≤ 300µs, Duty cycle ≤ 2%
5. Essentially independent of operating temperature

Typical Characteristics

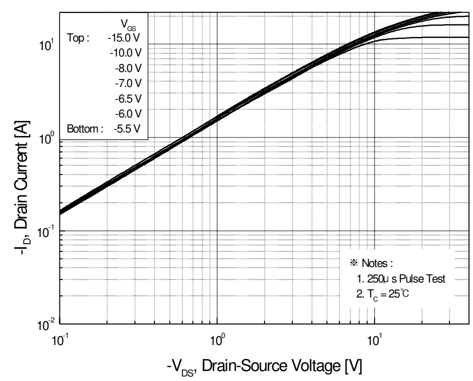


Figure 1. On-Region Characteristics

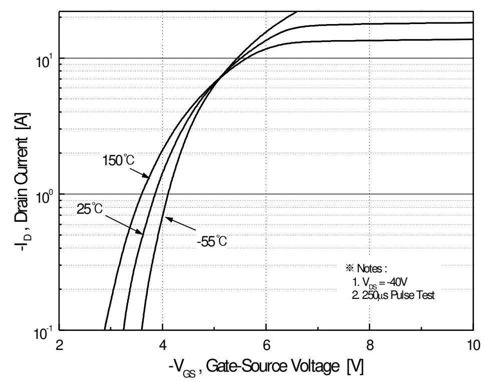


Figure 2. Transfer Characteristics

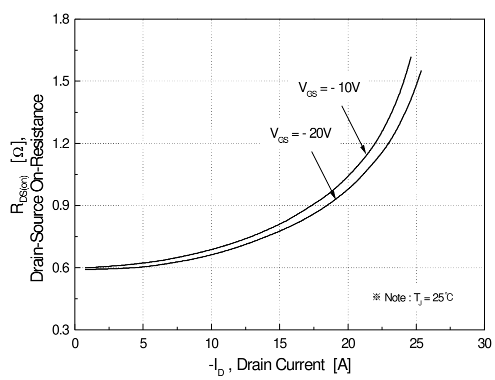


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

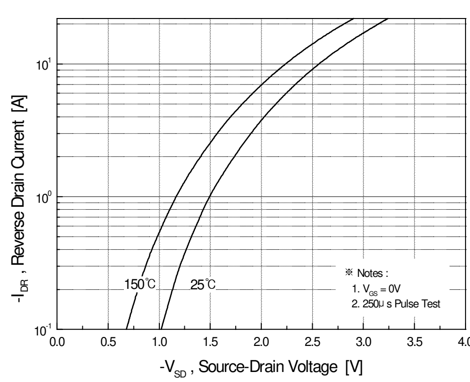


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

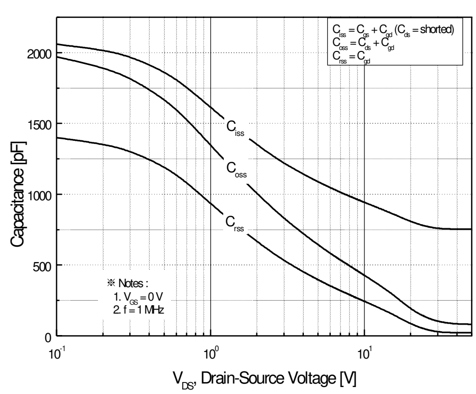


Figure 5. Capacitance Characteristics

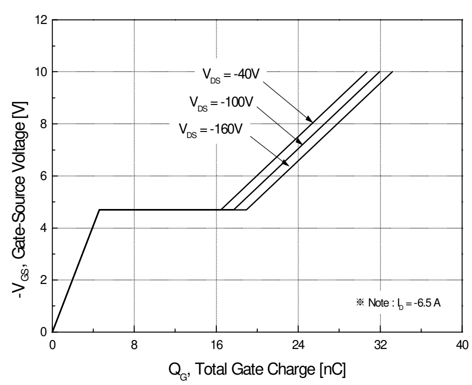


Figure 6. Gate Charge Characteristics

Typical Characteristics (Continued)

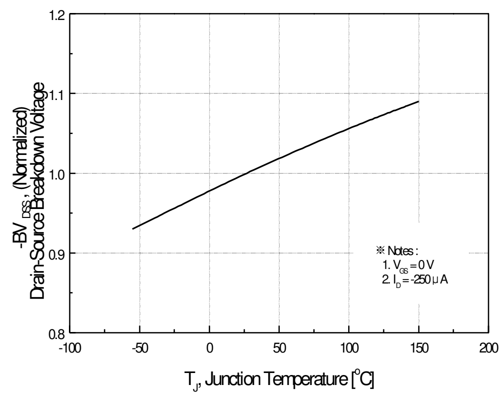


Figure 7. Breakdown Voltage Variation vs. Temperature

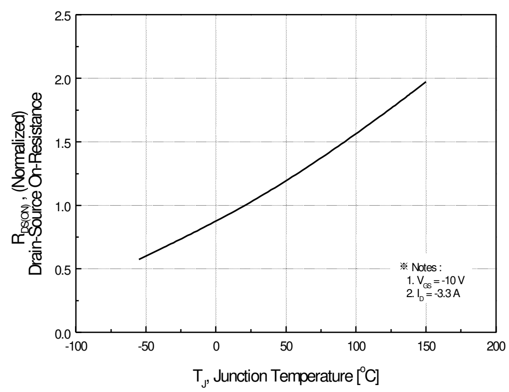


Figure 8. On-Resistance Variation vs. Temperature

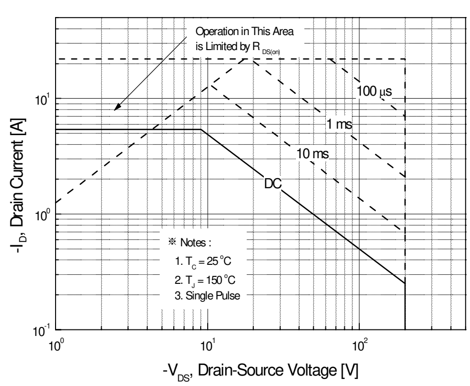


Figure 9. Maximum Safe Operating Area

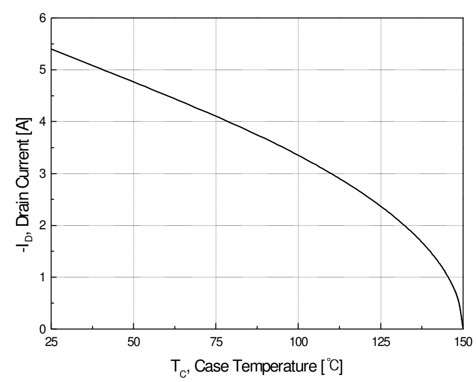


Figure 10. Maximum Drain Current vs. Case Temperature

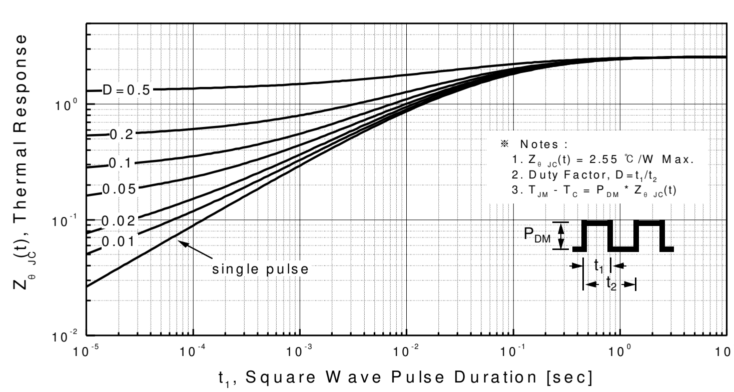
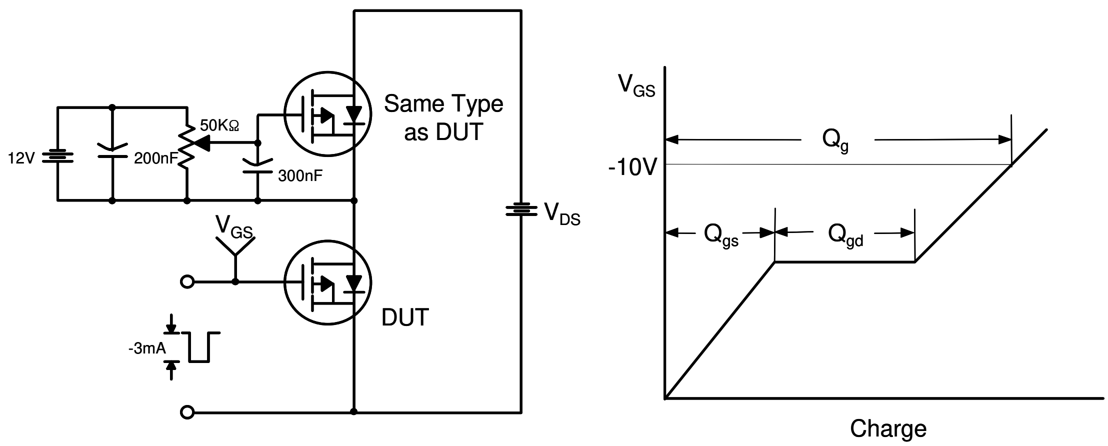
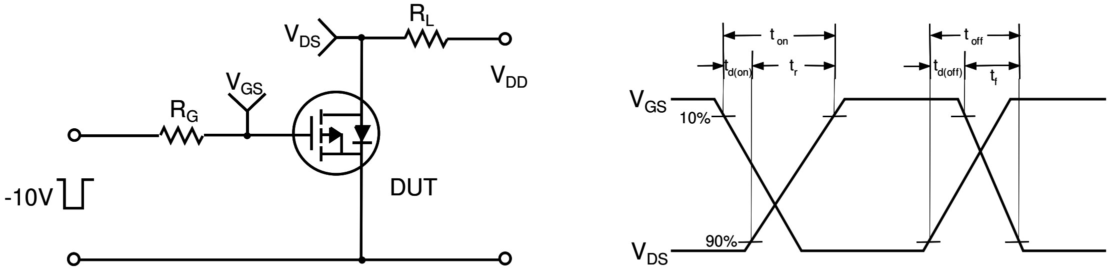


Figure 11. Transient Thermal Response Curve

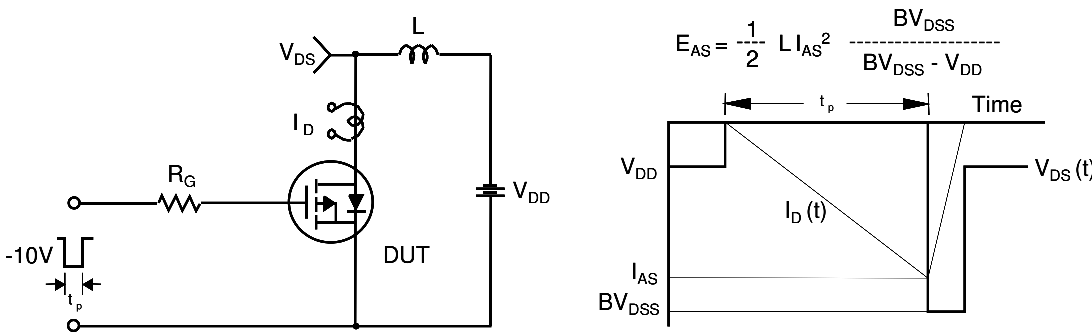
Gate Charge Test Circuit & Waveform



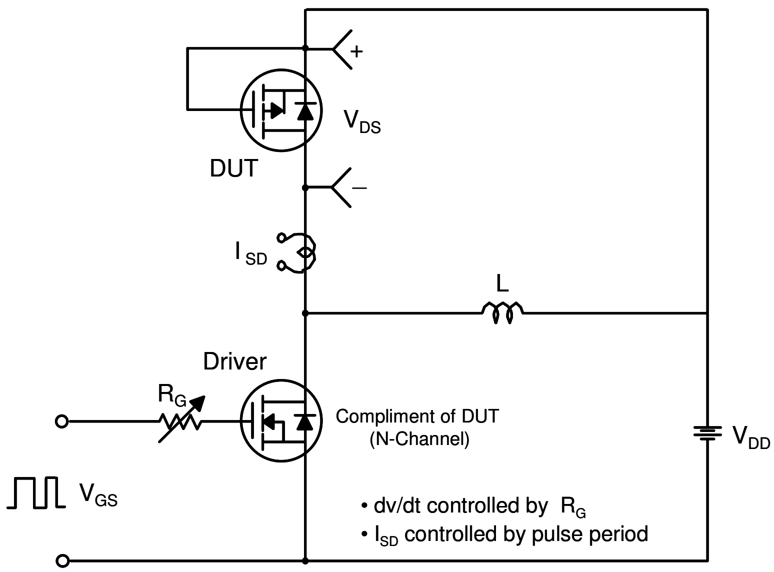
Resistive Switching Test Circuit & Waveforms

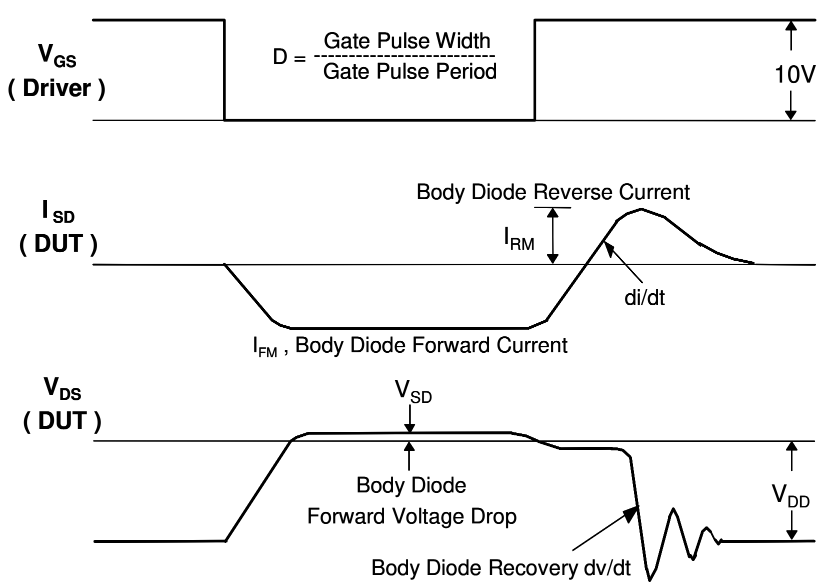


Unclamped Inductive Switching Test Circuit & Waveforms



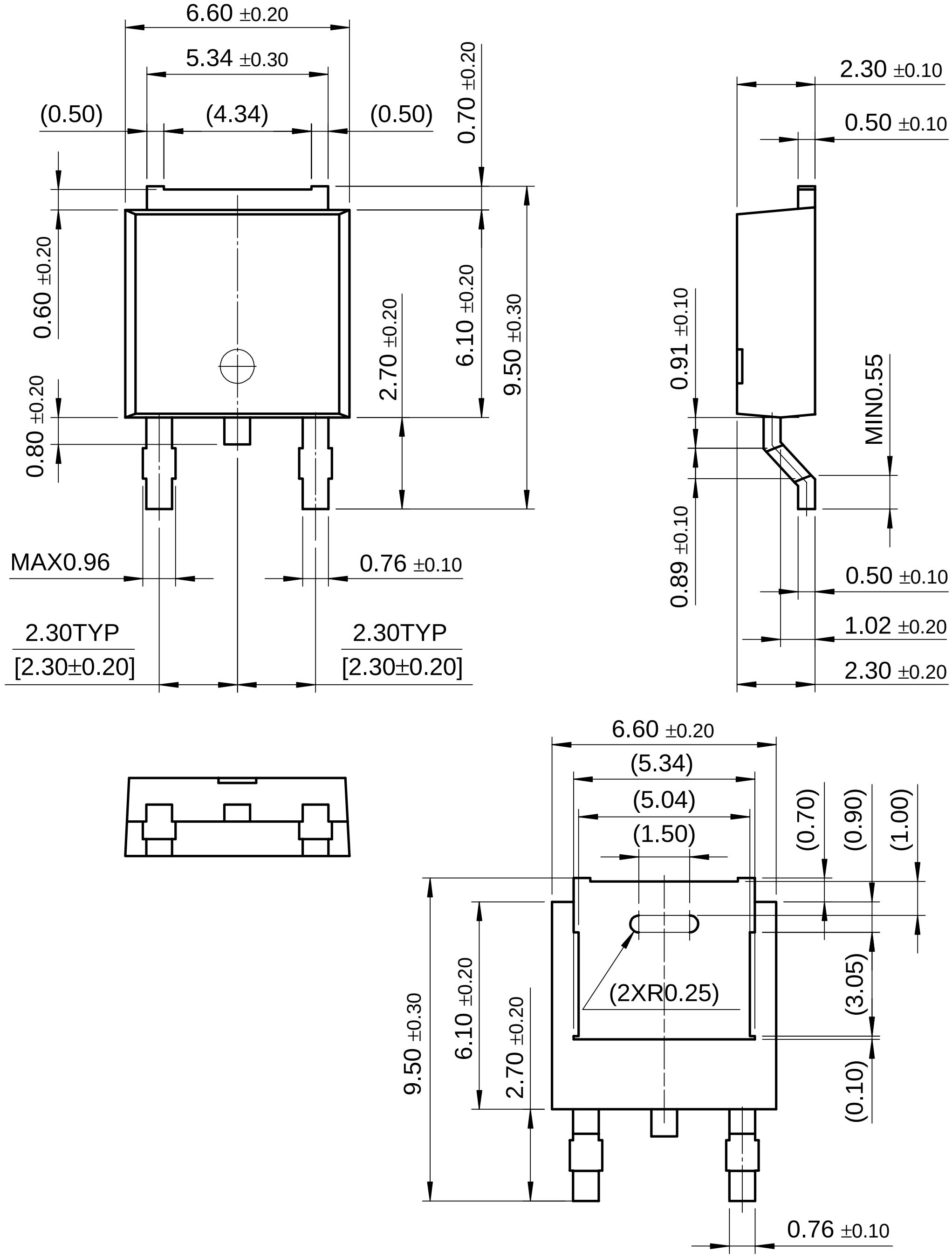
Peak Diode Recovery dv/dt Test Circuit & Waveforms





Package Dimensions

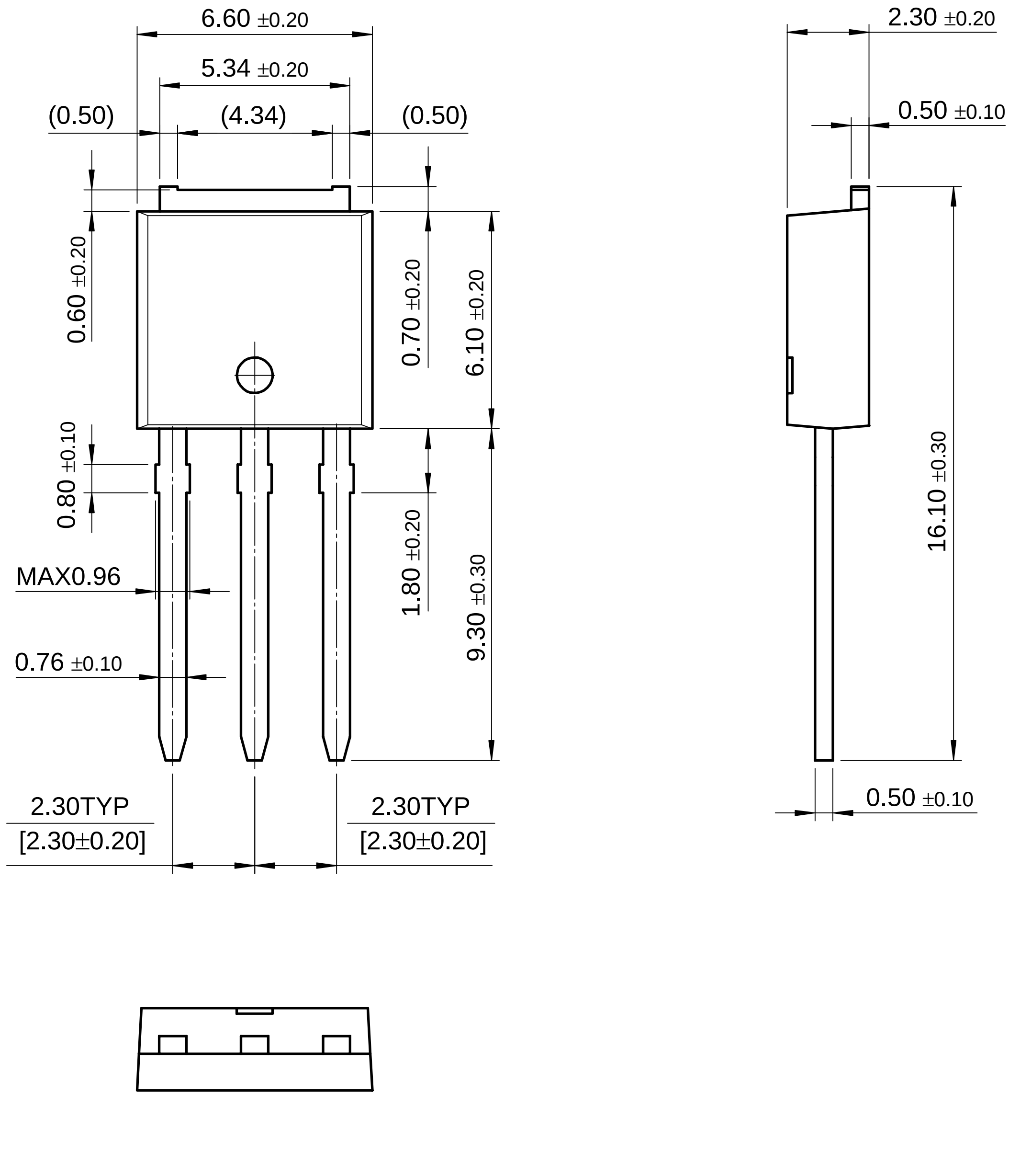
D-PAK



Dimensions in Millimeters

Package Dimensions (Continued)

I-PAK



Dimensions in Millimeters

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