MP38671

10A, 25V, 600KHz Step-Down Converter with Synchronizable Gate Driver

The Future of Analog IC Technology®

DESCRIPTION

The MP38671 is a monolithic step-down switch mode converter with a built in internal power MOSFET. It achieves 10A continuous output current over a wide input supply range with excellent load and line regulation.

Current mode operation provides fast transient response and eases loop stabilization.

Fault condition protection includes cycle-by-cycle current limiting and thermal shutdown.

The MP38671 requires a minimum number of readily available standard external components and is available in a space saving 3 x4mm 14-pin QFN package.

FEATURES

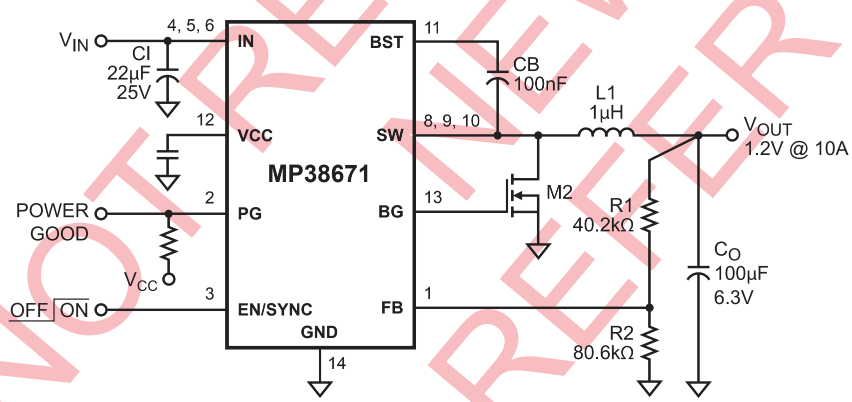
- Wide 4.5V to 25V Operating Input Range
- 10A Continuous Output Current
- 60mΩ Internal Power MOSFET Switch
- Power Good Indicator
- Synchronous Gate Driver Delivers up to 95% Efficiency
- Fixed 600KHz Frequency
- Synchronizable to >1MHz External Clock
- Cycle-by-Cycle Over Current Protection
- Thermal Shutdown
- Output Adjustable from 0.8V to 15V
- Stable with Low ESR Output Ceramic Capacitor
- Available in a 3x4mm 14-Pin QFN Package

APPLICATIONS

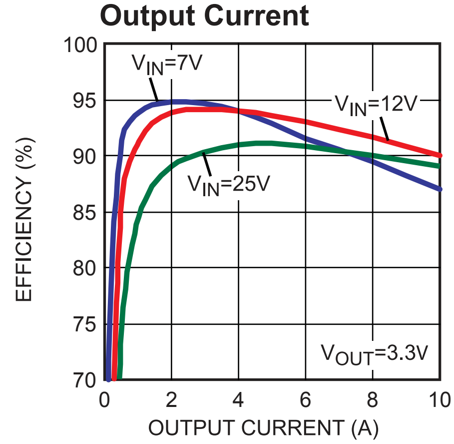
- Point of Load Regulator in Distributed Power System
- Digital Set Top Boxes
- Personal Video Recorders
- Broadband Communications
- Flat Panel Television and Monitors

For MPS green status, please visit MPS website under Quality Assurance.

TYPICAL APPLICATION



Efficiency vs. Output Current

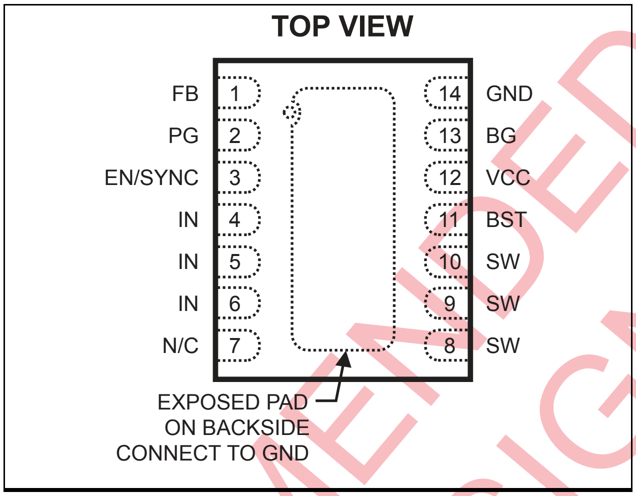


ORDERING INFORMATION

Part Number*	Package	Top Marking	Free Air Temperature (T_A)
MP38671DL	3x4 QFN14	3867	-40°C to +85°C

* For Tape & Reel, add suffix –Z (e.g. MP38671DL–Z);
For RoHS Compliant Packaging, add suffix –LF (e.g. MP MP38671DL–LF–Z)

PACKAGE REFERENCE



ABSOLUTE MAXIMUM RATINGS [1]

Supply Voltage VIN....................................28V
VSW .... -0.3V (-5V for < 10ns) to 29V
VBS .... VSW + 6V
All Other Pins................................ –0.3V to +6V
Junction Temperature..............................150°C
Lead Temperature ....260°C
Storage Temperature.............. –65°C to +150°C

Recommended Operating Conditions [3]

Supply Voltage VIN......................... 4.5V to 25V
Output Voltage VOUT .... 0.8V to 15V
Maximum Junction Temp. (T_J) .... +125°C

Thermal Resistance [4]

	θ_{JA}	θ_{JC}	
3x4 QFN14	48	11	°C/W

Notes:

1) Exceeding these ratings may damage the device.
2) The maximum allowable power dissipation is a function of the maximum junction temperature T_J(MAX), the junction-to-ambient thermal resistance θ_{JA}, and the ambient temperature T_A. The maximum allowable continuous power dissipation at any ambient temperature is calculated by $P_D(MAX)=(T_J(MAX)-T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown. Internal thermal shutdown circuitry protects the device from permanent damage.
3) The device is not guaranteed to function outside of its operating conditions.
4) Measured on JESD5 1-7, 4-layer PCB.. The exposed pad must be thermally connected to a ground plane (or most negative supply plane in split-supply applications).

ELECTRICAL CHARACTERISTICS

V_{IN} = 12V, T_A = +25°C, unless otherwise noted.

Parameters	Symbol	Condition	Min	Typ	Max	Units
Feedback Voltage	V_{FB}	4.5V ≤ V_{IN} ≤ 25V	0.788	0.808	0.828	V
Feedback Current	I_{FB}	V_{FB} = 0.8V		10		nA
Switch On Resistance (5)	$R_{DS(ON)}$			60		mΩ
Switch Leakage		V_{EN} = 0V, V_{SW} = 0V		0	10	μA
Current Limit (5)				12		A
Oscillator Frequency	f_{SW}	V_{FB} = 0.6V	400	600	800	KHz
Fold-back Frequency		V_{FB} = 0V		150		KHz
Maximum Duty Cycle		V_{FB} = 0.6V	85	90		%
Minimum On Time (5)	t_{ON}			100		ns
Under Voltage Lockout Threshold Rising			3.9	4.1	4.3	V
Under Voltage Lockout Threshold Hysteresis				880		mV
EN Input Low Voltage					0.4	V
En Input High Voltage			1.2			V
EN Input Current		V_{EN} = 2V		2		μA
		V_{EN} = 0V		0		
Supply Current (Shutdown)		V_{EN} = 0V		0	10	μA
Supply Current (Quiescent)		V_{EN} = 2V, V_{FB} = 1V			1.1	mA
Thermal Shutdown				150		°C
BG Driver Bias Supply Voltage	V_{CC}		4.5	5		V
Gate Driver Sink Impedance (5)	R_{SINK}			1		Ω
Gate Driver Source Impedance (5)	R_{SOURCE}			4		Ω
Gate Drive Current Sense Trip Threshold	V_{SW}			20		mV
Power Good Threshold			0.69	0.74	0.79	V
Power Good Threshold Hysteresis				40		mV
PG Pin Level	V_{PG}	PG Sink 4mA			0.4	V
Soft Start Time	T_{SS}		1	1.5	5	ms

Notes:
5) Guaranteed by design.

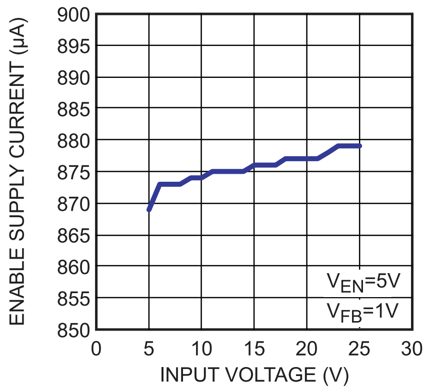
PIN FUNCTIONS

Pin #	Name	Description
1	FB	Feedback. An external resistor divider from the output to GND, tapped to the FB pin sets the output voltage. To prevent current limit run away during a short circuit fault condition the frequency foldback comparator lowers the oscillator frequency when the FB voltage is below 250mV.
2	PG	Power Good Indicator. **Connect this pin to V_{CC} or V_{OUT} by a 100kΩ pull-up resistor.** The output of this pin is low if the output voltage is 10% less than the nominal voltage, otherwise it is an open drain.
3	EN/SYNC	On/Off Control and External Frequency Synchronization Input.
4, 5, 6	IN	Supply Voltage. The MP38671 operates from a +4.5V to +25V unregulated input. C1 is needed to prevent large voltage spikes from appearing at the input.
7	N/C	No Connect.
8, 9, 10	SW	Switch Output.
11	BST	Bootstrap. This capacitor is needed to drive the power switch's gate above the supply voltage. It is connected between SW and BST pins to form a floating supply across the power switch driver.
12	VCC	BG Driver Bias Supply. Decouple with a 1µF ceramic capacitor.
13	BG	Gate Driver Output. Connect this pin to the synchronous MOSFET Gate.
14	GND, Exposed pad	Ground. This pin is the voltage reference for the regulated output voltage. For this reason care must be taken in its layout. This node should be placed outside of the M2 to C1 ground path to prevent switching current spikes from inducing voltage noise into the part. The exposed pad and GND pin must be connected to the same ground plane.

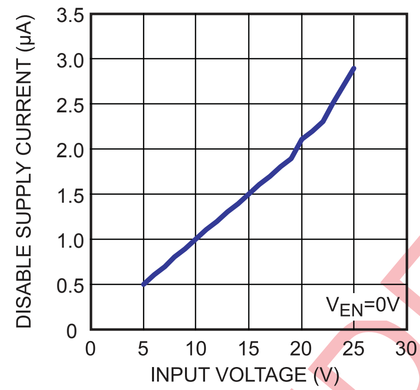
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = +26ºC, unless otherwise noted.

Enable Supply Current vs. Input Voltage

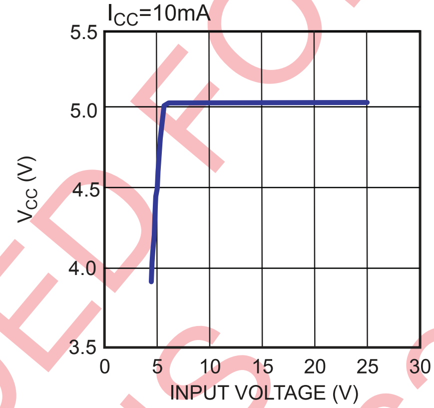


Disable Supply Current vs. Input Voltage

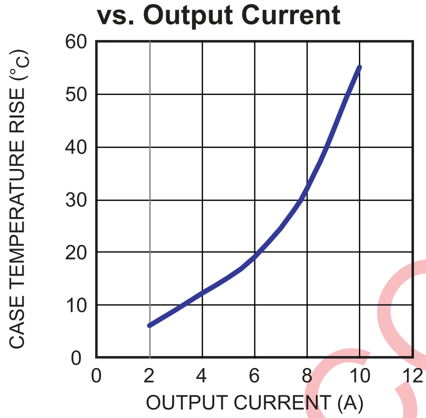


V_{CC} Regulator Line Regulation

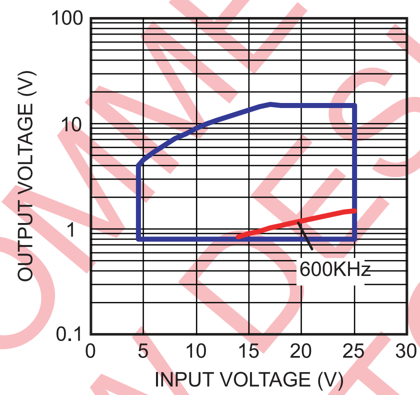
I_{CC}=10mA



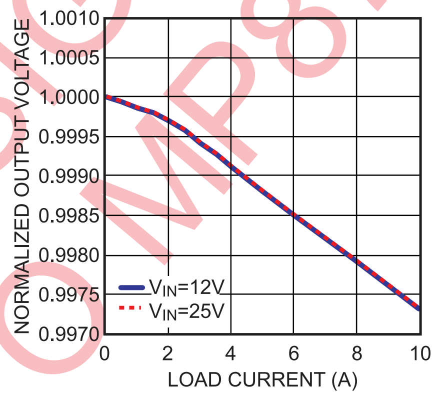
Case Temperature Rise vs. Output Current



Operating Range

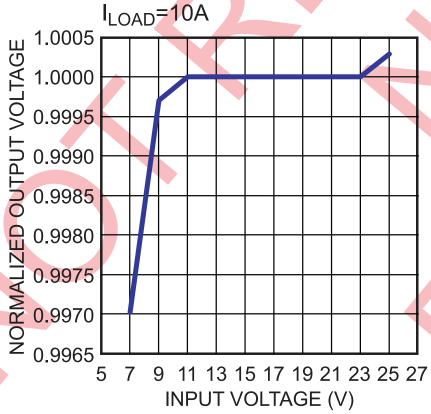


Load Regulation

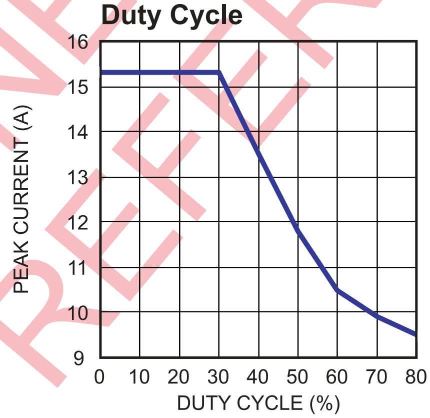


Line Regulation

I_{LOAD}=10A



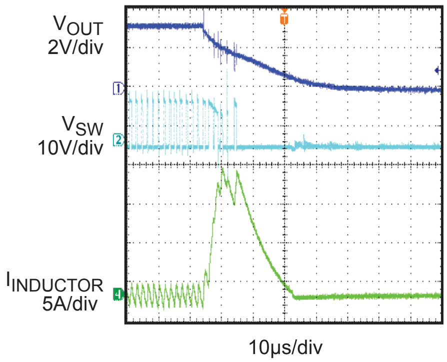
Peak Current vs. Duty Cycle



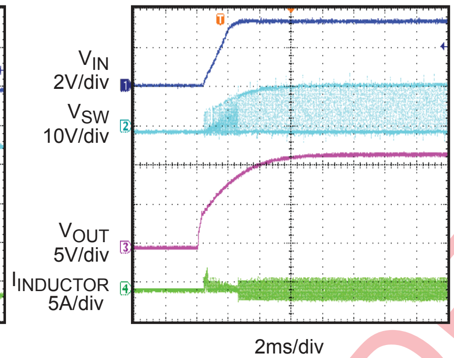
TYPICAL PERFORMANCE CHARACTERISTICS

V_{IN} = 12V, V_{OUT} = 3.3V, T_A = +26ºC, unless otherwise noted.

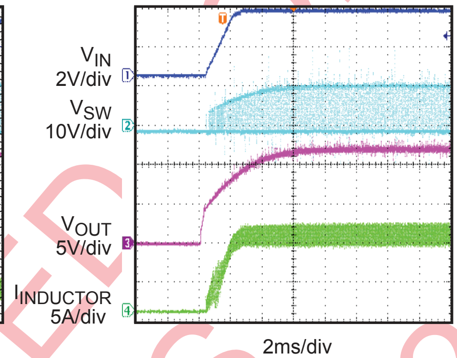
Latch Off with Output Short Circuit



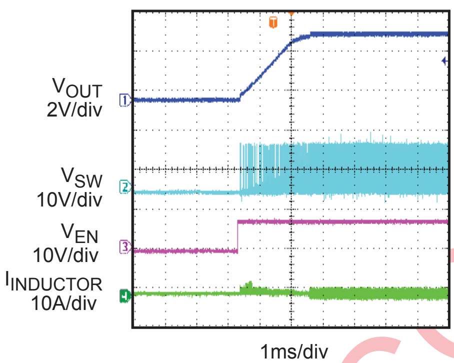
Power Up
No Load



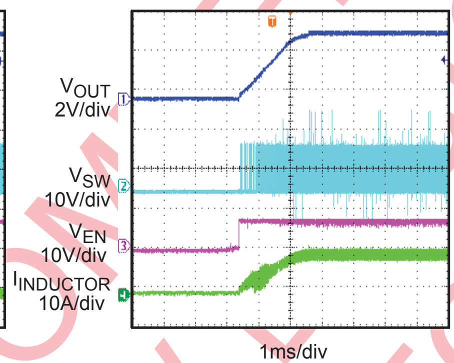
Power Up
Full Load



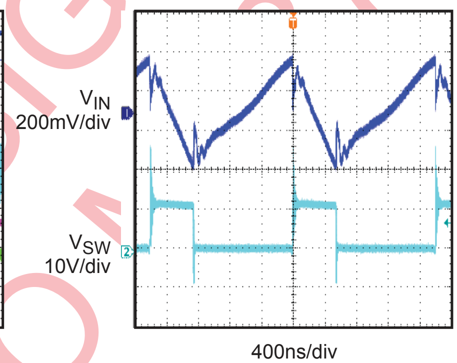
Enable Startup
No Load



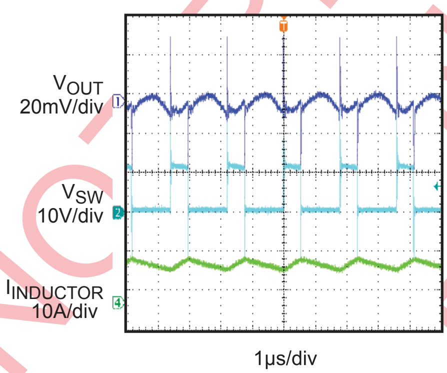
Enable Startup
Full Load



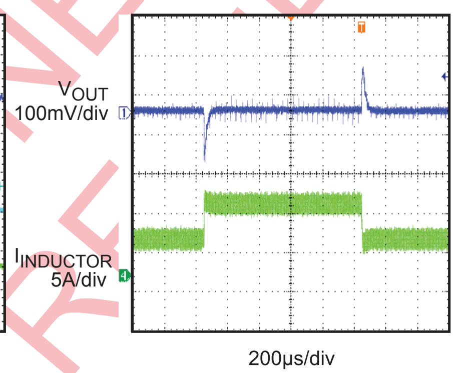
Input Ripple Voltage
I_{OUT}=10A



Output Ripple Voltage
I_{OUT}=10A



Load Transient Response



OPERATION

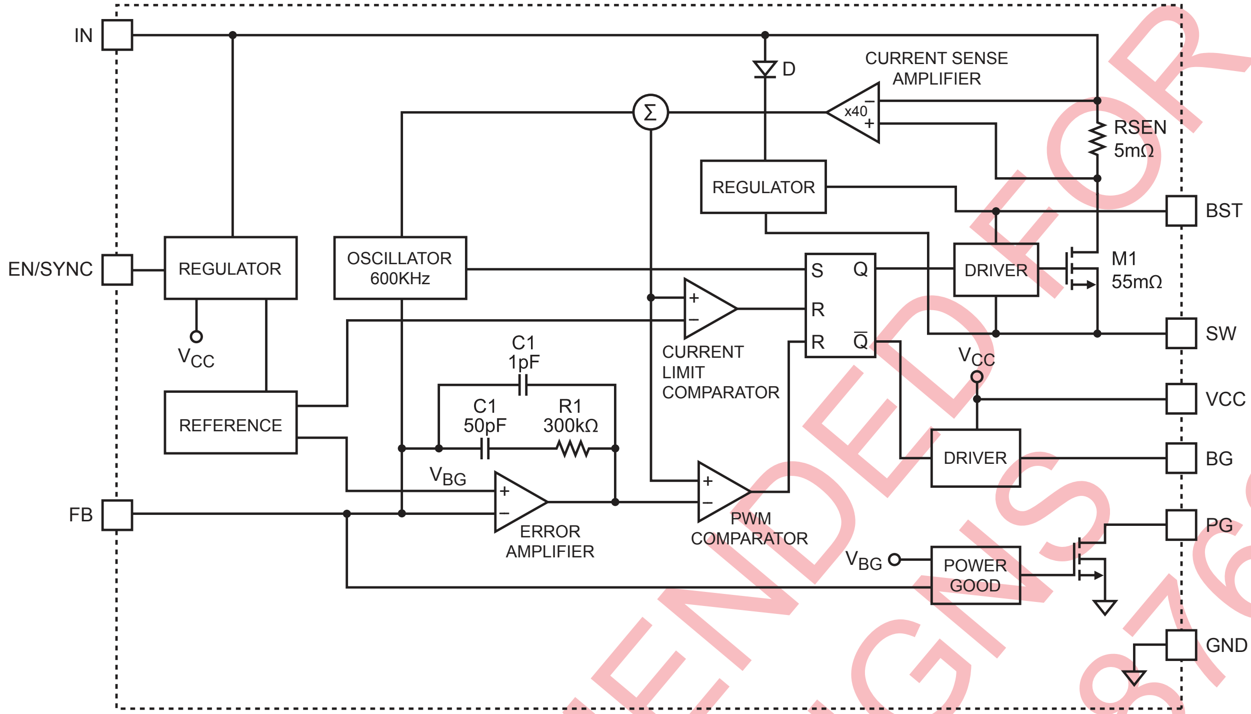


Figure 1—Functional Block Diagram

The MP38671 is a fixed frequency, synchronous, step-down switching regulator with an integrated high-side power MOSFET and a gate driver for a low-side external MOSFET. It achieves 10A continuous output current over a wide input supply range with excellent load and line regulation. It provides a single highly efficient solution with current mode control for fast loop response and easy compensation.

The MP38671 operates in a fixed frequency, peak current control mode to regulate the output voltage. A PWM cycle is initiated by the internal clock. The integrated high-side power MOSFET is turned on and remains on until its current reaches the value set by the COMP voltage. When the power switch is off, it remains off until the next clock cycle starts. If, in 90% of one PWM period, the current in the power MOSFET does not reach the COMP set current value, the power MOSFET will be forced to turn off.

Error Amplifier

The error amplifier compares the FB pin voltage with the internal 0.8V reference (REF) and outputs a current proportional to the difference between the two. This output current is then used to charge or discharge the internal compensation network to form the COMP voltage, which is used to control the power MOSFET current. The optimized internal compensation network minimizes the external component counts and simplifies the control loop design.

Internal Regulator

Most of the internal circuitries are powered from the 5V internal regulator. This regulator takes the VIN input and operates in the full VIN range. When VIN is greater than 5.0V, the output of the regulator is in full regulation. When VIN is lower than 5.0V, the output decreases. Since this internal regulator provides the bias current for the bottom gate driver that requires significant amount of current depending upon the external MOSFET selection, a 1uF ceramic capacitor for decoupling purpose is required.

Enable/Synch Control

The MP38671 has a dedicated Enable/Synch control pin (EN/SYNC). By pulling it high or low, the IC can be enabled and disabled by EN. Tie EN to VIN for automatic start up. To disable the part, EN must be pulled low for at least 5µs.

The MP38671 can be synchronized to external clock range from 300KHz up to 1.4MHz through the EN/SYNC pin. The internal clock rising edge is synchronized to the external clock rising edge.

Under-Voltage Lockout (UVLO)

Under-voltage lockout (UVLO) is implemented to protect the chip from operating at insufficient supply voltage. The MP38671 UVLO comparator monitors the output voltage of the internal regulator, VCC. The UVLO rising threshold is about 4.0V while its falling threshold is a consistent 3.2V.

Internal Soft-Start

The soft-start is implemented to prevent the converter output voltage from overshooting during startup. When the chip starts, the internal circuitry generates a soft-start voltage (SS) ramping up from 0V to 1.2V. When it is lower than the internal reference (REF), SS overrides REF so the error amplifier uses SS as the reference. When SS is higher than REF, REF regains control.

Over-Current-Protection (OCP)

The MP38671 has cycle-by-cycle over current limit when the inductor current peak value exceeds the set current limit threshold. Meanwhile, output voltage starts to drop until FB is below the Under-Voltage (UV) threshold, typically 30% below the reference. Once a output UV is triggered, the MP38671 enters latch off mode. Mode is especially useful to ensure system safety under fault condition. The MP38671 exits the latch off mode once the EN or input power is re-cycled.

Thermal Shutdown

Thermal shutdown is implemented to prevent the chip from operating at exceedingly high temperatures. When the silicon die temperature is higher than 150°C, it shuts down the whole chip. When the temperature is lower than its lower threshold, typically 140°C, the chip is enabled again.

Floating Driver and Bootstrap Charging

The floating power MOSFET driver is powered by an external bootstrap capacitor. This floating driver has its own UVLO protection. This UVLO's rising threshold is 2.2V with a hysteresis of 150mV. The bootstrap capacitor voltage is regulated internally (Figure 2). Even at no load condition, as long as V_{IN} is 3V higher than V_{OUT}, C4 will have enough voltage provided by V_{IN} through M2, M1, C4, L1 and C2. If (V_{IN}-V_{SW}) is more than 5V, U2 will regulate M1 to maintain a 5V BST voltage across C4.

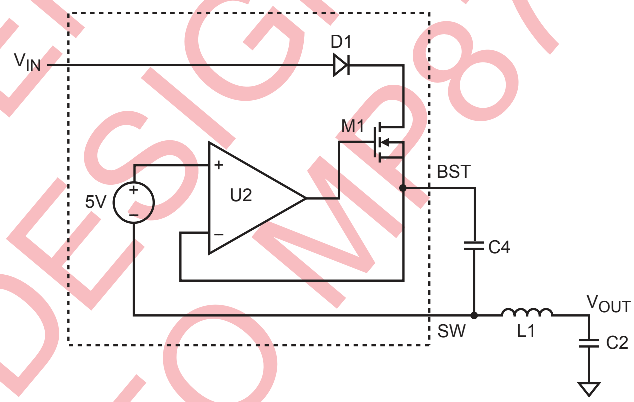


Figure 2—Internal Bootstrap Charging Circuit

Startup and Shutdown

If both VIN and EN are higher than their appropriate thresholds, the chip starts. The reference block starts first, generating stable reference voltage and currents, and then the internal regulator is enabled. The regulator provides stable supply for the remaining circuitries.

Four events can shut down the chip: OCP, EN low, VIN low and thermal shutdown. In the shutdown procedure, the signaling path is first blocked to avoid any fault triggering. The COMP voltage and the internal supply rail are then pulled down. The floating driver is not subject to this shutdown command.

APPLICATION INFORMATION

Setting the Output Voltage

The external resistor divider is used to set the output voltage (see the schematic on front page). The feedback resistor R1 also sets the feedback loop bandwidth with the internal compensation capacitor (see Figure 1). Choose R1 to be around 40.2kΩ for optimal transient response. R2 is then given by:

$$R2 = \frac{R1}{\frac{V_{OUT}}{0.8V} - 1}$$

Table 1—Resistor Selection for Common Output Voltages

V_{OUT} (V)	R1 (kΩ)	R2 (kΩ)
1.2	40.2 (1%)	80.6 (1%)
1.8	40.2 (1%)	32.4 (1%)
2.5	40.2 (1%)	19.1 (1%)

Selecting the Inductor

A 1µH to 10µH inductor with a DC current rating of at least 25% higher than the maximum load current is recommended for most applications. For highest efficiency, the inductor DC resistance should be less than 10mΩ. For most designs, the inductance value can be derived from the following equation.

$$L1 = \frac{V_{OUT} \times (V_{IN} - V_{OUT})}{V_{IN} \times \Delta I_L \times f_{OSC}}$$

Where ΔI_L is the inductor ripple current.

Choose inductor ripple current to be approximately 30% of the maximum load current, 10A. The maximum inductor peak current is:

$$I_{L(MAX)} = I_{LOAD} + \frac{\Delta I_L}{2}$$

Under light load conditions below 100mA, larger inductance is recommended for improving efficiency.

Synchronous MOSFET

The external synchronous MOSFET is used to freewheel the inductor current when the internal high-side switch is off. It reduces the power loss significantly compared against a Schottky rectifier.

Table 2 lists example synchronous MOSFETs and manufacturers.

Table 2—Synchronous MOSFET Selection Guide

Part No.	Manufacture
Si7114	Vishay
HAT2165	Renesas

Selecting the Input Capacitor

The input current to the step-down converter is discontinuous, therefore a capacitor is required to supply the AC current to the step-down converter while maintaining the DC input voltage. Use low ESR capacitors for the best performance. Ceramic capacitors with X5R or X7R dielectrics are highly recommended because of their low ESR and small temperature coefficients. For most applications, a 22µF capacitor is sufficient.

Since the input capacitor (C1) absorbs the input switching current it requires an adequate ripple current rating. The RMS current in the input capacitor can be estimated by:

$$I_{C1} = I_{LOAD} \times \sqrt{\frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)}$$

The worse case condition occurs at $V_{IN} = 2V_{OUT}$, where:

$$I_{C1} = \frac{I_{LOAD}}{2}$$

For simplification, choose the input capacitor whose RMS current rating greater than half of the maximum load current.

The input capacitor can be electrolytic, tantalum or ceramic. When using electrolytic or tantalum capacitors, a small, high quality ceramic capacitor, i.e. 0.1μF, should be placed as close to the IC as possible. When using ceramic capacitors, make sure that they have enough capacitance to provide sufficient charge to prevent excessive voltage ripple at input. The input voltage ripple caused by capacitance can be estimated by:

$$\Delta V_{IN} = \frac{I_{LOAD}}{f_S \times C1} \times \frac{V_{OUT}}{V_{IN}} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

Selecting the Output Capacitor

The output capacitor (C2) is required to maintain the DC output voltage. Ceramic, tantalum, or low ESR electrolytic capacitors are recommended. Low ESR capacitors are preferred to keep the output voltage ripple low. The output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times \left(R_{ESR} + \frac{1}{8 \times f_S \times C2}\right)$$

Where L1 is the inductor value and R_{ESR} is the equivalent series resistance (ESR) value of the output capacitor.

In the case of ceramic capacitors, the impedance at the switching frequency is dominated by the capacitance. The output voltage ripple is mainly caused by the capacitance. For simplification, the output voltage ripple can be estimated by:

$$\Delta V_{OUT} = \frac{V_{OUT}}{8 \times f_S^{\,2} \times L1 \times C2} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right)$$

In the case of tantalum or electrolytic capacitors, the ESR dominates the impedance at the switching frequency. For simplification, the output ripple can be approximated to:

$$\Delta V_{OUT} = \frac{V_{OUT}}{f_S \times L1} \times \left(1 - \frac{V_{OUT}}{V_{IN}}\right) \times R_{ESR}$$

The characteristics of the output capacitor also affect the stability of the regulation system. The MP38671 can be optimized for a wide range of capacitance and ESR values.

PCB Layout

The high current paths (GND, IN and SW) should be placed very close to the device with short, direct and wide traces. The input capacitor needs to be as close as possible to the IN and GND pins. The external feedback resistors should be placed next to the FB pin. Keep the switching node SW short and away from the feedback network.

External Bootstrap Diode

An external bootstrap diode may enhance the efficiency of the regulator, the applicable conditions of external BST diode are:

- V_{OUT}=5V or 3.3V; and
- Duty cycle is high: $D=\frac{V_{OUT}}{V_{IN}}>65\%$

In these cases, an external BST diode is recommended from the output of the voltage regulator to BST pin, as shown in Figure 3

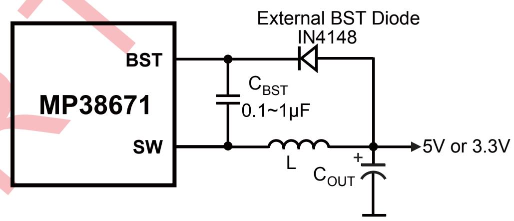
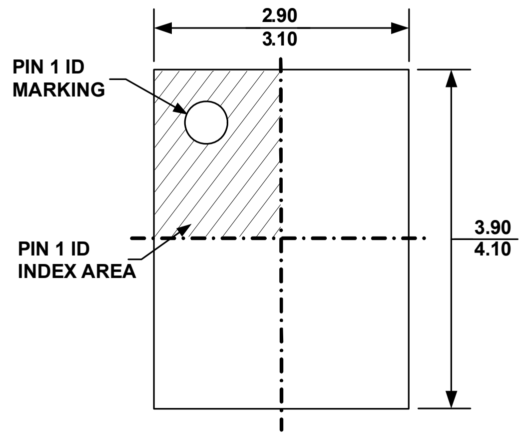


Figure 3—Add Optional External Bootstrap Diode to Enhance Efficiency

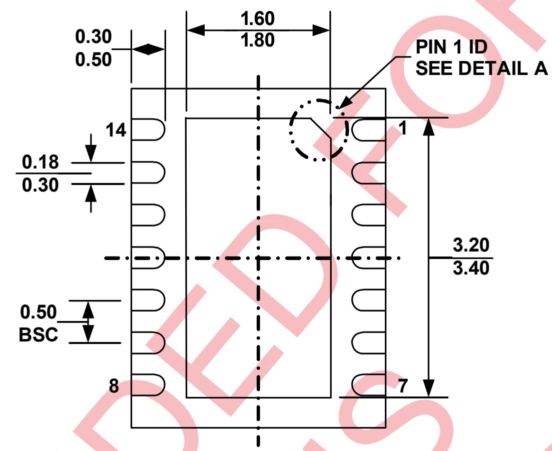
The recommended external BST diode is IN4148, and the BST cap is 0.1~1μF.

PACKAGE INFORMATION

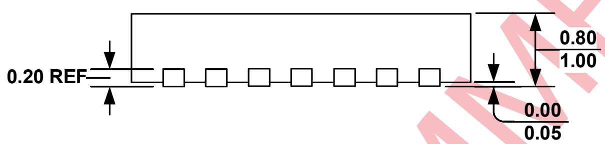
3mm x 4mm QFN14



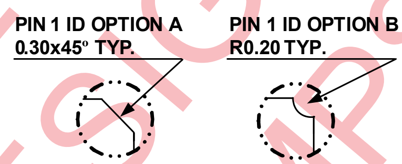
TOP VIEW



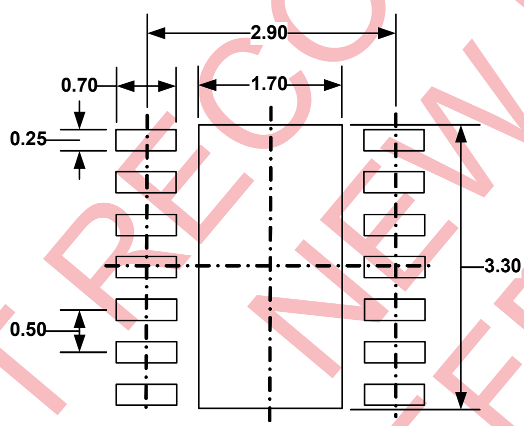
BOTTOM VIEW



SIDE VIEW



DETAIL A



RECOMMENDED LAND PATTERN

NOTE:

1) ALL DIMENSIONS ARE IN MILLIMETERS
2) EXPOSED PADDLE SIZE DOES NOT INCLUDE MOLD FLASH
3) LEAD COPLANARITY SHALL BE0.10 MILLIMETER MAX
4) JEDEC REFERENCE IS MO-229, VARIATION VGED-3.
5) DRAWING IS NOT TO SCALE

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