

DDR2 SDRAM Mini-RDIMM

MT5HTF3272(P)K – 256MB

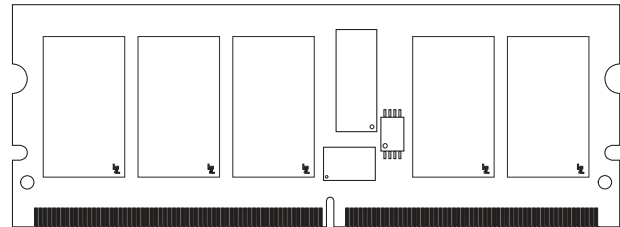
For component data sheets, refer to Micron's Web site: www.micron.com

Features

- 244-pin, mini-registered dual in-line memory module (mini-RDIMM)
- Fast data transfer rates: PC-3200, PC2-4200, or PC2-5300
- Supports ECC error detection and correction
- 256MB (32 Meg x 72)
- $V_{DD} = V_{DDQ} = +1.8V$
- $V_{DDSPD} = +1.7V$ to $+3.6V$
- JEDEC-standard 1.8V I/O (SSTL_18-compatible)
- Differential data strobe (DQS, DQS#) option
- 4n-bit prefetch architecture
- Single rank
- Multiple internal device banks for concurrent operation
- Supports duplicate output strobe (RDQS/RDQS#)
- Programmable CAS# latency (CL)
- Posted CAS# additive latency (AL)
- WRITE latency = READ latency - 1 t_{CK}
- Programmable burst lengths: 4 or 8
- Adjustable data-output drive strength
- 64ms, 8,192-cycle refresh
- On-die termination (ODT)
- Serial presence-detect (SPD) with EEPROM
- Gold edge contacts

Figure 1: 244-Pin Mini-RDIMM (MO-244 R/C B)

Module height: 30.0mm (1.18in)



Options

- Parity
- Operating temperature¹
 - Commercial ($0^{\circ}C \leq T_A \leq +70^{\circ}C$)
 - Industrial ($-40^{\circ}C \leq T_A \leq +85^{\circ}C$)
- Package
 - 244-pin mini-RDIMM (Pb-free)
- Frequency/CAS latency²
 - 3.0ns @ CL = 5 (DDR2-667)
 - 3.75ns @ CL = 4 (DDR2-533)
 - 5.0ns @ CL = 3 (DDR2-400)
- PCB height
 - 30mm (1.18in)

Marking

- P
- None
- I
- Y
- 667
- 53E
- 40E

Notes: 1. Contact Micron for industrial temperature module offerings.

2. CL = CAS (READ) latency; registered mode will add one clock cycle to CL.

Table 1: Key Timing Parameters

Speed Grade	Industry Nomenclature	Data Rate (MT/s)			t_{RCD} (ns)	t_{RP} (ns)	t_{RC} (ns)
		CL = 5	CL = 4	CL = 3			
-667	PC2-5300	667	533	400	15	15	55
-53E	PC2-4200	–	533	400	15	15	55
-40E	PC2-3200	–	400	400	15	15	55

Table 2: Addressing

	256MB
Refresh count	8K
Row addressing	8K (A0–A12)
Device bank addressing	4 (BA0, BA1)
Device page size per bank	1KB
Device configuration	512Mb (32 Meg x 16)
Column addressing	1K (A0–A9)
Module rank addressing	1 (S0#)

Table 3: Part Numbers and Timing Parameters – 256MB

 Base device: MT47H32M16¹, 512Mb DDR2 SDRAM

Part Number ²	Module Density	Configuration	Module Bandwidth	Memory Clock/ Data Rate	Latency (CL ^t -RCD ^t -RP)
MT5HTF3272(P)KY-667__	256MB	32 Meg x 72	5.3 GB/s	3.0ns/667 MT/s	5-5-5
MT5HTF3272(P)KY-53E__	256MB	32 Meg x 72	4.3 GB/s	3.75ns/533 MT/s	4-4-4
MT5HTF3272(P)KY-40E__	256MB	32 Meg x 72	3.2 GB/s	5.0ns/400 MT/s	3-3-3

- Notes:
1. Data sheets for the base devices can be found on Micron's Web site.
 2. All part numbers end with a two-place code (not shown), designating component and PCB revisions. Consult factory for current revision codes. Example: MT5HTF3272KY-40ED1.



Pin Assignments and Descriptions

Table 4: Pin Assignments

244-Pin Mini-RDIMM Front								244-Pin Mini-RDIMM Back							
Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol	Pin	Symbol		
1	VREF	32	Vss	63	VDDQ	94	DQS5#	123	Vss	154	DQ28	185	A3	216	NC
2	Vss	33	DQ24	64	A2	95	DQS5	124	DQ4	155	DQ29	186	A1	217	Vss
3	DQ0	34	DQ25	65	VDD	96	Vss	125	DQ5	156	Vss	187	VDD	218	DQ46
4	DQ1	35	Vss	66	Vss	97	DQ42	126	Vss	157	DM3	188	CK0	219	DQ47
5	Vss	36	DQS3#	67	Vss	98	DQ43	127	DM0	158	NC	189	CK0#	220	Vss
6	DQS0#	37	DQS3	68 ²	NC/ PAR_IN	99	Vss	128	NC	159	Vss	190	VDD	221	DQ52
7	DQS0	38	Vss	69	VDD	100	DQ48	129	Vss	160	DQ30	191	A0	222	DQ53
8	Vss	39	DQ26	70	A10	101	DQ49	130	DQ6	161	DQ31	192	BA1	223	Vss
9	DQ2	40	DQ27	71	BA0	102	Vss	131	DQ7	162	Vss	193	VDD	224	RFU
10	DQ3	41	Vss	72	VDD	103	SA2	132	Vss	163	CB4	194	RAS#	225	RFU
11	Vss	42	CB0	73	WE#	104	NC	133	DQ12	164	CB5	195	VDDQ	226	Vss
12	DQ8	43	CB1	74	VDDQ	105	Vss	134	DQ13	165	Vss	196	S0#	227	DM6
13	DQ9	44	Vss	75	CAS#	106	DQS6#	135	Vss	166	DM8	197	VDDQ	228	NC
14	Vss	45	DQS8#	76	VDDQ	107	DQS6	136	DM1	167	NC	198	ODT0	229	Vss
15	DQS1#	46	DQS8	77	NC	108	Vss	137	NC	168	Vss	199	NC	230	DQ54
16	DQS1	47	Vss	78	NC	109	DQ50	138	Vss	169	CB6	200	VDD	231	DQ55
17	Vss	48	CB2	79	VDDQ	110	DQ51	139	RFU	170	CB7	201	NC	232	Vss
18	RESET#	49	CB3	80	NC	111	Vss	140	RFU	171	Vss	202	Vss	233	DQ60
19	NC	50	Vss	81	Vss	112	DQ56	141	Vss	172	NC	203	DQ36	234	DQ61
20	Vss	51	NC	82	DQ32	113	DQ57	142	DQ14	173	VDDQ	204	DQ37	235	Vss
21	DQ10	52	VDDQ	83	DQ33	114	Vss	143	DQ15	174	NC	205	Vss	236	DM7
22	DQ11	53	CKE0	84	Vss	115	DQS7#	144	Vss	175	VDD	206	DM4	237	NC
23	Vss	54	VDD	85	DQS4#	116	DQS7	145	DQ20	176	NC	207	NC	238	Vss
24	DQ16	55	NC	86	DQS4	117	Vss	146	DQ21	177	NC	208	Vss	239	DQ62
25	DQ17	56 ¹	NC/ ERR_OUT	87	Vss	118	DQ58	147	Vss	178	VDDQ	209	DQ38	240	DQ63
26	Vss	57	VDDQ	88	DQ34	119	DQ59	148	DM2	179	A12	210	DQ39	241	Vss
27	DQS2#	58	A11	89	DQ35	120	Vss	149	NC	180	A9	211	Vss	242	SDA
28	DQS2	59	A7	90	Vss	121	SA0	150	Vss	181	VDD	212	DQ44	243	SCL
29	Vss	60	VDD	91	DQ40	122	SA1	151	DQ22	182	A8	213	DQ45	244	VDDSPD
30	DQ18	61	A5	92	DQ41			152	DQ23	183	A6	214	Vss		
31	DQ19	62	A4	93	Vss			153	Vss	184	VDDQ	215	DM5		

- Notes: 1. Pin 56 is NC for non-parity and ERR_OUT and parity.
2. Pin 68 is NC for non-parity and PAR_IN for parity.

Table 5: Pin Descriptions

Symbol	Type	Description
ODT0	Input (SSTL_18)	On-die termination: ODT (registered HIGH) enables termination resistance internal to the DDR2 SDRAM. When enabled, ODT is only applied to each of the following pins: DQ, DQS, DQS#, RDQS, RDQS#, CB, and DM. The ODT input will be ignored if disabled via the LOAD MODE (LM) command.
CK0, CK0#	Input (SSTL_18)	Clock: CK and CK# are differential clock inputs. All address and control input signals are sampled on the crossing of the positive edge of CK and negative edge of CK#. Output data (DQs and DQS/DQS#) is referenced to the crossings of CK and CK#.
CKE0	Input (SSTL_18)	Clock enable: CKE (registered HIGH) activates and CKE (registered LOW) deactivates clocking circuitry on the DDR2 SDRAM.
S0#	Input (SSTL_18)	Chip select: S# enables (registered LOW) and disables (registered HIGH) the command decoder. All commands are masked when S# is registered HIGH. S# provides for external rank selection on systems with multiple ranks. S# is considered part of the command code.
RAS#, CAS#, WE#	Input (SSTL_18)	Command inputs: RAS#, CAS#, and WE# (along with S#) define the command being entered.
BA0, BA1	Input (SSTL_18)	Bank address inputs: BA0–BA1 define to which device bank an ACTIVE, READ, WRITE, or PRECHARGE command is being applied. BA0–BA1 define which mode register, including MR, EMR, EMR(2), or EMR(3), is loaded during the LM command.
A0–A12	Input (SSTL_18)	Address inputs: Provide the row address for ACTIVE commands and the column address and auto precharge bit (A10) for READ/WRITE commands to select one location out of the memory array in the respective bank. A10 sampled during a PRECHARGE command determines whether the PRECHARGE applies to one device bank (A10 LOW, device bank selected by BA0–BA1) or all device banks (A10 HIGH). The address inputs also provide the op-code during an LM command.
PAR_IN	Input (SSTL_18)	Parity bit for the address and control bus.
SCL	Input (SSTL_18)	Serial clock for presence-detect: SCL is used to synchronize the presence-detect data transfer to and from the module.
SA0–SA2	Input (SSTL_18)	Presence-detect address inputs: These pins are used to configure the presence-detect device.
RESET#	Input (SSTL_18)	Asynchronously forces all registered outputs LOW when RESET# is LOW. This signal can be used during power-up to ensure that CKE is LOW and DQs are High-Z.
DQ0–DQ63	I/O (SSTL_18)	Data input/output: Bidirectional data bus.
DQS0–DQS8, DQS0#–DQS8#	I/O (SSTL_18)	Data strobe: Output with read data, input with write data for source synchronous operation. Edge-aligned with read data, center-aligned with write data. DQS# is only used when differential data strobe mode is enabled via the LM command. DQS9#–DQS17# are only used when RDQS# is enabled via the LM command.
DM0–DM8	I/O (SSTL_18)	Input data mask: DM is an input mask signal for write data. Input data is masked when DM is sampled HIGH along with that input data during a WRITE access. DM is sampled on both edges of DQS. Although DM pins are input-only, the DM loading is designed to match that of DQ and DQS pins. If RDQS is enabled, DQS9#–DQS17# are used only during the READ command.
CB0–CB7	I/O (SSTL_18)	Check bits.
SDA	I/O (SSTL_18)	Serial presence-detect data: SDA is a bidirectional pin used to transfer addresses and data into and out of the presence-detect portion of the module.
ERR_OUT	Output (open drain)	Parity error found on the address and control bus.
VDD/VDDQ	Supply	Power supply: 1.8V ±0.1V.
VREF	Supply	SSTL_18 reference voltage.

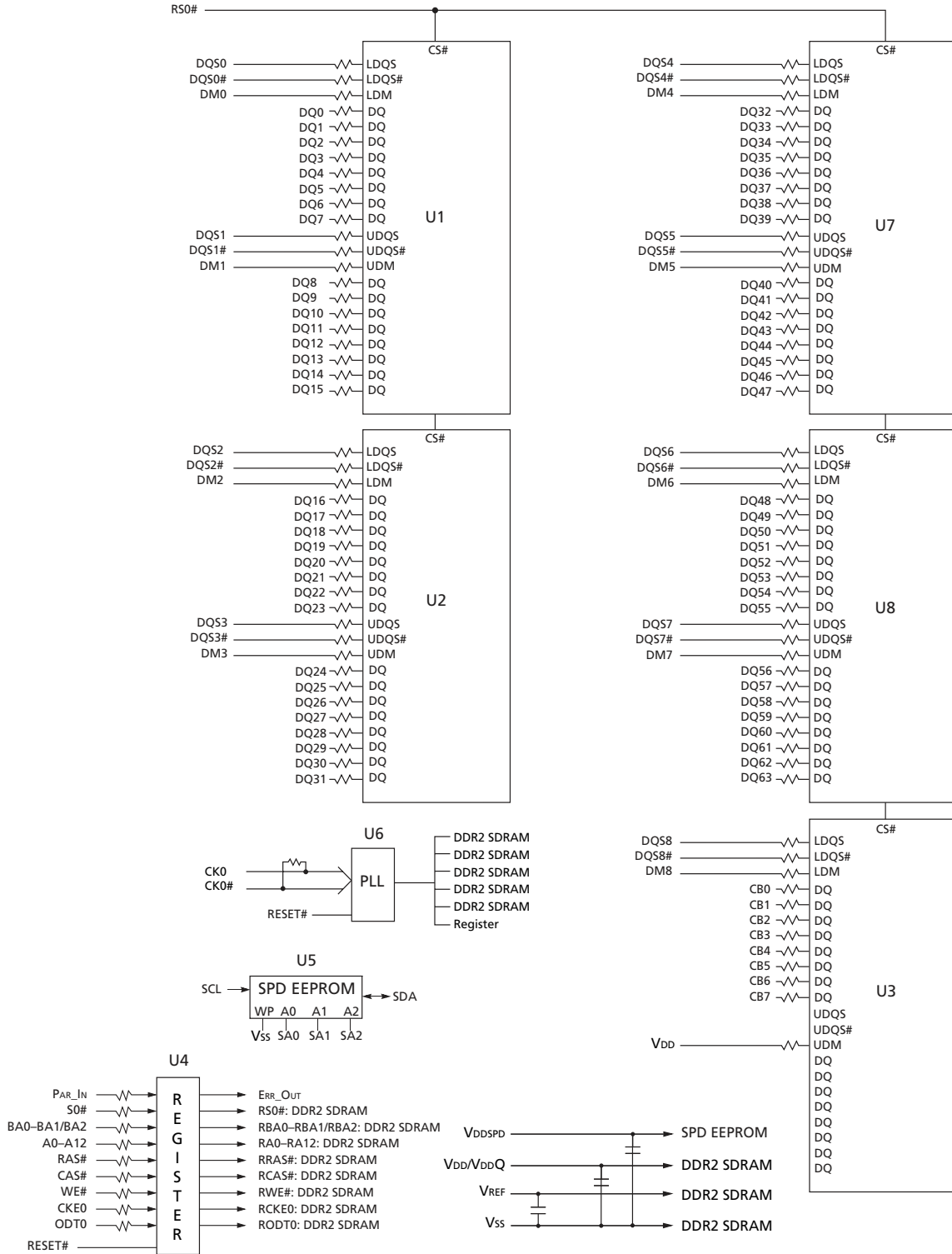


Table 5: Pin Descriptions (continued)

Symbol	Type	Description
Vss	Supply	Ground.
VDDSPD	Supply	Serial EEPROM positive power supply: +1.7V to +3.6V.
NC	–	No connect: These pins should be left unconnected.
RFU	–	Reserved for future use.

Functional Block Diagram

Figure 2: Functional Block Diagram



General Description

The MT5HTF3272(P)K DDR2 SDRAM module is a high-speed, CMOS, dynamic random-access 256MB memory module organized in a x72 configuration. This DDR2 SDRAM module uses an internally configured 4-bank (512Mb) DDR2 SDRAM device.

DDR2 SDRAM modules use double data rate architecture to achieve high-speed operation. The double data rate architecture is essentially a 4n-prefetch architecture with an interface designed to transfer two data words per clock cycle at the I/O pins. A single read or write access for the DDR2 SDRAM module effectively consists of a single 4n-bit-wide, one-clock-cycle data transfer at the internal DRAM core and four corresponding n-bit-wide, one-half-clock-cycle data transfers at the I/O pins.

A bidirectional data strobe (DQS, DQS#) is transmitted externally, along with data, for use in data capture at the receiver. DQS is a strobe transmitted by the DDR2 SDRAM device during READs and by the memory controller during WRITEs. DQS is edge-aligned with data for READs and center-aligned with data for WRITEs.

DDR2 SDRAM modules operate from a differential clock (CK and CK#); the crossing of CK going HIGH and CK# going LOW will be referred to as the positive edge of CK. Commands are registered at every positive edge of CK. Input data is registered on both edges of DQS, and output data is referenced to both edges of DQS, as well as to both edges of CK.

Register and PLL Operation

DDR2 SDRAM modules operate in registered mode, where the command/address input signals are latched in the registers on the rising clock edge and sent to the DDR2 SDRAM devices on the following rising clock edge (data access is delayed by one clock cycle). A phase-lock loop (PLL) on the module receives and redrives the differential clock signals (CK, CK#) to the DDR2 SDRAM devices. The register(s) and PLL reduce address, command, control, and clock signal loading by isolating DRAM from the system controller. PLL clock timing is defined by JEDEC specifications and ensured by use of the JEDEC clock reference board. Registered mode will add one clock cycle to CL.

Serial Presence-Detect Operation

DDR2 SDRAM modules incorporate serial presence-detect (SPD). The SPD function is implemented using a 2,048-bit EEPROM. This nonvolatile storage device contains 256 bytes. The first 128 bytes can be programmed by Micron to identify the module type and various SDRAM organizations and timing parameters. The remaining 128 bytes of storage are available for use by the customer. System READ/WRITE operations between the master (system logic) and the slave EEPROM device occur via a standard I²C bus using the DIMM's SCL (clock) and SDA (data) signals, together with SA (2:0), which provide eight unique DIMM/EEPROM addresses. Write protect (WP) is tied to VSS on the module, permanently disabling hardware write protect.

Electrical Specifications

Stresses greater than those listed in Table 6 may cause permanent damage to the module. This is a stress rating only, and functional operation of the module at these or any other conditions above those indicated in each device's data sheet is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Table 6: Absolute Maximum Ratings

Symbol	Parameter	Min	Max	Units
VDD/VDDQ	VDD/VDDQ supply voltage relative to Vss	-0.5	+2.3	V
VIN, VOUT	Voltage on any pin relative to Vss	-0.5	+2.3	V
II	Input leakage current; Any input $0V \leq V_{IN} \leq V_{DD}$; VREF input $0V \leq V_{IN} \leq 0.95V$; (All other pins not under test = 0V)	-5	+5	μA
	Command/address RAS#, CAS#, WE#, S#, CKE, DM, ODT, BA			
	CK, CK#	-250	+250	
IOZ	Output leakage current; $0V \leq V_{OUT} \leq V_{DDQ}$; DQs and ODT are disabled	-5	+5	μA
IVREF	VREF leakage current; VREF = valid VREF level	-10	+10	μA
TA	Module ambient operating temperature			
	Commercial	0	+70	$^{\circ}C$
	Industrial	-40	+85	$^{\circ}C$
TC ¹	DDR2 SDRAM component case operating temperature ²			
	Commercial	0	+85	$^{\circ}C$
	Industrial	-40	+95	$^{\circ}C$

- Notes: 1. The refresh rate is required to double when $85^{\circ}C < T_C \leq 95^{\circ}C$.
2. For further information, refer to technical note TN-00-08: "Thermal Applications," available on Micron's Web site.

Input Capacitance

Micron encourages designers to simulate the performance of the module to achieve optimum values. Simulations are significantly more accurate and realistic than a gross estimation of module capacitance when inductance and delay parameters associated with trace lengths are used in simulations. JEDEC modules are currently designed using simulations to close timing budgets.

Component AC Timing and Operating Conditions

Recommended AC operating conditions are given in the DDR2 component data sheets. Component specifications are available on Micron's Web site. Module speed grades correlate with component speed grades, as shown in Table 7.

Table 7: Module and Component Speed Grades

Module Speed Grade	Component Speed Grade
-667	-3
-53E	-37E
-40E	-5E

IDD Specifications

Table 8: DDR2 IDD Specifications and Conditions – 256MB

Values shown for MT47H32M16 DDR2 SDRAM only and are computed from values specified in the 512Mb (32 Meg x 16) component data sheet

Parameter/Condition	Symbol	-667	-53E	-40E	Units	
Operating one bank active-precharge current: $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} MIN (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD0	600	550	550	mA	
Operating one bank active-read-precharge current: $I_{OUT} = 0mA$; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RAS} = t_{RAS} MIN (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data pattern is same as IDD4W	IDD1	750	675	650	mA	
Precharge power-down current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2P	35	35	35	mA	
Precharge quiet standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are stable; Data bus inputs are floating	IDD2Q	275	225	200	mA	
Precharge standby current: All device banks idle; $t_{CK} = t_{CK} (IDD)$; CKE is HIGH, S# is HIGH; Other control and address bus inputs are switching; Data bus inputs are switching	IDD2N	300	250	225	mA	
Active power-down current: All device banks open; $t_{CK} = t_{CK} (IDD)$; CKE is LOW; Other control and address bus inputs are stable; Data bus inputs are floating	Fast PDN exit MR[12] = 0	IDD3P	175	150	125	mA
		Slow PDN exit MR[12] = 1	60	60	60	mA
Active standby current: All device banks open; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} MAX (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD3N	350	300	250	mA	
Operating burst write current: All device banks open; Continuous burst writes; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} MAX (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4W	1,250	1,025	800	mA	
Operating burst read current: All device banks open; Continuous burst reads; $I_{OUT} = 0mA$; BL = 4, CL = CL (IDD), AL = 0; $t_{CK} = t_{CK} (IDD)$, $t_{RAS} = t_{RAS} MAX (IDD)$, $t_{RP} = t_{RP} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are switching; Data bus inputs are switching	IDD4R	1,175	975	775	mA	
Burst refresh current: $t_{CK} = t_{CK} (IDD)$; REFRESH command at every $t_{RFC} (IDD)$ interval; CKE is HIGH, S# is HIGH between valid commands; Other control and address bus inputs are switching; Data bus inputs are switching	IDD5	925	875	850	mA	
Self refresh current: CK and CK# at 0V; CKE $\leq 0.2V$; Other control and address bus inputs are floating; Data bus inputs are floating	IDD6	35	35	35	mA	
Operating bank interleave read current: All device banks interleaving reads; $I_{OUT} = 0mA$; BL = 4, CL = CL (IDD), AL = $t_{RCD} (IDD) - 1 \times t_{CK} (IDD)$; $t_{CK} = t_{CK} (IDD)$, $t_{RC} = t_{RC} (IDD)$, $t_{RRD} = t_{RRD} (IDD)$, $t_{RCD} = t_{RCD} (IDD)$; CKE is HIGH, S# is HIGH between valid commands; Address bus inputs are stable during deselects; Data bus inputs are switching	IDD7	1,750	1,700	1,700	mA	

Register and PLL Specifications

Table 9: Register Specifications
SSTU32866 devices or equivalent JESD82-10

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	V _{IH(DC)}	Address, control, command	SSTL_18	V _{REF(DC)} + 125	V _{DDQ} + 250	mV
DC low-level input voltage	V _{IL(DC)}	Address, control, command	SSTL_18	0	V _{REF(DC)} - 125	mV
AC high-level input voltage	V _{IH(AC)}	Address, control, command	SSTL_18	V _{REF(DC)} + 250	V _{DD}	mV
AC low-level input voltage	V _{IL(AC)}	Address, control, command	SSTL_18	0	V _{REF(DC)} - 250	mV
Output high voltage	V _{OH}	Parity output	LVC MOS	1.2	–	V
Output low voltage	V _{OL}	Parity output	LVC MOS	–	0.5	V
Input current	I _I	All pins	V _I = V _{DDQ} or V _{SSQ}	–5	5	μA
Static standby	I _{DD}	All pins	RESET# = V _{SSQ} (I _o = 0)	–	100	μA
Static operating	I _{DD}	All pins	RESET# = V _{SSQ} ; V _I = V _{IH(AC)} or V _{IL(DC)} I _o = 0	–	40	mA
Dynamic operating (clock tree)	I _{DDD}	n/a	RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , I _o = 0; CK and CK# switching 50% duty cycle	–	Varies by manufacturer	μA
Dynamic operating (per each input)	I _{DDD}	n/a	RESET# = V _{DD} , V _I = V _{IH(AC)} or V _{IL(AC)} , I _o = 0; CK and CK# switching 50% duty cycle; One data input switching at ^t CK/2, 50% duty cycle	–	Varies by manufacturer	μA
Input capacitance (per device, per pin)	C _I	All inputs except RESET#	V _I = V _{REF} ±250mV; V _{DDQ} = 1.8V	2.5	3.5	pF
Input capacitance (per device, per pin)	C _I	RESET#	V _I = V _{DDQ} or V _{SSQ}	–	Varies by manufacturer	pF

Notes: 1. Timing and switching specifications for the register listed above are critical for proper operation of the DDR2 SDRAM registered DIMMs. These are meant to be a subset of the parameters for the specific device used on the module. Detailed information for this register is available in JEDEC standard JESD82.

Table 10: PLL Specifications
CU877 device or equivalent JESD82-8.01

Parameter	Symbol	Pins	Condition	Min	Max	Units
DC high-level input voltage	V _{IH}	RESET#	LVC MOS	0.65 × V _{DD}	–	V
DC low-level input voltage	V _{IL}	RESET#	LVC MOS	–	0.35 × V _{DD}	V
Input voltage (limits)	V _{IN}	RESET#, CK, CK#		–0.3	V _{DDQ} + 0.3	V
DC high-level input voltage	V _{IH}	CK, CK#	Differential input	0.65 × V _{DD}	–	V
DC low-level input voltage	V _{IL}	CK, CK#	Differential input	–	0.35 × V _{DD}	V
Input differential-pair cross voltage	V _{IX}	CK, CK#	Differential input	(V _{DDQ} /2) - 0.15	(V _{DDQ} /2) + 0.15	V
Input differential voltage	V _{ID(DC)}	CK, CK#	Differential input	0.3	V _{DDQ} + 0.4	V
Input differential voltage	V _{ID(AC)}	CK, CK#	Differential input	0.6	V _{DDQ} + 0.4	V
Input current	I _I	RESET#	V _I = V _{DDQ} or V _{SSQ}	–10	10	μA
		CK, CK#	V _I = V _{DDQ} or V _{SSQ}	–250	250	μA
Output disabled current	I _{ODL}		RESET# = V _{SSQ} ; V _I = V _{IH(AC)} or V _{IL(DC)}	100	–	μA
Static supply current	I _{DDLD}		CK = CK# = LOW	–	500	μA
Dynamic supply	I _{DD}	n/a	CK, CK# = 270 MHz, all outputs open (not connected to PCB)	–	300	mA
Input capacitance	C _{IN}	Each input	V _I = V _{DDQ} or V _{SSQ}	2	3	pF

Table 11: PLL Clock Driver Timing Requirements and Switching Characteristics

Parameter	Symbol	Min	Max	Units
Stabilization time	t _L	–	15	μs
Input clock slew rate	t _{LS1}	1.0	4	V/ns
SSC modulation frequency		30	33	kHz
SSC clock input frequency deviation		0.0	–0.50	%
PLL loop bandwidth (–3dB from unity gain)		2.0	–	MHz

- Notes: 1. PLL timing and switching specifications are critical for proper operation of the DDR2 DIMM. This is a subset of parameters for the specific PLL used. Detailed PLL information is available in JEDEC standard JESD82.

Serial Presence-Detect

Table 12: Serial Presence-Detect EEPROM DC Operating Conditions

All voltages referenced to VSS; VDDSPD = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units
Supply voltage	VDDSPD	1.7	3.6	V
Input high voltage: Logic 1; All inputs	V _{IH}	VDDSPD × 0.7	VDDSPD + 0.5	V
Input low voltage: Logic 0; All inputs	V _{IL}	-0.6	VDDSPD × 0.3	V
Output low voltage: I _{OUT} = 3mA	V _{OL}	-	0.4	V
Input leakage current: V _{IN} = GND to VDDSPD	I _{LI}	0.10	3	μA
Output leakage current: V _{OUT} = GND to VDDSPD	I _{LO}	0.05	3	μA
Standby current	I _{SB}	1.6	4	μA
Power supply current, READ: SCL clock frequency = 100 kHz	I _{CC_R}	0.4	1	mA
Power supply current, WRITE: SCL clock frequency = 100 kHz	I _{CC_W}	2	3	mA

Table 13: Serial Presence-Detect EEPROM AC Operating Conditions

All voltages referenced to VSS; VDDSPD = +1.7V to +3.6V

Parameter/Condition	Symbol	Min	Max	Units	Notes
SCL LOW to SDA data-out valid	t _{AA}	0.2	0.9	μs	1
Time the bus must be free before a new transition can start	t _{BUF}	1.3	-	μs	
Data-out hold time	t _{DH}	200	-	ns	
SDA and SCL fall time	t _F	-	300	ns	2
Data-in hold time	t _{HD:DAT}	0	-	μs	
Start condition hold time	t _{HD:STA}	0.6	-	μs	
Clock HIGH period	t _{HIGH}	0.6	-	μs	
Noise suppression time constant at SCL, SDA inputs	t _I	-	50	ns	
Clock LOW period	t _{LOW}	1.3	-	μs	
SDA and SCL rise time	t _R	-	0.3	μs	2
SCL clock frequency	f _{SCL}	-	400	kHz	
Data-in setup time	t _{SU:DAT}	100	-	ns	
Start condition setup time	t _{SU:STA}	0.6	-	μs	3
Stop condition setup time	t _{SU:STO}	0.6	-	μs	
WRITE cycle time	t _{WRC}	-	10	ms	4

- Notes:
1. To avoid spurious start and stop conditions, a minimum delay is placed between SCL = 1 and the falling or rising edge of SDA.
 2. This parameter is sampled.
 3. For a restart condition, or following a WRITE cycle.
 4. The SPD EEPROM WRITE cycle time (t_{WRC}) is the time from a valid stop condition of a write sequence to the end of the EEPROM internal ERASE/PROGRAM cycle. During the WRITE cycle, the EEPROM bus interface circuit is disabled, SDA remains HIGH due to pull-up resistance, and the EEPROM does not respond to its slave address.

Table 14: Serial Presence-Detect Matrix

Byte	Description	Entry (Version)	256MB
0	Number of SPD bytes used by Micron	128	80
1	Total number of bytes in SPD device	256	08
2	Fundamental memory type	DDR2 SDRAM	08
3	Number of row addresses on SDRAM	13	0D
4	Number of column addresses on SDRAM	9, 10	0A
5	DIMM height and module ranks	30mm, single rank	60
6	Module data width	72	48
7	Reserved	0	00
8	Module voltage interface levels	SSTL 1.8V	05
9	SDRAM cycle time, t_{CK} (CL = MAX value, see byte 18)	-667 -53E -40E	30 3D 50
10	SDRAM access from clock, t_{AC} (CL = MAX value, see byte 18)	-667 -53E -40E	45 50 60
11	Module configuration type	ECC ECC and parity	02 06
12	Refresh rate/type	7.81 μ s/SELF	82
13	SDRAM device width (primary SDRAM)	16	10
14	Error-checking SDRAM data width	16	10
15	Reserved	0	00
16	Burst lengths supported	4, 8	0C
17	Number of banks on SDRAM device	4	04
18	CAS latencies supported	-667 (5, 4, 3) -53E/-40E (4, 3)	38 18
19	Module thickness		01
20	DDR2 DIMM type	Mini-RDIMM	10
21	SDRAM module attributes	1 PLL; 1 register	04
22	SDRAM device attributes: weak driver (01) and 50 Ω ODT (03)	-667 -53E/-40E	03 01
23	SDRAM cycle time, t_{CK} , MAX CL - 1	-667 -53E/-40E	3D 50
24	SDRAM access from CK, t_{AC} , MAX CL - 1	-667 -53E -40E	45 50 60
25	SDRAM cycle time, t_{CK} , MAX CL - 2	-667 -53E/-40E	50 00
26	SDRAM access from CK, t_{AC} , MAX CL - 2	-667 -53E/-40E	45 00
27	MIN row precharge time, t_{RP}		3C
28	MIN row active-to-row active, t_{RRD}		28
29	MIN RAS#-to-CAS# delay, t_{RCD}		32
30	MIN RAS# pulse width, t_{RAS}	-667/-53E -40E	2D 28
31	Module rank density	128MB, 256MB, 512MB	40

Table 14: Serial Presence-Detect Matrix (continued)

Byte	Description	Entry (Version)	256MB
32	Address and command setup time, t_{IS_b}	-667 -53E -40E	20 25 35
33	Address and command hold time, t_{IH_b}	-667 -53E -40E	27 37 47
34	Data/data mask input setup time, t_{DS_b}	-667/-53E -40E	10 15
35	Data/data mask input hold time, t_{DH_b}	-667 -53E -40E	17 22 27
36	Write recovery time, t_{WR}		3C
37	WRITE-to-READ command delay, t_{WTR}	-667/-53E -40E	1E 28
38	READ-to-PRECHARGE command delay, t_{RTP}		1E
39	Memory analysis probe		00
40	Extension for bytes 41 and 42		00
41	MIN active-to-active/refresh time, t_{RC}^1	-667/-53E -40E	3C 37
42	MIN AUTO REFRESH-to-ACTIVE/AUTO REFRESH command period, t_{RFC}		69
43	SDRAM device MAX cycle time, $t_{CK} (MAX)$		80
44	SDRAM device MAX DQS-DQ skew time, t_{DQSQ}	-667 -53E -40E	18 1E 23
45	SDRAM device MAX read data hold skew factor, t_{QHS}	-667 -53E -40E	22 28 2D
46	PLL relock time		0F
47-61	Optional features, not supported		00
62	SPD revision	Release 1.2	12
63	Checksum for bytes 0-62 ECC/ECC and parity	-667 -53E -40E	7E/82 29/2D 90/94
64	Manufacturer's JEDEC ID code	MICRON	2C
65-71	Manufacturer's JEDEC ID code	(continued)	FF
72	Manufacturing location	1-12	01-0C
73-90	Module part number (ASCII)	-	Variable data
91	PCB identification code	1-9	01-09
92	Identification code (continued)	0	00
93	Year of manufacture in BCD	-	Variable data
94	Week of manufacture in BCD	-	Variable data
95-98	Module serial number	-	Variable data
99-127	Reserved for manufacturer-specific data		00
128-255	Reserved for customer-specific data		FF

Notes: 1. The t_{RC} SPD values shown are JEDEC DDR2 device specification values. The actual Micron DDR2 device specification is $t_{RC} = 55ns$ for all speed grades.

