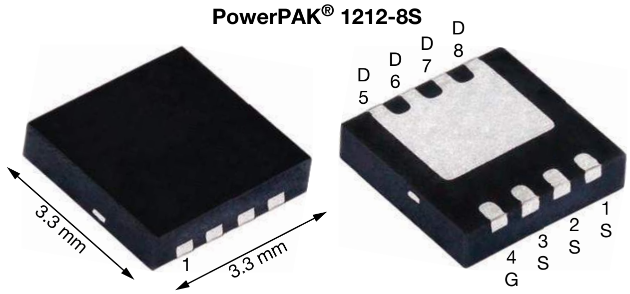
N-Channel 200 V (D-S) MOSFET

PowerPAK® 1212-8S



Top View   Bottom View

PRODUCT SUMMARY	
V_{DS} (V)	200
$R_{DS(on)}$ max. (Ω) at V_{GS} = 10 V	0.075
$R_{DS(on)}$ max. (Ω) at V_{GS} = 7.5 V	0.078
Q_g typ. (nC)	11
I_D (A)	19.5
Configuration	Single

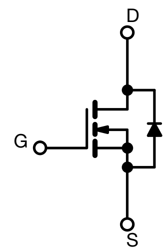
FEATURES

- TrenchFET® with ThunderFET technology optimizes balance of $R_{DS(on)}$, Q_g, Q_{sw}, and Q_{oss}
- Leadership $R_{DS(on)}$
- 100 % R_g and UIS tested
- Material categorization: for definitions of compliance please see www.vishay.com/doc?99912

RoHS COMPLIANT
HALOGEN FREE

APPLICATIONS

- Primary side switching
- Synchronous rectification
- DC/DC topologies
- Lighting
- Load switch
- Boost converter
- Motor drive control



N-Channel MOSFET

ORDERING INFORMATION	
Package	PowerPAK 1212-8S
Lead (Pb)-free and halogen-free	SiSS94DN-T1-GE3

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, unless otherwise noted)

PARAMETER		SYMBOL	LIMIT	UNIT
Drain-source voltage		V_{DS}	200	V
Gate-source voltage		V_{GS}	± 20	
Continuous drain current (T_J = 150 °C)	T_C = 25 °C	I_D	19.5	A
	T_C = 70 °C		15.6	
	T_A = 25 °C		5.4 [b, c]	
	T_A = 70 °C		4.3 [b, c]	
Pulsed drain current (t = 100 μs)		I_{DM}	25	
Continuous source-drain diode current	T_C = 25 °C	I_S	19.5	
	T_A = 25 °C		4.2 [b, c]	
Single pulse avalanche current	L = 0.1 mH	I_{AS}	10	
Single pulse avalanche energy		E_{AS}	5	mJ
Maximum power dissipation	T_C = 25 °C	P_D	65.8	W
	T_C = 70 °C		42.1	
	T_A = 25 °C		5.1 [b, c]	
	T_A = 70 °C		3.2 [b, c]	
Operating junction and storage temperature range		T_J, T_{stg}	-55 to +150	°C
Soldering recommendations (peak temperature) [c]			260	

THERMAL RESISTANCE RATINGS					
PARAMETER		**SYMBOL**	**TYPICAL**	**MAXIMUM**	**UNIT**
Maximum junction-to-ambient [b]	t ≤ 10 s	R_{thJA}	20	25	°C/W
Maximum junction-to-case (drain)	Steady state	R_{thJC}	1.5	1.9	

Notes

a. T_C = 25 °C
b. Surface mounted on 1" x 1" FR4 board
c. t = 10 s
d. See solder profile (www.vishay.com/doc?73257). The PowerPAK 1212-8S is a leadless package. The end of the lead terminal is exposed copper (not plated) as a result of the singulation process in manufacturing. A solder fillet at the exposed copper tip cannot be guaranteed and is not required to ensure adequate bottom side solder interconnection
e. Rework conditions: manual soldering with a soldering iron is not recommended for leadless components
f. Maximum under steady state conditions is 65 °C/W

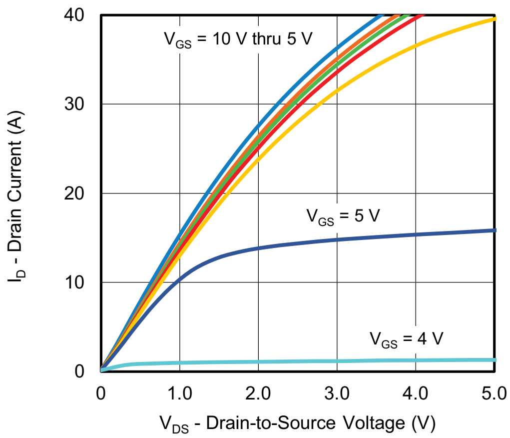
SPECIFICATIONS (T_J = 25 °C, unless otherwise noted)						
PARAMETER	**SYMBOL**	**TEST CONDITIONS**	**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static						
Drain-source breakdown voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 μA	200	-	-	V
V_{DS} temperature coefficient	$\Delta V_{DS}/T_J$	I_D = 250 μA	-	187	-	mV/°C
$V_{GS(th)}$ temperature coefficient	$\Delta V_{GS(th)}/T_J$	I_D = 250 μA	-	-6.4	-	
Gate-source threshold voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 250 μA	2	-	4	V
Gate-source leakage	I_{GSS}	V_{DS} = 0 V, V_{GS} = ± 20 V	-	-	100	nA
Zero gate voltage drain current	I_{DSS}	V_{DS} = 200 V, V_{GS} = 0 V	-	-	1	μA
		V_{DS} = 200 V, V_{GS} = 0 V, T_J = 70 °C	-	-	15	
On-state drain current [a]	$I_{D(on)}$	$V_{DS} \leq$ 10 V, V_{GS} = 10 V	25	-	-	A
Drain-source on-state resistance [a]	$R_{DS(on)}$	V_{GS} = 10 V, I_D = 5.4 A	-	0.061	0.075	Ω
		V_{GS} = 7.5 V, I_D = 5.3 A	-	0.063	0.078	
Forward transconductance [a]	g_{fs}	V_{DS} = 15 V, I_D = 5.4 A	-	12	-	S
Dynamic [b]						
Input capacitance	C_{iss}	V_{DS} = 100 V, V_{GS} = 0 V, f = 1 MHz	-	350	-	pF
Output capacitance	C_{oss}		-	77	-	
Reverse transfer capacitance	C_{rss}		-	10	-	
Total gate charge	Q_g	V_{DS} = 100 V, V_{GS} = 10 V, I_D = 5.4 A	-	14	21	nC
		V_{DS} = 100 V, V_{GS} = 7.5 V, I_D = 5.4 A	-	11	17	
Gate-source charge	Q_{gs}		-	3.5	-	
Gate-drain charge	Q_{gd}		-	3.8	-	
Output charge	Q_{oss}	V_{DS} = 100 V, V_{GS} = 0 V	-	29	44	
Gate resistance	R_g	f = 1 MHz	1	2.3	4.6	Ω
Turn-on delay time	$t_{d(on)}$	V_{DD} = 100 V, R_L = 23.3 Ω, $I_D \cong$ 4.3 A, V_{GEN} = 10 V, R_g = 1 Ω	-	12	24	ns
Rise time	t_r		-	5	10	
Turn-off delay time	$t_{d(off)}$		-	20	40	
Fall time	t_f		-	7	14	
Turn-on delay time	$t_{d(on)}$	V_{DD} = 100 V, R_L = 23.3 Ω, $I_D \cong$ 4.3 A, V_{GEN} = 7.5 V, R_g = 1 Ω	-	14	28	
Rise time	t_r		-	7	14	
Turn-off delay time	$t_{d(off)}$		-	18	36	
Fall time	t_f		-	9	18	
Drain-Source Body Diode Characteristics						
Continuous source-drain diode current	I_S	T_C = 25 °C	-	-	19.5	A
Pulse diode forward current	I_{SM}		-	-	25	
Body diode voltage	V_{SD}	I_S = 4.3 A, V_{GS} = 0 V	-	0.79	1.2	V
Body diode reverse recovery time	t_{rr}	I_F = 4.3 A, di/dt = 100 A/μs, T_J = 25 °C	-	80	160	ns
Body diode reverse recovery charge	Q_{rr}		-	230	460	nC
Reverse recovery fall time	t_a		-	65	-	ns
Reverse recovery rise time	t_b		-	15	-	

Notes

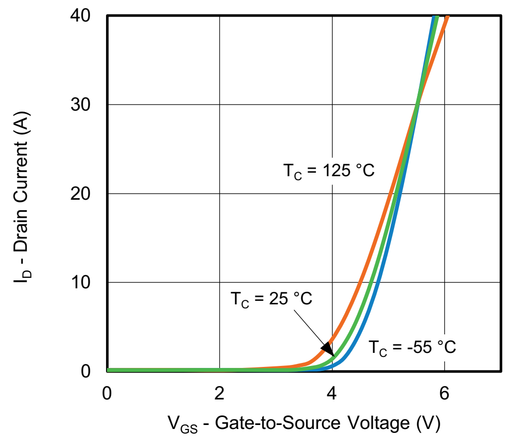
a. Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %
b. Guaranteed by design, not subject to production testing

Stresses beyond those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

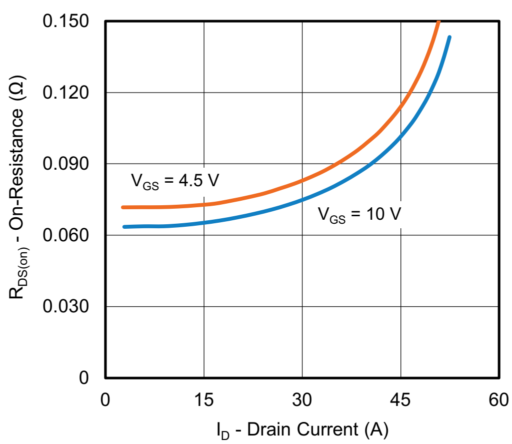
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



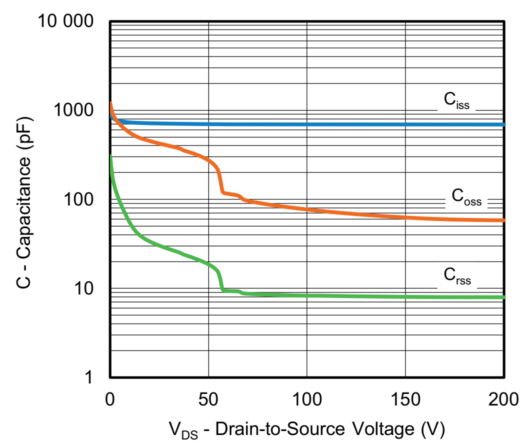
Output Characteristics



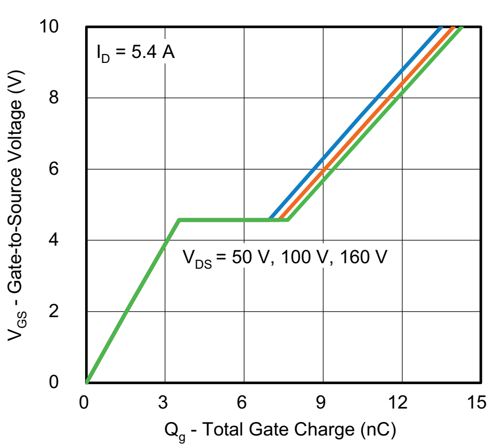
Transfer Characteristics



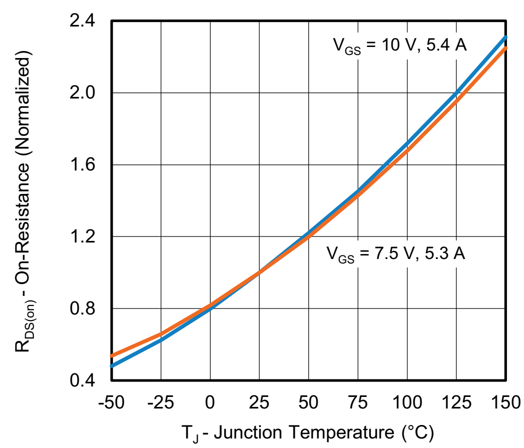
On-Resistance vs. Drain Current and Gate Voltage



Capacitance

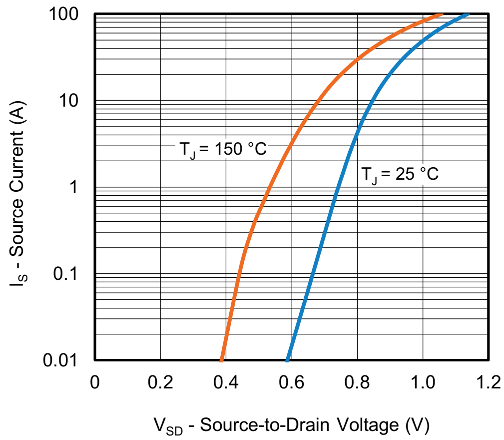


Gate Charge

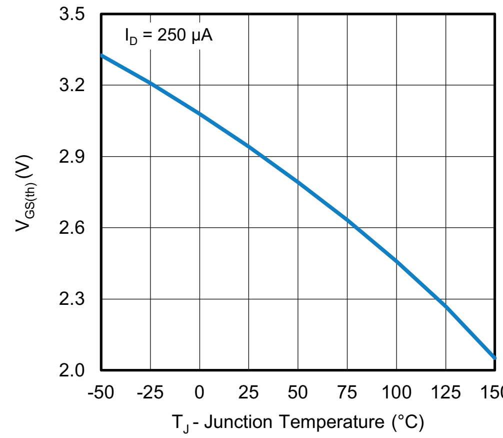


On-Resistance vs. Junction Temperature

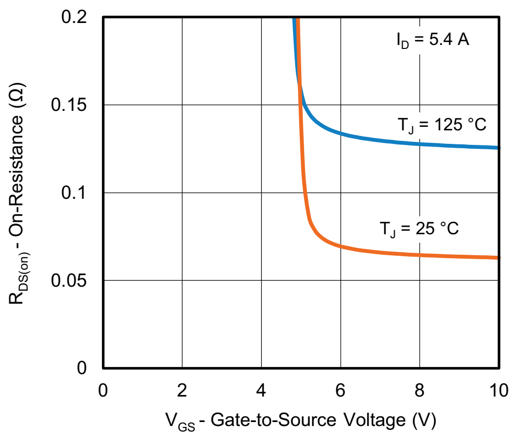
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



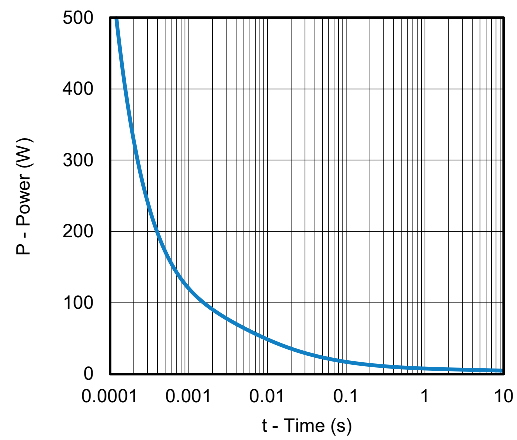
Source-Drain Diode Forward Voltage



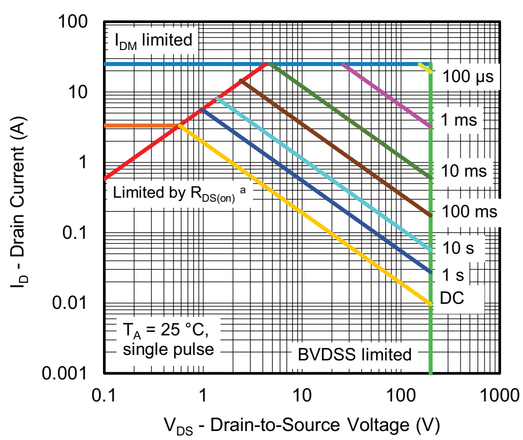
Threshold Voltage



On-Resistance vs. Gate-to-Source Voltage



Single Pulse Power, Junction-to-Ambient

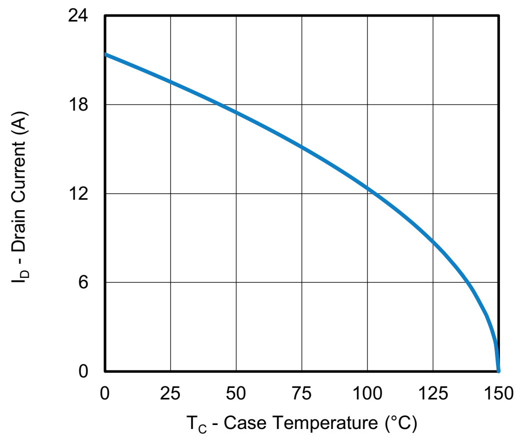


Safe Operating Area, Junction-to-Ambient

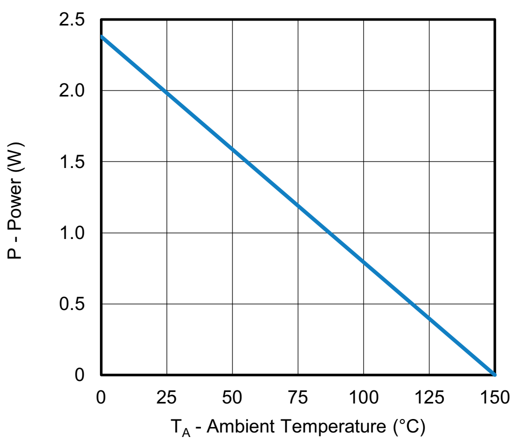
Note

a. V_{GS} > minimum V_{GS} at which $R_{DS(on)}$ is specified

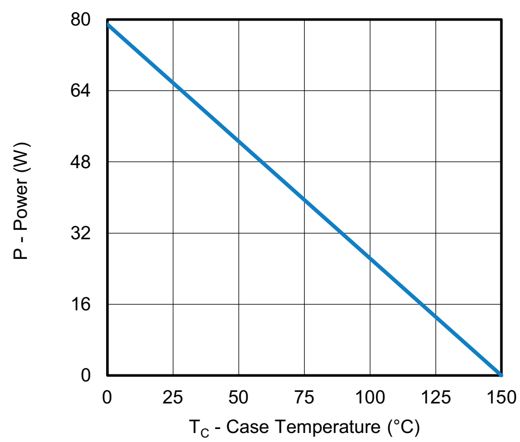
TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



Current Derating [a]



Power, Junction-to-Ambient

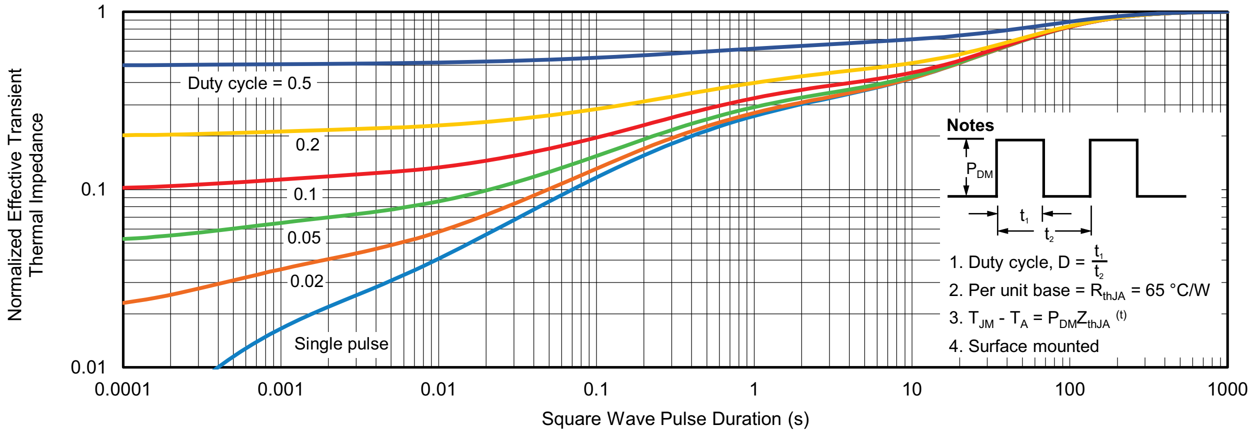


Power, Junction-to-Case

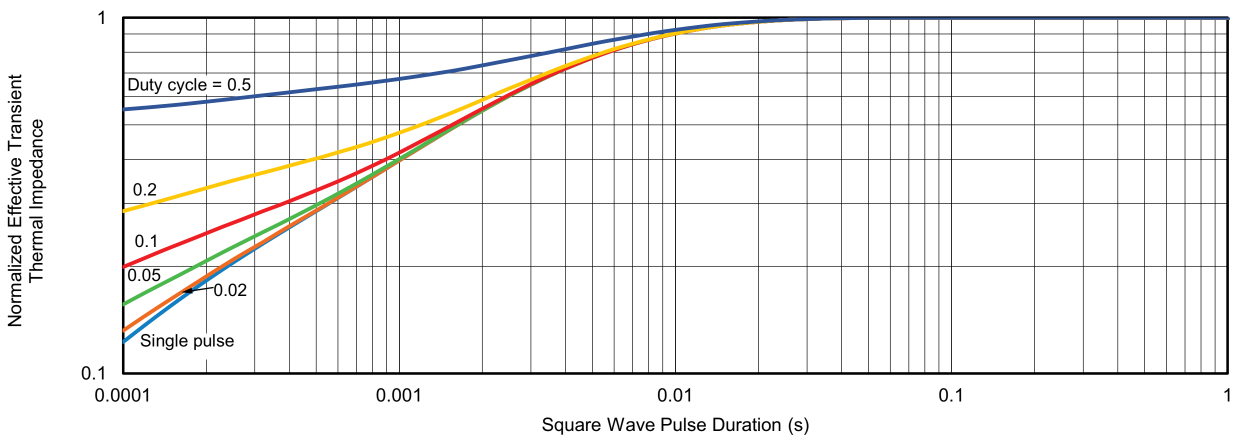
Note

a. The power dissipation P_D is based on T_J max. = 150 °C, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit

TYPICAL CHARACTERISTICS (25 °C, unless otherwise noted)



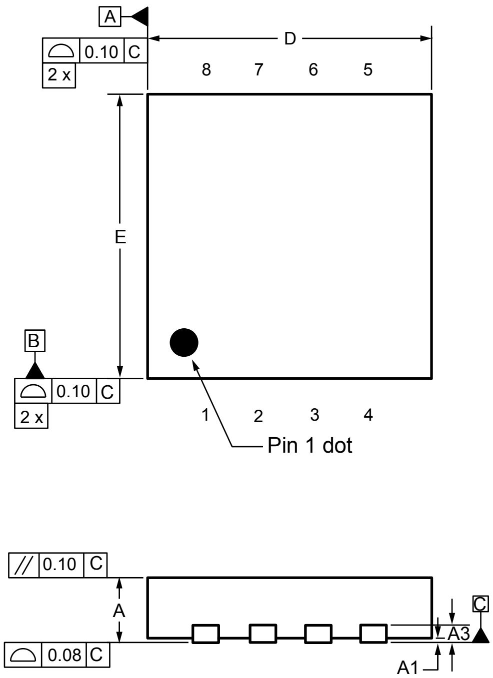
Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package / tape drawings, part marking, and reliability data, see www.vishay.com/ppg?77350.

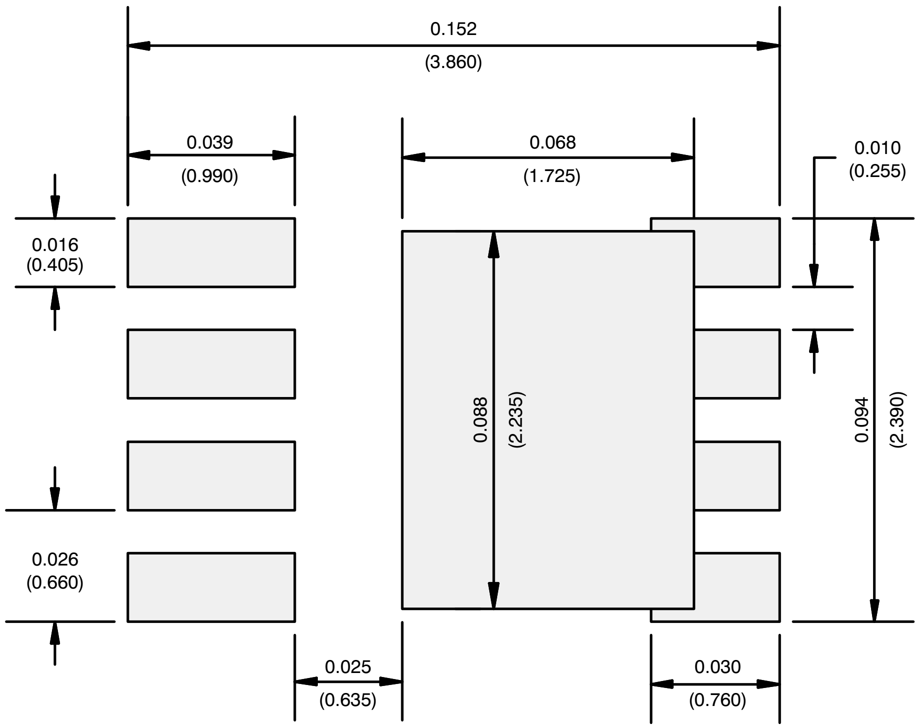
Case Outline for PowerPAK® 1212-8S



DIM.	MILLIMETERS			INCHES		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.67	0.75	0.83	0.026	0.030	0.033
A1	0.00	-	0.05	0.000	-	0.002
A3	0.20 ref.			0.008 ref		
b	0.25	0.30	0.35	0.010	0.012	0.014
D	3.20	3.30	3.40	0.126	0.130	0.134
D1	2.15	2.25	2.35	0.085	0.089	0.093
E	3.20	3.30	3.40	0.126	0.130	0.134
E1	1.60	1.70	1.80	0.063	0.067	0.071
e	0.65 bsc.			0.026 bsc.		
K	0.76 ref.			0.030 ref.		
K1	0.41 ref.			0.016 ref.		
L	0.33	0.43	0.53	0.013	0.017	0.021
Z	0.525 ref.			0.021 ref.		

ECN: C20-0862-Rev. B, 20-Jul-2020
DWG: 6008

RECOMMENDED MINIMUM PADS FOR PowerPAK® 1212-8 Single



Recommended Minimum Pads
Dimensions in Inches/(mm)

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