HEF4516B

Binary up/down counter

Rev. 7 — 11 November 2011 Product data sheet

1. General description

The HEF4516B is an edge-triggered synchronous 4-bit binary up/down counter with a clock input (CP), an up/down count control input (UP/$\overline{DN}$), an active LOW count enable input ($\overline{CE}$), an asynchronous active HIGH parallel load input (PL), four parallel inputs (D0 to D3), four parallel outputs (Q0 to Q3), an active LOW terminal count output ($\overline{TC}$), and an overriding asynchronous master reset input (MR).

Information on D0 to D3 is loaded into the counter while PL is HIGH, independent of all other input conditions except for MR which must be LOW. When PL and $\overline{CE}$ are LOW, the counter changes on the LOW-to-HIGH transition of CP. Input UP/$\overline{DN}$ determines the direction of the count, counting up when HIGH and counting down when LOW. When counting up, $\overline{TC}$ is LOW when Q0 and Q3 are HIGH and $\overline{CE}$ is LOW. When counting down, $\overline{TC}$ is LOW when Q0 to Q3 and $\overline{CE}$ are LOW. A HIGH on MR resets the counter (Q0 to Q3 = LOW) independent of all other input conditions.

It operates over a recommended V_{DD} power supply range of 3 V to 15 V referenced to V_{SS} (usually ground). Unused inputs must be connected to V_{DD}, V_{SS}, or another input.

2. Features and benefits

- Fully static operation
- 5 V, 10 V, and 15 V parametric ratings
- Standardized symmetrical output characteristics
- Specified from −40 °C to +85 °C
- Complies with JEDEC standard JESD 13-B

3. Ordering information

Table 1. Ordering information

All types operate from −40 °C to +85 °C.

Type number	Package		
	Name	Description	Version
HEF4516BP	DIP16	plastic dual in-line package; 16-leads (300 mil)	SOT38-4
HEF4516BT	SO16	plastic small outline package; 16 leads; body width 3.9 mm	SOT109-1

4. Functional diagram

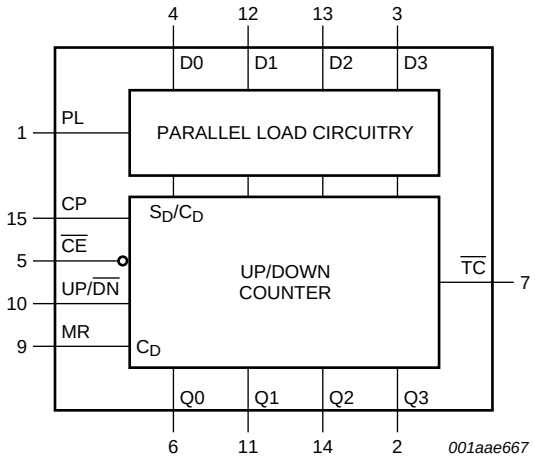

Fig 1. Functional diagram

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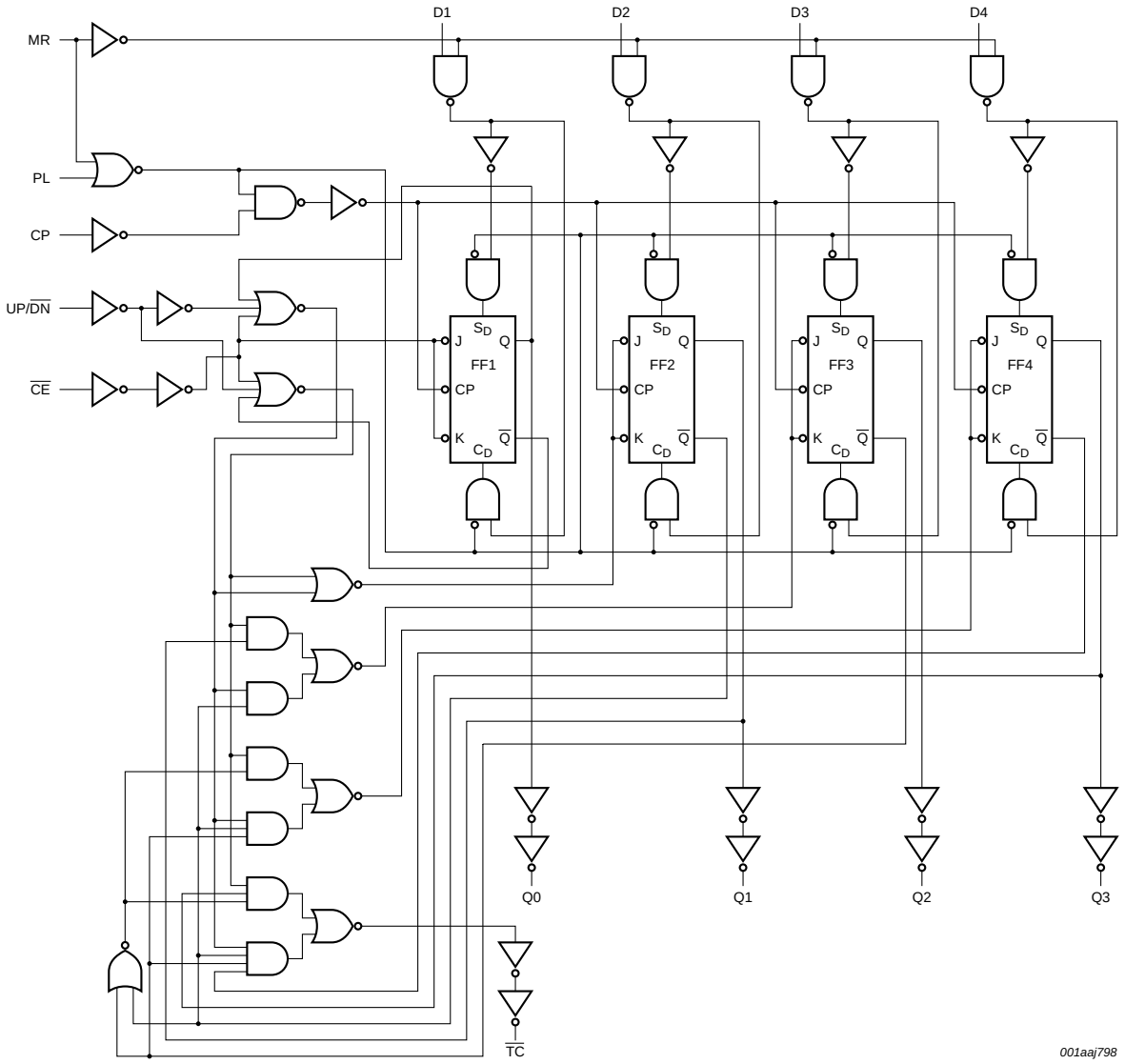

Fig 2. Logic diagram

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5. Pinning information

5.1 Pinning

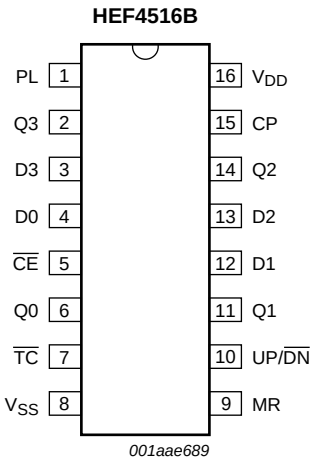

Fig 3. Pin configuration

5.2 Pin description

Table 2. Pin description

Symbol	Pin	Description
PL	1	parallel load input (active HIGH)
D0 to D3	4, 12, 13, 3	parallel input
$\overline{CE}$	5	count enable input (active LOW)
Q0 to Q3	6, 11, 14, 2	parallel output
V_{SS}	8	ground supply voltage
$\overline{TC}$	7	terminal count output (active LOW)
MR	9	master reset input
UP/$\overline{DN}$	10	up/down count control input
CP	15	clock pulse input (LOW to HIGH, edge triggered)
V_{DD}	16	supply voltage

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6. Functional description

Table 3. Function table[1]

MR	PL	UP/$\overline{DN}$	$\overline{CE}$	CP	MODE
L	H	X	X	X	parallel load
L	L	X	H	X	no change
L	L	L	L	↑	count down
L	L	H	L	↑	count up
H	X	X	X	X	reset

[1] H = HIGH voltage level; L = LOW voltage level; X = don't care; ↑ = positive-going transition.

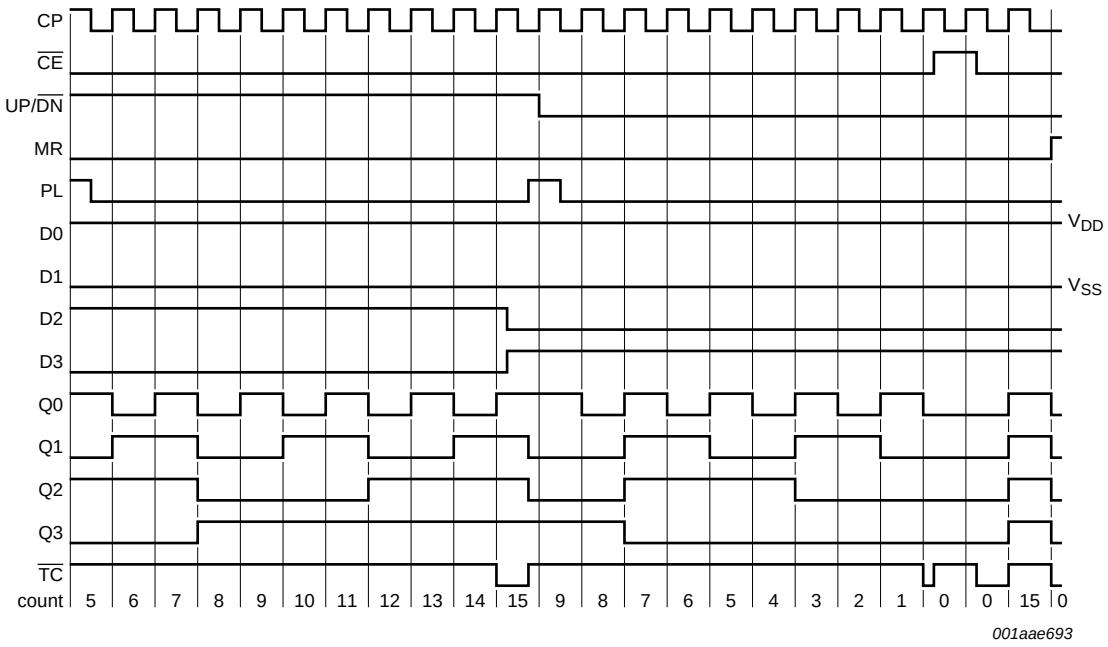

Fig 4. Timing diagram

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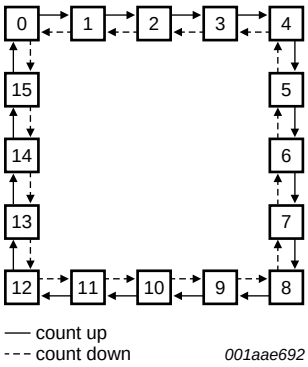

Logic equation for terminal count:

$$\overline{TC} = \overline{\overline{CE} \bullet \{(UP/\overline{DN}) \bullet Q0 \bullet Q1 \bullet Q2 \bullet Q3 + (\overline{UP/\overline{DN}}) \bullet \overline{Q0} \bullet \overline{Q1} \bullet \overline{Q2} \bullet \overline{Q3}\}}.$$

Fig 5. State diagram

7. Limiting values

Table 4. Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DD}	supply voltage			−0.5	+18	V
I_{IK}	input clamping current	$V_I < -0.5$ V or $V_I > V_{DD} + 0.5$ V		-	±10	mA
V_I	input voltage			−0.5	$V_{DD} + 0.5$	V
I_{OK}	output clamping current	$V_O < -0.5$ V or $V_O > V_{DD} + 0.5$ V		-	±10	mA
$I_{I/O}$	input/output current			-	±10	mA
I_{DD}	supply current			-	50	mA
T_{stg}	storage temperature			−65	+150	°C
T_{amb}	ambient temperature			−40	+85	°C
P_{tot}	total power dissipation	DIP16 package	[1]	-	750	mW
		SO16 package	[2]	-	500	mW
P	power dissipation	per output		-	100	mW

[1] For DIP16 package: P_{tot} derates linearly with 12 mW/K above 70 °C.

[2] For SO16 package: P_{tot} derates linearly with 8 mW/K above 70 °C.

8. Recommended operating conditions

Table 5. Recommended operating conditions

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DD}	supply voltage		3	-	15	V
V_I	input voltage		0	-	V_{DD}	V
T_{amb}	ambient temperature	in free air	−40	-	+85	°C

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Table 5. Recommended operating conditions *…continued*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$\Delta t/\Delta V$	input transition rise and fall rate	V_{DD} = 5 V	-	-	3.75	µs/V
		V_{DD} = 10 V	-	-	0.5	µs/V
		V_{DD} = 15 V	-	-	0.08	µs/V

9. Static characteristics

Table 6. Static characteristics

V_{SS} = 0 V; V_I = V_{SS} or V_{DD} unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}	T_{amb} = –40 °C		T_{amb} = 25 °C		T_{amb} = 85 °C		Unit
				Min	Max	Min	Max	Min	Max	
V_{IH}	HIGH-level input voltage	$\|I_O\|$ < 1 µA	5 V	3.5	-	3.5	-	3.5	-	V
			10 V	7.0	-	7.0	-	7.0	-	V
			15 V	11.0	-	11.0	-	11.0	-	V
V_{IL}	LOW-level input voltage	$\|I_O\|$ < 1 µA	5 V	-	1.5	-	1.5	-	1.5	V
			10 V	-	3.0	-	3.0	-	3.0	V
			15 V	-	4.0	-	4.0	-	4.0	V
V_{OH}	HIGH-level output voltage	$\|I_O\|$ < 1 µA; V_I = V_{SS} or V_{DD}	5 V	4.95	-	4.95	-	4.95	-	V
			10 V	9.95	-	9.95	-	9.95	-	V
			15 V	14.95	-	14.95	-	14.95	-	V
V_{OL}	LOW-level output voltage	$\|I_O\|$ < 1 µA; V_I = V_{SS} or V_{DD}	5 V	-	0.05	-	0.05	-	0.05	V
			10 V	-	0.05	-	0.05	-	0.05	V
			15 V	-	0.05	-	0.05	-	0.05	V
I_{OH}	HIGH-level output current	V_O = 2.5 V	5 V	-	–1.7	-	–1.4	-	–1.1	mA
		V_O = 4.6 V	5 V	-	–0.52	-	–0.44	-	–0.36	mA
		V_O = 9.5 V	10 V	-	–1.3	-	–1.1	-	–0.9	mA
		V_O = 13.5 V	15 V	-	–3.6	-	–3.0	-	–2.4	mA
I_{OL}	LOW-level output current	V_O = 0.4 V	5 V	0.52	-	0.44	-	0.36	-	mA
		V_O = 0.5 V	10 V	1.3	-	1.1	-	0.9	-	mA
		V_O = 1.5 V	15 V	3.6	-	3.0	-	2.4	-	mA
I_I	input leakage current	V_{DD} = 15 V	15 V	-	±0.3	-	±0.3	-	±1.0	µA
I_{DD}	supply current	I_O = 0 A; V_I = V_{SS} or V_{DD}	5 V	-	20	-	20	-	150	µA
			10 V	-	40	-	40	-	300	µA
			15 V	-	80	-	80	-	600	µA
C_I	input capacitance		-	-	-	-	7.5	-	-	pF

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10. Dynamic characteristics

Table 7. Dynamic characteristics

V_{SS} = 0 V; T_{amb} = 25 °C; for test circuit see Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}		Extrapolation formula	Min	Typ	Max	Unit
t_{PHL}	HIGH to LOW propagation delay	CP to Qn	5 V	[1]	118 ns + (0.55 ns/pF)C_L	-	145	290	ns
			10 V		49 ns + (0.23 ns/pF)C_L	-	60	120	ns
			15 V		37 ns + (0.16 ns/pF)C_L	-	45	90	ns
		CP to $\overline{TC}$	5 V		233 ns + (0.55 ns/pF)C_L	-	260	525	ns
			10 V		94 ns + (0.23 ns/pF)C_L	-	105	210	ns
			15 V		67 ns + (0.16 ns/pF)C_L	-	75	150	ns
		PL to Qn	5 V		98 ns + (0.55 ns/pF)C_L	-	125	255	ns
			10 V		44 ns + (0.23 ns/pF)C_L	-	55	110	ns
			15 V		32 ns + (0.16 ns/pF)C_L	-	40	85	ns
		PL to $\overline{TC}$	5 V		223 ns + (0.55 ns/pF)C_L	-	250	500	ns
			10 V		99 ns + (0.23 ns/pF)C_L	-	110	220	ns
			15 V		72 ns + (0.16 ns/pF)C_L	-	80	160	ns
		$\overline{CE}$ to $\overline{TC}$	5 V		138 ns + (0.55 ns/pF)C_L	-	165	330	ns
			10 V		54 ns + (0.23 ns/pF)C_L	-	65	135	ns
			15 V		42 ns + (0.16 ns/pF)C_L	-	50	100	ns
		MR to Qn, $\overline{TC}$	5 V		178 ns + (0.55 ns/pF)C_L	-	205	405	ns
			10 V		54 ns + (0.23 ns/pF)C_L	-	65	130	ns
			15 V		37 ns + (0.16 ns/pF)C_L	-	45	85	ns
t_{PLH}	LOW to HIGH propagation delay	CP to Qn	5 V	[1]	128 ns + (0.55 ns/pF)C_L	-	155	310	ns
			10 V		54 ns + (0.23 ns/pF)C_L	-	65	130	ns
			15 V		37 ns + (0.16 ns/pF)C_L	-	45	90	ns
		CP to $\overline{TC}$	5 V		153 ns + (0.55 ns/pF)C_L	-	180	360	ns
			10 V		64 ns + (0.23 ns/pF)C_L	-	75	150	ns
			15 V		47 ns + (0.16 ns/pF)C_L	-	55	115	ns
		PL to Qn	5 V		143 ns + (0.55 ns/pF)C_L	-	170	340	ns
			10 V		59 ns + (0.23 ns/pF)C_L	-	70	140	ns
			15 V		42 ns + (0.16 ns/pF)C_L	-	50	105	ns
		PL to $\overline{TC}$	5 V		223 ns + (0.55 ns/pF)C_L	-	250	500	ns
			10 V		99 ns + (0.23 ns/pF)C_L	-	110	220	ns
			15 V		72 ns + (0.16 ns/pF)C_L	-	80	160	ns
		$\overline{CE}$ to $\overline{TC}$	5 V		118 ns + (0.55 ns/pF)C_L	-	145	290	ns
			10 V		49 ns + (0.23 ns/pF)C_L	-	60	125	ns
			15 V		37 ns + (0.16 ns/pF)C_L	-	45	95	ns
		MR to $\overline{TC}$	5 V		198 ns + (0.55 ns/pF)C_L	-	225	450	ns
			10 V		64 ns + (0.23 ns/pF)C_L	-	75	150	ns
			15 V		42 ns + (0.16 ns/pF)C_L	-	50	100	ns

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Table 7. Dynamic characteristics *…continued*

V_{SS} = 0 V; T_{amb} = 25 °C; for test circuit see Figure 8; unless otherwise specified.

Symbol	Parameter	Conditions	V_{DD}		Extrapolation formula	Min	Typ	Max	Unit
t_t	transition time		5 V	[1]	10 ns + (1.00 ns/pF)C_L	-	60	120	ns
			10 V		9 ns + (0.42 ns/pF)C_L	-	30	60	ns
			15 V		6 ns + (0.28 ns/pF)C_L	-	20	40	ns
f_{max}	maximum frequency	see Figure 6	5 V			3	6	-	MHz
			10 V			7	14	-	MHz
			15 V			9	18	-	MHz
t_W	pulse width	CP input LOW; minimum width; see Figure 6	5 V			95	45	-	ns
			10 V			35	20	-	ns
			15 V			25	15	-	ns
		PL input HIGH; minimum width; see Figure 7	5 V			105	55	-	ns
			10 V			45	25	-	ns
			15 V			35	15	-	ns
		MR input HIGH; minimum width; see Figure 7	5 V			120	60	-	ns
			10 V			50	25	-	ns
			15 V			40	20	-	ns
t_{rec}	recovery time	MR input; see Figure 7	5 V			130	65	-	ns
			10 V			45	20	-	ns
			15 V			30	15	-	ns
		PL input; see Figure 7	5 V			150	75	-	ns
			10 V			50	25	-	ns
			15 V			30	15	-	ns
t_{su}	set-up time	Dn to PL; see Figure 7	5 V			100	50	-	ns
			10 V			50	25	-	ns
			15 V			40	20	-	ns
		UP/$\overline{DN}$ to CP; see Figure 6	5 V			250	125	-	ns
			10 V			100	50	-	ns
			15 V			75	35	-	ns
		$\overline{CE}$ to CP; see Figure 6	5 V			120	60	-	ns
			10 V			40	20	-	ns
			15 V			25	10	-	ns
t_h	hold time	Dn to PL; see Figure 7	5 V			+10	–40	-	ns
			10 V			+5	–20	-	ns
			15 V			0	–20	-	ns
		UP/$\overline{DN}$ to CP; see Figure 6	5 V			+35	–90	-	ns
			10 V			+15	–35	-	ns
			15 V			+15	–25	-	ns
		$\overline{CE}$ to CP; see Figure 6	5 V			+20	–40	-	ns
			10 V			+5	–15	-	ns
			15 V			+5	–10	-	ns

[1] The typical values of the propagation delay and transition times are calculated from the extrapolation formulas shown (C_L in pF).

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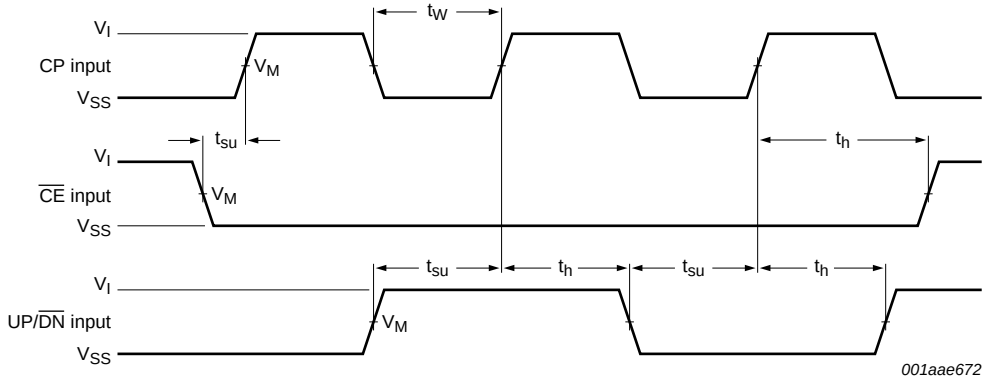
Table 8. Dynamic power dissipation P_D

P_D can be calculated from the formulas shown. V_{SS} = 0 V; C_L = 50 pF; $t_r = t_f \leq 20$ ns; T_{amb} = 25 °C.

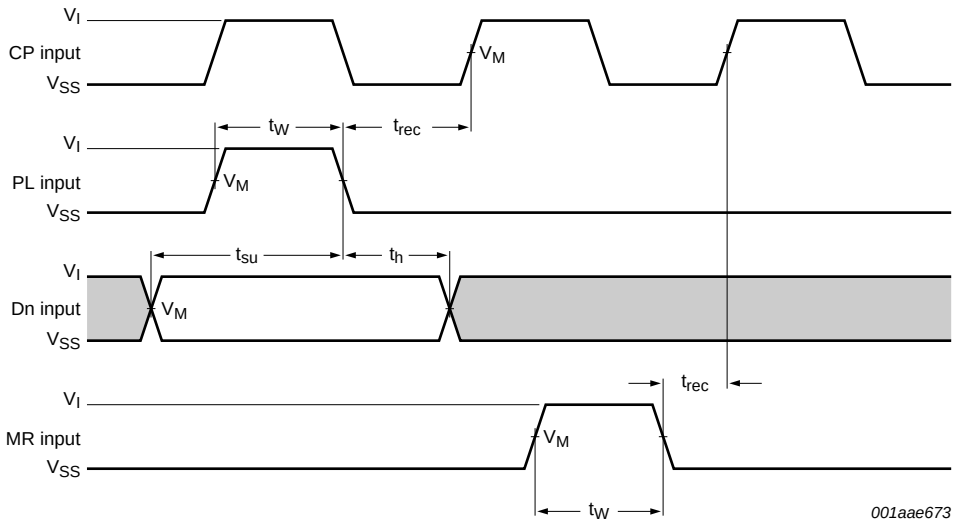
Symbol	Parameter	V_{DD}	Typical formula for P_D (µW)	Where:
P_D	dynamic power dissipation	5 V	$P_D = 1000 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_i = input frequency in MHz;
		10 V	$P_D = 4500 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	f_o = output frequency in MHz;
		15 V	$P_D = 11200 \times f_i + \Sigma(f_o \times C_L) \times V_{DD}^2$	C_L = output load capacitance in pF;
				V_{DD} = supply voltage in V;
				$\Sigma(f_o \times C_L)$ = sum of the outputs.

11. Waveforms



Measurement points are given in Table 9.

Fig 6. Waveforms showing minimum pulse width for CP, set-up and hold times for $\overline{CE}$ to CP and UP/$\overline{DN}$ to CP



Measurement points are given in Table 9.

Fig 7. Waveforms showing PL and MR minimum pulse widths and recovery times, and Dn to PL set-up and hold times

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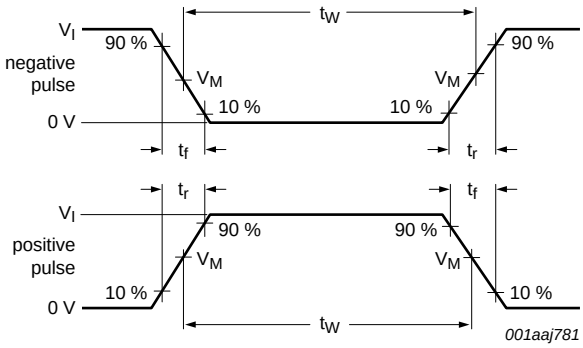
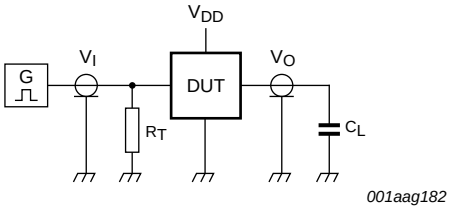


a. Input waveforms



b. Test circuit

Test data is given in Table 9.

Definitions for test circuit:

DUT = Device Under Test

C_L = Load capacitance including jig and probe capacitance;

R_T = Termination resistance should be equal to output impedance Z_o of the pulse generator.

Fig 8. Test circuit for measuring switching times

Table 9. Measurement points and test data

Supply voltage	Input			Load
	V_I	V_M	t_r, t_f	C_L
5 V to 15 V	V_{DD}	$0.5V_I$	≤ 20 ns	50 pF

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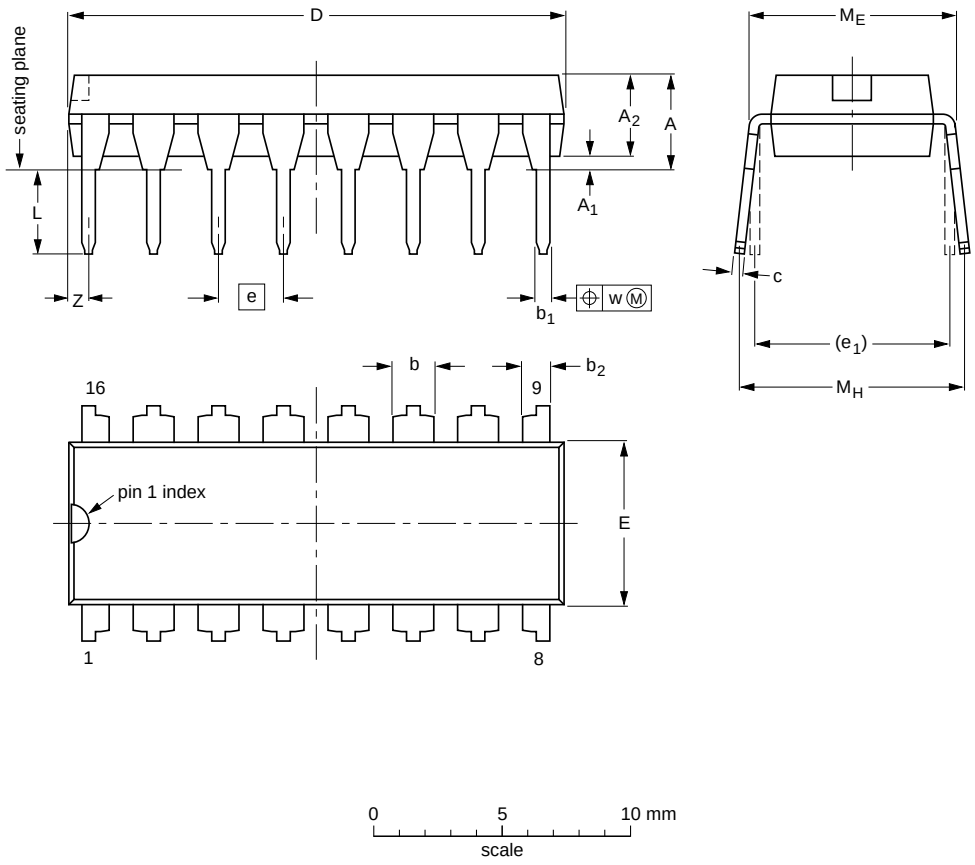
12. Package outline

DIP16: plastic dual in-line package; 16 leads (300 mil) **SOT38-4**



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1 min.	A_2 max.	b	b_1	b_2	c	D (1)	E (1)	e	e_1	L	M_E	M_H	w	Z (1) max.
mm	4.2	0.51	3.2	1.73 1.30	0.53 0.38	1.25 0.85	0.36 0.23	19.50 18.55	6.48 6.20	2.54	7.62	3.60 3.05	8.25 7.80	10.0 8.3	0.254	0.76
inches	0.17	0.02	0.13	0.068 0.051	0.021 0.015	0.049 0.033	0.014 0.009	0.77 0.73	0.26 0.24	0.1	0.3	0.14 0.12	0.32 0.31	0.39 0.33	0.01	0.03

Note

1. Plastic or metal protrusions of 0.25 mm (0.01 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT38-4						~~95-01-14~~ 03-02-13

Fig 9. Package outline SOT38-4 (DIP16)

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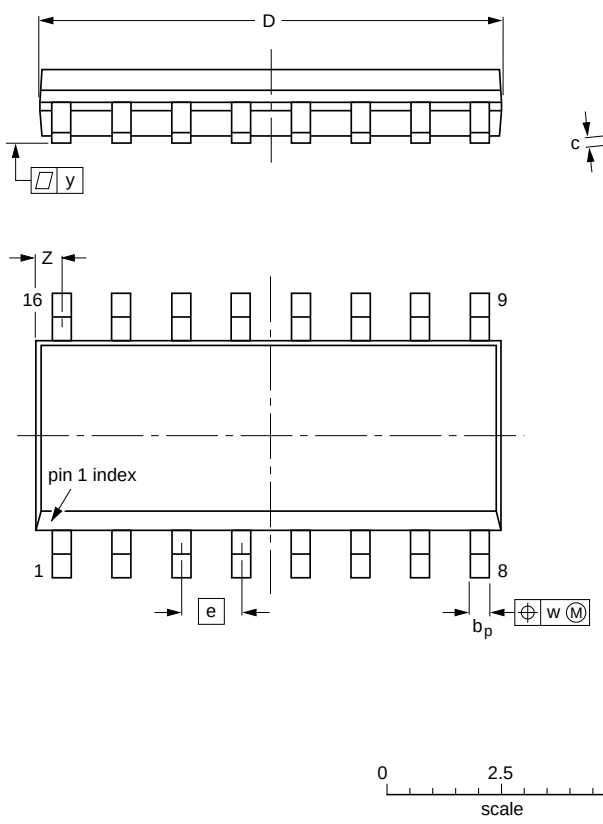
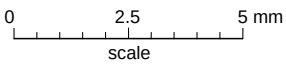
SO16: plastic small outline package; 16 leads; body width 3.9 mm **SOT109-1**





DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	$D^{(1)}$	$E^{(1)}$	e	H_E	L	L_p	Q	v	w	y	$Z^{(1)}$	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8^o 0^o
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.05	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

Note

1. Plastic or metal protrusions of 0.15 mm (0.006 inch) maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT109-1	076E07	MS-012				~~99-12-27~~ 03-02-19

Fig 10. Package outline SOT109-1 (SO16)

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13. Revision history

Table 10. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
HEF4516B v.7	20111111	Product data sheet	-	HEF4516B v.6
Modifications:	• Section Applications removed • Table 6: I_{OH} minimum values changed to maximum			
HEF4516B v.6	20091211	Product data sheet	-	HEF4516B v.5
HEF4516B v.5	20090812	Product data sheet	-	HEF4516B v.4
HEF4516B v.4	20090312	Product data sheet	-	HEF4516B_CNV v.3
HEF4516B_CNV v.3	19950101	Product specification	-	HEF4516B_CNV v.2
HEF4516B_CNV v.2	19950101	Product specification	-	-

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Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

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