

FEATURES

- **Guaranteed AC performance over temperature and voltage:**
 - >10.7Gbps data throughput
 - <60ps t_r/t_f times
 - <350ps t_{pd} (IN-to-Q)
 - <20ps skew
- **Low jitter:**
 - <10ps_{PP} total jitter (clock)
 - <1ps_{RMS} random jitter (data)
 - <10ps_{PP} deterministic jitter (data)
- **Crosstalk induced jitter: <0.7ps_{RMS}**
- **Unique, patent-pending input isolation minimizes adjacent channel crosstalk**
- **Accepts an input signal as low as 100mV**
- **Unique, patent-pending input termination and VT pin accepts DC-coupled and AC-coupled differential inputs: LVPECL, LVDS, and CML**
- **Fully differential inputs/outputs**
- **50Ω source terminated CML outputs**
- **Power supply 2.5V ±5% and 3.3V ±10%**
- **Industrial –40°C to +85°C temperature range**
- **Available in 32-pin (5mm × 5mm) MLF[®] package**

APPLICATIONS

- Gigabit Ethernet data/clock routing
- SONET data/clocking routing
- Switch fabric clock routing
- Redundant switchover
- Backplane redundancy

Precision Edge[®]**DESCRIPTION**

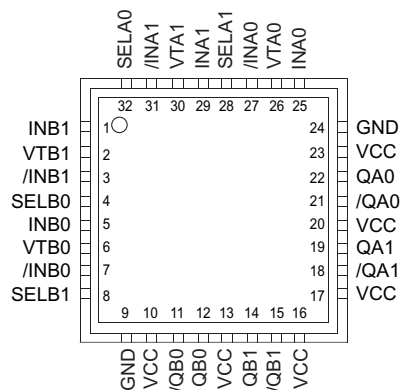
The SY58024U is a 2.5V/3.3V precision, high-speed, fully differential dual CML crosspoint switch. The SY58024U is optimized to provide two identical output copies with less than 20ps of skew and ultra-low jitter. The SY58024U can process clock signals as fast as 6GHz or data patterns up to 10.7Gbps.

The differential input includes Micrel's unique, 3-pin input termination architecture that allows the SY58024U to directly interface to LVPECL, LVDS, and CML differential signal (AC- or DC-coupled) without any level-shifting or termination resistor networks in the signal path. The CML outputs features a 400mV typical swing into 50Ω loads, and provides an extremely fast rise/fall time guaranteed to be less than 60ps.

The SY58024U operates from a 2.5V ±5% supply or 3.3V ±10% supply and is guaranteed over the full industrial temperature range (–40°C to +85°C). For applications that require high-speed single channel CML switches, consider the SY58023U. The SY58024U is part of Micrel's high-speed, Precision Edge[®] product line.

Datasheets and support documentation can be found on Micrel's website at: www.micrel.com.

PACKAGE/ORDERING INFORMATION



32-Pin MLF® (MLF-32)

Ordering Information⁽¹⁾

Part Number	Package Type	Operating Range	Package Marking	Lead Finish
SY58024UMI	MLF-32	Industrial	SY58024U	Sn-Pb
SY58024UMITR ⁽²⁾	MLF-32	Industrial	SY58024U	Sn-Pb
SY58024UMG ⁽³⁾	MLF-32	Industrial	SY58024U with Pb-Free bar-line indicator	Pb-Free NiPdAu
SY58024UMGTR ^(2, 3)	MLF-32	Industrial	SY58024U with Pb-Free bar-line indicator	Pb-Free NiPdAu

Notes:

1. Contact factory for die availability. Dice are guaranteed at T_A = 25°C, DC electricals only.
2. Tape and Reel.
3. Pb-Free package recommended for new designs.

PIN DESCRIPTION

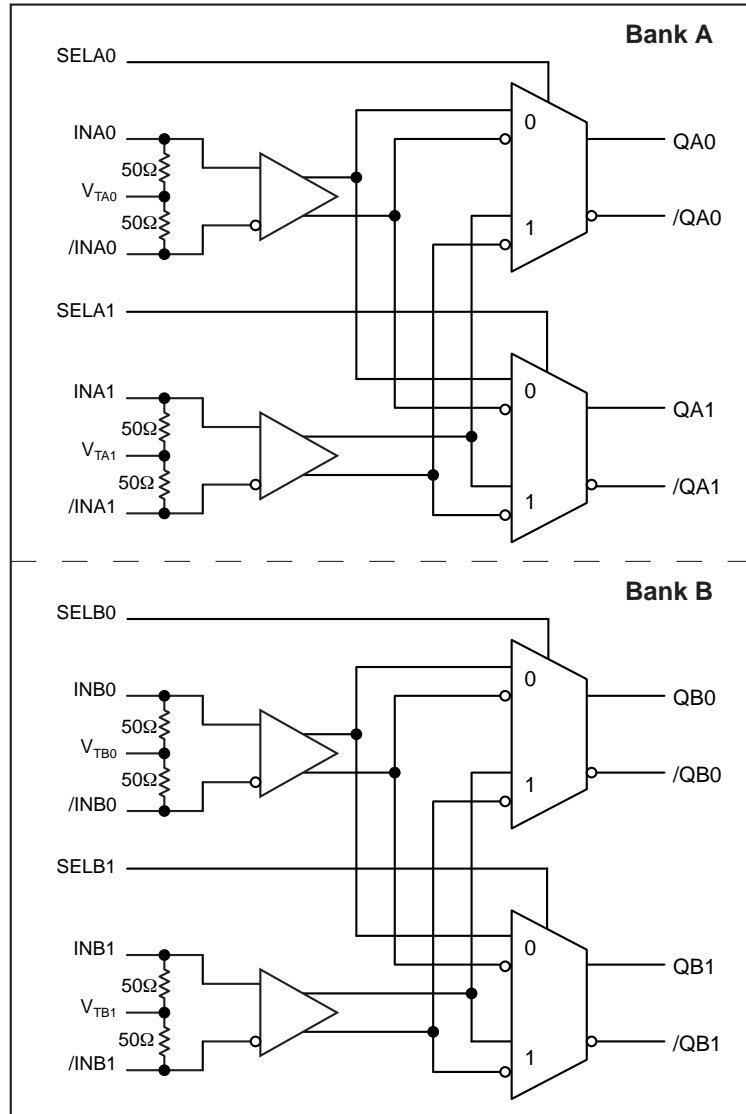
Pin Number	Pin Name	Pin Function
25, 27 29, 31, 1, 3, 5, 7	INA0, /INA0, INA1, /INA1, INB1, /INB1 INB0, /INB0	Differential Signal: Each pin of this pair internally terminates with 50Ω to the VT pin. The input will default to an indeterminate state if left open. See “Input Interface Application” section.
26, 30 2, 6	VTA0, VTA1, VTB1, VTB0	Input Termination Center-Tap: Each input terminates to this pin. The VT pin provides a center-tap for each input (IN, /IN) to a termination network for maximum interface flexibility. See “Input Interface Application” section.
32, 28, 8, 4	SELA0, SELA1, SELB1, SELB0	Select Input: TTL/CMOS select input controls that selects inputs IN0, or IN1, for their respective banks A and B. Each input is internally connected to a 25kΩ pull-up resistor and will default to a logic high state if left open.
9,24	GND, Exposed Pad	Ground. Exposed pad must be connected to a ground plane that is the same potential as the device ground pins.
10,13,16, 17, 20, 23	VCC	Positive Power Supply: Bypass with 0.1μF 0.01μF low ESR capacitors as close to the V _{CC} pins as possible.
11, 12, 15, 14 18, 19, 21, 22	/QB0, QB0, /QB1, QB1, /QA1, QA1, /QA0, QA0	CML Differential Output Pairs: Differential buffered output copy of the selected input signal. The CML single-ended output swing is typically 400mV into 50Ω or 100Ω across the pair. Unused output pairs may be left floating with no impact on jitter. See “CML Output Termination” section.

TRUTH TABLE

SELA0	SELA1	QA0	QA1	SELB0	SELB1	QB0	QB1
0	0	INA0	INA0	0	0	INB0	INB0
0	1	INA0	INA1	0	1	INB1	INB1
1	0	INA1	INA0	1	0	INB1	INB0
1	1	INA1	INA1	1	1	INB1	INB1

FUNCTIONAL BLOCK DIAGRAM

SY58024U Dual 2 × 2 Crosspoint Switch



Absolute Maximum Ratings⁽¹⁾

Supply Voltage (V_{CC}) -0.5V to +4.0V
 Input Voltage (V_{IN}) -0.5V to V_{CC}
 CML Output Voltage (V_{OUT}) $V_{CC} - 1.0V$ to $V_{CC} + 0.5V$
 Current (V_T)
 Source or Sink Current on V_T pin $\pm 100mA$
 Input Current (V_T)
 Source or Sink Current on IN, /IN $\pm 50mA$
 Lead Temperature (soldering, 20 sec.) 260°C
 Storage Temperature (T_S) -65°C +150°C

Operating Ratings⁽²⁾

Supply Voltage (V_{CC}) +2.375V to +3.60V
 Ambient Temperature (T_A) -40°C to +85°C
 Package Thermal Resistance⁽³⁾
 MLF® (θ_{JA})
 Still-Air 35°C/W
 500lfpm 28°C/W
 MLF® (ψ_{JB})
 Junction-to-board resistance 20°C/W

DC ELECTRICAL CHARACTERISTICS⁽⁴⁾

$T_A = -40^\circ C$ to $+85^\circ C$.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{CC}	Power Supply Voltage	2.5V nominal	2.375	2.5	2.625	V
		3.3V nominal	3.0	3.3	3.60	V
I_{CC}	Power Supply Current	$V_{CC} = \text{max.}$, current through internal 50Ω source termination resistor included.		200	250	mA
V_{IH}	Input HIGH Voltage	IN, /IN, Note 5	$V_{CC} - 1.6$		V_{CC}	V
V_{IL}	Input LOW Voltage	IN, /IN	0		$V_{IH} - 0.1$	V
V_{IN}	Input Voltage Swing	IN, /IN, see Figure 1a.	0.1		1.7	V
V_{DIFF_IN}	Differential Input Swing	IN, /IN, see Figure 1b.	0.2			V
R_{IN}	IN-to- V_T Resistance		40	50	60	Ω
IN to V_T					1.28	V

LVTTL/CMOS DC ELECTRICAL CHARACTERISTICS⁽⁴⁾

$V_{CC} = 2.5V \pm 5\%$ or $3.3V \pm 10\%$; $T_A = -40^\circ C$ to $85^\circ C$

Symbol	Parameter	Condition	Min	Typ	Max	Units
V_{IH}	Input HIGH Voltage		2.0			V
V_{IL}	Input LOW Voltage				0.8	V
I_{IH}	Input HIGH Current				40	μA
I_{IL}	Input LOW Current		-300			μA

Notes:

1. Permanent device damage may occur if ratings in the "Absolute Maximum Ratings" section are exceeded. This is a stress rating only and functional operation is not implied for conditions other than those detailed in the operational sections of this data sheet. Exposure to absolute maximum ratings conditions for extended periods may affect device reliability.
2. The data sheet limits are not guaranteed if the device is operated beyond the operating ratings.
3. Thermal performance assumes exposed pad is soldered (or equivalent) to the device's most negative potential (GND) on the PCB. θ_{JA} uses 4-layer in still-air, unless otherwise stated.
4. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.
5. V_{IH} (min) not lower than 1.2V.

CML OUTPUT DC ELECTRICAL CHARACTERISTICS⁽⁶⁾

V_{CC} = +3.3V ±10% or +2.5V ±5%; R_L = 100Ω across each pair; T_A = -40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
V _{OH}	Output HIGH Voltage	Q0, /Q0; Q1, /Q1	V _{CC} -0.020		V _{CC}	V
V _{OUT}	Output Voltage Swing	Q0, /Q0; Q1, /Q1; see Figure 1a.	325	400	500	mV
V _{DIFF_OUT}	Differential Voltage Swing	Q0, /Q0; Q1, /Q1; see Figure 1b.	650	800	1000	mV
R _{OUT}	Output Source Impedance	Q0, /Q0; Q1, /Q1	40	50	60	Ω

Notes:

6. The circuit is designed to meet the DC specifications shown in the above table after thermal equilibrium has been established.

AC ELECTRICAL CHARACTERISTICS⁽⁷⁾

V_{CC} = +2.5V ±5% or +3.3V ±10%; R_L = 100Ω across each output pair; T_A = -40°C to +85°C, unless otherwise stated.

Symbol	Parameter	Condition	Min	Typ	Max	Units
f _{MAX}	Maximum Operating Frequency	V _{IN} ≥ 100mV; V _{OUT} ≥ 200mV Clock	6			GHz
		NRZ Data	10.7			Gbps
t _{pd}	Propagation Delay	IN-to-Q	200		350	ps
		SEL-to-Q	100		400	ps
t _{SKEW}	Channel-to-Channel Skew (Within Bank)	Note 8			20	ps
	Part-to-Part Skew	Note 9			75	ps
t _{JITTER}	Clock	Cycle-to-Cycle Jitter	Note 10		1	ps _{RMS}
		Total Jitter	Note 11		10	ps _{PP}
	Data	Random Jitter	Note 12		1	ps _{RMS}
		Deterministic Jitter	Note 13		10	ps _{PP}
	Crosstalk Induced Jitter Adjacent Channel	Note 14			0.7	ps _{RMS}
t _r , t _f	Output Rise/Fall Time	20% to 80% at full swing.	25		60	ps

Notes:

- High frequency AC-parameters are guaranteed by design and characterization.
- Skew is measured between outputs of the same bank under identical transitions.
- Skew is defined for two parts with identical power supply voltages at the same temperature and with no skew of the edges at the respective inputs.
- Cycle-to-cycle jitter definition: The variation of periods between adjacent cycles, T_n-T_{n-1} where T is the time between rising edges of the output signal.
- Total jitter definition: With an ideal clock input of frequency ≤ f_{MAX}, no more than one output edge in 10¹² output edges will deviate by more than the specified peak-to-peak jitter value.
- Random jitter is measured with a K28.7 comma detect character pattern, measured at 2.5Gbps-3.2Gbps.
- Deterministic jitter is measured at 2.5Gbps-3.2Gbps with both K28.5 and 2²³-1 PRBS pattern.
- Crosstalk induced jitter is defined as the added jitter that results from signals applied to two adjacent channels. It is measured at the output while applying similar, differential clock frequencies that are asynchronous with respect to each other at inputs.

SINGLE-ENDED AND DIFFERENTIAL SWINGS

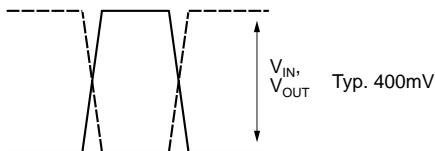


Figure 1a. Single-Ended Voltage Swing

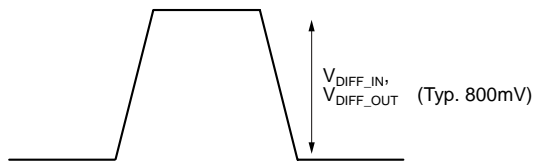


Figure 1b. Differential Voltage Swing

TIMING DIAGRAM

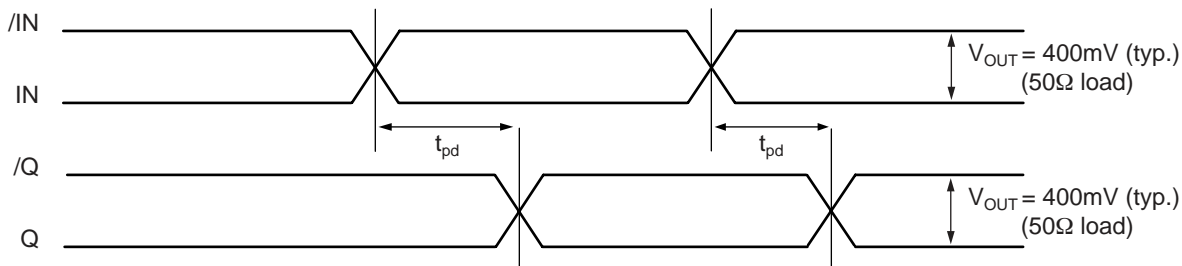
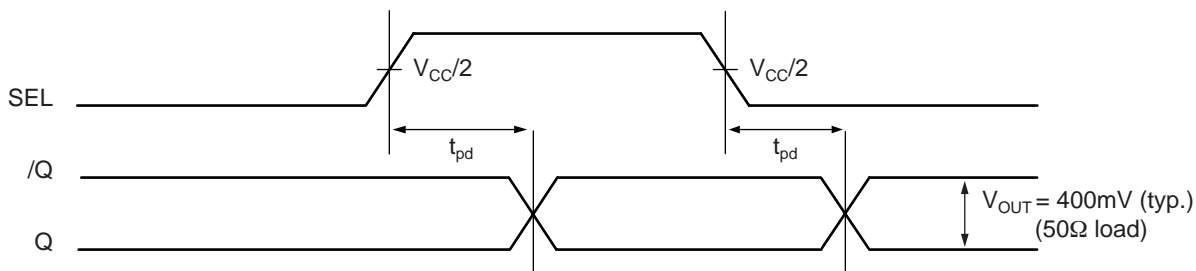


Figure 2a. AC Timing Diagram IN-to-Q

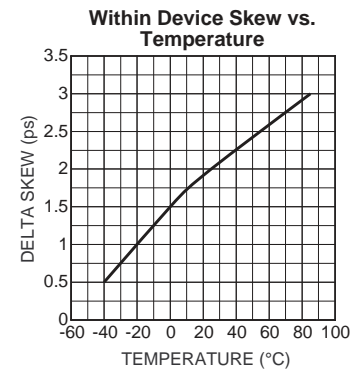
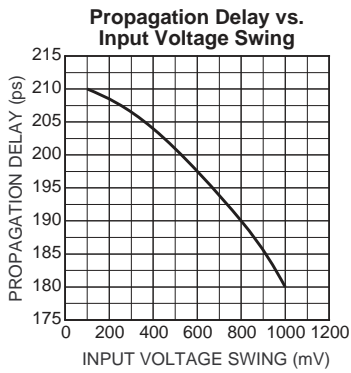
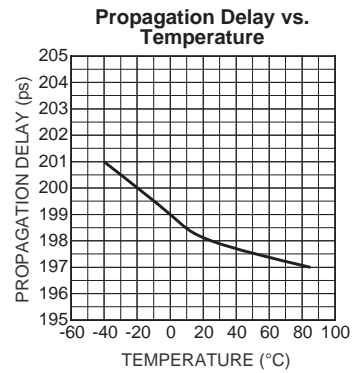
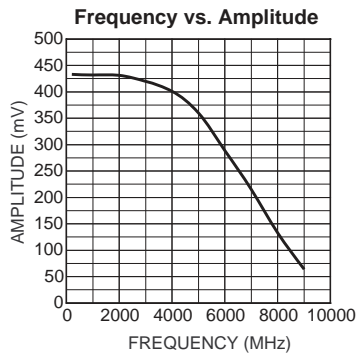


IN0, /IN1 = LOW, /IN0, IN1 = HIGH

Figure 2b. AC Timing Diagram SEL-to-Q

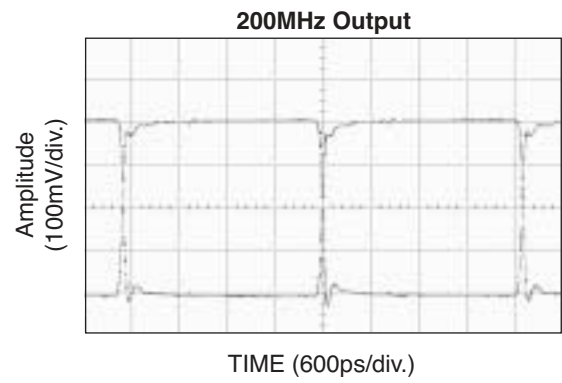
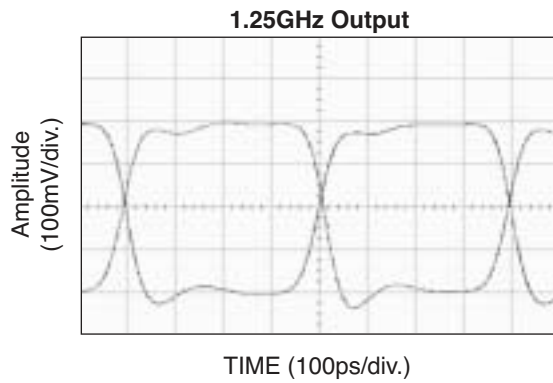
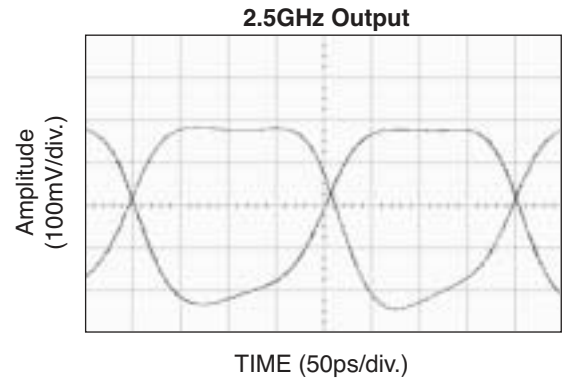
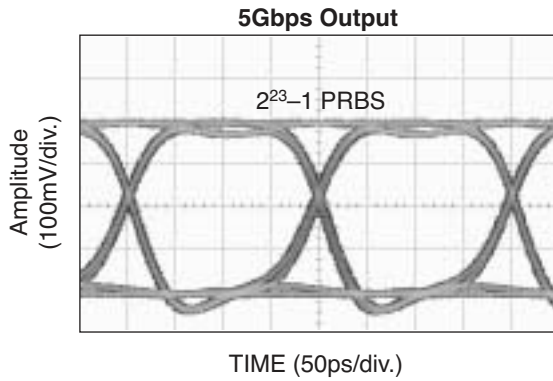
TYPICAL OPERATING CHARACTERISTICS

$V_{CC} = 2.5V$, $V_{IN} = 100mV$, $T_A = 25^{\circ}C$, unless otherwise noted.



FUNCTIONAL CHARACTERISTICS

$V_{CC} = 2.5V$, $V_{IN} = 100mV$, $T_A = 25^\circ C$, unless otherwise noted.



INPUT STAGE

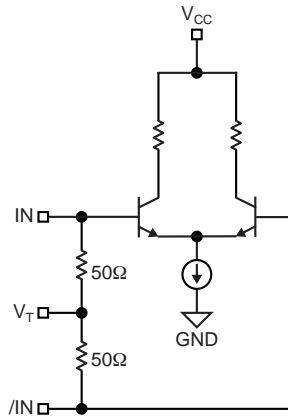


Figure 3. Simplified Differential Input Buffer

INPUT INTERFACE APPLICATIONS

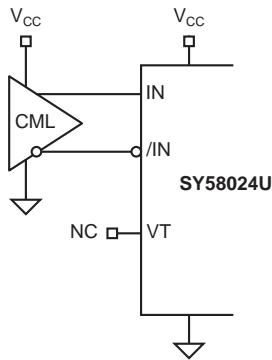
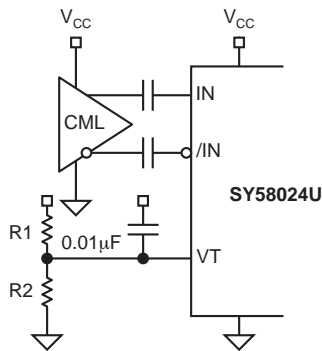


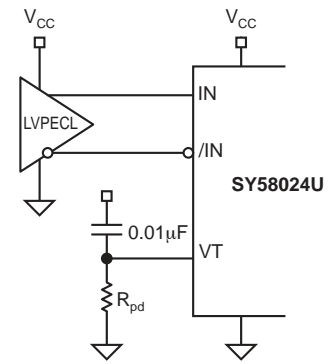
Figure 4a. DC-Coupled CML Input Interface

Option: may connect VT to Vcc



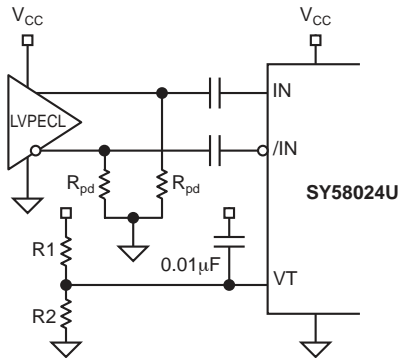
For 2.5V, R1 = 1kΩ, R2 = 1.1kΩ.
For 3.3V, R1 = 649Ω, R2 = 1kΩ.

Figure 4b. AC-Coupled CML Input Interface



For 2.5V, Rpd = 19Ω.
For 3.3V, Rpd = 50Ω.

Figure 4c. DC-Coupled LVPECL Input Interface



For 2.5V, Rpd = 50Ω, R1 = 1kΩ, R2 = 1.1kΩ.
For 3.3V, Rpd = 100Ω, R1 = 649Ω, R2 = 1kΩ.

Figure 4d. AC-Coupled LVPECL Input Interface

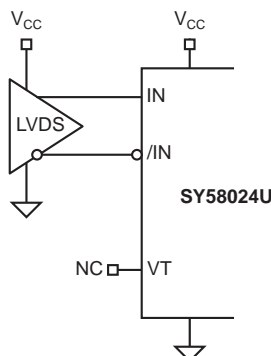


Figure 4e. LVDS Input Interface

CML OUTPUT TERMINATION

Figures 5 and Figure 6 illustrates how to terminate a CML output using both the AC-coupled and DC-coupled configuration. All outputs of the SY58024U are 50Ω with a 16mA current source.

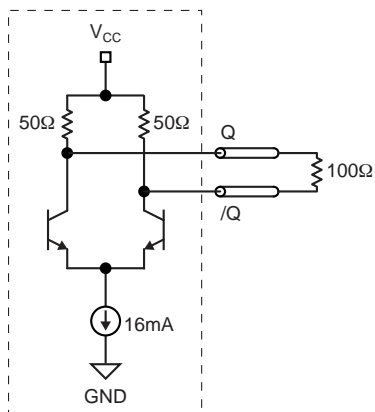


Figure 5. CML DC-Coupled Termination

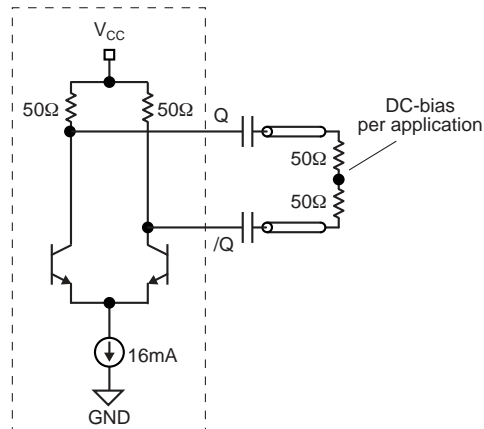
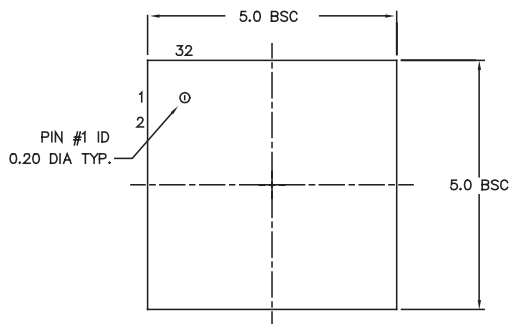


Figure 6. CML AC-Coupled Termination

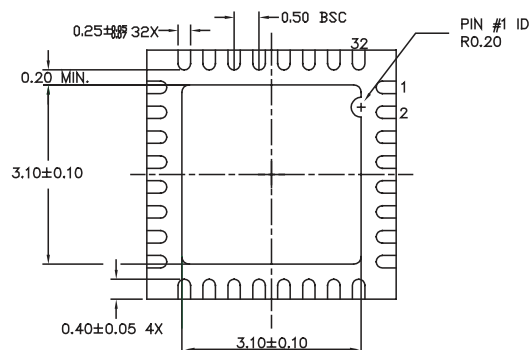
RELATED PRODUCT AND SUPPORT DOCUMENTATION

Part Number	Function	Data Sheet Link
SY58023U	Ultra-low Jitter 2x2 Crosspoint Switch w/CML Outputs and Internal I/O Termination	http://www.micrel.com/product-info/products/SY58023U.shtml
SY58024U	Ultra-low Jitter Dual 2x2 Crosspoint Switch w/CML Outputs and Internal I/O Termination	http://www.micrel.com/product-info/products/sy58024u.shtml
	32-MLF Manufacturing Guidelines Exposed Pad Application Note	www.amkor.com/products/notes_papers/MLF_AppNote.pdf
	HBW Solutions	http://www.micrel.com/product-info/as/solutions.shtml

32-PIN MicroLeadFrame® (MLF-32)



TOP VIEW



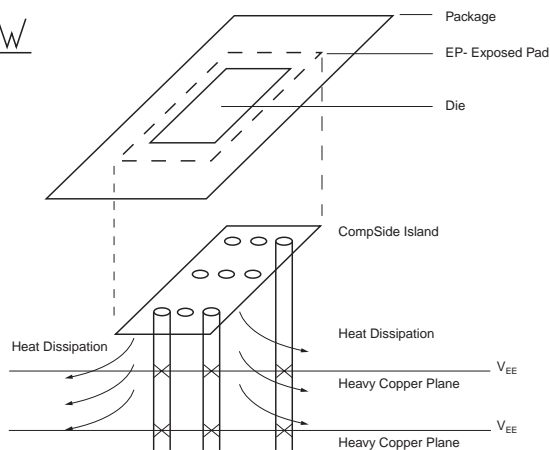
BOTTOM VIEW



SIDE VIEW

NOTE:

1. ALL DIMENSIONS ARE IN MILLIMETERS.
2. MAX. PACKAGE WARPAGE IS 0.05 mm.
3. MAXIMUM ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
4. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



**PCB Thermal Consideration for 32-Pin MLF® Package
(Always solder, or equivalent, the exposed pad to the PCB)**

Package Notes:

1. Package meets Level 2 qualification.
2. All parts are dry-packaged before shipment.
3. Exposed pads must be soldered to a ground for proper thermal management.

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