

512K (32K x 16) Static RAM

Features

- Pin- and function-compatible with CY7C1020V33
- Temperature Ranges
 - Commercial: 0°C to 70°C
 - Industrial: -40°C to 85°C
 - Automotive: -40°C to 125°C
- High speed
 - $t_{AA} = 10$ ns
- CMOS for optimum speed/power
- Low active power
 - 325 mW (max.)
- Automatic power-down when deselected
- Independent control of upper and lower bits
- Available in Pb-free and non Pb-free 44-pin TSOP II package

Functional Description

The CY7C1020CV33 is a high-performance CMOS static RAM organized as 32,768 words by 16 bits. This device has an automatic power-down feature that significantly reduces power consumption when deselected.

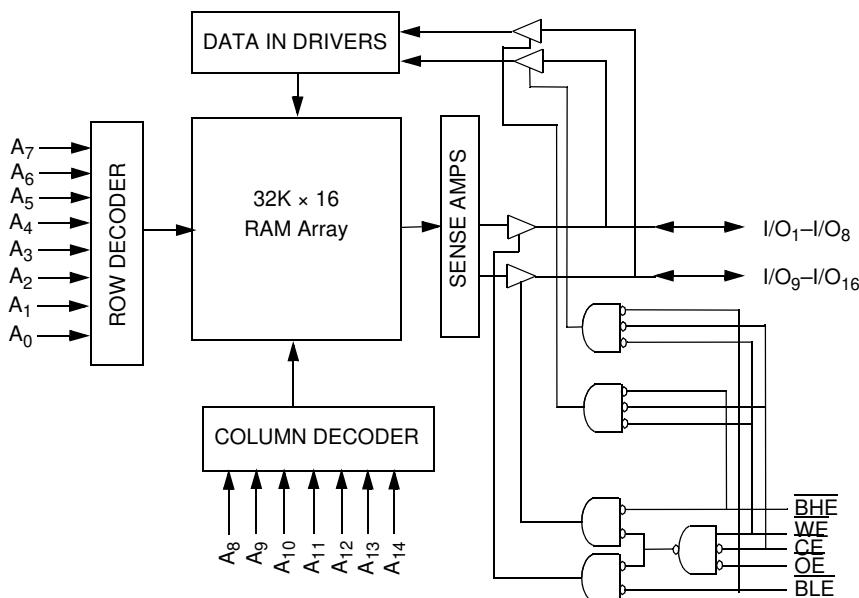
Writing to the device is accomplished by taking Chip Enable (\overline{CE}) and Write Enable (\overline{WE}) inputs LOW. If Byte Low Enable (\overline{BLE}) is LOW, then data from I/O pins (I/O_1 through I/O_8), is written into the location specified on the address pins (A_0 through A_{14}). If Byte High Enable (\overline{BHE}) is LOW, then data from I/O pins (I/O_9 through I/O_{16}) is written into the location specified on the address pins (A_0 through A_{14}).

Reading from the device is accomplished by taking Chip Enable (\overline{CE}) and Output Enable (\overline{OE}) LOW while forcing the Write Enable (\overline{WE}) HIGH. If Byte Low Enable (\overline{BLE}) is LOW, then data from the memory location specified by the address pins will appear on I/O_1 to I/O_8 . If Byte High Enable (\overline{BHE}) is LOW, then data from memory will appear on I/O_9 to I/O_{16} . See the truth table at the back of this data sheet for a complete description of read and write modes.

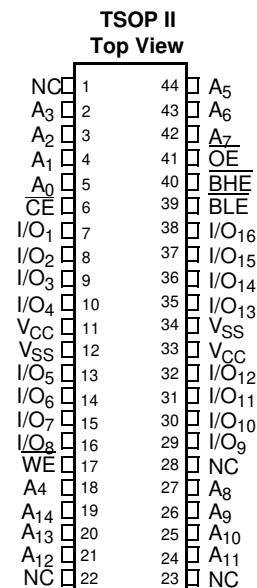
The input/output pins (I/O_1 through I/O_{16}) are placed in a high-impedance state when the device is deselected (\overline{CE} HIGH), the outputs are disabled (\overline{OE} HIGH), the \overline{BHE} and \overline{BLE} are disabled (\overline{BHE} , \overline{BLE} HIGH), or during a write operation (\overline{CE} LOW, and \overline{WE} LOW).

The CY7C1020CV33 is available in standard 44-pin TSOP Type II package.

Logic Block Diagram



Pin Configuration^[1]



Note:

1. NC pins are not connected on the die

Selection Guide

		-10	-12	-15	Unit
Maximum Access Time		10	12	15	ns
Maximum Operating Current	Com'l/Ind'l	90	85	80	mA
	Automotive	-	-	85	mA
Maximum CMOS Standby Current	Com'l/Ind'l	5	5	5	mA
	Automotive	-	-	10	mA

Pin Definitions

Pin Name	TSOP - Pin Number	I/O Type	Description
A ₀ -A ₁₄	5, 4, 3, 2, 18, 44, 43, 42, 27, 26, 25, 24, 21, 20, 19	Input	Address Inputs used to select one of the address locations.
I/O ₁ -I/O ₁₆	7-10, 13-16, 29-32, 35-38	Input/Output	Bidirectional Data I/O lines. Used as input or output lines depending on operation.
NC	1, 22, 23, 28	No Connect	No Connects. Not connected to the die.
\overline{WE}	17	Input/Control	Write Enable Input, active LOW. When selected LOW, a Write is conducted. When deselected HIGH, a Read is conducted.
\overline{CE}	6	Input/Control	Chip Enable Input, active LOW. When LOW, selects the chip. When HIGH, deselects the chip.
\overline{BHE} , \overline{BLE}	40, 39	Input/Control	Byte Write Select Inputs, active LOW. \overline{BHE} controls I/O ₁₆ -I/O ₉ , \overline{BLE} controls I/O ₈ -I/O ₁ .
\overline{OE}	41	Input/Control	Output Enable, active LOW. Controls the direction of the I/O pins. When LOW, the I/O pins are allowed to behave as outputs. When deasserted HIGH, I/O pins are tri-stated, and act as input data pins.
V _{SS}	12, 34	Ground	Ground for the device. Should be connected to ground of the system.
V _{CC}	11, 33	Power Supply	Power Supply inputs to the device.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature	-65°C to +150°C
Ambient Temperature with Power Applied.....	-55°C to +125°C
Supply Voltage on V _{CC} to Relative GND ^[1]	-0.5V to +4.6V
DC Voltage Applied to Outputs in High-Z State ^[2]	-0.5V to V _{CC} + 0.5V
DC Input Voltage ^[2]	-0.5V to V _{CC} + 0.5V

Current into Outputs (LOW).....	20 mA
Static Discharge Voltage.....	> 2001V (per MIL-STD-883, Method 3015)
Latch-up Current.....	> 200 mA

Operating Range

Range	Ambient Temperature	V _{CC}
Commercial	0°C to +70°C	3.3V ± 10%
Industrial	-40°C to +85°C	3.3V ± 10%
Automotive	-40°C to +125°C	3.3V ± 10%

Electrical Characteristics Over the Operating Range

Parameter	Description	Test Conditions	-10		-12		-15		Unit	
			Min.	Max.	Min.	Max.	Min.	Max.		
V _{OH}	Output HIGH Voltage	V _{CC} = Min., I _{OH} = -4.0 mA	2.4		2.4		2.4		V	
V _{OL}	Output LOW Voltage	V _{CC} = Min., I _{OL} = 8.0 mA		0.4		0.4		0.4	V	
V _{IH}	Input HIGH Voltage		2.0	V _{CC} + 0.3	2.0	V _{CC} + 0.3	2.0	V _{CC} + 0.3	V	
V _{IL}	Input LOW Voltage ^[2]		-0.3	0.8	-0.3	0.8	-0.3	0.8	V	
I _{IX}	Input Leakage Current	GND ≤ V _I ≤ V _{CC}	Com'l/Ind'l	-1	+1	-1	+1	-1	+1	μA
			Auto					-20	+20	μA
I _{OZ}	Output Leakage Current	GND ≤ V _I ≤ V _{CC} , Output Disabled	Com'l/Ind'l	-1	+1	-1	+1	-1	+1	μA
			Auto					-20	+20	μA
I _{CC}	V _{CC} Operating Supply Current	V _{CC} = Max., I _{OUT} = 0 mA, f = f _{MAX} = 1/t _{RC}	Com'l/Ind'l		90		85		80	mA
			Auto						85	mA
I _{SB1}	Automatic CE Power-down Current —TTL Inputs	Max. V _{CC} , CE ≥ V _{IH} , V _{IN} ≥ V _{IH} or V _{IN} ≤ V _{IL} , f = f _{MAX}	Com'l/Ind'l		15		15		15	mA
			Auto						20	mA
I _{SB2}	Automatic CE Power-down Current —CMOS Inputs	Max. V _{CC} , CE ≥ V _{CC} - 0.3V, V _{IN} ≥ V _{CC} - 0.3V, or V _{IN} ≤ 0.3V, f = 0	Com'l/Ind'l		5		5		5	mA
			Auto						10	mA

Capacitance^[3]

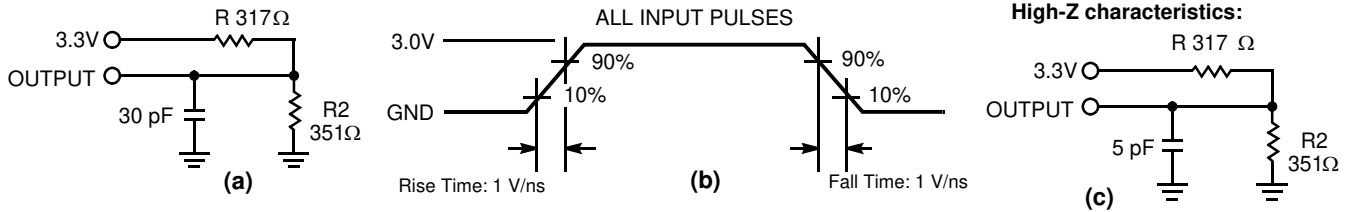
Parameter	Description	Test Conditions	Max.	Unit
C _{IN}	Input Capacitance	T _A = 25°C, f = 1 MHz, V _{CC} = 3.3V	8	pF
C _{OUT}	Output Capacitance			

Thermal Resistance^[3]

Parameter	Description	Test Conditions	44-pin TSOP-II	Unit
θ _{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, per EIA/JESD51.	76.92	°C/W
θ _{JC}	Thermal Resistance (Junction to Case)		15.86	°C/W

Notes:

- V_{IL} (min.) = -2.0V and V_{IH} (max) = V_{CC} + 0.5V for pulse durations of less than 20 ns.
- Tested initially and after any design or process changes that may affect these parameters.

AC Test Loads and Waveforms^[4]

Switching Characteristics Over the Operating Range^[4]

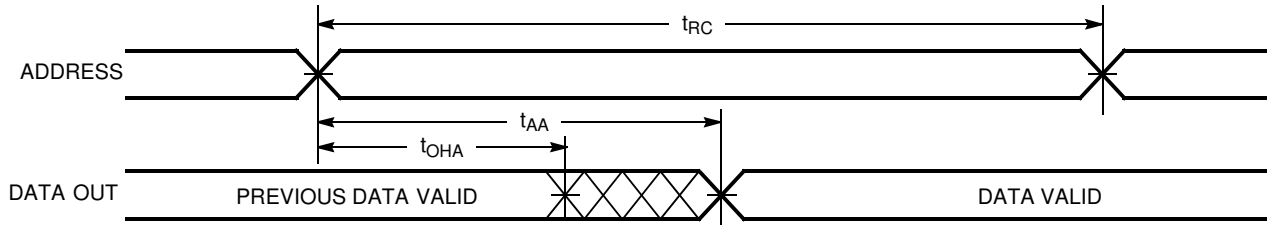
Parameter	Description	-10		-12		-15		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	
Read Cycle								
t_{RC}	Read Cycle Time	10		12		15		ns
t_{AA}	Address to Data Valid		10		12		15	ns
t_{OHA}	Data Hold from Address Change	3		3		3		ns
t_{ACE}	\overline{CE} LOW to Data Valid		10		12		15	ns
t_{DOE}	\overline{OE} LOW to Data Valid		5		6		7	ns
t_{LZOE}	\overline{OE} LOW to Low-Z ^[5]	0		0		0		ns
t_{HZOE}	\overline{OE} HIGH to High-Z ^[5, 6]		5		6		7	ns
t_{LZCE}	\overline{CE} LOW to Low-Z ^[5]	3		3		3		ns
t_{HZCE}	\overline{CE} HIGH to High-Z ^[5, 6]		5		6		7	ns
$t_{PU}^{[7]}$	\overline{CE} LOW to Power-up	0		0		0		ns
$t_{PD}^{[7]}$	\overline{CE} HIGH to Power-down		10		12		15	ns
t_{DBE}	Byte Enable to Data Valid		5		6		7	ns
t_{LZBE}	Byte Enable to Low-Z	0		0		0		ns
t_{HZBE}	Byte Disable to High-Z		5		6		7	ns
Write Cycle^[8]								
t_{WC}	Write Cycle Time	10		12		15		ns
t_{SCE}	\overline{CE} LOW to Write End	8		9		10		ns
t_{AW}	Address Set-up to Write End	7		8		10		ns
t_{HA}	Address Hold from Write End	0		0		0		ns
t_{SA}	Address Set-up to Write Start	0		0		0		ns
t_{PWE}	\overline{WE} Pulse Width	7		8		10		ns
t_{SD}	Data Set-up to Write End	5		6		8		ns
t_{HD}	Data Hold from Write End	0		0		0		ns
t_{LZWE}	\overline{WE} HIGH to Low-Z ^[5]	3		3		3		ns
t_{HZWE}	\overline{WE} LOW to High-Z ^[5, 6]		5		6		7	ns
t_{BW}	Byte Enable to End of Write	7		8		9		ns

Notes:

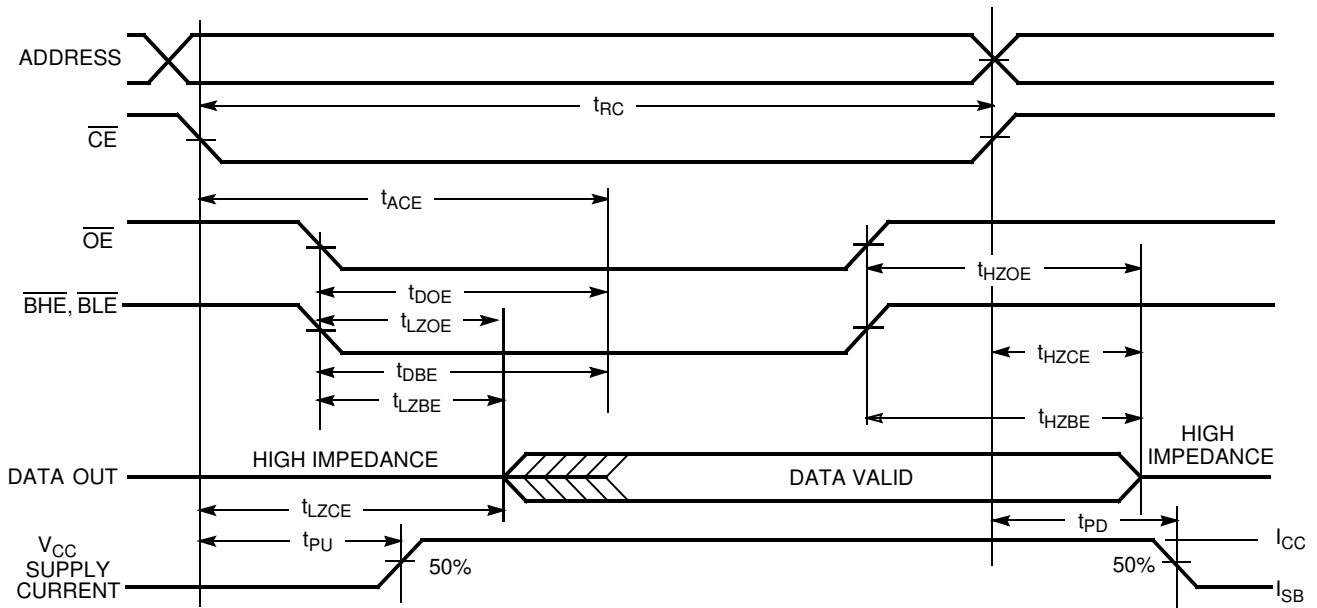
4. Test conditions assume signal transition time of 3 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V.
5. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE} , t_{HZOE} is less than t_{LZOE} , and t_{HZWE} is less than t_{LZWE} for any given device.
6. t_{HZOE} , t_{HZBE} , t_{HZCE} , and t_{HZWE} are specified with a load capacitance of 5 pF as in part (c) of AC Test Loads. Transition is measured ± 500 mV from steady-state voltage.
7. This parameter is guaranteed by design and is not tested.
8. The internal Write time of the memory is defined by the overlap of \overline{CE} LOW, \overline{WE} LOW and $\overline{BHE}/\overline{BLE}$ LOW. \overline{CE} , \overline{WE} and $\overline{BHE}/\overline{BLE}$ must be LOW to initiate a Write, and the transition of these signals can terminate the Write. The input data set-up and hold timing should be referenced to the leading edge of the signal that terminates the Write.

Switching Waveforms

Read Cycle No. 1^[9, 10]



Read Cycle No. 2 (\overline{OE} Controlled)^[10, 11]

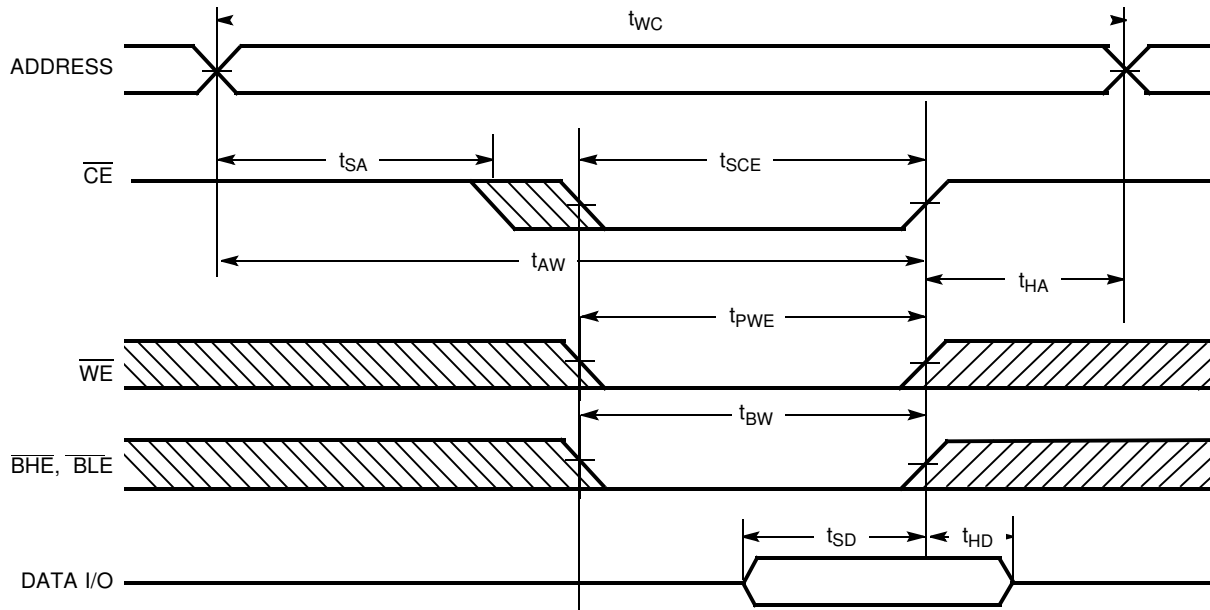


Notes:

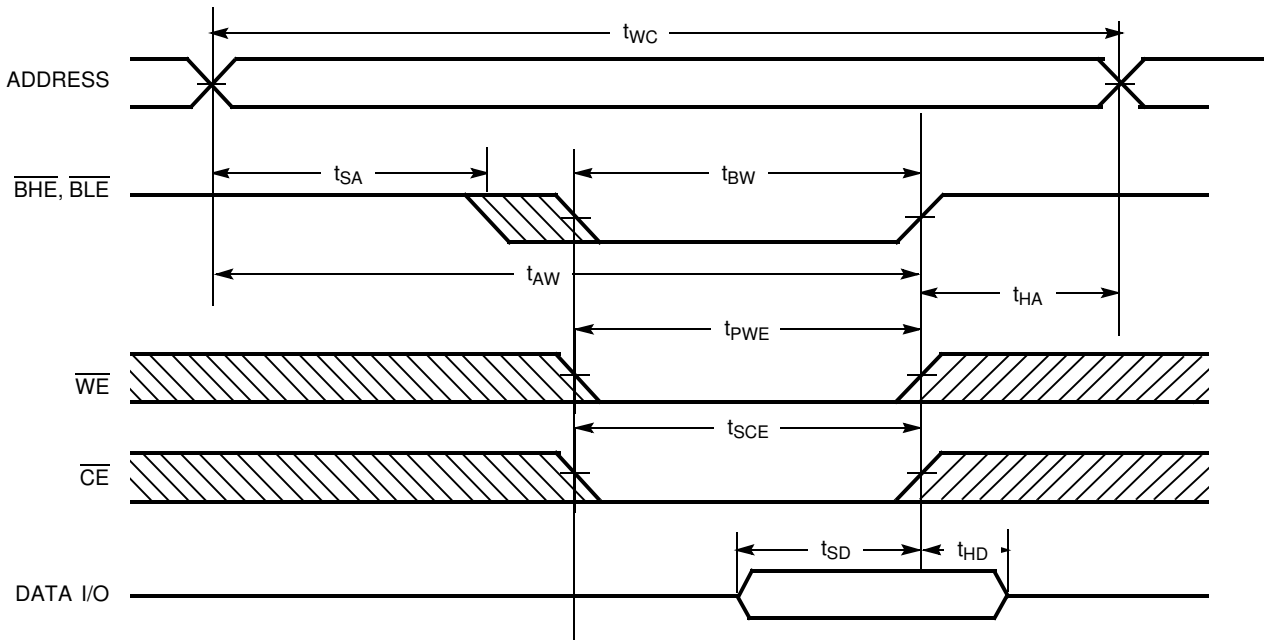
- 9. Device is continuously selected. \overline{OE} , \overline{CE} , \overline{BHE} and/or \overline{BLE} = V_{IL} .
- 10. \overline{WE} is HIGH for Read cycle.
- 11. Address valid prior to or coincident with \overline{CE} transition LOW.

Switching Waveforms (continued)

Write Cycle No. 1 (\overline{CE} Controlled)^[12, 13]



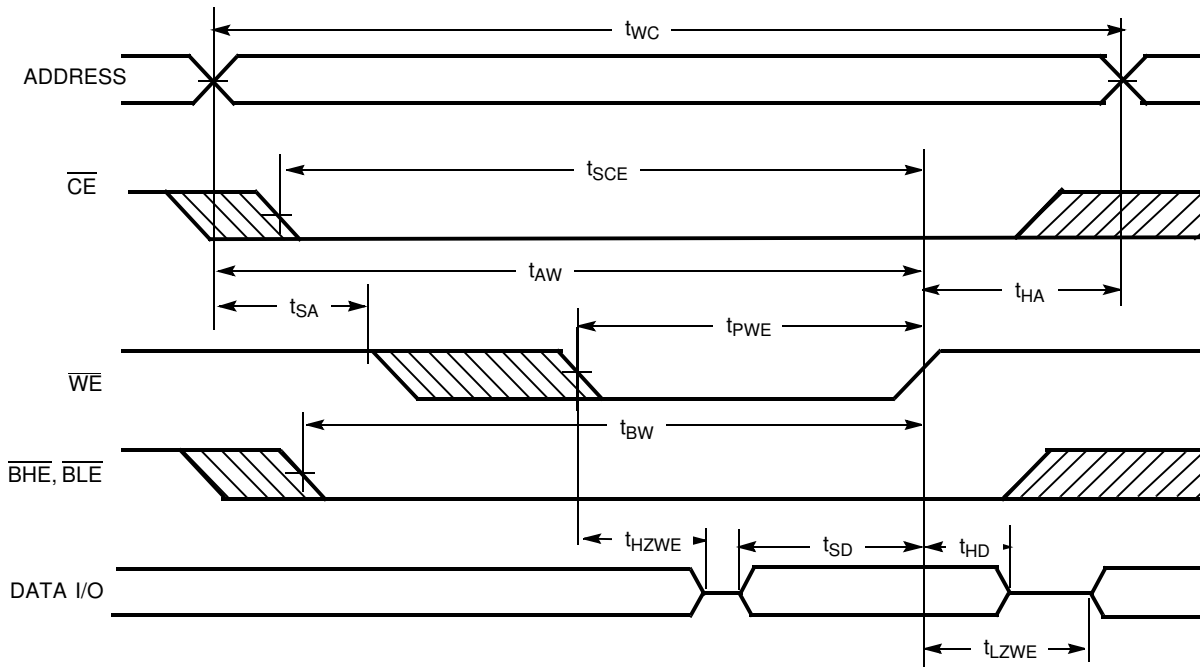
Write Cycle No. 2 (\overline{BLE} or \overline{BHE} Controlled)



Notes:

- 12. Data I/O is high impedance if \overline{CE} or \overline{BHE} and/or $\overline{BLE} = V_{IH}$.
- 13. If \overline{CE} goes HIGH simultaneously with \overline{WE} going HIGH, the output remains in a high-impedance state.

Switching Waveforms (continued)

Write Cycle No. 3 (\overline{WE} Controlled, \overline{OE} LOW)

Truth Table

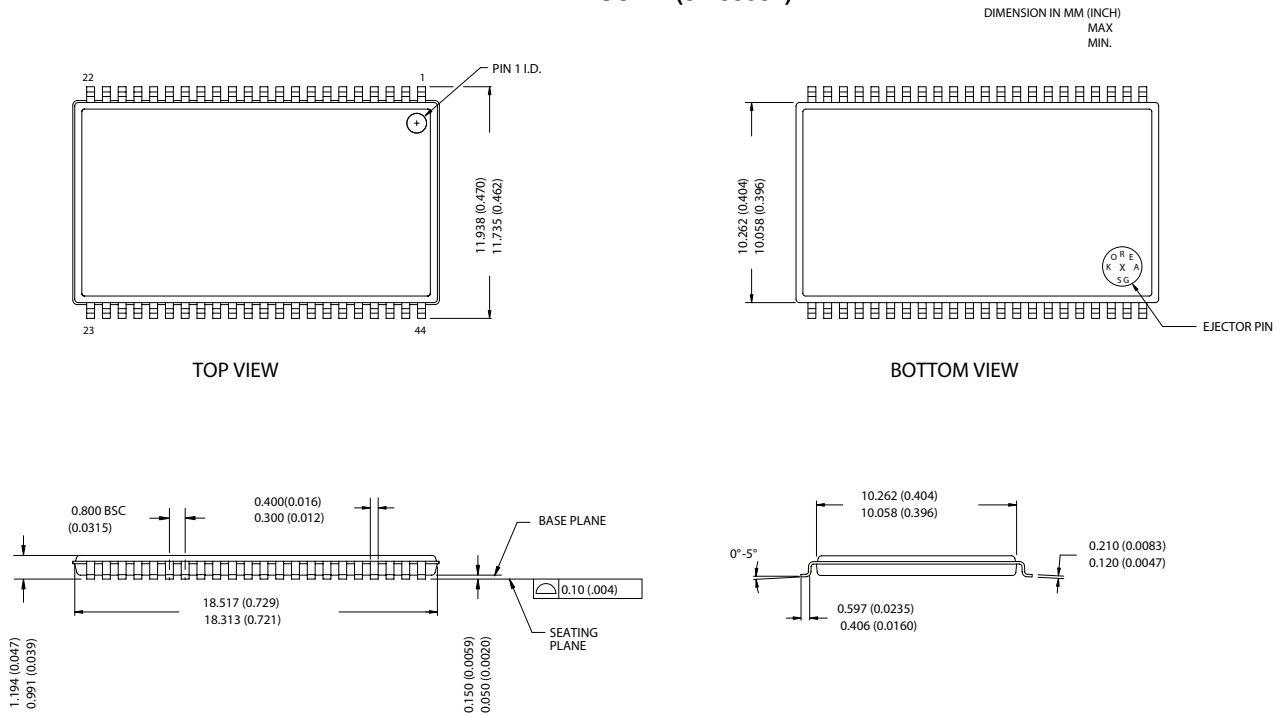
CE	OE	WE	BLE	BHE	I/O ₁ -I/O ₈	I/O ₉ -I/O ₁₆	Mode	Power
H	X	X	X	X	High-Z	High-Z	Power-down	Standby (I_{SB})
L	L	H	L	L	Data Out	Data Out	Read—All bits	Active (I_{CC})
			L	H	Data Out	High-Z	Read—Lower bits only	Active (I_{CC})
			H	L	High-Z	Data Out	Read—Upper bits only	Active (I_{CC})
L	X	L	L	L	Data In	Data In	Write—All bits	Active (I_{CC})
			L	H	Data In	High-Z	Write—Lower bits only	Active (I_{CC})
			H	L	High-Z	Data In	Write—Upper bits only	Active (I_{CC})
L	H	H	X	X	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})
L	X	X	H	H	High-Z	High-Z	Selected, Outputs Disabled	Active (I_{CC})

Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
10	CY7C1020CV33-10ZC	51-85087	44-pin TSOP Type II	Commercial
	CY7C1020CV33-10ZXC		44-pin TSOP Type II (Pb-Free)	
12	CY7C1020CV33-12ZC		44-pin TSOP Type II	Commercial
15	CY7C1020CV33-15ZC		44-pin TSOP Type II	Commercial
	CY7C1020CV33-15ZE		44-pin TSOP Type II	Automotive
	CY7C1020CV33-15ZSXE		44-pin TSOP Type II (Pb-Free)	

Package Diagrams

44-Pin TSOP II (51-85087)



51-85087-*A

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Document History Page

Document Title: CY7C1020CV33 512K (32K x 16) Static RAM				
Document Number: 38-05133				
REV.	ECN NO.	Issue Date	Orig. of Change	Description of Change
**	109428	12/16/01	HGK	New Data Sheet
*A	115045	05/30/02	HGK	I _{CC} and I _{SB1} data modified
*B	117615	08/14/02	DFP	Pin 1 = NC Pin 18 = A4; remove SOJ package option; remove 8ns option.
*C	262949	See ECN	RKF	Added Automotive Specs to Data sheet
*D	334398	See ECN	SYT	Added Lead-Free Product Information
*E	493543	See ECN	NXR	Added note #1 on page #1 Changed the description of I _{Ix} from Input Load Current to Input Leakage Current in DC Electrical Characteristics table Removed I _{OS} parameter from DC Electrical Characteristics table Updated Ordering Information Table