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GENERAL DESCRIPTION

The DS26522DK is an easy-to-use demo kit for the DS26522 T1/E1/J1 dual transceiver. The DS26522DK is a stand-alone system. The board comes complete with a transceiver, transformer, termination resistors, configuration switches, network connectors, microprocessor, and RS-232 connector. The on-board processor and Dallas' ChipView software give point-and-click access to configuration and status registers from a Windows®-based PC. On-board LEDs indicate receive loss-of-signal and interrupt status, as well as multiple clock and signal routing configurations.

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DEMO KIT CONTENTS

- DS26522DK PCB
- CD_ROM Including:
 - ChipView Software
 - DS26522 Definition files
 - DS26522 Initialization files
 - DS26522DK Data Sheet
 - DS26522 Data Sheet
- DS26522 Errata Sheet (if applicable)

FEATURES

- Demonstrates Key Functions of DS26522 T1/E1/J1 Dual Transceiver
- Includes Transceiver, Transformers, and Termination Passives
- BNC Connections for 75Ω E1
- RJ48 Connector for 120Ω E1 and 100Ω T1
- On-Board Processor and ChipView Software Provide Point-and-Click Access to the DS26522 Register Set
- Accessible Address/Data Bus with Tri-State Control to Allow Interface for External Processor
- All Equipment-Side Framer Pins are Easily Accessible for External Data Source/Sink
- LEDs for Loss-of-Signal and Interrupt Status
- Easy-to-Read Silkscreen Labels Identify the Signals Associated with All Connectors, Jumpers, and LEDs

ORDERING INFORMATION

PART	DESCRIPTION
DS26522DK	Demo kit for DS26522

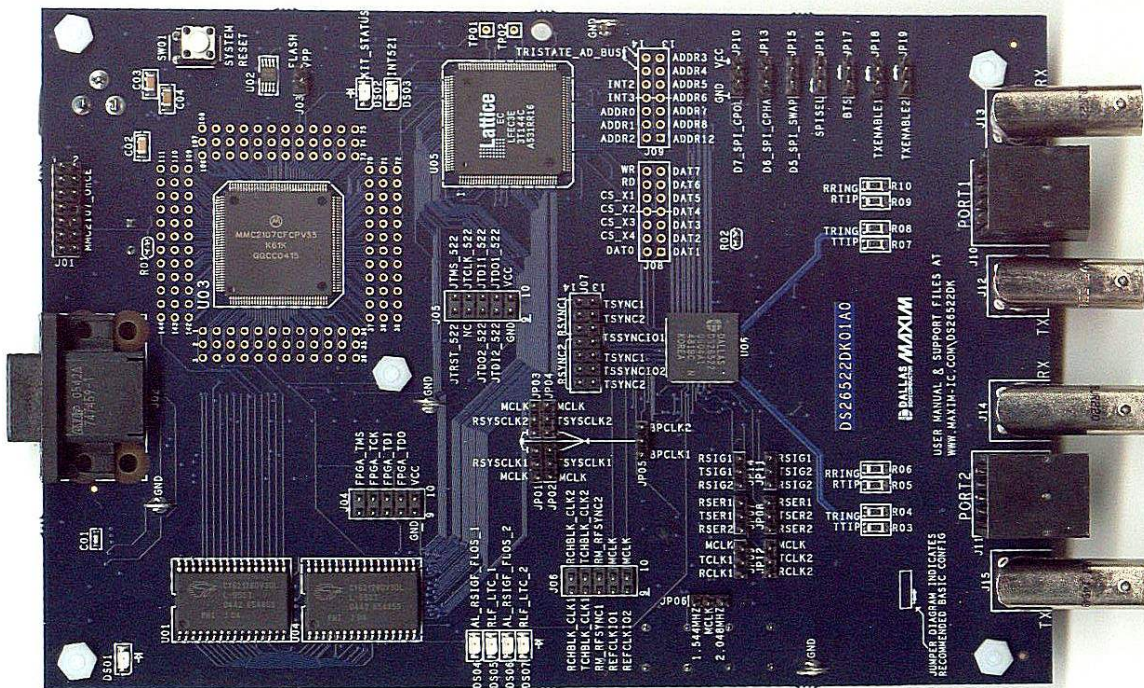


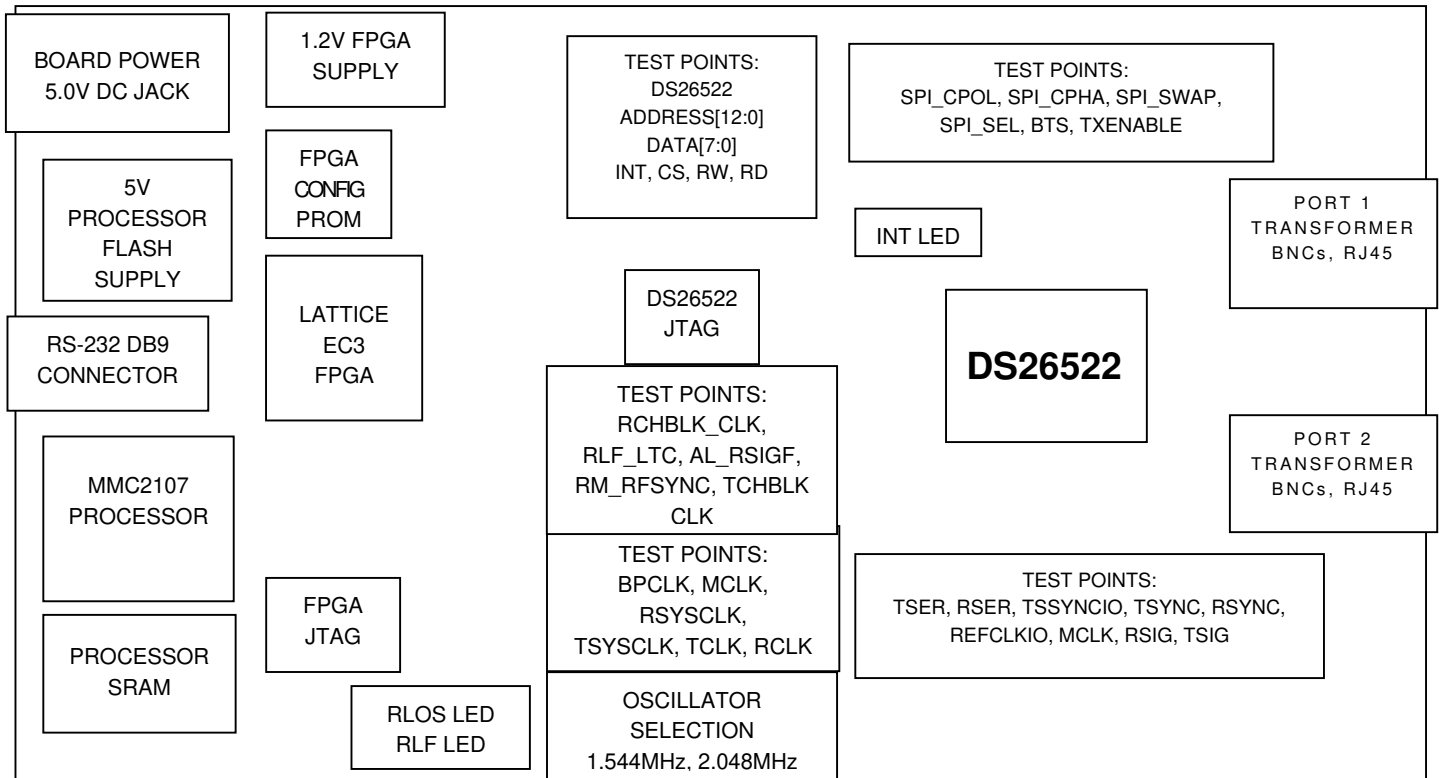
TABLE OF CONTENTS

1.	BOARD FLOORPLAN	3
2.	PCB ERRATA	3
3.	BASIC OPERATION	4
3.1	HARDWARE CONFIGURATION	4
3.1.1	<i>General</i>	4
3.2	QUICK SETUP (REGISTER VIEW)	4
3.2.1	<i>Miscellaneous</i>	4
4.	ADDRESS MAP	5
5.	TEST POINTS AND CONNECTORS	5
6.	ADDITIONAL INFORMATION/RESOURCES	6
6.1	DS26522 INFORMATION.....	6
6.2	DS26522DK INFORMATION.....	6
6.3	TECHNICAL SUPPORT	6
7.	COMPONENT LIST	7
8.	SCHEMATICS	9

LIST OF TABLES

Table 4-1.	Address Map	5
Table 5-1.	Main Board PCB Configuration	5

1. BOARD FLOORPLAN



2. PCB ERRATA

DS26522DK01A0

4/17/2006:

A 100pF capacitor has been added between processor reset and VCC. This was added to eliminate crosstalk issues present in the OnCE programming pod.

3. BASIC OPERATION

This design kit relies upon several supporting files, which are available for downloading on our website at www.maxim-ic.com/DS26522DK QuickView page.

3.1 Hardware Configuration

- Supply 5.0V to the wall jack receptacle on the bottom of the PCB.
- Install the following jumpers (see [Table 5-1](#)):
 - JP06: MCLK driven by 1.544MHz for T1. (Set E1 for 2.048MHz.)
 - JP01, JP03: RSYCLK driven by MCLK.
 - JP02, JP04: TSYCLK driven by MCLK.
 - JP09, JP12: TCLK driven by MCLK.
 - JP16 SPI_SEL to GND. JP17 BTS to VCC. JP18, JP19 TXENABLE to VCC.
- From the **Programs** menu, launch the host application named *ChipView.exe*. Run the ChipView application. If the default installation options were used, click the **Start** button on the Windows toolbar and select **Programs** → **ChipView** → **ChipView**.

3.1.1 General

Upon power-up, the RLF and AL_LOS LEDs (red) will be lit, but the INT LED (red) will not be lit. The board draws approximately 200mA at power-up.

3.2 Quick Setup (Register View)

- 1) The PC loads ChipView, offering a choice among DEMO MODE, REGISTER VIEW, and TERMINAL MODE. Select REGISTER VIEW.
- 2) The program will request a definition file. Navigate to the .def files in the T1 or E1 folder, then select the file named *DS26522_GLB_T1_DEV1.def* (T1 mode) or *DS26522_GLB_E1_DEV1.def* (E1 mode).
Note: Through the *Links* section, this will also load the LIU def file and framer def file.
- 3) Repeat Step 2 for *DS26522_GLB_T1_DEV2.def* (or *DS26522_GLB_E1_DEV2.def*).
- 4) The **Register View Screen** will appear, showing the register names, acronyms, and values for the DS26522.
- 5) Predefined register settings for several functions are available as initialization files.
 - .ini files are loaded by selecting the menu **File**→**Reg Ini File**→**Load Ini File**.
 - Load the .ini file *Load_T1_LBO0_0_133_impMatchOn_DEV1.ini* (T1 mode) or *Load_E1_75_impMatchOn_DEV1.ini* (E1 mode).
 - Load the .ini file *Load_T1_LBO0_0_133_impMatchOn_DEV2.ini* (T1 mode) or *Load_E1_75_impMatchOn_DEV2.ini* (E1 mode).
- 6) After loading the .ini file, the following may be observed:
 - The DS26522 begins transmitting AIS with impedance match.
 - The AL_LOS LEDs extinguishes upon external loopback.

3.2.1 Miscellaneous

The DS26522 uses three register definition files. All three files are loaded when the *DS26522_GLOBAL*.def* file is loaded. Individual files are selected from the **Def File Selection** menu in ChipView.

4. ADDRESS MAP

The on-board microcontroller is configured to start the user address space at 0x81000000. All offsets given in [Table 4-1](#) are relative to the beginning of the user address space.

Table 4-1. Address Map

OFFSET	DEVICE	DESCRIPTION
0X0000 to 0X0087	FPGA	Board identification and FPGA test registers
0X2000 to 0X3FFF	DS26522	DS26522 framer, LIU, and BERT registers on CS1
0X4000 to 0X5FFF	DS26522	DS26522 framer, LIU and BERT registers on CS2

5. TEST POINTS AND CONNECTORS

The DS26522DK has several connectors, test points, oscillators, and jumpers. [Table 5-1](#) provides a description of these signals, given in order of appearance on the PCB from left to right, then top to bottom (with the board held so that the RS-232 connector is on the top edge).

Table 5-1. Main Board PCB Configuration

SILKSCREEN REFERENCE	FUNCTION	DEFAULT SETTING	SCHEMATIC PAGE	DESCRIPTION
JB01 (PCB bottom side)	Power supply	5.0V	3	System V _{DD} . Always connected to power supply.
DS01	LED	On (green)	3	Power OK LED.
J02	RS-232 Connector	Connected to host PC	6	Used for communication with host PC. Basic setting is 57.6K baud, 8 bits, no stop bit, 1 parity bit (57.6, 8, N, 1).
J01	OnCE BDM Connector	—	6	OnCE debug connector for MMC2107 processor.
SW01	System Reset	—	4	System reset. Connects to all device reset pins.
J03	Flash VPP Jumper	Not Installed	6	Provides flash programming voltage (5V) to processor.
J04	Lattice FPGA	—	9	JTAG connector for Lattice EC3 FPGA.
DS04, DS06	LED	—	11	DS26522 LEDs. Analog loss or receive signaling freeze or framer LOS.
DS05, DS07	LED	—	11	DS26522 LEDs. Receive loss of frame or loss of transmit clock.
J05	DS26522 Test points	—	10	DS26522 JTAG chains.
J06	DS26522 Test points	—	14	DS26522 test points for RCHBLK, TCHBLK, RMSYNC, REFCLKIO.
JP01, JP03	RSYSCLK Selection	Jumpered Pins 1+2	14	RSYSCLK selection: MCLK (default), BPCLK.
JP02, JP04	TSYSCLK Selection	Jumpered Pins 1+2	14	TSYSCLK selection: MCLK (default), BPCLK.
JP05	BPCLK MUX	Jumpered Pins 1 + 2	14	BPCLK mux, driven to pin 3 of JP01, JP02, JP03, JP04.
J07	DS26522 Test points	—	14	DS26522 test points for RSYNC, TSYNC, and TSSYNCIO.
YB01, YB02 (PCB bottom side)	Oscillators	—	14	Oscillators for 2.048MHz and 1.544MHz.
J08, J09	Test points	—	8	Test points for DS26522 address/data bus and control lines.

SILKSCREEN REFERENCE	FUNCTION	DEFAULT SETTING	SCHEMATIC PAGE	DESCRIPTION
J09.12 + J09.14	Bus Tri-state	Not Jumpered	8	Install jumper to tri-state the FPGA pins that connect to the DS26522.
JP06	MCLK Selection	Jumpered Pins 2+3	14	MCLK Selection: 1.544MHz, 2.048MHz (default).
JP09, JP12	TCLK Selection	Jumpered Pins 1+2	14	TCLK Selection: MCLK (default), RCLK.
JP07, JP08	TSER Selection	Not Jumpered	14	TSERx Selection: RSER2, RSER1.
JP14, JP11	TSIG Selection	Not Jumpered	14	TSIGx Selection: RSIG2, RSIG1.
JP10	SPI_CPOL Bias	Not Jumpered	10	SPI_CPOL Selection: pulldown, pullup.
JP13	SPI_CPHA Bias	Not Jumpered	10	SPI_CPHA Selection: pulldown, pullup
JP15	SPI_SWAP Bias	Not Jumpered	10	SPI_SWAP Selection: pulldown, pullup
JP16	SPI_SEL Bias	Jumpered Pins 1+2	10	SPI_SEL Selection: pulldown (default), pullup.
JP17	BTS Bias	Jumpered Pins 2+3	10	BTS Selection: pulldown, pullup (default).
JP18, JP19	TXENABLE Bias	Jumpered Pins 2+3	10	TXENABLE Selection: pulldown, pullup (default).
J15 + J14	Network BNC	—	12	Port 2 BNC for 75Ω network connection and RJ48 network connection.
J11	Network RJ48			
J12 + J13	Network BNC	—	13	Port 1 BNC for 75Ω network connection and RJ48 network connection.
J10	Network RJ48			

6. ADDITIONAL INFORMATION/RESOURCES

6.1 DS26522 Information

For more information about the DS26522, refer to the DS26522 data sheet at www.maxim-ic.com/DS26522.

6.2 DS26522DK Information

For more information about the DS26522DK including software downloads, refer to the DS26522DK Quick View page at www.maxim-ic.com/DS26522DK.

6.3 Technical Support

For additional technical support, e-mail your questions to telecom.support@dalsemi.com.

7. COMPONENT LIST

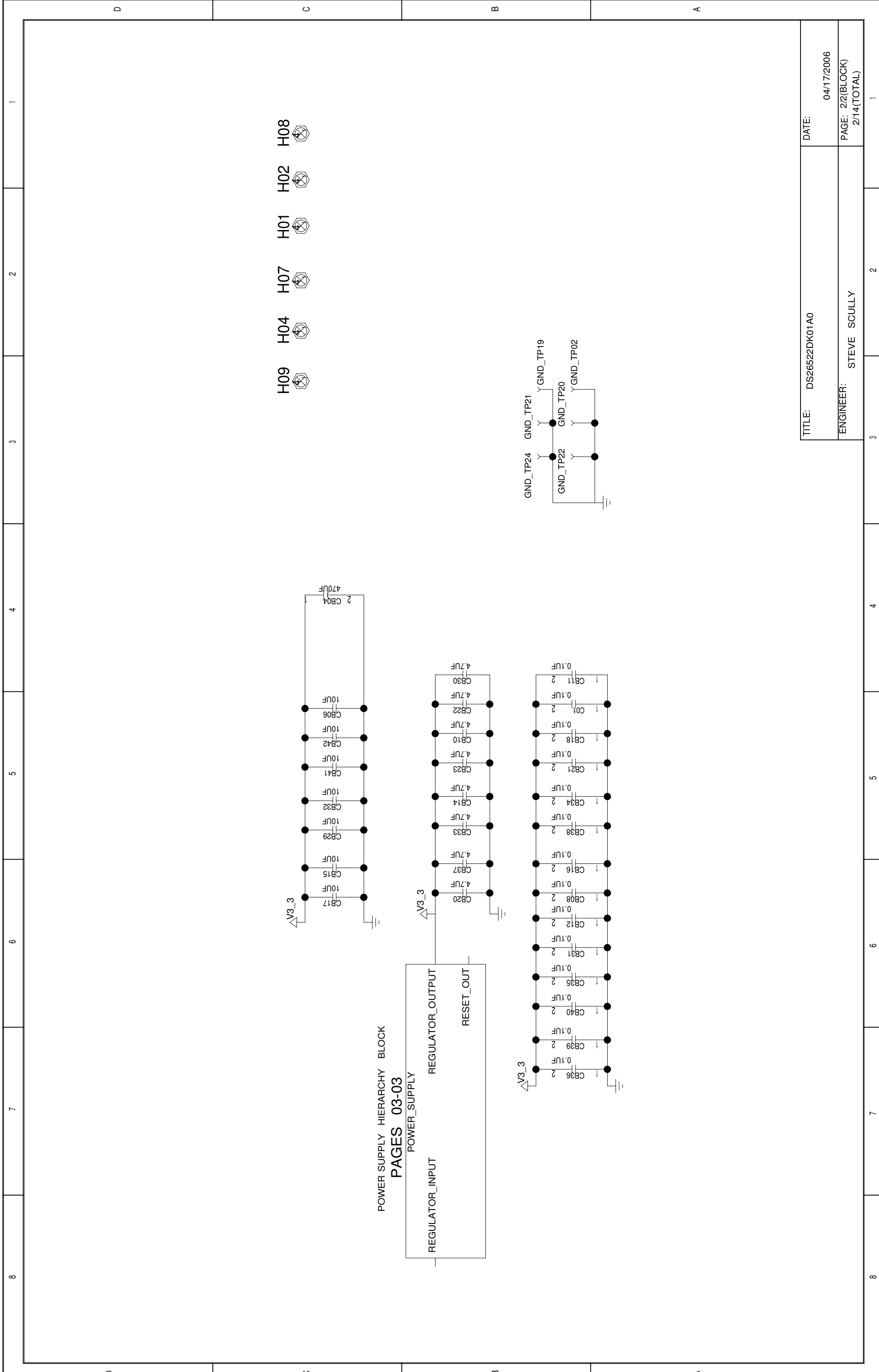
DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
C01, CB08, CB11-CB13, CB16, CB18, CB21, CB31, CB34-CB36, CB38-CB40	15	0.1 μ F \pm 10%, 16V ceramic capacitors (0603)	Phycomp	06032R104K7B20D
C02	1	1 μ F \pm 10%, 16V ceramic capacitor (1206)	Panasonic	ECJ-3YB1C105K
C03, C04, CB01, CB02	4	10F \pm 20%, 10V ceramic capacitors (1206)	Panasonic	ECJ-3YB1A106M
CB03, CB05	2	68 μ F \pm 20%, 16V tantalum capacitors (D case)	Panasonic	ECS-T1CD686R
CB04	1	470 μ F \pm 20%, 6.3V tantalum capacitor (D case)	Digi-Key	399-3002-1-ND
CB06, CB09, CB15, CB17, CB19, CB25, CB27, CB29, CB32, CB41, CB42	11	10 μ F \pm 20% 10V ceramic capacitors (1206)	Panasonic	ECJ-3YB1A106M
CB07, CB24, CB26, CB28, CB43, CB44	6	0.1 μ F \pm 20%, 16V X7R ceramic capacitors (0603)	AVX	0603YC104MAT
CB10, CB14, CB20, CB22, CB23, CB30, CB33, CB37	8	4.7 μ F, 6.3V multilayer ceramic capacitors (0603)	Digi-Key	ECJ-1VB0J475M
CB45, CB46	2	560pF \pm 5%, 50V ceramic capacitors (1206)	Digi-Key	478-1489-2-ND
DB01	1	1A, 40V Schottky diode	Internatioanl Rectifier	10BQ040
DS01	1	Green LED (SMD)	Panasonic	LN1351C
DS02	1	Green LED (SMD)	Panasonic	LN1351C
DS03–DS07	5	Red LEDs (SMD)	Panasonic	LN1251C
GND_TP02, GND_TP19– GND_TP22, GND_TP24	6	Standard ground clip	Keystone Electronics	4954
H01, H02, H04, H07, h08, H09	6	Kit, 4-40 hardware, 0.50 nylon standoff and nylon hex-nut	—	4-40KIT4
J01	1	100-mil 2-7 position jumper	Lab Stock	—
J02	1	DB9 right-angle connector (long case)	AMP	747459-1
J03	1	100-mil 2-position jumper	Lab Stock	—
J04, J05, J06	3	10-pin terminal strip headers (dual row, vertical)	Samtec	TSW-105-07-T-D
J07	1	14-pin header (dual row, vertical)	Samtec	HDR-TSW-107-14-T-D
J08, J09	2	14-pin headers (dual row, vertical) NON POPULATED	Samtec	NOPOP-HDR-TSW- 107-14-T-D

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
J10, J11	2	8-pin single-port connectors (RJ48)	Molex	15-43-8588
J12–J15	4	5-pin right-angle BNC connectors	Trompetor	UCBJR220
JB01	1	2.1mm/5.5mm closed frame power jack, high current (right angle PCB, 24VDC at 5A) Also requires 5V AC-DC adapter. Input: 100–240VAC, 50–60Hz, 0.6A. Output: DC 5V, 2.6A. PN DMS050260-P5P-SZ. Model 3Z-161WP05	CUI Inc.	PJ-002AH
JP01–JP09, JP10–JP19	19	3 position jumpers (100 mils)	Lab Stock	—
R01, R02, RB28, RB41, RB42, RB43, RB48–RB52	11	1.0k Ω \pm 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ102V
R03–R09, R10, RB09	9	0 Ω \pm 5%, 1/8W resistors (1206)	Panasonic	ERJ-8GEYJ0R00V
RB01–RB06, RB11–RB17, RB20, RB21, RB23, RB30	17	10k Ω \pm 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V
RB07	1	1.0M Ω \pm 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ105V
RB08, RB24, RB32–RB35	6	330 Ω \pm 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ331V
RB10, RB19, RB25, RB26, RB31, RB38, RB39, RB40	8	10k Ω \pm 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ103V
RB18	1	1.0k Ω \pm 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ102V
RB22	1	330 Ω \pm 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEYJ331V
RB27	1	0.0 Ω \pm 5%, 1/16W resistor (0603)	Panasonic	ERJ-3GEY0R00V
RB29	1	10k Ω \pm 1%, 1/10W resistor (0805)	Panasonic	ERJ-6ENF1002V
RB36, RB37	2	30 Ω \pm 5%, 1/16W resistors (0603)	Panasonic	ERJ-3GEYJ300V
RB44–RB47	4	61.9 Ω \pm 1%, 1/10W resistors (0805)	Panasonic	ERJ-6ENF61R9V
RB53, RB54	2	51.1 Ω \pm 1%, 1/10W resistors (0805)	Panasonic	ERJ-6ENF51R1V
RPB01–RPB07	7	30 Ω \pm 5% 4-pack resistors (0402)	Panasonic	EXB-N8V300JX
SW01	1	4-pin single-pole switch	Panasonic	EVQPAE04M
TB01, TB02	2	16-pin SMT transformers	Pulse Engineering	TX1099
TP01, TP02	2	1 plated hole test points DO NOT STUFF	Lab Stock	—
U01, U04	2	Cypress SRAM	Lab Stock	—
U02	1	3V to 5V Regulating charge pump	Maxim	MAX1686HEUA
U03	1	Processor	Freescale Semiconductor	MMC2107

DESIGNATION	QTY	DESCRIPTION	SUPPLIER	PART
U05	1	1.2V FPGA (144-pin, 20mm x 20mm TQFP)	Lattice	LFEC3E-3T144C
U06	1	Dual T1/E1/J1 transceiver (144-pin, 12mm x 12mm CSBGA)	Dallas Semiconductor	DS26522
UB01	1	Dual RS-232 transceivers with 3.3V/5V internal capacitors	Maxim	MAX3233E
UB02	1	Linear regulator (1.5W, 3.3V or adjustable, 1A, 16-pin TSSOP-EP)	Maxim	MAX1793EUE-33
UB03	1	Microprocessor voltage monitor (2.93V reset, 4-pin SOT143)	Maxim	MAX811SEUS-T
UB04	1	2Mb High-speed serial flash memory (2.7V to 3.6V, 8-pin SO)	Atmel	AT25F2048N-10SU-2.7
UB05	1	300mA LDO regulator with $\overline{\text{RESET}}$ (1.20V output, 6-pin thin SOT23-6)	Maxim	MAX1963EZT120-T
UB06, UB07	2	High-speed buffers	Fairchild	NC7SZ86
XB01	1	8.0MHz low-profile crystal	ECL	EC1-8.000M
YB01	1	3.3V 1.544MHz crystal clock oscillator	SaRonix	NTH 039A3-1.5440
YB02	1	3.3V 2.048MHz crystal clock oscillator	SaRonix	NTH 039A3-2.0480

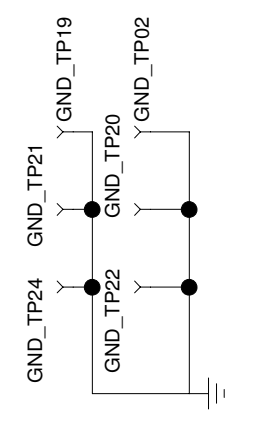
8. SCHEMATICS

The DS26522DK schematics are featured in the following 14 pages.



H09 H04 H07 H01 H02 H08

POWER_SUPPLY HIERARCHY BLOCK
PAGES 03-03

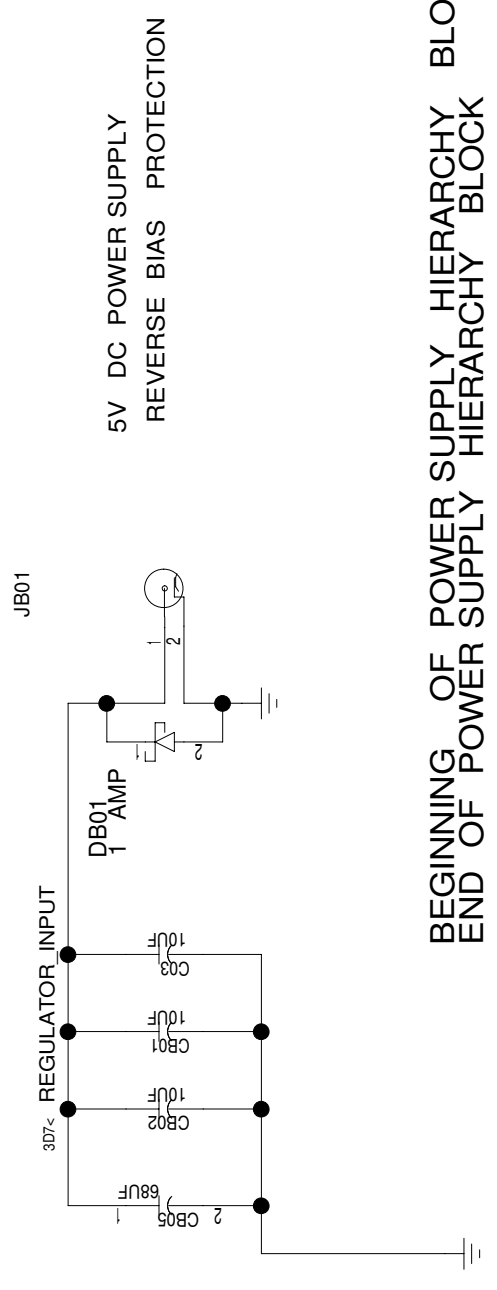
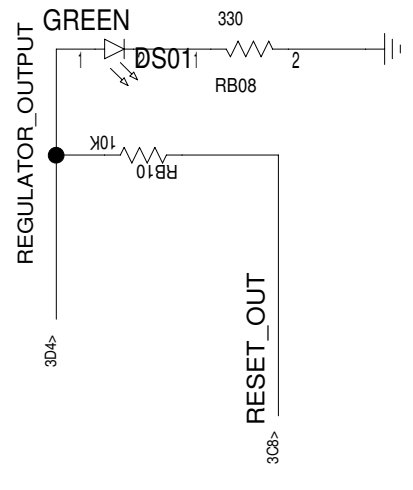
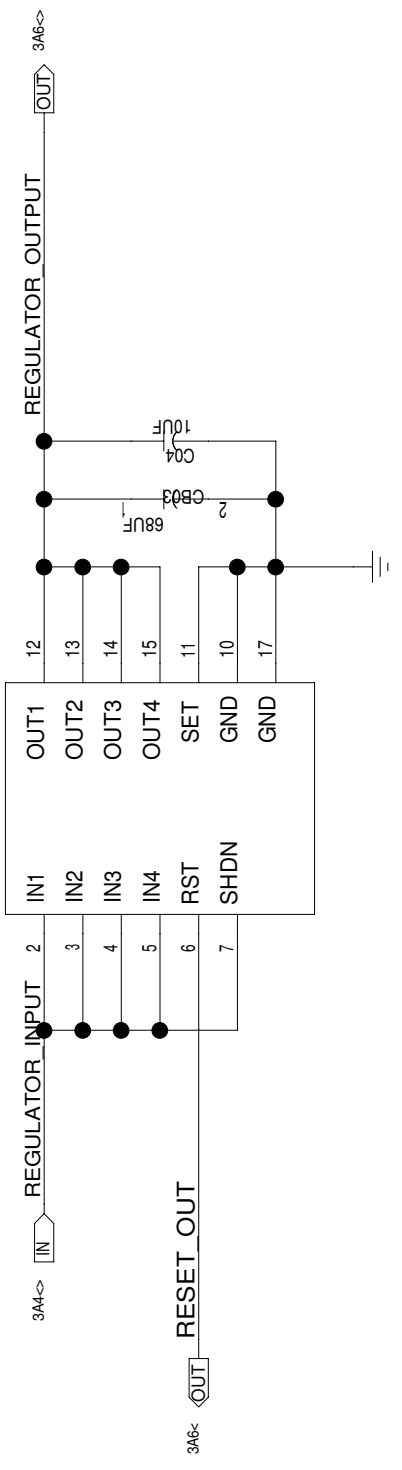


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ENGINEER: STEVE SCULLY	PAGE: 2/2(BLOCK) 2/14(TOTAL)

3.3V 1% REGULATOR

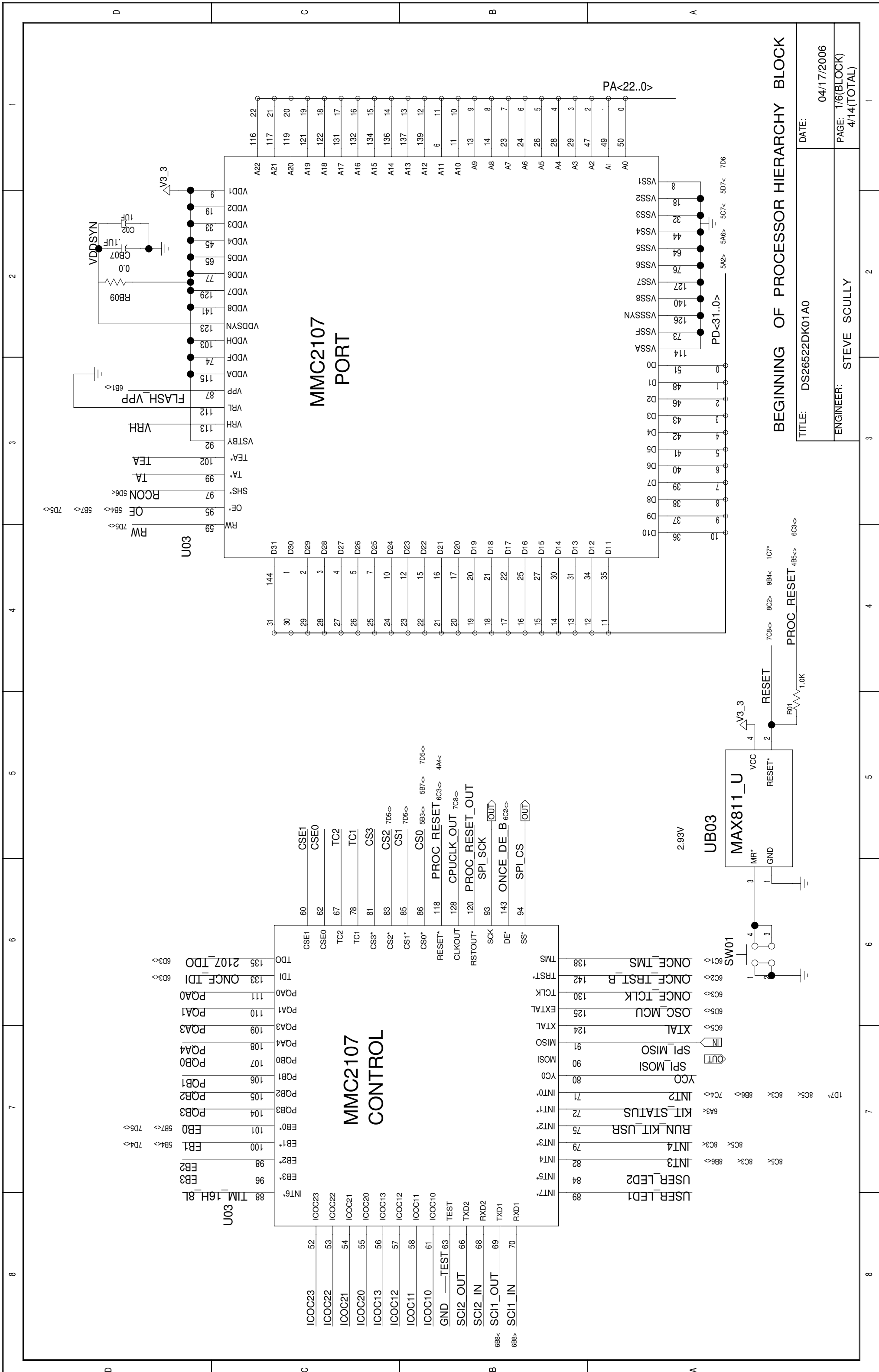
3.3V

UB02
MAX1793_U



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END OF POWER SUPPLY HIERARCHY BLOCK

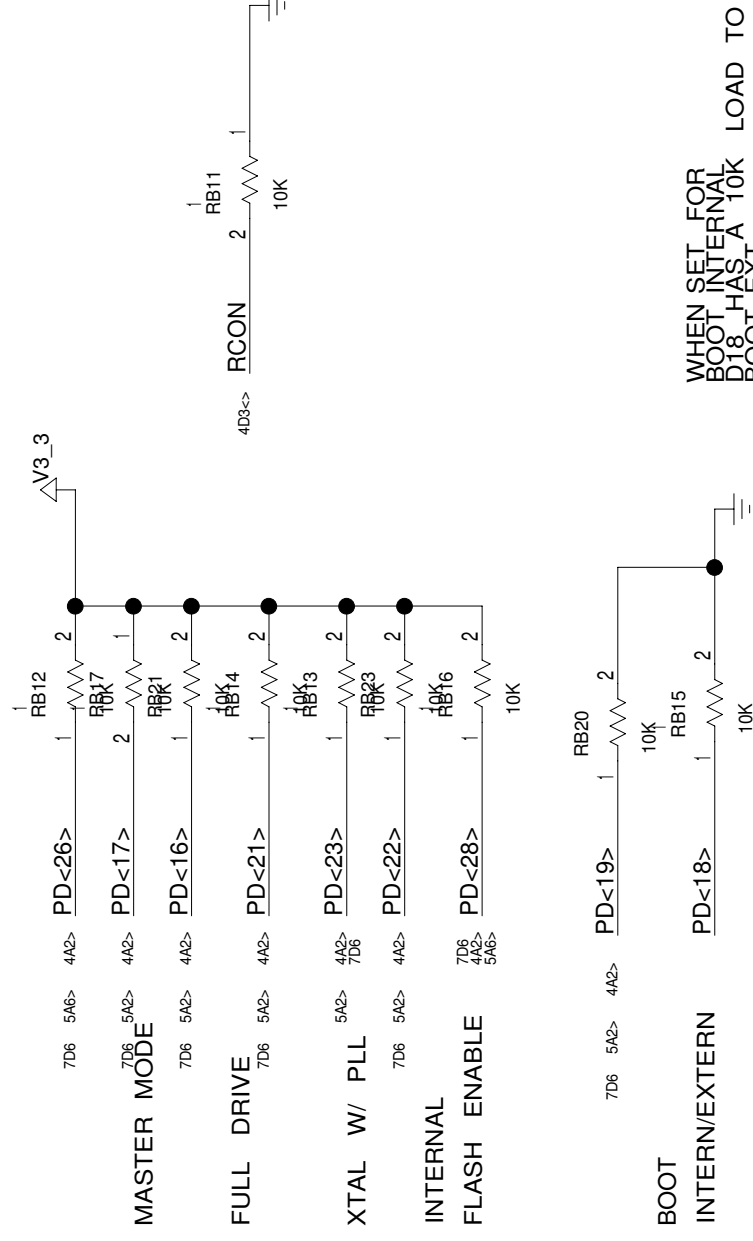
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ENGINEER: STEVE SCULLY	PAGE: 1/1(BLOCK) 3/14(TOTAL)



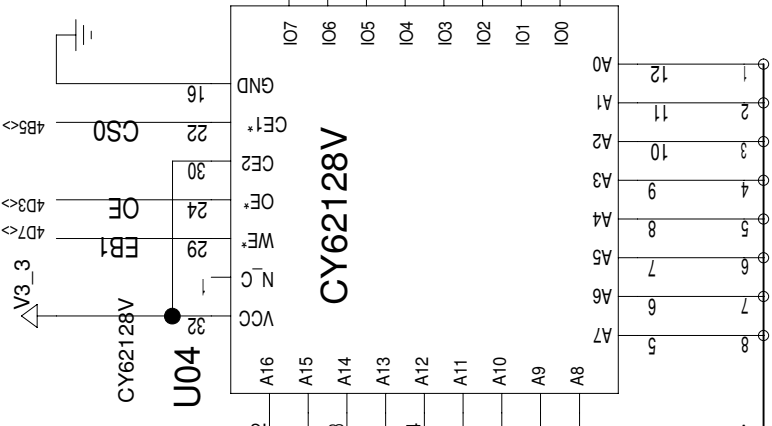
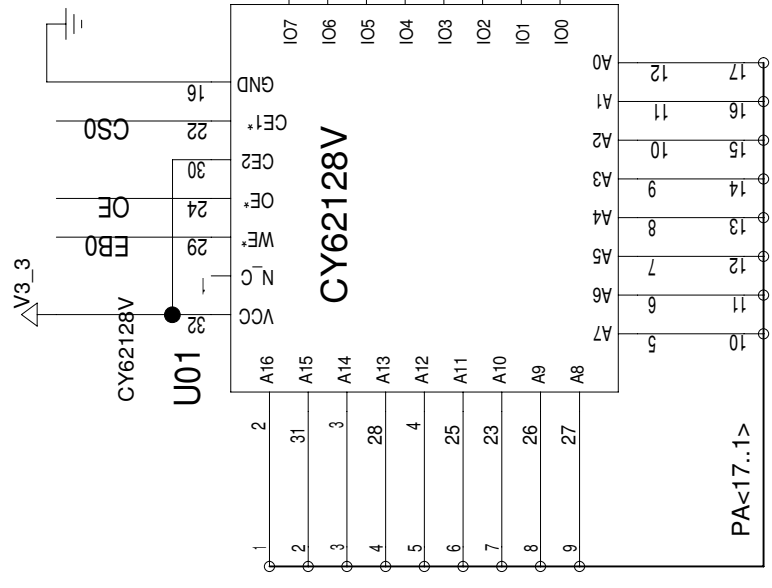
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ENGINEER: STEVE SCULLY	PAGE: 1/6(BLOCK) 4/14(TOTAL)

RESET CONFIGURATION



WHEN SET FOR
BOOT INTERNAL
D18 HAS A 10K LOAD TO GND
BOOT EXT
D18 HAS A 10.5K LOAD TO V3V

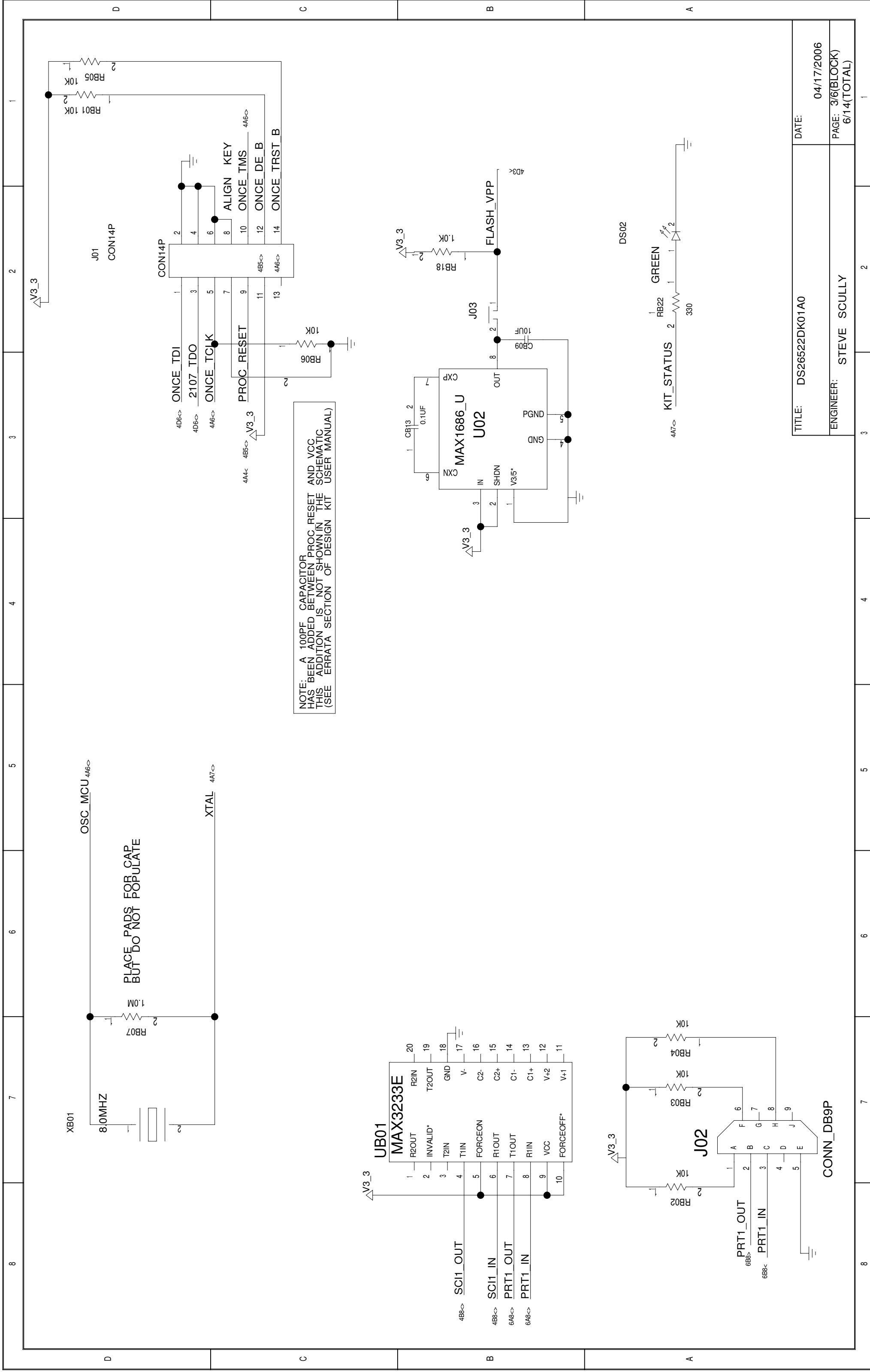


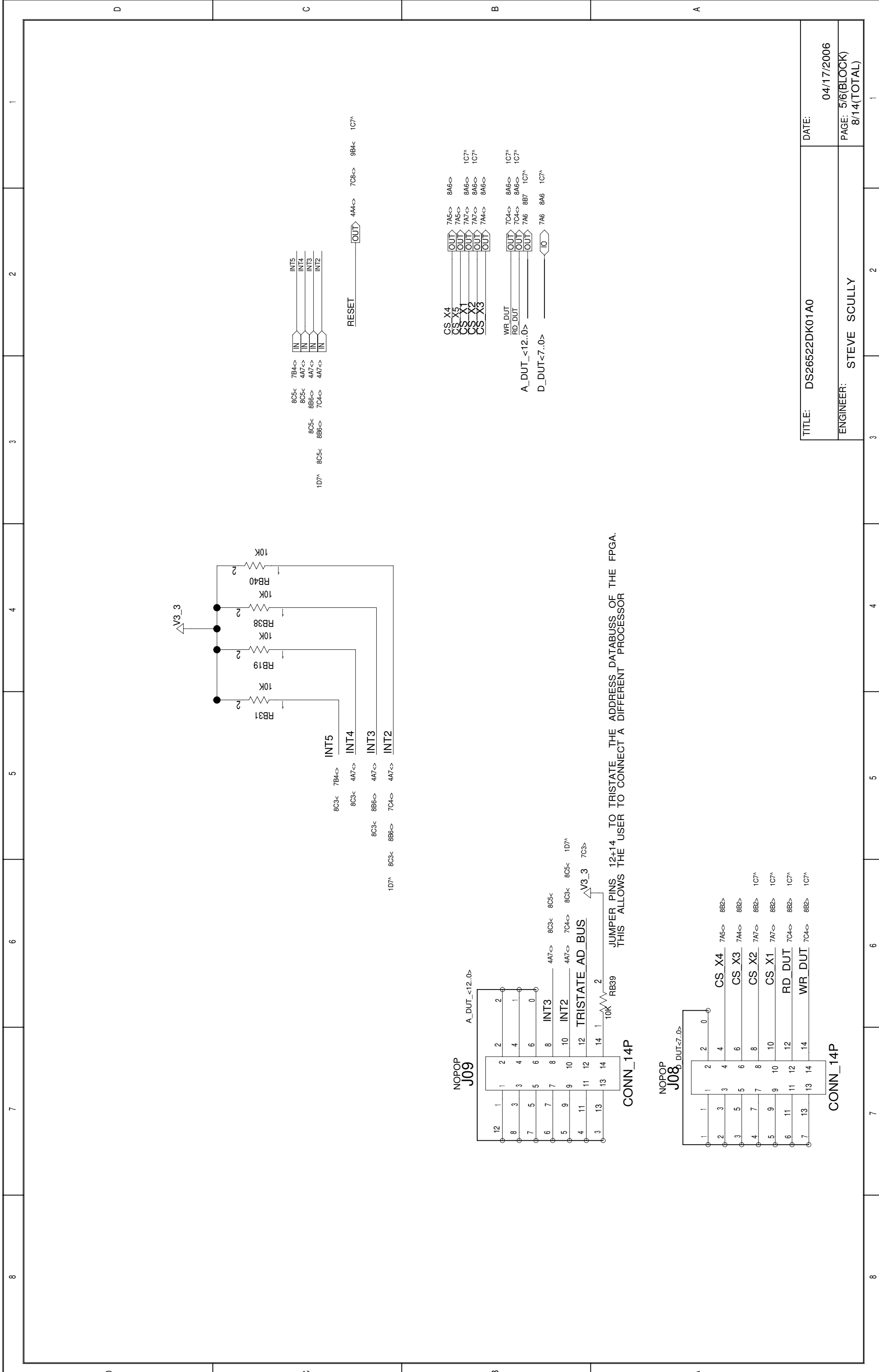
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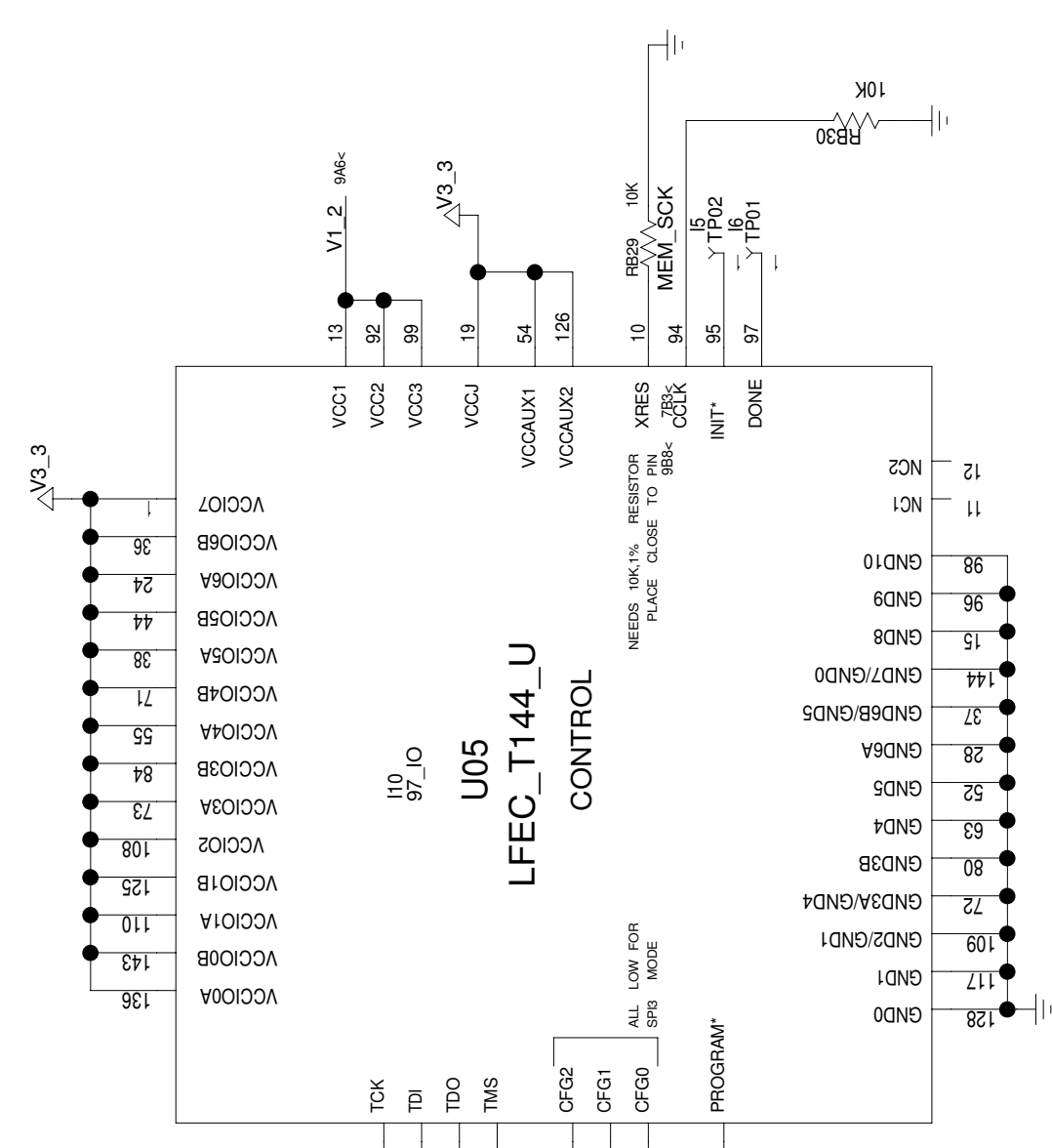
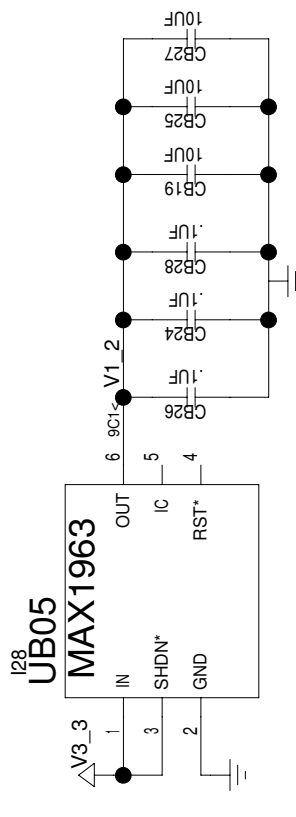
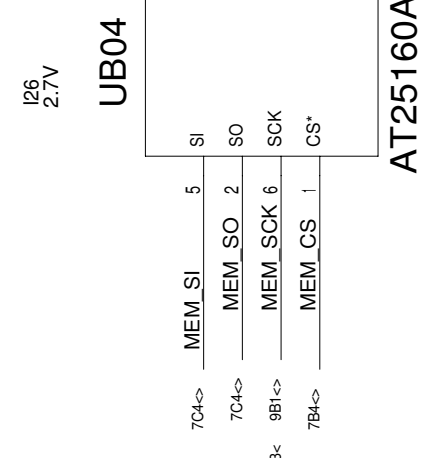
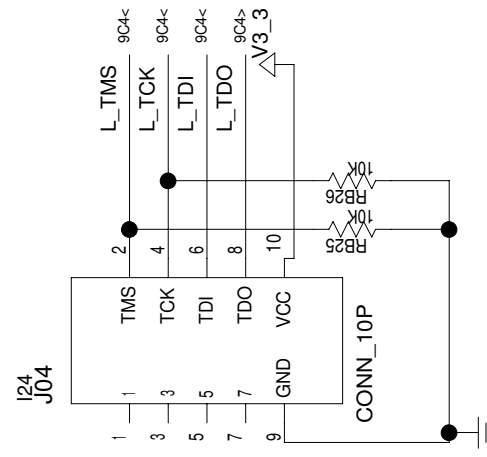


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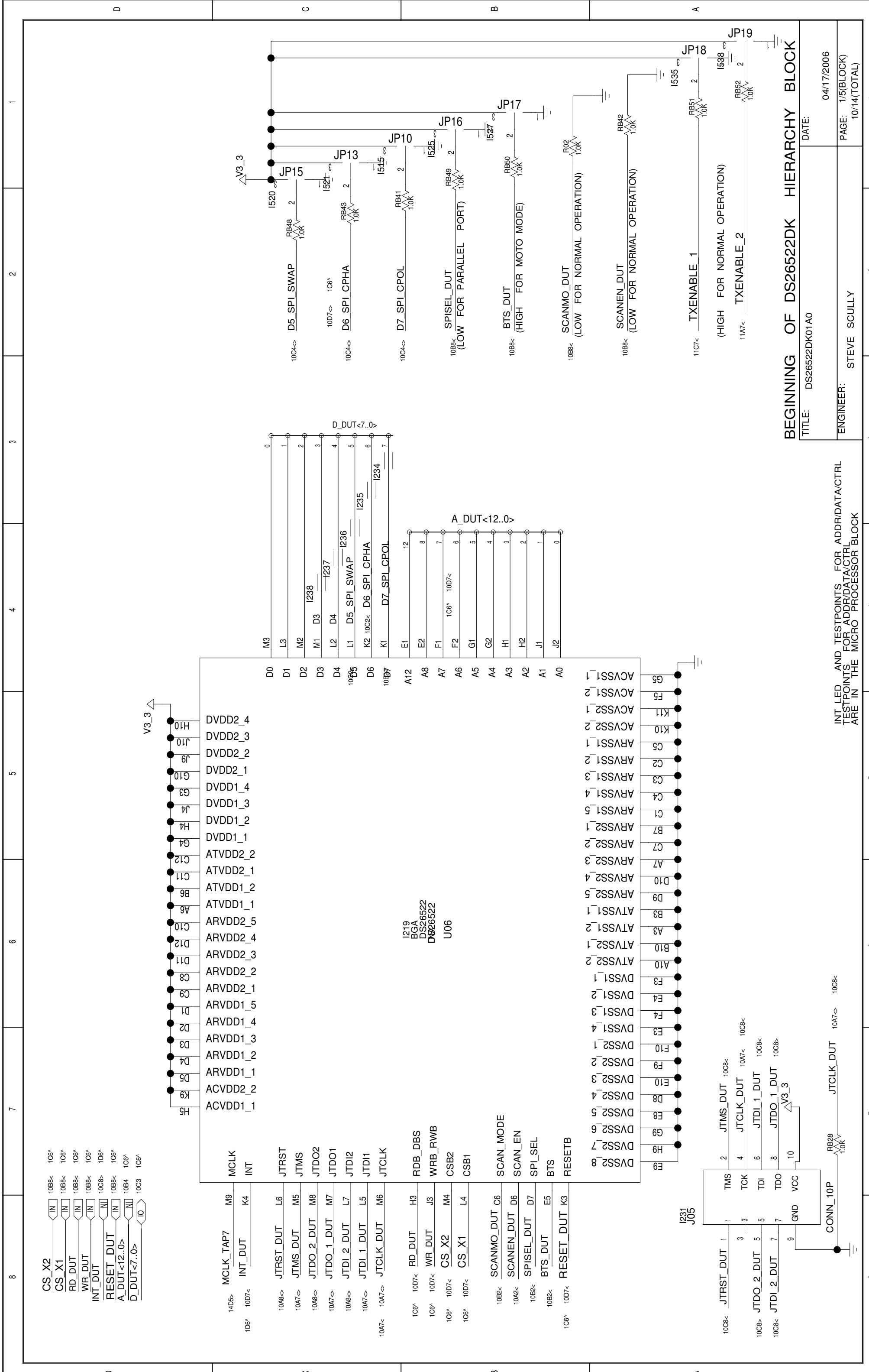
ENGINEER: STEVE SCULLY

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8/14(TOTAL)



END OF PROCESSOR HIERARCHY BLOCK

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ENGINEER: STEVE SCULLY	PAGE: 6/6(BLOCK) 9/14(TOTAL)



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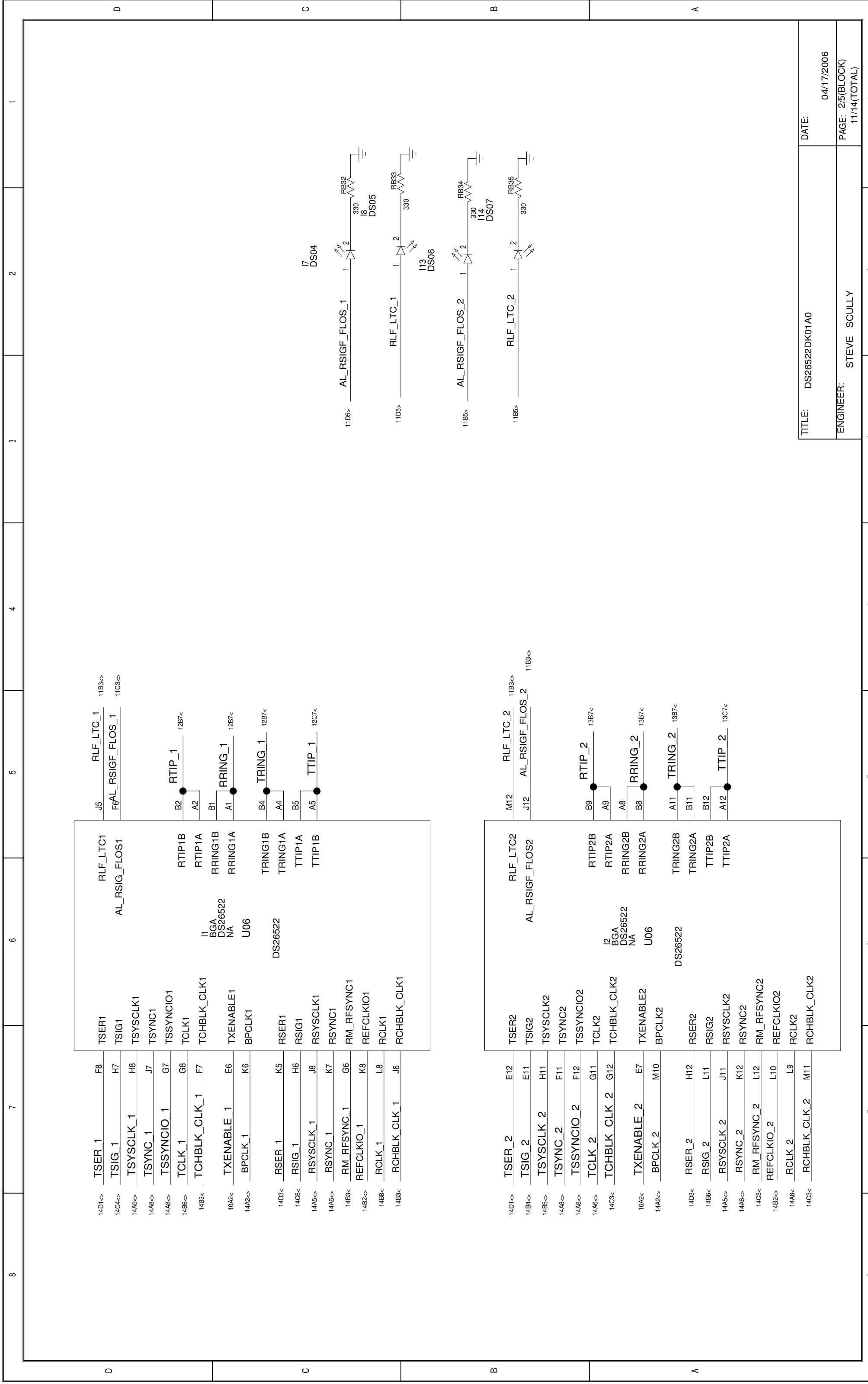
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ENGINEER: STEVE SCULLY

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10/14(TOTAL)

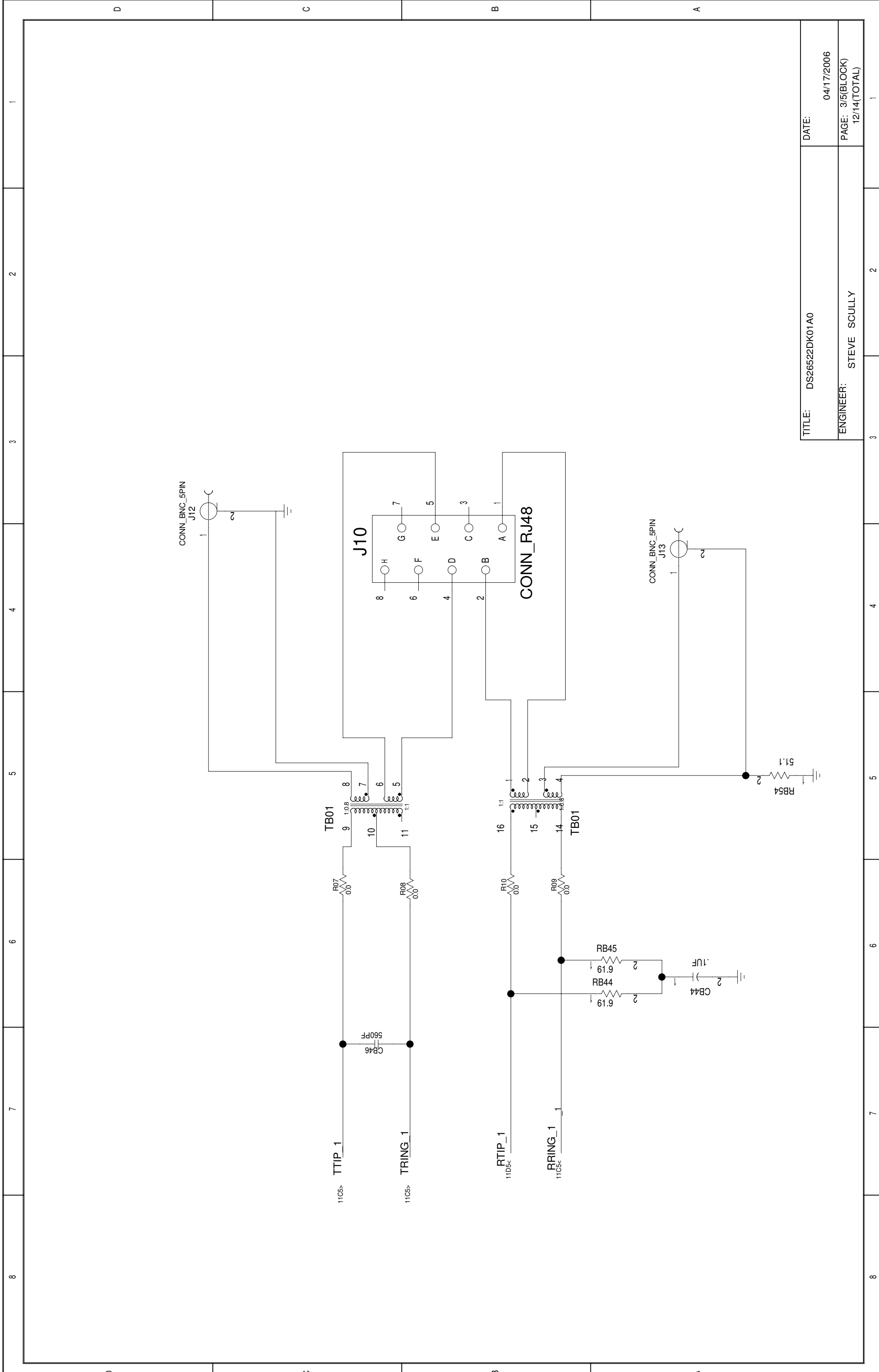
INT LED AND TESTPOINTS FOR ADDR/DATA/CTRL TESTPOINTS FOR ADDR/DATA/CTRL ARE IN THE MICRO PROCESSOR BLOCK



14D1<>	TSER 1	F8	RLF_LTC1	J5	RLF_LTC_1	11B3<>
14C4<>	TSIG 1	H7	AL_RSIGF_FLOS1	F6	AL_RSIGF_FLOS_1	11C3<>
14A5<>	TSYSCLK 1	H8				
14A8<>	TSYNC 1	J7				
14A8<>	TSSYNCIO 1	G7				
14B6<>	TCLK 1	G8				
14B3<>	TCHBLK_CLK 1	F7				
10A2<	TXENABLE 1	E6				
14A2<>	BPCLK 1	K6				
14D3<	RSER 1	K5				
14C8<	RSIG 1	H6				
14A5<>	RSYSCLK 1	J8				
14A6<>	RSYNC 1	K7				
14B3<>	RM_RFSYNC 1	G6				
14B2<>	REFCLKIO 1	K8				
14B8<	RCLK 1	L8				
14B3<>	RCHBLK_CLK 1	J6				

14D1<>	TSER 2	E12	RLF_LTC2	M12	RLF_LTC_2	11B3<>
14B4<>	TSIG 2	E11	AL_RSIGF_FLOS2	J12	AL_RSIGF_FLOS_2	11B3<>
14B5<>	TSYSCLK 2	H11				
14A8<>	TSYNC 2	F11				
14A8<>	TSSYNCIO 2	F12				
14A6<>	TCLK 2	G11				
14C3<	TCHBLK_CLK 2	G12				
10A2<	TXENABLE 2	E7				
14A2<>	BPCLK 2	M10				
14D3<	RSER 2	H12				
14B6<	RSIG 2	L11				
14A5<>	RSYSCLK 2	J11				
14A6<>	RSYNC 2	K12				
14C3<	RM_RFSYNC 2	L12				
14B2<>	REFCLKIO 2	L10				
14A8<	RCLK 2	L9				
14C3<>	RCHBLK_CLK 2	M11				

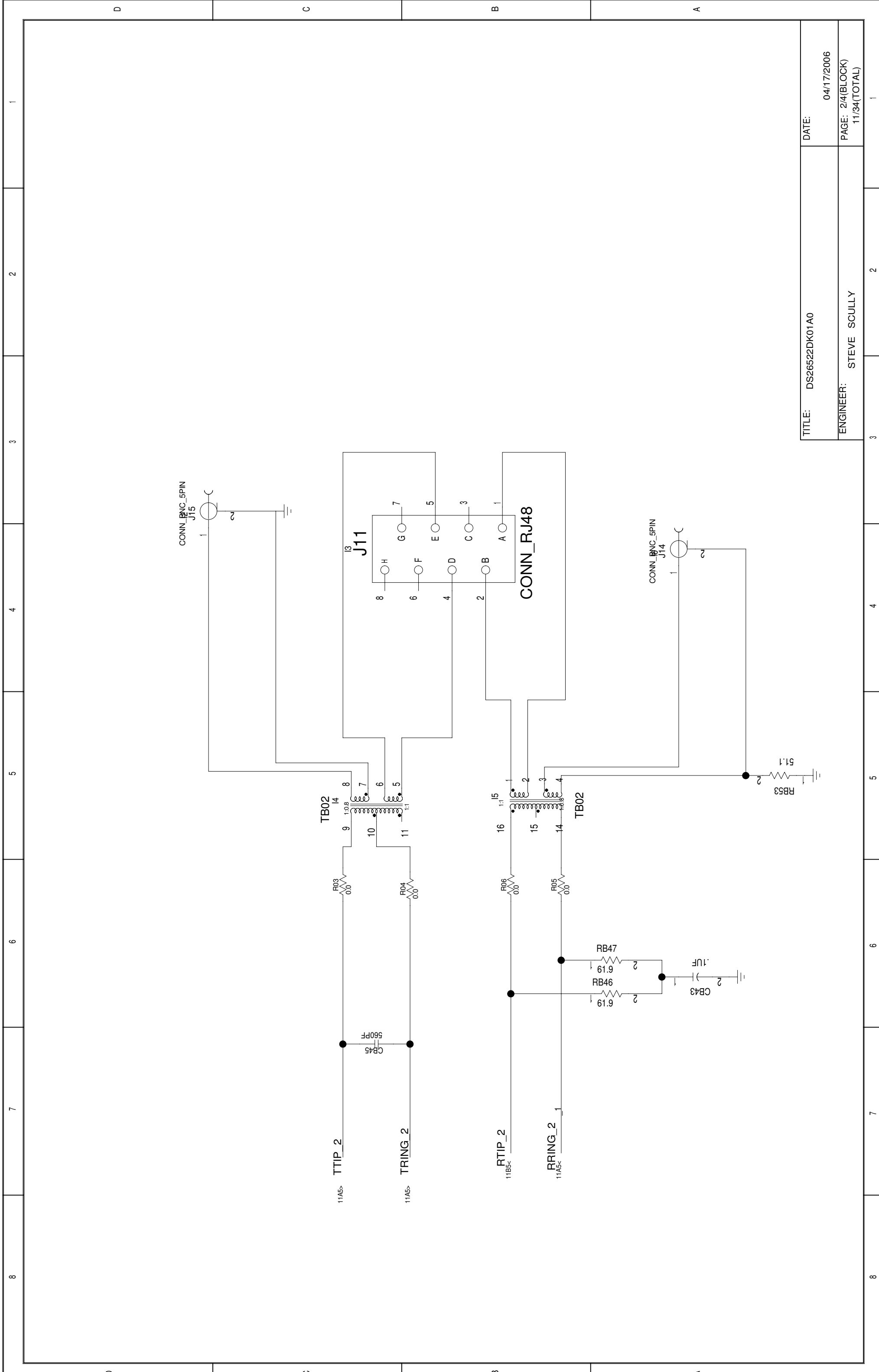
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 DATE: 04/17/2006
 ENGINEER: STEVE SCULLY
 PAGE: 2/5(BLOCK)
 11/14(TOTAL)



TITLE: DS26522DK01A0	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 3/5(BLOCK) 12/14(TOTAL)

8 7 6 5 4 3 2 1

D C B A



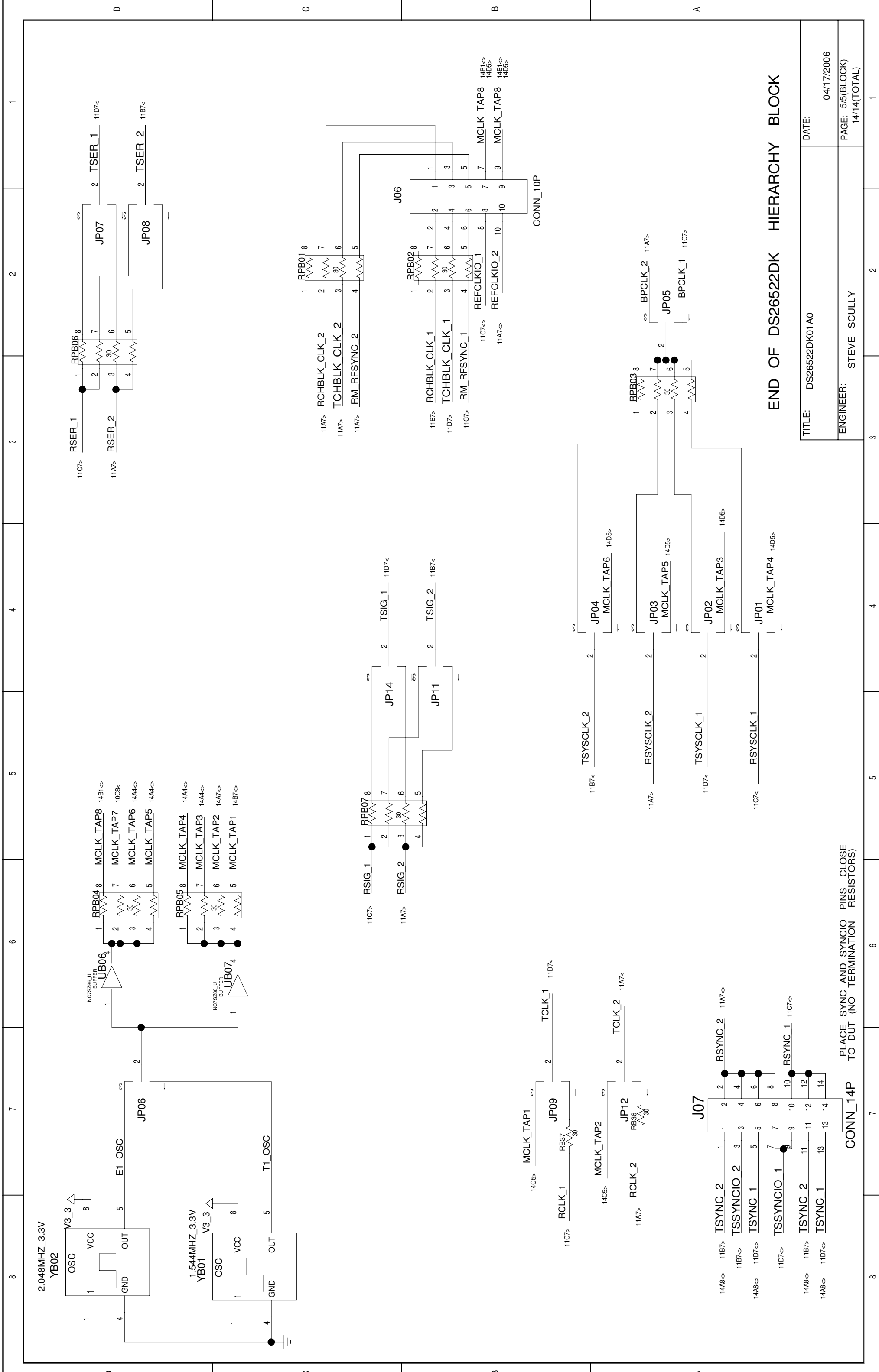
TITLE: DS26522DK01A0	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 2/4(BLOCK) 11/34(TOTAL)

1 2 3 4 5 6 7 8

D C B A

1 2 3 4 5 6 7 8

D C B A



END OF DS26522DK HIERARCHY BLOCK

TITLE: DS26522DK01A0	DATE: 04/17/2006
ENGINEER: STEVE SCULLY	PAGE: 5/5(BLOCK) 14/14(TOTAL)

PLACE SYNC AND SYNCIO PINS CLOSE TO DUT (NO TERMINATION RESISTORS)