S1D13743 Mobile Graphics Engine

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The S1D13743 is a color mobile graphics engine with an embedded 464K byte display buffer. The S1D13743 supports a 8/16-bit Intel 80 CPU architecture while providing high performance bandwidth into 24 bpp display memory allowing for fast screen updates.
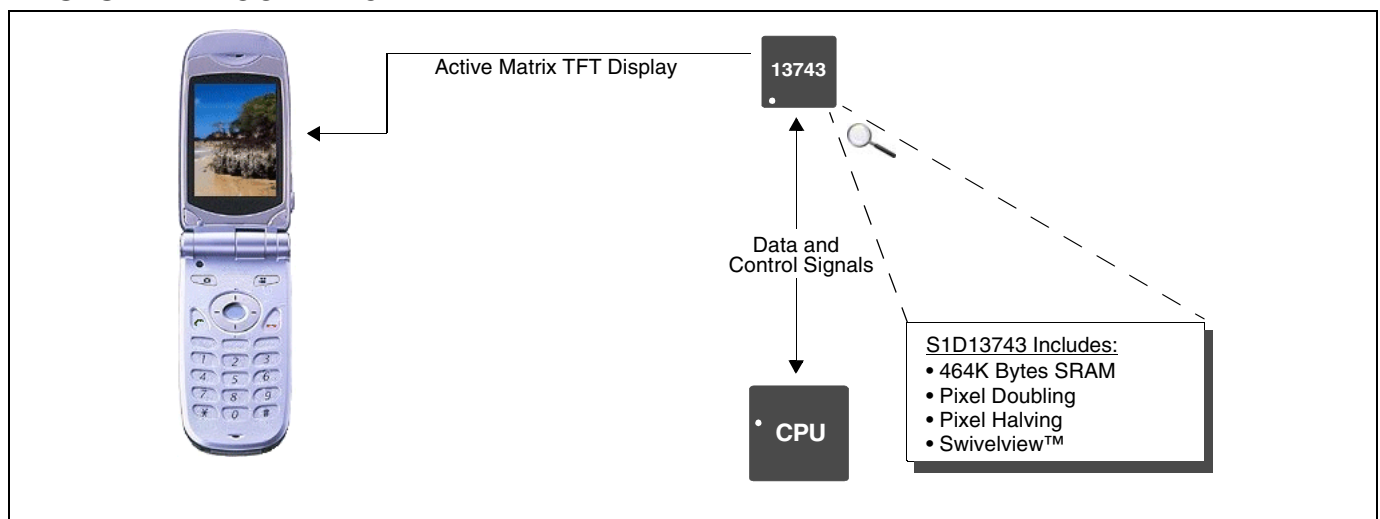
Products requiring a rotated display image can take advantage of the SwivelView™ feature which provides hardware rotation of the display memory transparent to the software application. Resolutions supported include 352x440 @ 24 bpp single buffered or 320x240 @ 24 bpp double-buffered. The S1D13743 uses a double-buffer architecture to prevent any visual tearing during streaming video screen updates.

■ FEATURES

- Embedded 464K byte SRAM Display Buffer
- Low Operating Voltage
- 8/16-bit Intel 80 interface (used for display or register data).
- Input data formats: RGB 8:8:8, 6:6:6, 5:6:5 and YUV 4:2:2, 4:2:0.
- All input data is converted and stored as RGB 8:8:8.
- Active Matrix TFT interface - 18/24-bit interface.
- Supports resolutions up to 352x440.
- Hardware / Software Power Save mode.

- 24 bit-per-pixel (bpp) color depth.
- SwivelView™: 90°, 180°, 270° counter-clockwise hardware rotation of display image
- Double-Buffer available to prevent image tearing during streaming input
- Pixel Doubling: Horizontal and Vertical averaging for smooth doubling of a single window
- Pixel Halving: no limitation on number of windows
- Internal programmable PLL.
- Single MHz clock input: CLKI.
- General Purpose Input/Output pins.

■ SYSTEM BLOCK DIAGRAM

Active Matrix TFT Display

13743

Data and Control Signals

CPU

S1D13743 Includes:
- 464K Bytes SRAM
- Pixel Doubling
- Pixel Halving
- Swivelview™

■ DESCRIPTION

Integrated Frame Buffer

- Embedded 464K byte SRAM display buffer

CPU Interface

- 8/16-bit Intel 80 interface (used for display or register data)

Panel Support

- Active Matrix TFT 18/24-bit interface
- Frame Rate Modulation using 24 bpp data when configured for an 18-bit LCD panel.
- Supports resolutions up to 352x440

Input Data Format

- RGB: 8:8:8, 6:6:6, 5:6:5.
- YUV 4:2:2, 4:2:0.
- All input data is converted and stored as RGB 8:8:8

Display Features

- 24 bit-per-pixel (bpp) color depths.
- All display writes are handled by window apertures/position for complete or partial display updates. All window coordinates are referenced to top left corner of the displayed image (even in a rotated display, the top-left corner is maintained and no host side translation need take place).
- SwivelView™: 90°, 180°, 270° counter-clockwise hardware rotation of display image. All displayed windows can have independent rotation. No additional programming necessary when enabling these modes.
- Double-Buffer available to prevent image tearing during streaming input. Resolutions supported must fit inside 228K bytes. Typical resolution of 320x240.
- Pixel Doubling: Horizontal and Vertical averaging for smooth doubling of a single window.
- Pixel Halving: no limitation on number of windows.

Miscellaneous

- Internal programmable PLL.
- Single MHz clock input: CLKI.
- CLKI available as CLKOUT (separate CLKOUTEN pin associated with output).
- Hardware / Software Power Save mode.
- Input pin to Enable/Disable Power Save Mode.
- General Purpose Input/Output pins are available (GPIO[7:0]).
- COREVDD 1.5 volts and IOVDD 1.65 ~ 3.6 volts
- QFP20 144-pin package

CONTACT YOUR SALES REPRESENTATIVE FOR THESE COMPREHENSIVE DESIGN TOOLS

- S1D13743 Technical Documentation
- S1D13743 Evaluation Boards

- CPU Independent Software Utilities
- Royalty Free source level driver code

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