TLV840EVM Voltage Supervisor User Guide

This user guide describes the TLV840EVM evaluation module (EVM). This guide contains the EVM schematic, bill of materials (BOM), assembly drawing, and top and bottom board layouts.

Contents

1 Introduction 3
1.1 Related Documentation 4
1.2 TLV840 Applications 4
2 Schematic, Bill of Materials, and Layout 4
2.1 TLV840EVM Schematic 5
2.2 TLV840EVM Bill of Materials 6
2.3 Layout and Component Placement 7
3 EVM Connectors 9
3.1 EVM Test Points 9
3.2 EVM Jumpers 9
4 EVM Setup and Operation 10
4.1 Input Power (V_{DD}) 10
4.2 Monitoring Voltage on VDD 10
4.3 Reset Output ($\overline{RESET}$) 11
4.4 Reset Time Delay Programming (Program t_D via CT) 11

List of Figures

1 TLV840EVM Board Top 3
2 TLV840EVM Board Bottom 4
3 TLV840EVM Schematic 5
4 Component Placement—Top Assembly 7
5 Component Placement—Bottom Assembly 7
6 Layout—Top 7
7 Layout—Bottom 7
8 Top Layer 7
9 Bottom Layer 7
10 Top Solder Mask 8
11 TLV840EVM $\overline{RESET}$ Asserted Due to $\overline{MR}$ Pulled Low 10
12 TLV840EVM $\overline{RESET}$ Deasserted Due to $\overline{MR}$ Pulled High, C_T Floating 10
13 TLV840EVM Glitch Immunity 10
14 TLV840EVM $\overline{RESET}$ Delay Time (t_D) with C_T Tied to GND Through 0.1-µF Capacitor 12
15 TLV840EVM $\overline{RESET}$ Delay Time (t_D) with C_T Tied to GND Through 0.01-µF Capacitor 12
16 TLV840EVM $\overline{RESET}$ Delay Time (t_D) with C_T Floating 12

List of Tables

1 BOM 6
2 Test Points 9
3 List of Onboard Jumpers 9
4 Nominal Supply and Typical Threshold Voltages 10

Trademarks

All trademarks are the property of their respective owners.

1 Introduction

The TLV840EVM is an evaluation module (EVM) for the TLV840 voltage supervisor. The TLV840EVM can be used with any TLV840 device variant but note that if using the push-pull variants (TLV840PLXX or TLV840PHXX), the shunt on J2 must be removed as push-pull devices do not use a pull-up resistor so R1 must be disconnected. If using TLV840EVM with the active-high variant (TLV840PHXX), the active-low $\overline{\text{RESET}}$ label on the EVM board and throughout this user guide becomes active-high RESET. The TLV840 has a supply voltage range of 0.7 V to 6 V, and offers input connections for all device input and output pins. Test points are provided to give the user access to an extra ground connection if needed for oscilloscope or multimeter measurements.

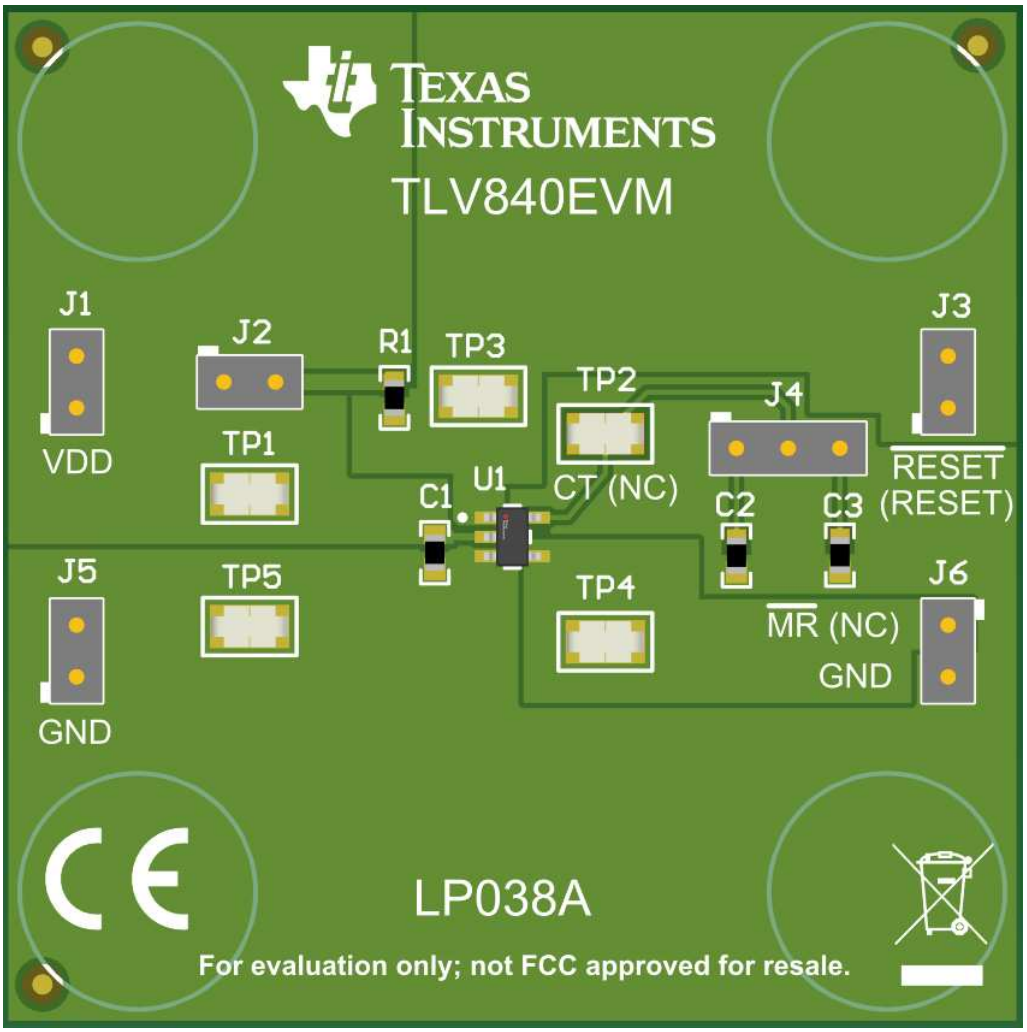

Figure 1. TLV840EVM Board Top

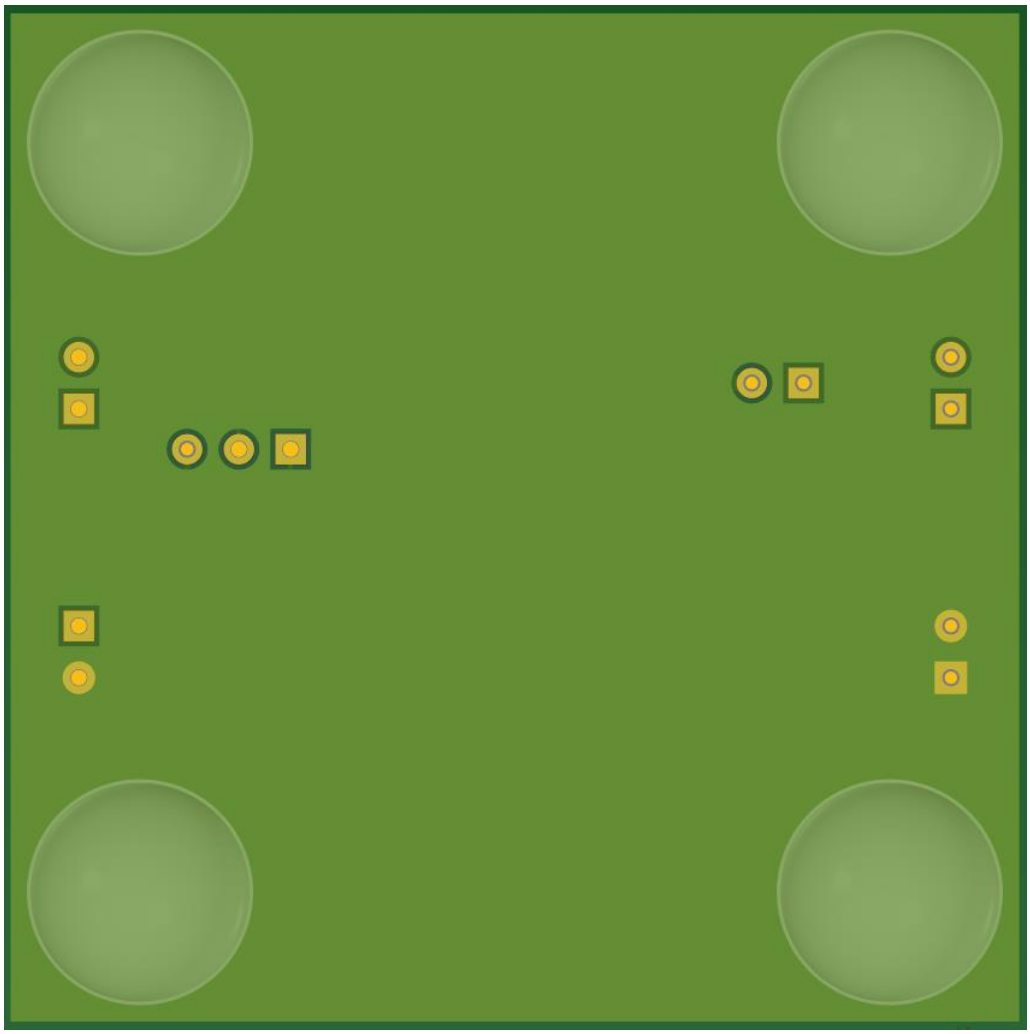

Figure 2. TLV840EVM Board Bottom

1.1 Related Documentation

TLV840 Nano-Power, Ultra-Low Voltage Supervisor with Ajustable Reset Time Delay data sheet, SBVSBC3

1.2 TLV840 Applications

- Motor Drives
- Factory Automation and Control
- Home Theater and Entertainment
- Electronic Point of Sale
- Grid Infrastructure
- Data Center and Enterprise Computing
- Multifunction Printer

2 Schematic, Bill of Materials, and Layout

This section provides a detailed description of the TLV840EVM schematic, bill of materials (BOM), and layout.

2.1 TLV840EVM Schematic

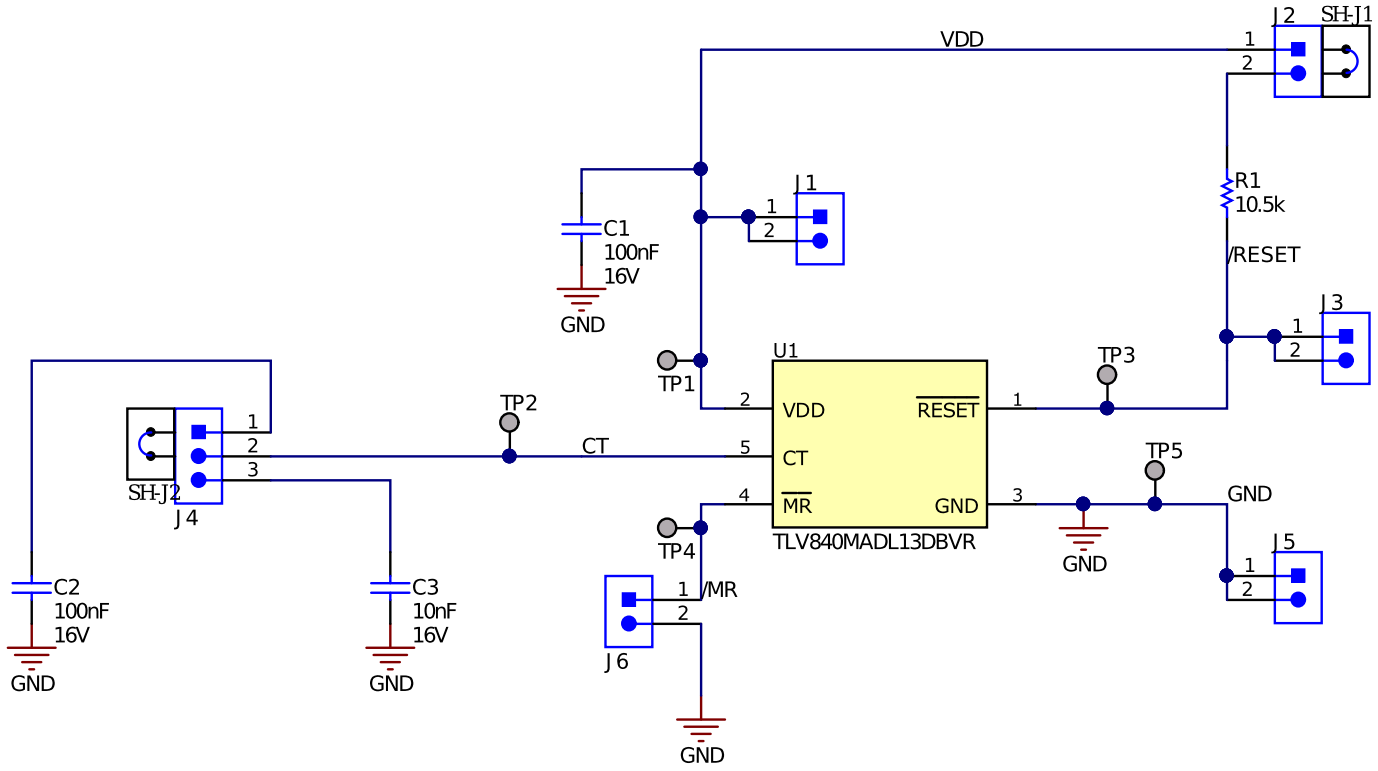

Figure 3. TLV840EVM Schematic

2.2 TLV840EVM Bill of Materials

Table 1. BOM

DESIGNATOR	QTY	VALUE	DESCRIPTION	PACKAGE REFERENCE	PART NUMBER	MANUFACTURER
!PCB	1		Printed Circuit Board		TLV840EVM	Any
C1, C2	2	0.1 µF	CAP, CERM, 0.1 µF, 16 V, ± 10%, X7R, 0603	0603	C0603C104K4RACTU	Kemet
C3	1	0.01 µF	CAP, CERM, 0.01 uF, 16 V, +/- 10%, X7R, 0603	0603	C0603C103K4RACTU	Kemet
H1, H2, H3, H4	4		Bumpon, Hemisphere, 0.44 X 0.20, Clear	Transparent Bumpon	SJ-5303 (CLEAR)	3M
J1, J2, J3, J5, J6	5		Header, 100mil, 2x1, TH	Header, 2x1, 100mil, TH	800-10-002-10-001000	Mill-Max
J4	1		Header, 100mil, 3x1, TH	Header, 3x1, 100mil, TH	800-10-003-10-001000	Mill-Max
R1	1	10.5k	RES, 10.5 k, 1%, 0.1 W, 0603	0603	RC0603FR-0710K5L	Yageo America
SH-J1, SH-J2	2		Shunt, 100mil, Tin plated, Black	Shunt Connector Black Open Top, 2x1	SNT-100-BK-T-H	Samtec
TP1, TP2, TP3, TP4, TP5	5		Test Point, Miniature, SMT	Test Point, Miniature, SMT	5019	Keystone
U1	1		Ultra-Low Voltage Supervisor with Adjustable Reset Time Delay and Manual Reset Option	SOT23-5	TLV840MADL13DBVR	Texas Instruments
FID1, FID2, FID3	0		Fiducial mark. There is nothing to buy or mount.	Fiducial	N/A	N/A

2.3 Layout and Component Placement

Figure 4 and Figure 5 show the top and bottom assemblies of the printed circuit board (PCB) to show the component placement on the EVM.

Figure 6 and Figure 7 show the top and bottom layouts, Figure 8 and Figure 9 show the top and bottom layers, and Figure 10 shows the top solder mask of the EVM.

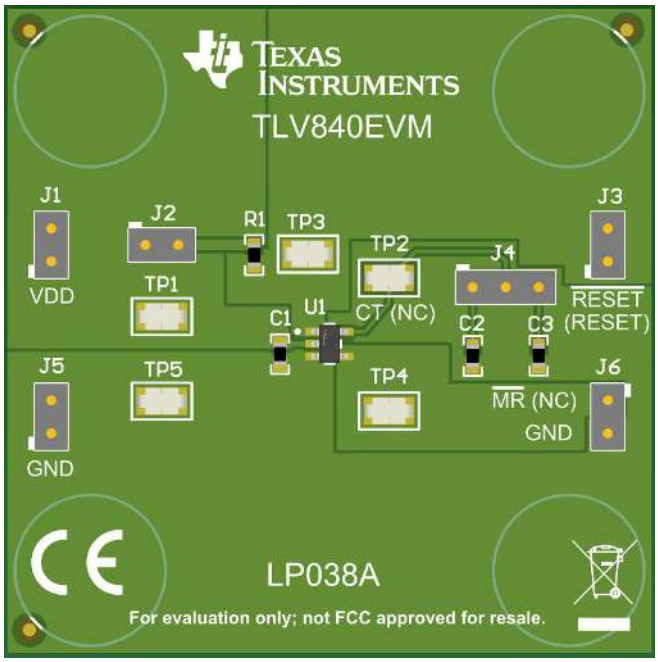

Figure 4. Component Placement—Top Assembly

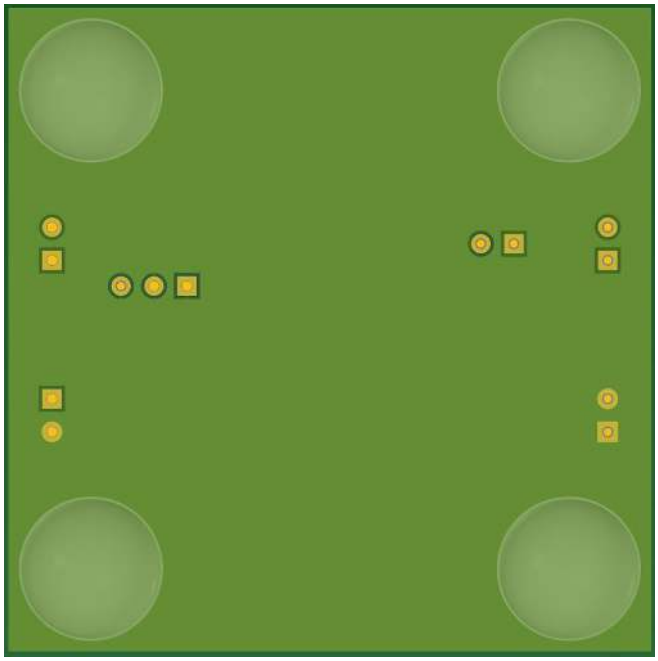

Figure 5. Component Placement—Bottom Assembly

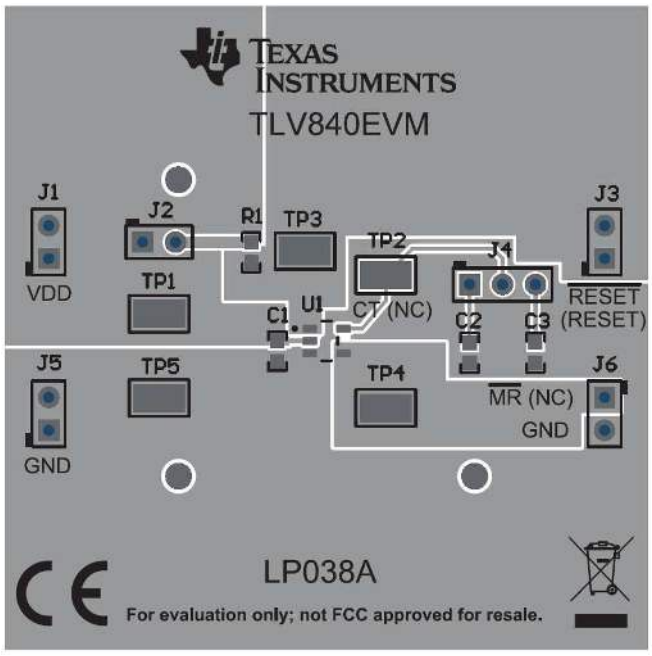

Figure 6. Layout—Top

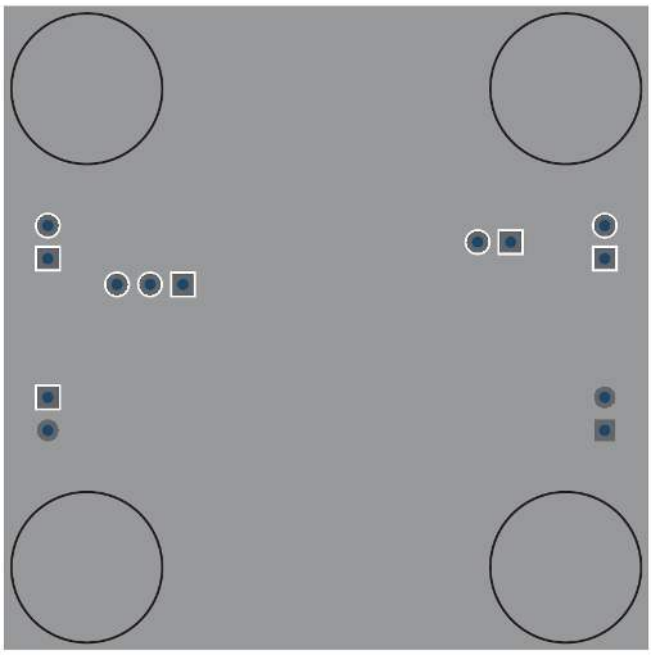

Figure 7. Layout—Bottom

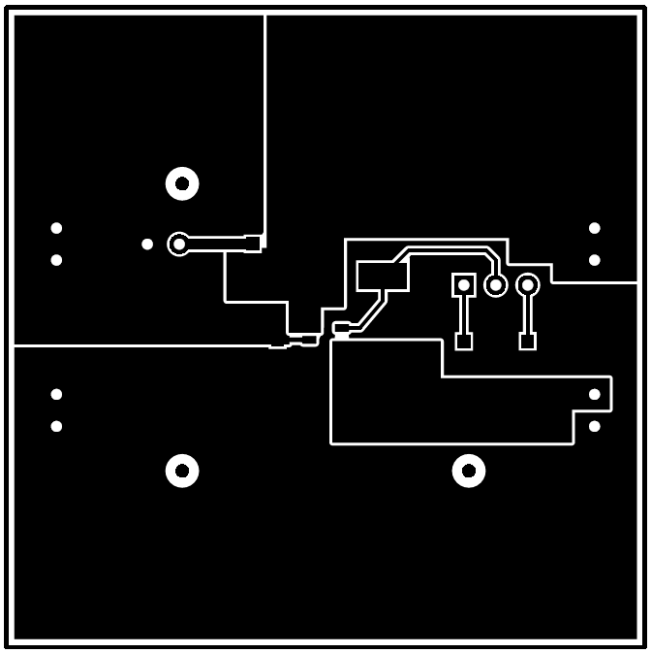

Figure 8. Top Layer

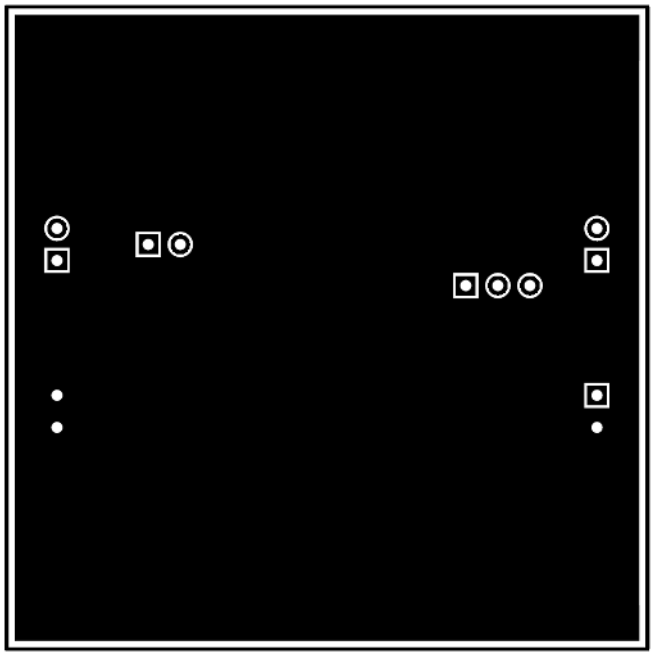

Figure 9. Bottom Layer

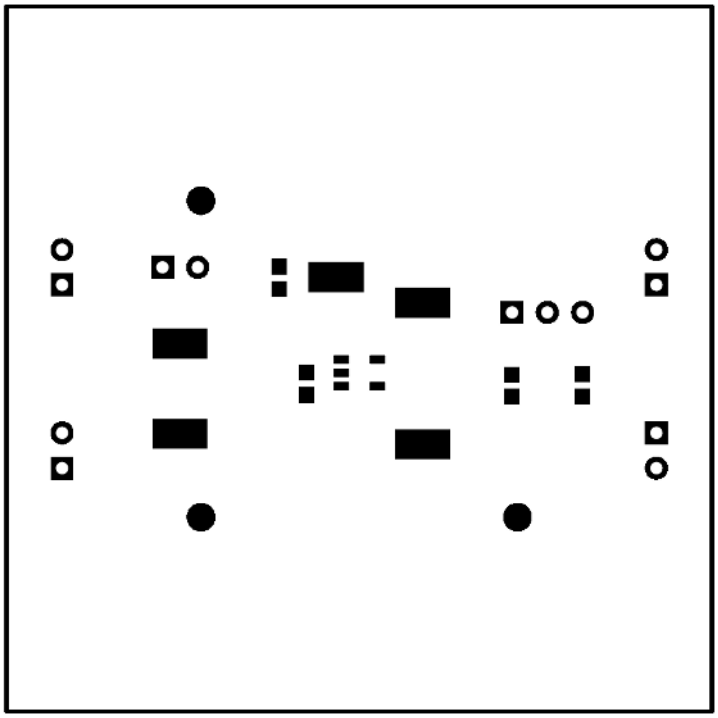

Figure 10. Top Solder Mask

3 EVM Connectors

This section describes the connectors, jumpers, and test points on the EVM as well as how to connect, set up, and properly use the EVM. Each device has an independent supply connection, but all grounds are connected on the board.

3.1 EVM Test Points

Table 2 lists the test points and functional descriptions. All pins of the device are broken out to test points on the EVM.

Table 2. Test Points

TEST POINT NUMBER	TEST POINT SILKSCREEN LABEL	FUNCTION	DESCRIPTION
TP1	VDD	Connection to VDD pin	Allows user to monitor the VDD pin. The VDD pin connects to the input power supply.
TP2	CT	Connection to CT pin	Allows user to monitor the CT pin. This pin charges up according to the CT pin configuration. The CT capacitor sets the reset delay.
TP3	$\overline{\text{RESET}}$	Connection to $\overline{\text{RESET}}$ pin	Allows user to monitor the $\overline{\text{RESET}}$ output pin.
TP4	$\overline{\text{MR}}$	Connection to $\overline{\text{MR}}$ pin	Allows user to monitor the logic level of the manual reset pin. Logic low on $\overline{\text{MR}}$ forces a reset.
TP5	GND	Connection to GND pin.	Allows user to connect to the ground plane.

3.2 EVM Jumpers

Table 3 lists the jumpers on the TLV840EVM. As ordered, the EVM will have five jumpers installed.

Table 3. List of Onboard Jumpers

JUMPER	DEFAULT CONNECTION	DESCRIPTION
J1	Shorted	Both pins on J1 are connected together. Connect either pin on jumper J1 to the input power supply.
J2	Closed	Connect a shunt jumper to jumper J2 to use R1 as the pull-up resistor on the $\overline{\text{RESET}}$ output pin.
J3	Shorted	Both pins on J3 are connected together. Use either pin on jumper J3 to monitor the $\overline{\text{RESET}}$ output pin.
J4	Closed (pin 1, pin 2)	Jumper J4 configures the CT pin to set the reset delay. Connect a shunt jumper to pin 1 and pin 2 of jumper J4 to use C2 as the delay capacitor for the CT pin. Connect shunt jumper to pin 2 and pin 3 of jumper J4 to use C3 as the delay capacitor. Remove shunt jumper from jumper J4 to set the default fixed delay of 80 µs (maximum).
J5	Shorted	Both pins on J5 are connected together. Use either pin on jumper J5 as the ground connection.
J6	Open	Jumper J6 configures the manual reset pin. Remove shunt jumper from J6 and leave floating for normal operation. Connect shunt jumper to J6 to force a reset. Pin 1 of jumper J6 can also be connected to a control signal to set the logic level on $\overline{\text{MR}}$ pin. If pin 1 on jumper J6 is logic low, the device remains in reset.

4 EVM Setup and Operation

This section describes the functionality and operation of the TLV840EVM. The user must read the TLV840 datasheet for electrical characteristics of the device.

4.1 Input Power (V_{DD})

The VDD supply is connected through the J1 header on board. Both pins of jumper J1 are connected together so power can be applied to either pin. Supply voltage is dependent on what the user wants to monitor, but the range is 0.7 V to 6 V. Table 4 details the nominal supply and typical threshold voltage.

Table 4. Nominal Supply and Typical Threshold Voltages

Device	Nominal Supply Voltage (V)	Typical Threshold Voltage (V)
TLV840MADL13	1.3	1.3 ± 1%

4.1.1 Manual Reset ($\overline{MR}$)

The TLV840 devices offers a manual reset pin that is utilized via jumper J6. If a shunt jumper is placed on jumper J6, the $\overline{RESET}$ pin is asserted and forced into a low state. After the shunt jumper is removed and VDD is above its reset threshold, $\overline{MR}$ returns to a logic high due to the internal pull-up resistor, and $\overline{RESET}$ is deasserted to logic high after the user-defined delay expires. If jumper J6 is left floating, the device operates normally as the $\overline{MR}$ pin defaults to logic high. Pin 1 of jumper J6 can also be connected to a control signal to set the logic level on $\overline{MR}$ pin. If pin 1 on jumper J6 is logic low, the device asserts a reset. There is also a test point TP4 connected directly to the $\overline{MR}$ pin in case the user wants to monitor the $\overline{MR}$ pin. See Figure 11 through Figure 14.

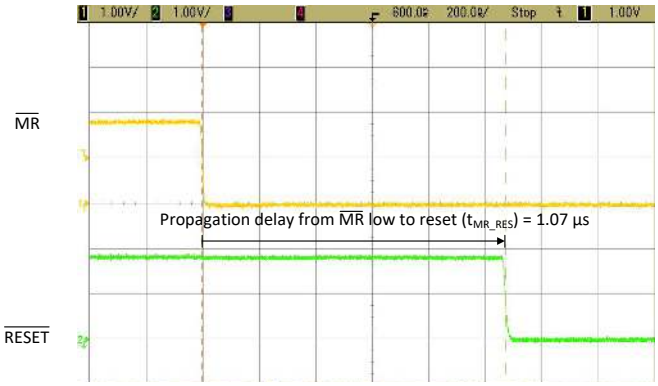

Figure 11. TLV840EVM $\overline{RESET}$ Asserted Due to $\overline{MR}$ Pulled Low

Figure 12. TLV840EVM $\overline{RESET}$ Deasserted Due to $\overline{MR}$ Pulled High, C_T Floating

4.2 Monitoring Voltage on VDD

The TLV840 device monitors voltage via the VDD pin. The EVM provides jumper J1 and test point TP1 for connecting the power supply input to the VDD pin. If the voltage on this pin drops below V_{IT-}, $\overline{RESET}$ is asserted low. The VDD pin is connected internally to a comparator through an internal resistor divider at the positive input and the negative input is connected to an internal reference. The internal resistor divider is set to provide the input voltage threshold to cause a reset, V_{IT-}, that corresponds to the chosen device variant. Please see the Device Comparison Table in the TLV840 Datasheet for more information on the different device variants.

Upon startup, the TLV840 requires VDD to be above $V_{DD\ (MIN)}$ = 0.7 V before the $\overline{RESET}$ output is in the correct logic state. The TLV840 has built-in glitch immunity so voltage transients on VDD are ignored if the pulse duration is 10 µs or less as shown in Figure 13. The glitch immunity specification depends on the amplitude of the voltage transient and the operating conditions. Please see the Glitch Immunity specification in the Timing Requirements section of the TLV840 Datasheet for more detailed information.

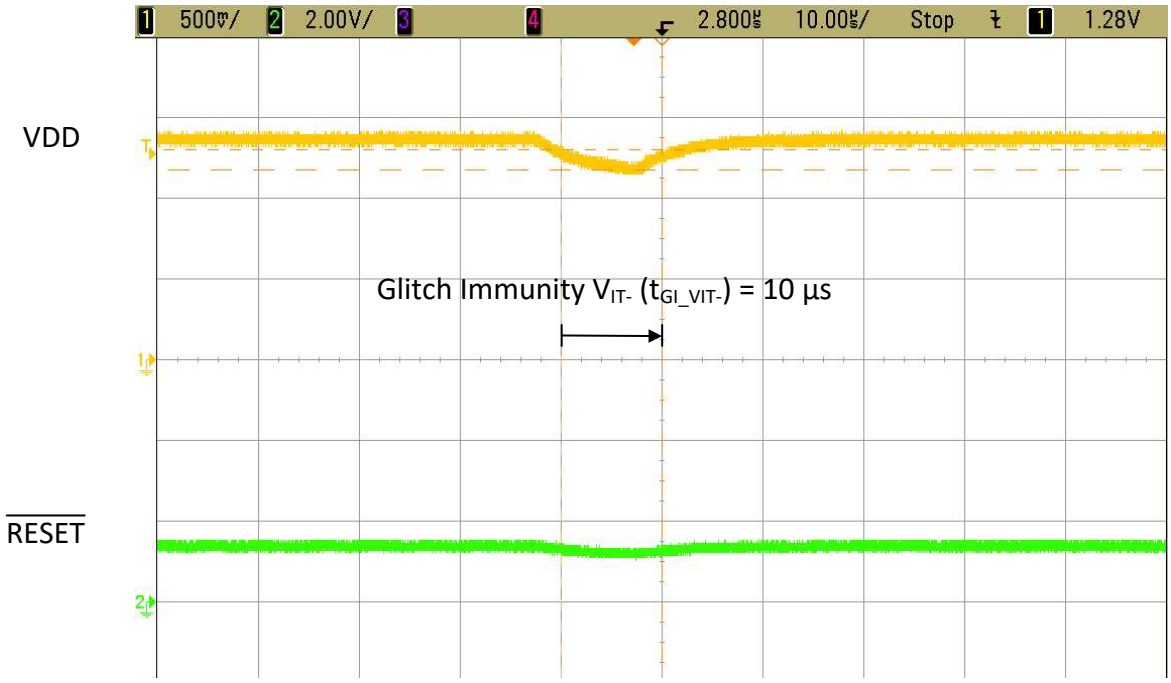

Figure 13. TLV840EVM Glitch Immunity

4.3 Reset Output ($\overline{RESET}$)

The TLV840EVM comes populated with TLV840MADL29 device variant which has open-drain, active-low output topology for the $\overline{RESET}$ pin. The other device variants provide different output topolgies and can be used on this EVM. Note: if using a TLV840 device variant with push-pull output topology, the pull-up resistor must be disconnected by leaving jumper J2 open. The EVM provides a jumper J3 and a test point TP3 connected directly to the $\overline{RESET}$ pin for monitoring and/or interfacing to other devices. The reset signal will be asserted low when $\overline{MR}$ is pulled low or when the voltage on the VDD pin falls below VIT-. When the voltage on VDD rises higher than the hysteresis voltage above the threshold voltage, and the $\overline{MR}$ pin is pulled high or floating, the reset pins will deassert and remain deasserted until a reset condition occurs again.

4.4 Reset Time Delay Programming (Program t_D via CT)

The TLV840 device has two options for setting the $\overline{RESET}$ time delay: connect CT pin to a capacitor to GND, or leave CT pin floating. The reset time delay can be set to a minimum value of 80 µs by leaving the CT pin floating, or a maximum value of approximately 6.2 seconds by connecting 10 µF delay capacitor. The reset time delay (t_D) can be programmed to any value within the range by connecting a capacitor no larger than 10 µF between CT pin and GND. The relationship between external capacitor (C_{CT_EXT}) at CT pin and the $\overline{RESET}$ time delay is given by Equation 1.

$$t_D = -\ln(0.29) \times R_{CT} \times C_{CT\_EXT} + t_D \text{ (no cap)} \quad (1)$$

Equation 1 is simplified to Equation 2 by plugging R_{CT} and $T_{D(no\ cap)}$ given in the Electrical Characteristics Table in TLV840 Datasheet

$$t_D = 618937 \times C_{CT\_EXT} + 80\mu s \quad (2)$$

Equation 3 solves for external capacitor value (C_{CT_EXT})

$$C_{CT\_EXT} = (t_D - 80\mu s) \div 618937 \quad (3)$$

The recommended maximum delay capacitor for the TLV840 is limited to 10 µF as this ensures there is enough time for the capacitor to fully discharge when the reset condition occurs. When a voltage fault occurs, the previously charged up capacitor discharges, and if the monitored voltage returns from the fault condition before the delay capacitor discharges completely, the delay capacitor will begin charging from a voltage above zero and the reset delay will be shorter than expected. Larger delay capacitors can be used so long as the capacitor has enough time to fully discharge during the duration of the voltage fault.

The EVM provides the jumper J4 to configure the CT pin and test point TP2 to monitor the CT pin. Place a shunt jumper on pin 1 (left pin) and pin 2 (middle pin) of jumper J4 to connect CT to delay capacitor C2. This connects the CT pin to a 0.1-µF capacitor to set the $\overline{\text{RESET}}$ delay (t_D) to ~61.9 ms as shown in Figure 14. Or place a shunt jumper on pin 2 (middle pin) and pin 3 (right pin) of jumper J4 to connect CT to delay capacitor C3. This connects the CT pin to a 0.01-µF capacitor to set the $\overline{\text{RESET}}$ delay (t_D) to ~6.2 ms as shown in Figure 15. By removing the shunt jumper from jumper J4, the $\overline{\text{RESET}}$ time delay defaults to the minimum value of 40 µs. Figure 16 shows the actual delay with no capacitor may be shorter than the typical value of 40 µs. If using a different delay capacitor, the capacitor must be ≥ 100pF to be recognized.

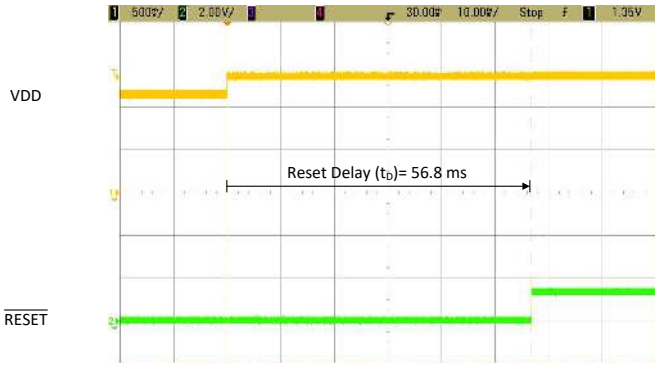

Figure 14. TLV840EVM $\overline{\text{RESET}}$ Delay Time (t_D) with C_T Tied to GND Through 0.1-µF Capacitor

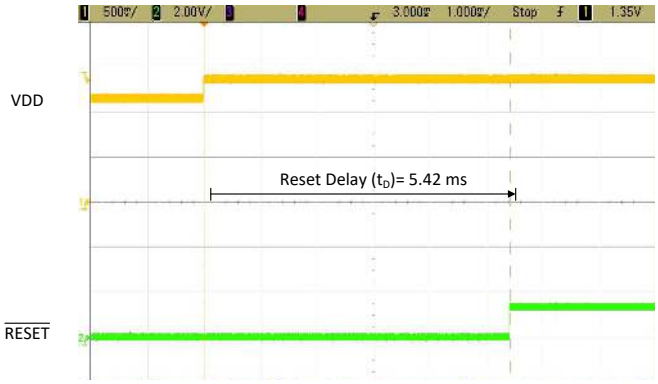

Figure 15. TLV840EVM $\overline{\text{RESET}}$ Delay Time (t_D) with C_T Tied to GND Through 0.01-µF Capacitor

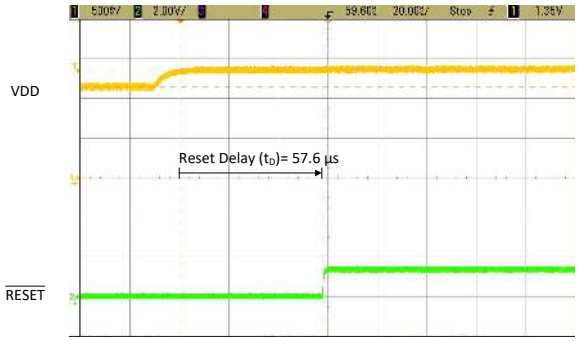

Figure 16. TLV840EVM $\overline{\text{RESET}}$ Delay Time (t_D) with C_T Floating

Revision History

DATE	REVISION	NOTES
February 2020	*	Initial Release

IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265