

# C3M0075120J

## Silicon Carbide Power MOSFET

### C3M™ MOSFET Technology

#### N-Channel Enhancement Mode

#### Features

- 3rd generation SiC MOSFET technology
- Low impedance package with driver source pin
- 7mm of creepage distance between drain and source
- High blocking voltage with low on-resistance
- High-speed switching with low capacitances
- Fast intrinsic diode with low reverse recovery ( $Q_{rr}$ )
- Halogen free, RoHS compliant

#### Benefits

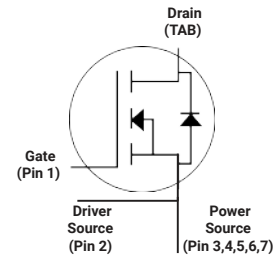
- Reduce switching losses and minimize gate ringing
- Higher system efficiency
- Reduce cooling requirements
- Increase power density
- Increase system switching frequency

#### Applications

- Renewable energy
- EV battery chargers
- High voltage DC/DC converters
- Switch Mode Power Supplies

$V_{DS}$	1200 V
$I_D @ 25^\circ\text{C}$	30 A
$R_{DS(on)}$	75 m $\Omega$

#### Package



Part Number	Package	Marking
C3M0075120J	TO-263-7	C3M0075120J

#### Maximum Ratings ( $T_C = 25^\circ\text{C}$ unless otherwise specified)

Symbol	Parameter	Value	Unit	Test Conditions	Note
$V_{DSmax}$	Drain - Source Voltage	1200	V	$V_{GS} = 0\text{ V}, I_D = 100\ \mu\text{A}$	
$V_{GSmax}$	Gate - Source Voltage (dynamic)	-8/+19	V	AC ( $f > 1\text{ Hz}$ )	Note: 1
$V_{GSop}$	Gate - Source Voltage (static)	-4/+15	V	Static	Note: 2
$I_D$	Continuous Drain Current	30	A	$V_{GS} = 15\text{ V}, T_C = 25^\circ\text{C}$	Fig. 19
		19.7		$V_{GS} = 15\text{ V}, T_C = 100^\circ\text{C}$	
$I_{D(pulse)}$	Pulsed Drain Current	80	A	Pulse width $t_p$ limited by $T_{jmax}$	Fig. 22
$P_D$	Power Dissipation	113.6	W	$T_C = 25^\circ\text{C}, T_J = 150^\circ\text{C}$	Fig. 20
$T_J, T_{stg}$	Operating Junction and Storage Temperature	-55 to +150	$^\circ\text{C}$		
$T_L$	Solder Temperature	260	$^\circ\text{C}$	1.6mm (0.063") from case for 10s	

Note (1): When using MOSFET Body Diode  $V_{GSmax} = -4\text{V}/+19\text{V}$

Note (2): MOSFET can also safely operate at  $0/+15\text{ V}$

### Electrical Characteristics (T<sub>c</sub> = 25°C unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Unit	Test Conditions	Note
V <sub>(BR)DSS</sub>	Drain-Source Breakdown Voltage	1200			V	V <sub>GS</sub> = 0 V, I <sub>D</sub> = 100 μA	
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.8	2.5	3.6	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 5 mA	Fig. 11
			2.2		V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 5 mA, T <sub>J</sub> = 150°C	
I <sub>DSS</sub>	Zero Gate Voltage Drain Current		1	50	μA	V <sub>DS</sub> = 1200 V, V <sub>GS</sub> = 0 V	
I <sub>GSS</sub>	Gate-Source Leakage Current		10	250	nA	V <sub>GS</sub> = 15 V, V <sub>DS</sub> = 0 V	
R <sub>DS(on)</sub>	Drain-Source On-State Resistance		75	90	mΩ	V <sub>GS</sub> = 15 V, I <sub>D</sub> = 20 A	Fig. 4, 5, 6
			100			V <sub>GS</sub> = 15 V, I <sub>D</sub> = 20 A, T <sub>J</sub> = 150°C	
g <sub>fs</sub>	Transconductance		12		S	V <sub>DS</sub> = 20 V, I <sub>DS</sub> = 20 A	Fig. 7
			13			V <sub>DS</sub> = 20 V, I <sub>DS</sub> = 20 A, T <sub>J</sub> = 150°C	
C <sub>iss</sub>	Input Capacitance		1390		pF	V <sub>GS</sub> = 0 V, V <sub>DS</sub> = 1000 V f = 1 MHz V <sub>AC</sub> = 25 mV	Fig. 17, 18
C <sub>oss</sub>	Output Capacitance		58				
C <sub>rss</sub>	Reverse Transfer Capacitance		2				
E <sub>oss</sub>	C <sub>oss</sub> Stored Energy		33		μJ		Fig. 16
E <sub>ON</sub>	Turn-On Switching Energy (Body Diode FWD)		200		μJ	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = -4 V/15 V, I <sub>D</sub> = 20 A, R <sub>G(ext)</sub> = 0 Ω, L = 156 μH, T <sub>J</sub> = 150°C	Fig. 26, 29
E <sub>OFF</sub>	Turn-Off Switching Energy (Body Diode FWD)		90				
t <sub>d(on)</sub>	Turn-On Delay Time		7		ns	V <sub>DD</sub> = 800 V, V <sub>GS</sub> = -4 V/15 V I <sub>D</sub> = 20 A, R <sub>G(ext)</sub> = 0 Ω, Timing relative to V <sub>DS</sub> Inductive load	Fig. 27, 28, 29
t <sub>r</sub>	Rise Time		15				
t <sub>d(off)</sub>	Turn-Off Delay Time		24				
t <sub>f</sub>	Fall Time		8				
R <sub>G(int)</sub>	Internal Gate Resistance		9		Ω	f = 1 MHz, V <sub>AC</sub> = 25 mV	
Q <sub>gs</sub>	Gate to Source Charge		18		nC	V <sub>DS</sub> = 800 V, V <sub>GS</sub> = -4 V/15 V I <sub>D</sub> = 20 A Per IEC60747-8-4 pg 21	Fig. 12
Q <sub>gd</sub>	Gate to Drain Charge		12				
Q <sub>g</sub>	Total Gate Charge		48				

### Reverse Diode Characteristics (T<sub>c</sub> = 25°C unless otherwise specified)

Symbol	Parameter	Typ.	Max.	Unit	Test Conditions	Note
V <sub>SD</sub>	Diode Forward Voltage	4.5		V	V <sub>GS</sub> = -4 V, I <sub>SD</sub> = 10 A	Fig. 8, 9, 10
		4.0		V	V <sub>GS</sub> = -4 V, I <sub>SD</sub> = 10 A, T <sub>J</sub> = 150 °C	
I <sub>S</sub>	Continuous Diode Forward Current		22.4	A	V <sub>GS</sub> = -4 V	Note 1
I <sub>S, pulse</sub>	Diode pulse Current	80		A	V <sub>GS</sub> = -4 V, pulse width t <sub>p</sub> limited by T <sub>Jmax</sub>	Note 1
t <sub>rr</sub>	Reverse Recover time	25		ns	V <sub>GS</sub> = -4 V, I <sub>SD</sub> = 20 A, V <sub>R</sub> = 800 V dif/dt = 1925 A/μs, T <sub>J</sub> = 25 °C	Note 1, Fig. 29
Q <sub>rr</sub>	Reverse Recovery Charge	109		nC		
I <sub>rrm</sub>	Peak Reverse Recovery Current	11		A		

### Thermal Characteristics

Symbol	Parameter	Max.	Unit	Test Conditions	Note
R <sub>θJC</sub>	Thermal Resistance from Junction to Case	1.1	°C/W		Fig. 21
R <sub>θJA</sub>	Thermal Resistance From Junction to Ambient	40			

## Typical Performance

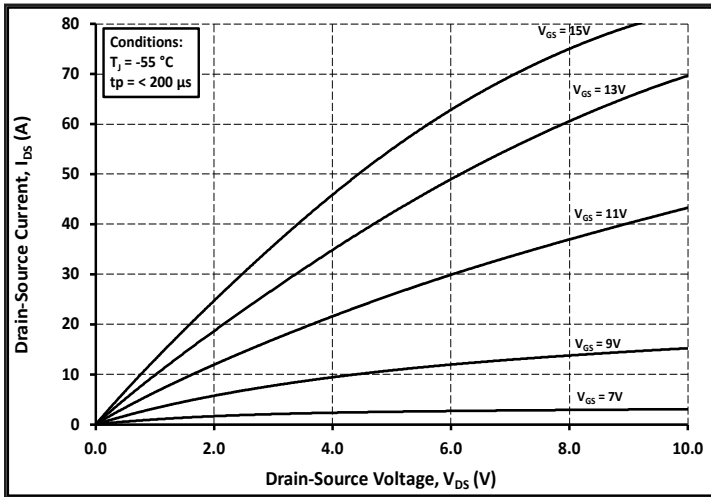


Figure 1. Output Characteristics  $T_J = -55\text{ }^\circ\text{C}$

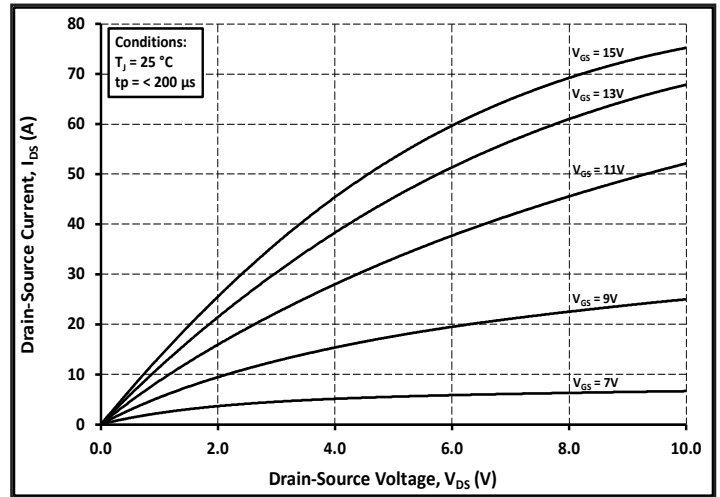


Figure 2. Output Characteristics  $T_J = 25\text{ }^\circ\text{C}$

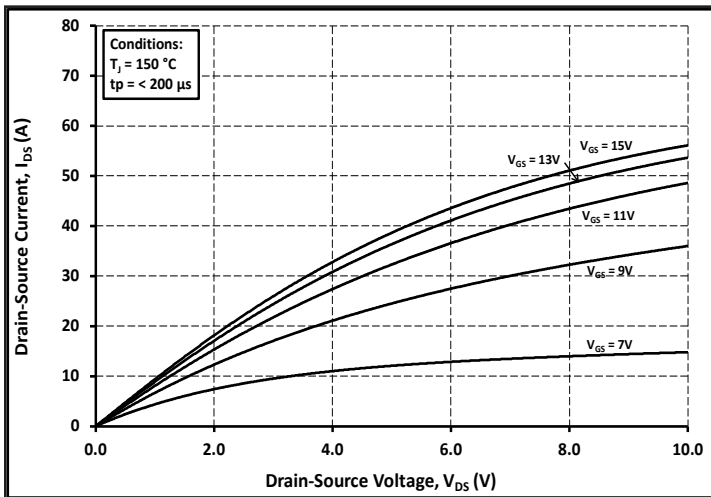


Figure 3. Output Characteristics  $T_J = 150\text{ }^\circ\text{C}$

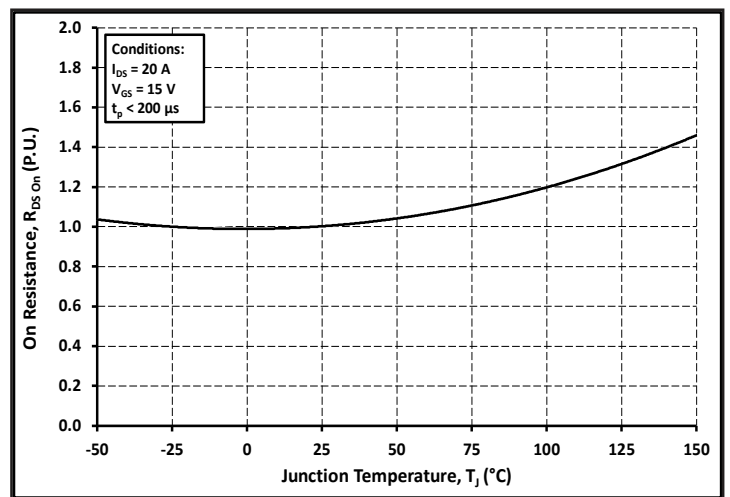


Figure 4. Normalized On-Resistance vs. Temperature

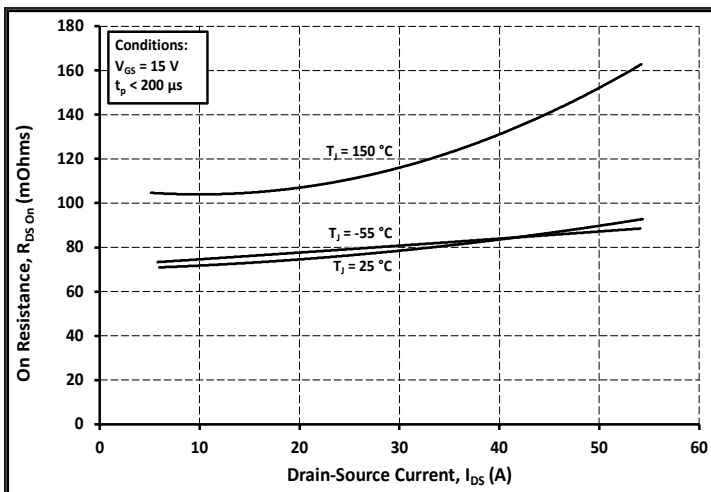


Figure 5. On-Resistance vs. Drain Current For Various Temperatures

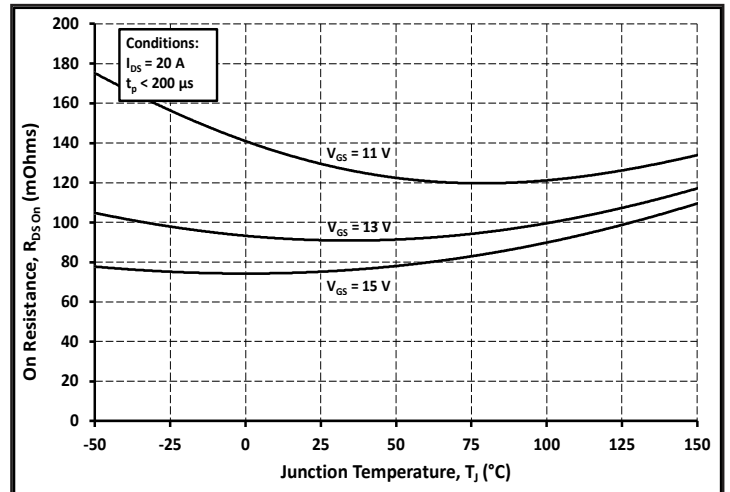


Figure 6. On-Resistance vs. Temperature For Various Gate Voltage

## Typical Performance

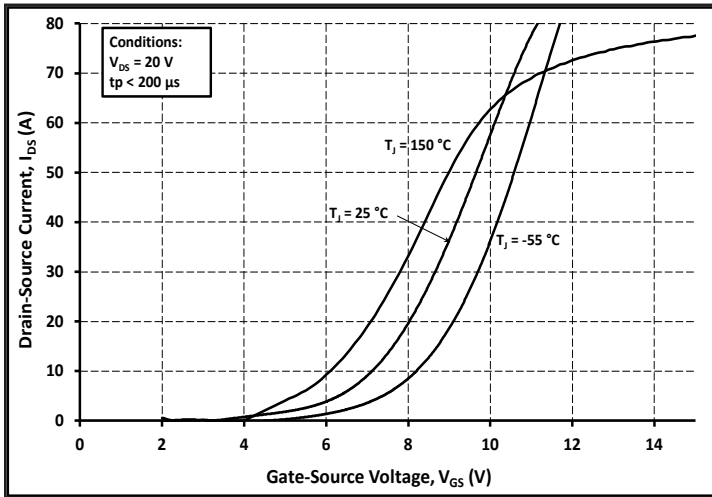


Figure 7. Transfer Characteristic for Various Junction Temperatures

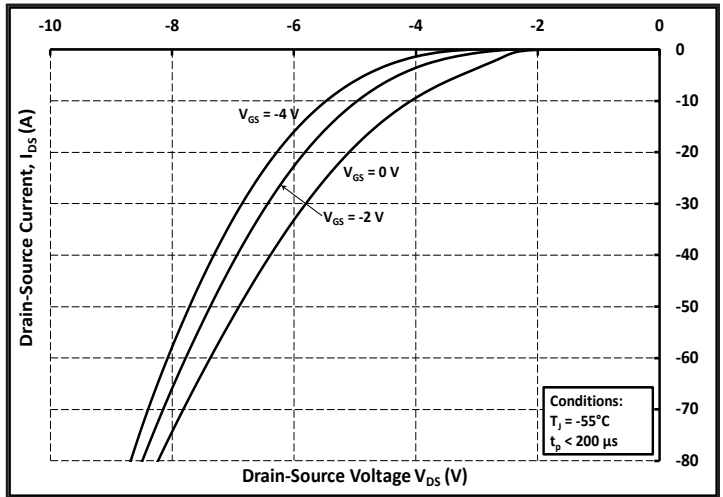


Figure 8. Body Diode Characteristic at -55 °C

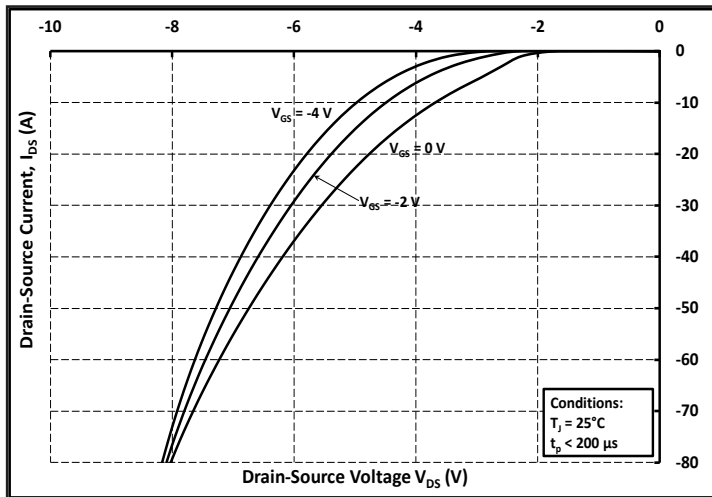


Figure 9. Body Diode Characteristic at 25 °C

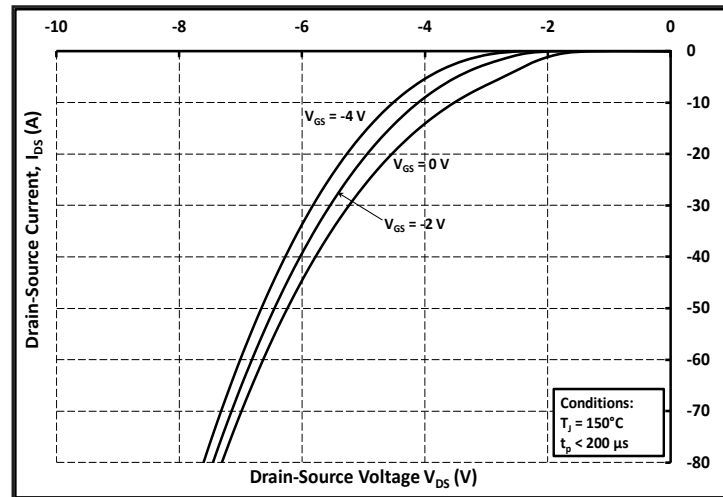


Figure 10. Body Diode Characteristic at 150 °C

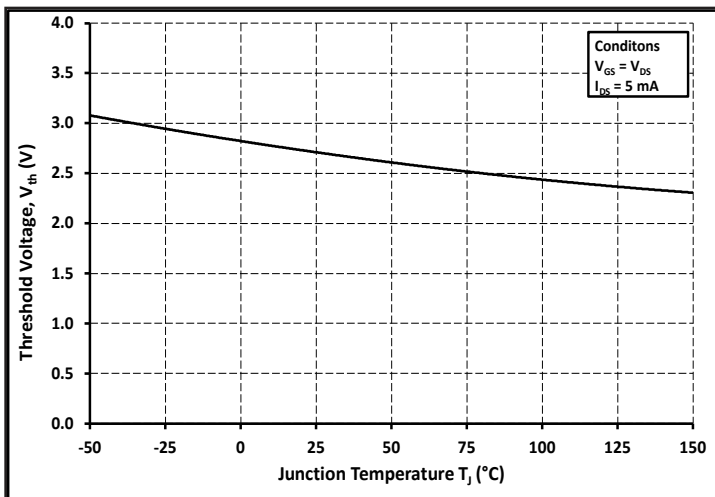


Figure 11. Threshold Voltage vs. Temperature

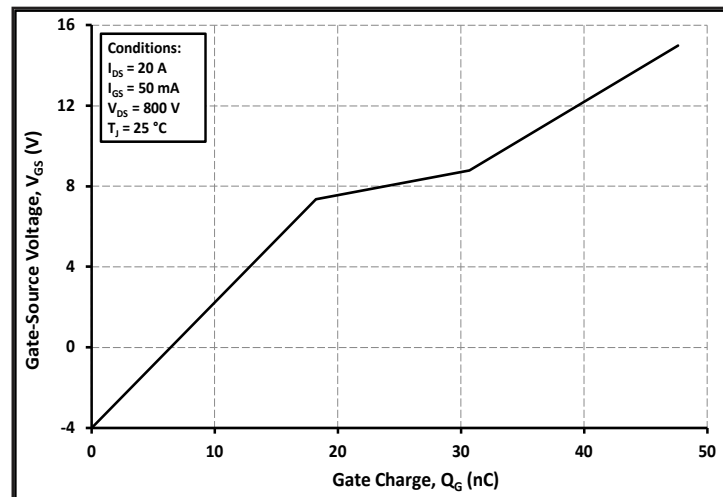


Figure 12. Gate Charge Characteristics

## Typical Performance

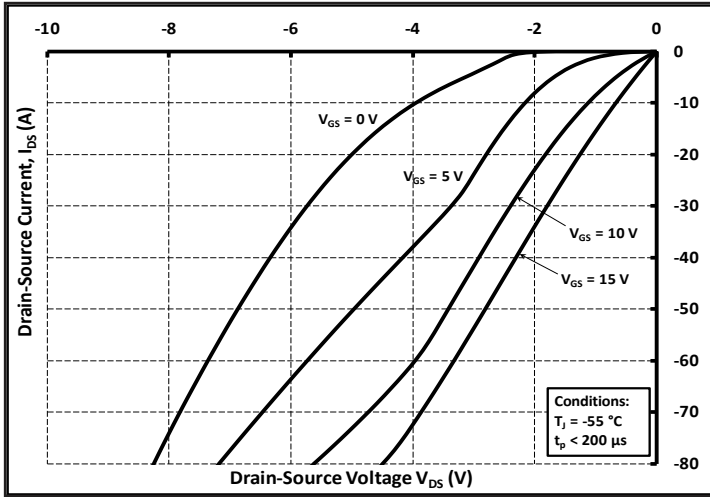


Figure 13. 3rd Quadrant Characteristic at -55 °C

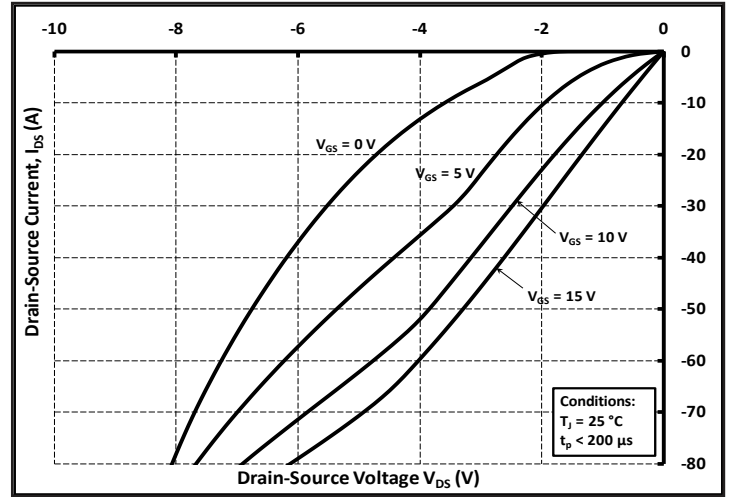


Figure 14. 3rd Quadrant Characteristic at 25 °C

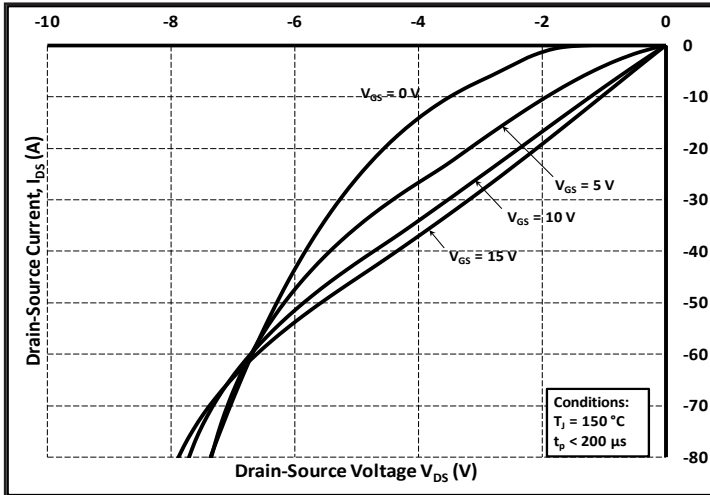


Figure 15. 3rd Quadrant Characteristic at 150 °C

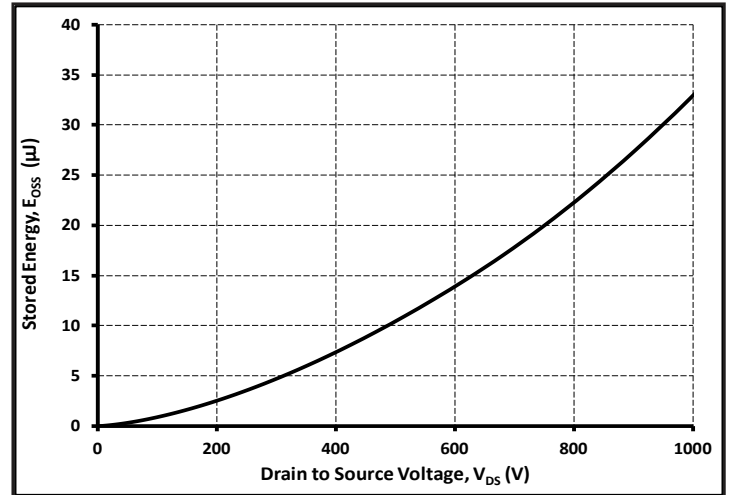


Figure 16. Output Capacitor Stored Energy

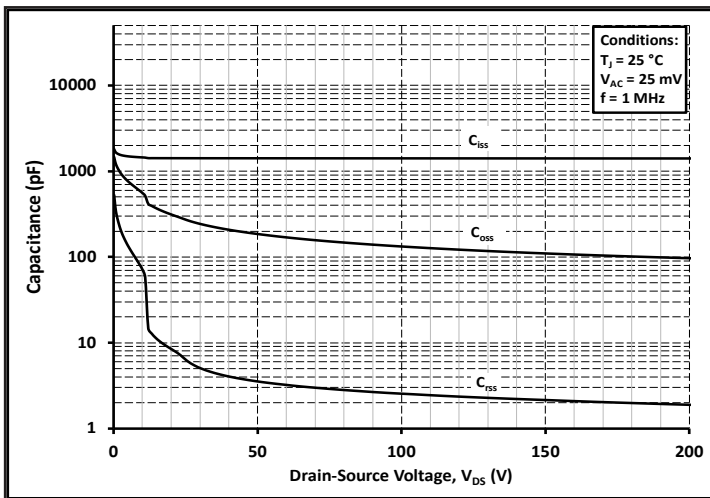


Figure 17. Capacitances vs. Drain-Source Voltage (0 - 200V)

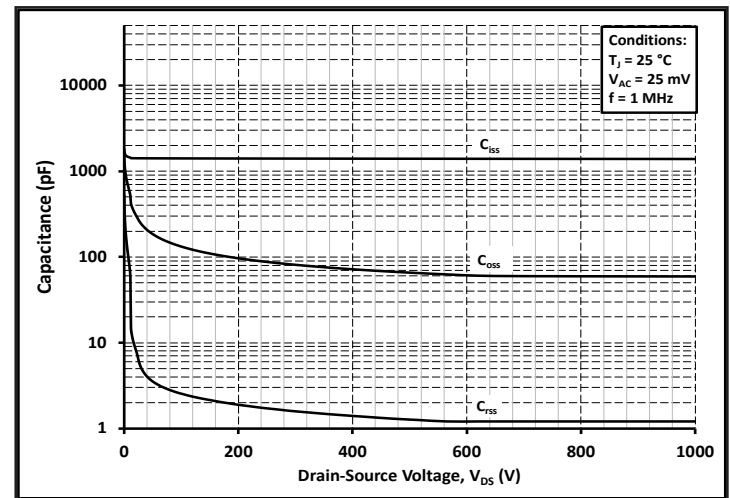


Figure 18. Capacitances vs. Drain-Source Voltage (0 - 1000V)

## Typical Performance

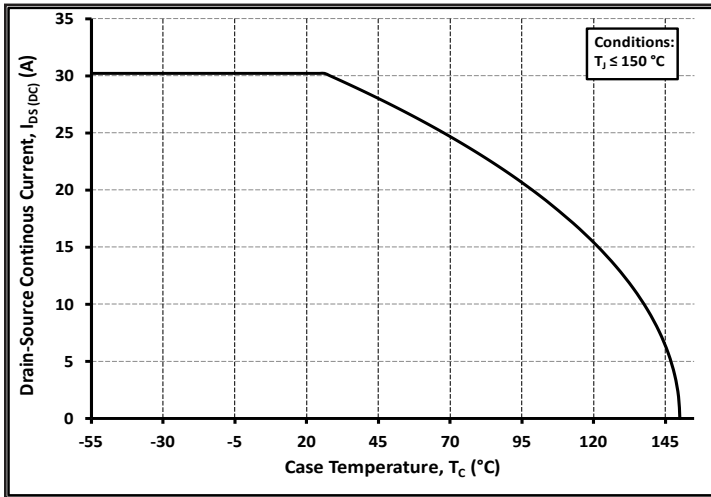


Figure 19. Continuous Drain Current Derating vs. Case Temperature

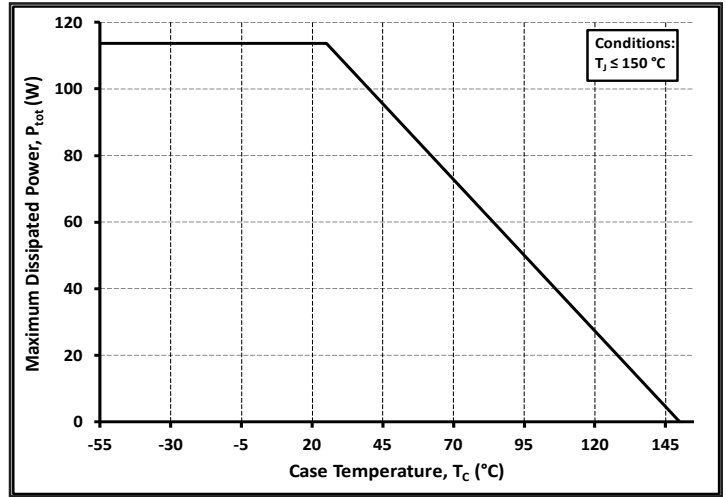


Figure 20. Maximum Power Dissipation Derating vs. Case Temperature

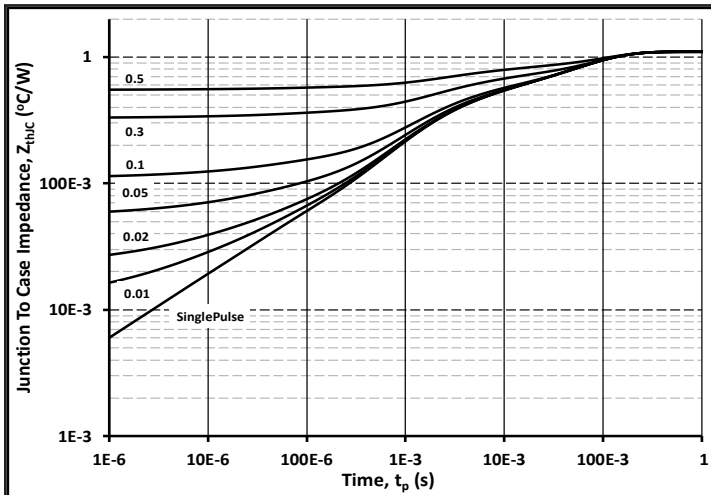


Figure 21. Transient Thermal Impedance (Junction - Case)

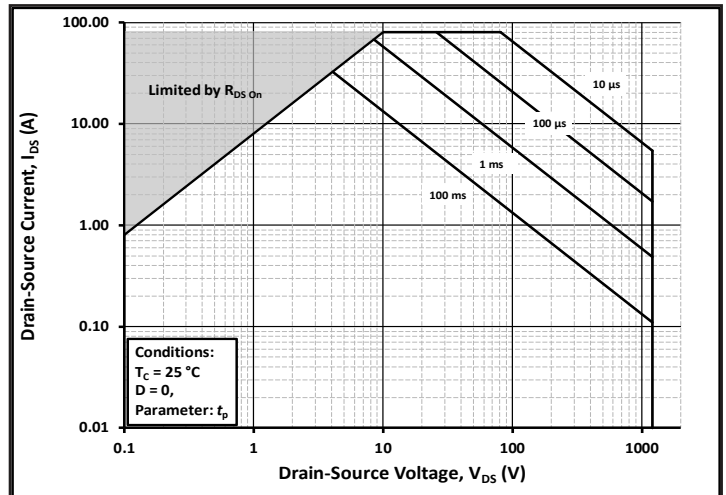


Figure 22. Safe Operating Area

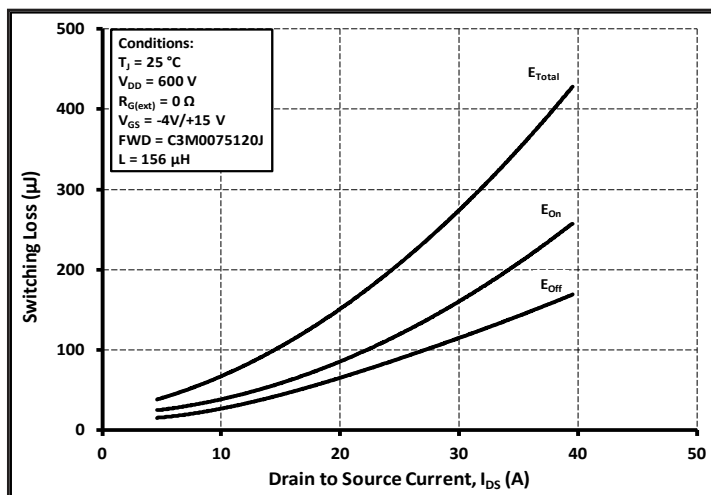


Figure 23. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 600V$ )

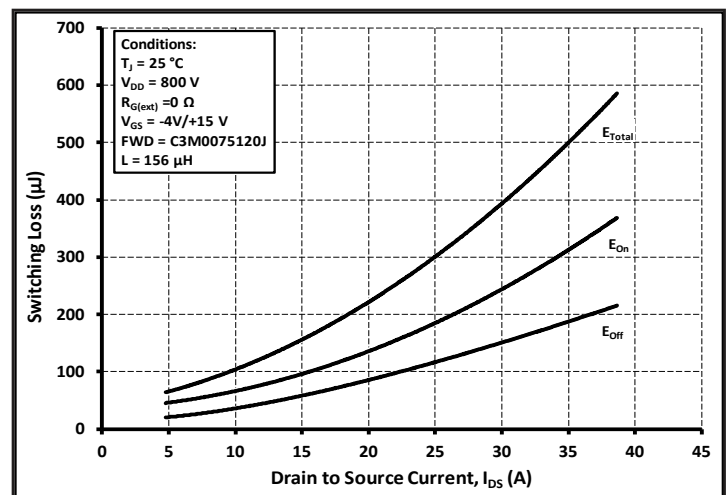


Figure 24. Clamped Inductive Switching Energy vs. Drain Current ( $V_{DD} = 800V$ )

## Typical Performance

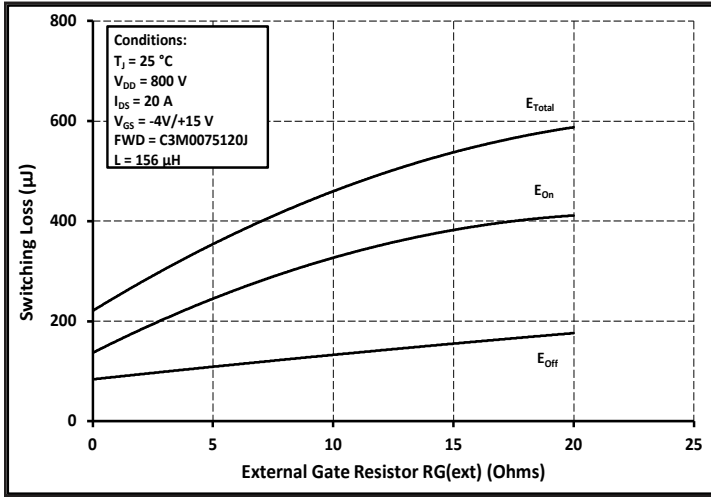


Figure 25. Clamped Inductive Switching Energy vs.  $R_{G(ext)}$

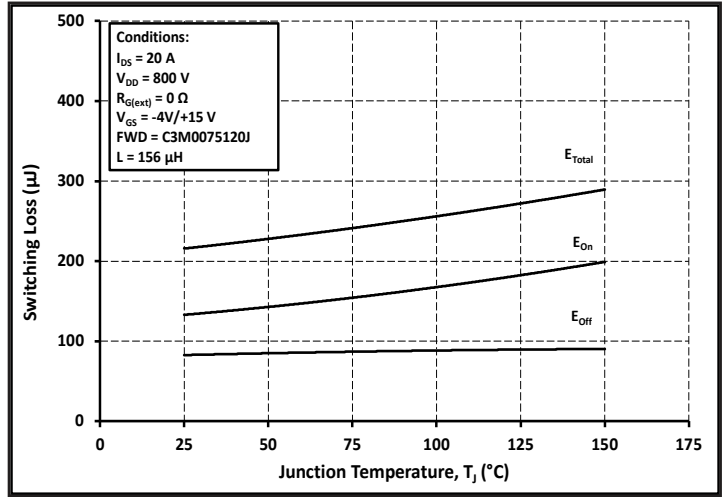


Figure 26. Clamped Inductive Switching Energy vs. Temperature

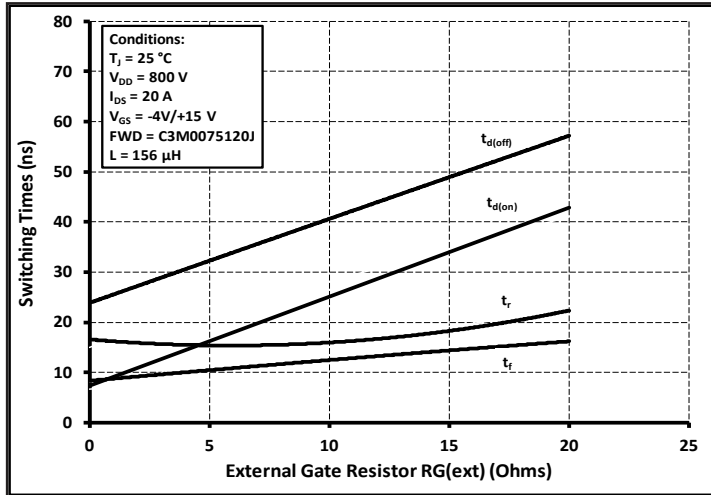


Figure 27. Switching Times vs.  $R_{G(ext)}$

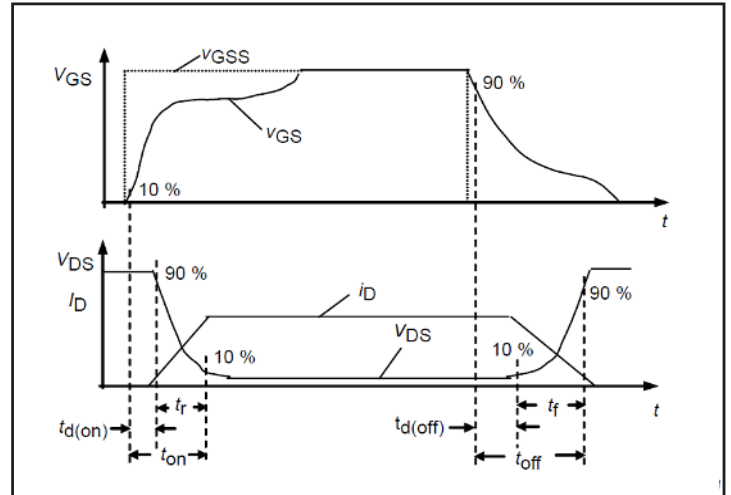


Figure 28. Switching Times Definition

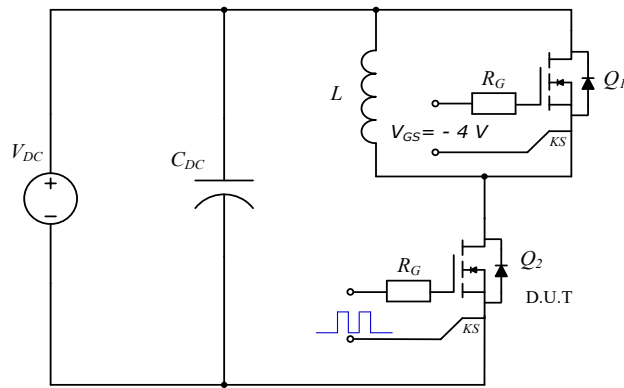


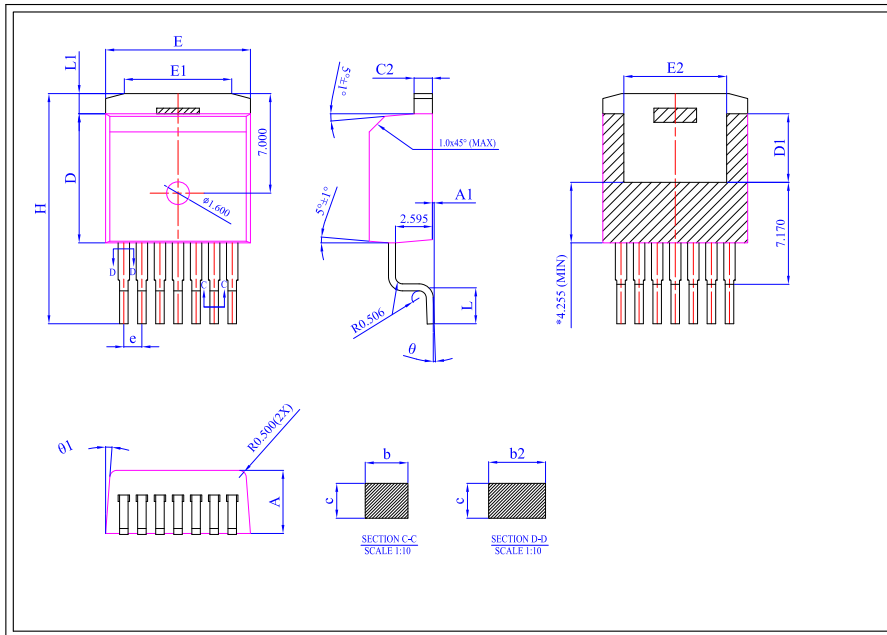
Figure 29. Clamped Inductive Switching Waveform Test Circuit

Note (3): Turn-off and Turn-on switching energy and timing values measured using SiC MOSFET Body Diode as shown above.

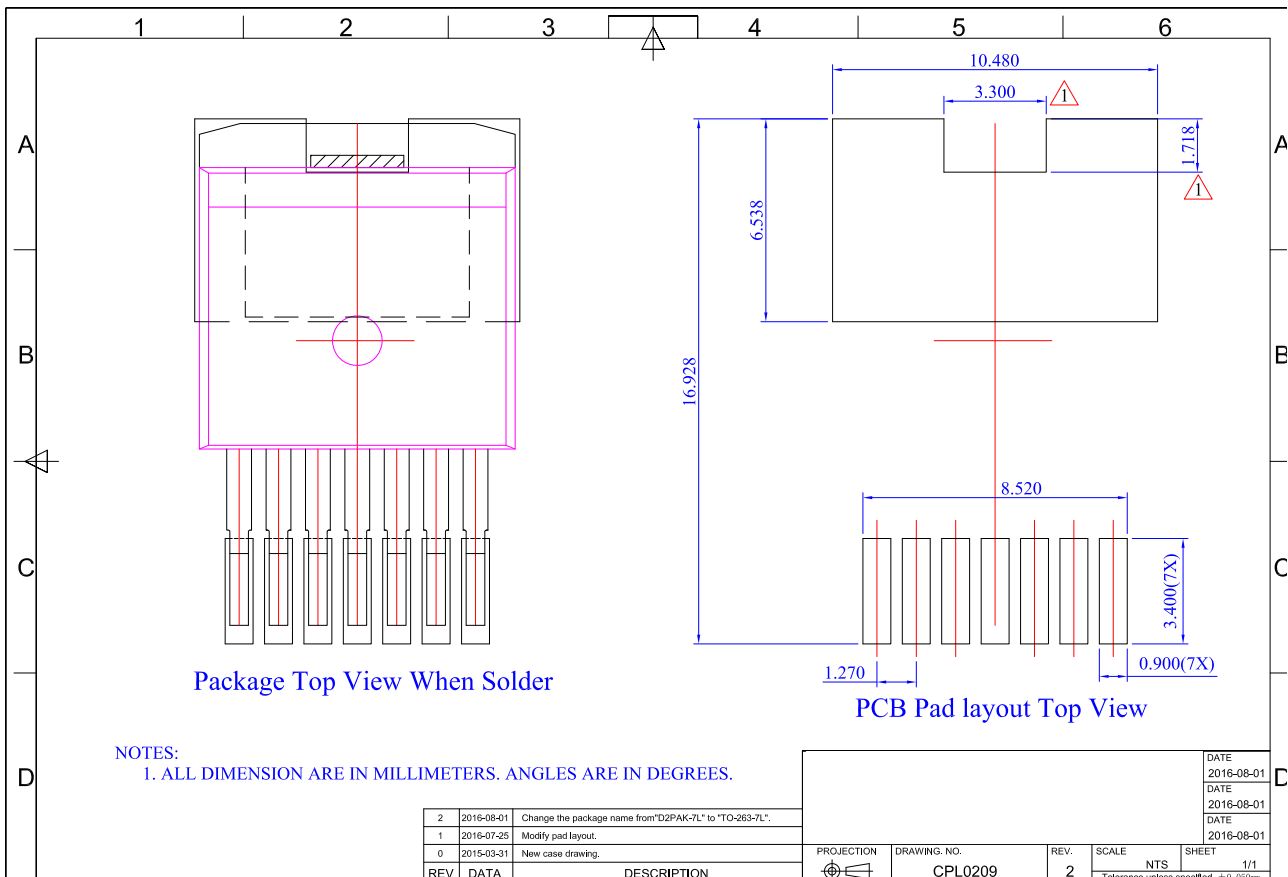


## Package Dimensions

### Package 7L D2PAK



Dim	All Dimensions in Millimeters		
	Min	typ	Max
A	4.300	4.435	4.570
A1	0.00	0.125	0.25
b	0.500	0.600	0.700
b2	0.600	0.800	1.000
c	0.330	0.490	0.650
C2	1.170	1.285	1.400
D	9.025	9.075	9.125
D1	4.700	4.800	4.900
E	10.130	10.180	10.230
E1	6.500	7.550	8.600
E2	6.778	7.223	7.665
e	1.27		
H	15.043	16.178	17.313
L	2.324	2.512	2.700
L1	0.968	1.418	1.868
$\theta$	0°	4°	8°
$\theta 1$	4.5°	5°	5.5°



## Notes

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- **RoHS Compliance**  
The levels of RoHS restricted materials in this product are below the maximum concentration values (also referred to as the threshold limits) permitted for such substances, or are used in an exempted application, in accordance with EU Directive 2011/65/EC (RoHS2), as implemented January 2, 2013. RoHS Declarations for this product can be obtained from your Cree representative or from the Product Documentation sections of [www.cree.com](http://www.cree.com).
- **REACH Compliance**  
REACH substances of high concern (SVHCs) information is available for this product. Since the European Chemical Agency (ECHA) has published notice of their intent to frequently revise the SVHC listing for the foreseeable future, please contact a Cree representative to insure you get the most up-to-date REACH SVHC Declaration. REACH banned substance information (REACH Article 67) is also available upon request.
- This product has not been designed or tested for use in, and is not intended for use in, applications implanted into the human body nor in applications in which failure of the product could lead to death, personal injury or property damage, including but not limited to equipment used in the operation of nuclear facilities, life-support machines, cardiac defibrillators or similar emergency medical equipment, aircraft navigation or communication or control systems, air traffic control systems.

## Related Links

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- **SPICE Models:** <http://wolfspeed.com/power/tools-and-support>
- **SiC MOSFET Isolated Gate Driver reference design:** <http://wolfspeed.com/power/tools-and-support>
- **SiC MOSFET Evaluation Board:** <http://wolfspeed.com/power/tools-and-support>