SJA1105

5-port automotive Ethernet switch

Rev. 1 — 7 November 2016 **Product data sheet**

1. General description

The SJA1105 is an IEEE 802.3-compliant 5-port automotive Ethernet switch. Each of the five ports can be individually configured to operate in MII, RMII and RGMII modes. This arrangement provides the flexibility to connect a mix of switches, microprocessors and PHY devices such as the TJA1100 BroadR-Reach PHY from NXP Semiconductors (Ref. 1 and Ref. 2) and other commercially available Fast Ethernet and Gigabit Ethernet PHYs. The high-speed interface makes it easy to cascade multiple SJA1105s for scalability. It can be used in various automotive scenarios such as gateway applications, body domain controllers or for interconnecting multiple ECUs in a daisy chain. Audio Video Bridging (AVB) support (Ref. 3) fully leverages infotainment and advanced driver assistance systems.

The SJA1105 comes in two pin-compatible variants. The SJA1105EL supports Ethernet and AVB. The SJA1105TEL includes additional functionality to support Time-Triggered Ethernet (TTEthernet) and Time-Sensitive Networking (TSN).

2. Features and benefits

2.1 General features

- 5-port store and forward architecture
- Each port individually configurable for MII and RMII operation at 10 Mbit/s or 100 Mbit/s and RGMII operation at 10 Mbit/s, 100 Mbit/s or 1000 Mbit/s
- Interface-dependent selectable I/O supply voltages; 1.2 V core voltage
- Small footprint: LFBGA159 (12 mm × 12 mm) package
- Automotive Grade 2 ambient operating temperature: –40 °C to +105 °C
- Automotive product qualification in accordance with AEC-Q100

2.2 Ethernet switching and AVB features

- IEEE 802.3 compliant
- 128 kB frame buffer
- 1024 entry MAC address learning table
- Address learning space can be configured for static and learned addresses
- 2 kB frame length handling
- IEEE 802.1Q defined tag support
- 4096 VLANs
- Egress tagging/untagging on a per-VLAN basis per port
- QoS handling based on IEEE 802.1Q
- Per-port priority remapping and 8 configurable egress queues per port

- Ingress rate-limiting on a per-port and per-priority basis for Unicast/Multicast and Broadcast traffic
- Frame replication and retagging of traffic
- Frame mirroring for enhanced diagnostics
- Hardware support for IEEE 802.1AS and IEEE 802.1Qav for AVB traffic support
- Ingress and egress timestamping per port
- Ten IEEE 802.1Qav credit-based shapers available; shapers can be freely allocated to any priority queue on a per port basis
- Support for AVB SR Class A, Class B and Class C traffic
- IEEE 1588v2 one-step sync forwarding in hardware
- IEEE 802.1X support for setting port reachability and disabling address learning
- Broadcast storm protection
- Statistics for dropped frames and buffer load

2.3 TT and TSN features (SJA1105TEL only)

- IEEE 802.1Qbv time-aware traffic
- IEEE 802.1Qci per-stream policing (pre-standard)
- Support for ring-based redundancy (for time-triggered traffic only)
- 1024 deterministic Ethernet flows with per-flow based:
  - Time-triggered traffic transmission
  - Ingress policing and reception window check
  - Active and redundant routes
  - Statistics

2.4 Interface features

- MII/RMII interfaces supporting all standard Ethernet PHY technologies such as (but not limited to) Fast Ethernet (IEEE 100BASE-TX), IEEE 100BASE-T1 and optical PHYs
- RGMII for interfacing with Gigabit Ethernet (1000BASE-T) PHYs (Gigabit Ethernet; Ref. 4)
- MAC and PHY modes for interfacing (MII/RMII/RGMII) directly with another switch or host processor
- Programmable drive strength for all interfaces
- SPI at up to 25 MHz for host processor access

2.5 Other features

- 25 MHz system clock input from crystal oscillator or AC-coupled single-ended clock
- 25 MHz reference clock output
- Device reset input from host processor
- IEEE 1149.1 compliant JTAG interface for TAP controller access and boundary scan

3. Ordering information

Table 1. Ordering information

Type number	Package		
	Name	Description	Version
SJA1105EL	LFBGA159	plastic low profile fine-pitch ball grid array package; 159 balls	SOT1427-1
SJA1105TEL			

4. Block diagram

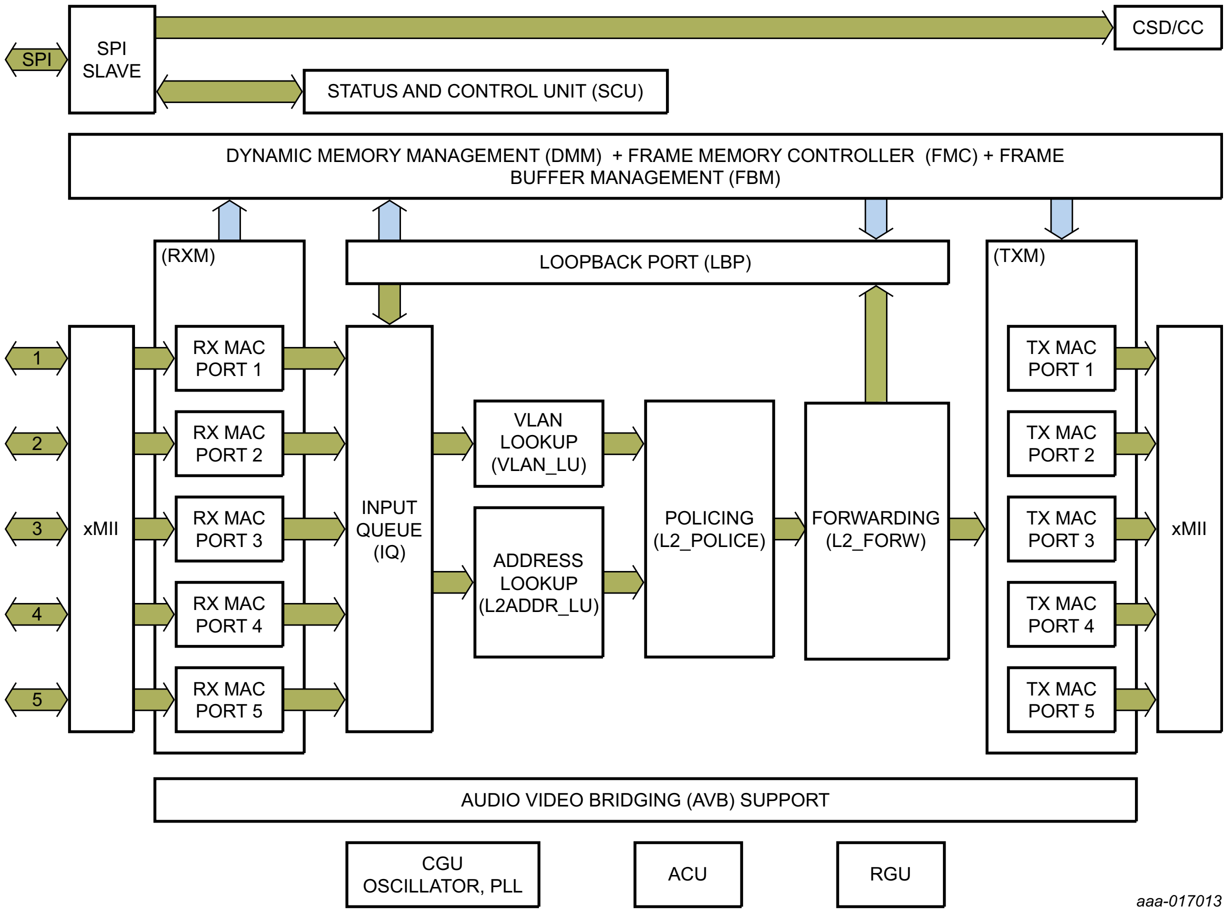


Fig 1. Block diagram of SJA1105EL

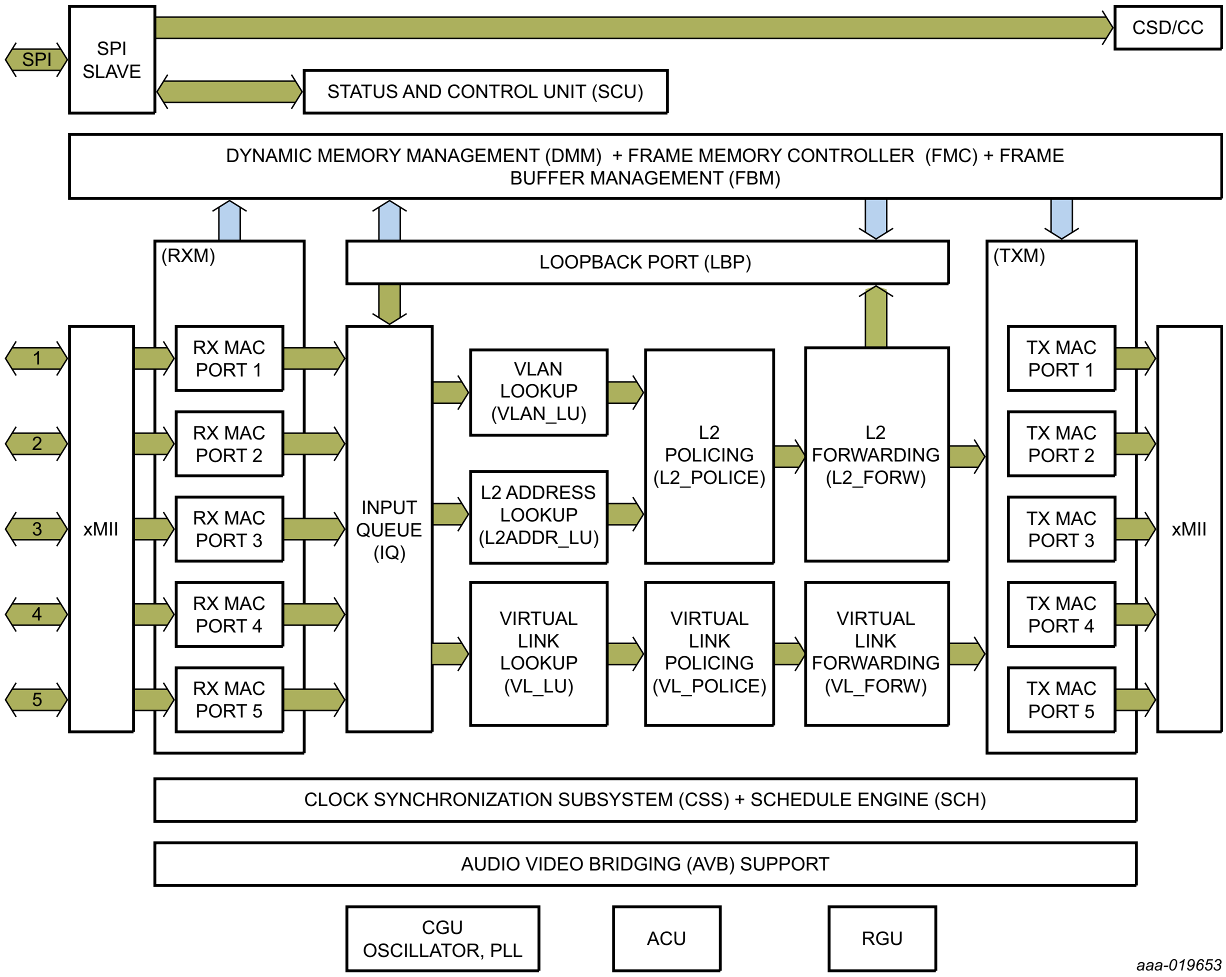


Fig 2. Block diagram of SJA1105TEL

5. Pinning information

5.1 Pinning

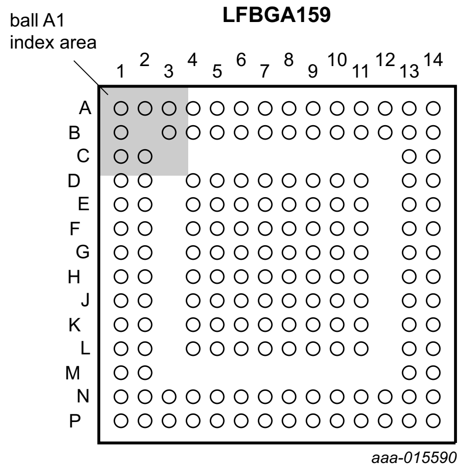


Fig 3. Pin configuration diagram

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	VSS	MII0_TXD0	MII0_TX_ER	MII1_RX_DV	MII1_RXD2	MII1_RXD0	MII1_TX_CLK	MII1_TXD3	MII1_TXD1	MII1_TX_ER	MII2_RX_DV	MII2_RXD2	MII2_RXD0	VSS
B	MII0_TXD1		MII1_RX_ER	MII1_RXD3	MII1_RXD1	MII1_RX_CLK	MII1_TX_EN	MII1_TXD2	MII1_TXD0	MII2_RX_ER	MII2_RXD3	MII2_RXD1	VSS	MII2_RX_CLK
C	MII0_TXD3	MII0_TXD2											MII2_TX_EN	MII2_TX_CLK
D	MII0_TX_CLK	MII0_TXEN		VDDIO_MII0	VDDIO_MII1	VDD_CORE	VDDIO_MII1	VDDIO_MII1	VDD_CORE	VDDIO_MII2	VDDIO_MII2		MII2_TXD2	MII2_TXD3
E	MII0_RXD0	MII0_RX_CLK		VDDIO_MII0	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO_MII2		MII2_TXD0	MII2_TXD1
F	MII0_RXD2	MII0_RXD1		VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE		MII3_RX_ER	MII2_TX_ER
G	MII0_RX_DV	MII0_RXD3		VDDIO_MII0	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO_MII3		MII3_RXD3	MII3_RX_DV
H	CLK_OUT	MII0_RX_ER		VDDIO_CLO	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO_MII3		MII3_RXD1	MII3_RXD2
J	VDDA_PLL	VSSA_PLL		VDD_CORE	VSS	VSS	VSS	VSS	VSS	VSS	VDD_CORE		MII3_RX_CLK	MII3_RXD0
K	VDDA_OSC	OSC_IN		VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDIO_MII3		MII3_TX_EN	MII3_TX_CLK
L	OSC_OUT	VSSA_OSC		i.c.	VDDIO_HOST	VDD_CORE	VSS	VDDIO_MII4	VDD_CORE	VDDIO_MII4	VDDIO_MII4		MII3_TXD2	MII3_TXD3
M	TRST_N	TDI											MII3_TXD0	MII3_TXD1
N	TCK	VSS	TDO	PTP_CLK	SDI	SS_N	MII4_TXD1	MII4_TXD3	MII4_TX_CLK	MII4_RXD0	MII4_RXD2	MII4_RX_DV	VSS	MII3_TX_ER
P	VSS	TMS	RST_N	SDO	SCK	MII4_TX_ER	MII4_TXD0	MII4_TXD2	MII4_TX_EN	MII4_RX_CLK	MII4_RXD1	MII4_RXD3	MII4_RX_ER	VSS

aaa-016468

Fig 4. Pin configuration

5.2 Pin description

Table 2. Pin description - xMII interface[1]

Symbol	Pin					Type[2]	Description
	MII interface:						
	0	1	2	3	4		
VDDIO_ MIIx	D4 E4 G4	D5 D7 D8	D10 D11 E11	G11 H11 K11	L8 L10 L11	P	3.3 V/2.5 V I/O supply voltage
TX_CLK/ REF_CLK/ TXC	D1	A7	C14	K14	N9	I/O I/O O	TX_CLK: MII interface transmit clock (also configurable as output) REF_CLK: RMII interface reference clock (also configurable as input) TXC: RGMII interface transmit clock
TX_EN/ TX_CTL	D2	B7	C13	K13	P9	O	TX_EN: MII/RMII interface transmit enable input TX_CTL: RGMII interface transmit control output
TX_ER	A3	A10	F14	N14	P6	O	MII/RMII interface transmit coding error output
TXD0	A2	B9	E13	M13	P7	O	MII/RMII/RGMII interface transmit data output, bit 0
TXD1	B1	A9	E14	M14	N7	O	MII/RMII/RGMII interface transmit data output, bit 1
TXD2	C2	B8	D13	L13	P8	O	MII/RGMII interface transmit data output, bit 2
TXD3	C1	A8	D14	L14	N8	O	MII/RGMII interface transmit data output, bit 3
RX_CLK/ RXC	E2	B6	B14	J13	P10	I/O I	RX_CLK: MII interface receive clock (also configurable as output) RXC: RGMII interface receive clock
RX_ER	H2	B3	B10	F13	P13	I	MII/RMII interface receive error input
RX_DV/ CRS_DV/ RX_CTL	G1	A4	A11	G14	N12	I	RX_DV: MII interface receive data valid input CRS_DV: RMII interface carrier sense/data valid input RX_CTL: RGMII interface receive control input
RXD0	E1	A6	A13	J14	N10	I	MII/RMII/RGMII interface receive data input, bit 0
RXD1	F2	B5	B12	H13	P11	I	MII/RMII/RGMII interface receive data input, bit 1
RXD2	F1	A5	A12	H14	N11	I	MII/RGMII interface receive data input, bit 2
RXD3	G2	B4	B11	G13	P12	I	MII/RGMII interface receive data input, bit 3

[1] xMII I/O pins will be floating until the configuration has been loaded.

[2] I: digital input; O: digital output; P: power supply.

Table 3. Pin description - core supply and ground

Symbol	Pin	Type[1]	Description
VDD_CORE	D6, D9, F4, F11, J4, J11, L6, L9	P	1.2 V core supply voltage
VSS	A1, A14, B13, E5, E6, E7, E8, E9, E10, F5, F6, F7, F8, F9, F10, G5, G6, G7, G8, G9, G10, H5, H6, H7, H8, H9, H10, J5, J6, J7, J8, J9, J10, K4, K5, K6, K7, K8, K9, K10, L7, N2, N13, P1, P14	G	supply ground

[1] P: power supply; G: ground.

Table 4. Pin description - general

Symbol	Pin	Type[1]	Description
RST_N[2]	P3	I	reset input (active LOW)
PTP_CLK	N4	O	PTP clock
VDDIO_HOST	L5	P	host interface supply voltage
i.c.	L4	G	internally connected; must be connected to ground
Clock generation (CGU)			
VDDA_OSC	K1	P	oscillator supply voltage
VSSA_OSC	L2	G	oscillator supply ground
VDDA_PLL	J1	P	PLL supply voltage
VSSA_PLL	J2	G	PLL supply ground
VDDIO_CLO	H4	P	clock output supply voltage (CLK_OUT)
CLK_OUT	H1	O	clock output
OSC_IN	K2	I	oscillator input
OSC_OUT	L1	O	oscillator output
SPI interface			
SCK	P5	I	SPI clock
SDI	N5	I	SPI data input
SDO	P4	O	SPI data output
SS_N	N6	I	SPI slave select (active LOW)
JTAG interface[3]			
TRST_N	M1	I	test reset (active LOW)
TDI	M2	I	test data in
TCK	N1	I	test clock
TMS	P2	I	test mode state
TDO	N3	O	test data out

[1] I: digital input; O: digital output; P: power supply, G: ground.

[2] Pins RST_N and TRST_N must be held LOW simultaneously to reset the device.

[3] JTAG pins have internal pull-ups.

6. Functional description

The SJA1105 is designed to provide a cost-optimized and flexible solution for automotive Ethernet switches. Each port can be independently configured for MII, RMII or RGMII operation. Switch configuration is performed via an SPI interface. A typical system diagram is shown in Figure 5.

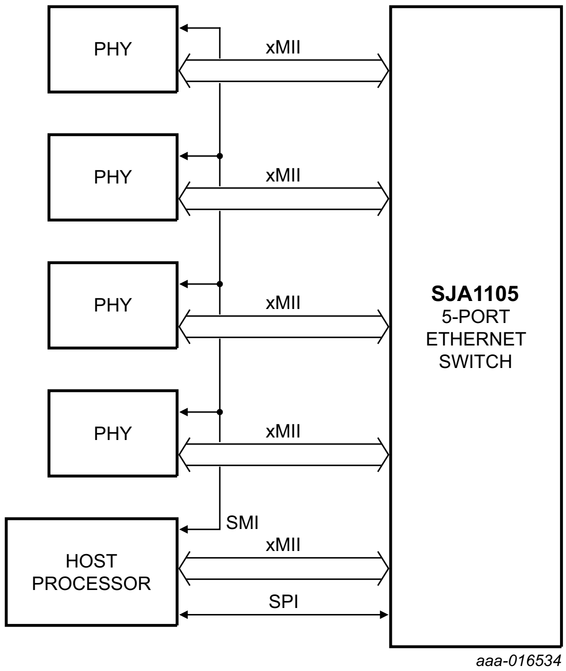


Fig 5. System diagram showing the SJA1105 Ethernet switch connected to PHYs and a host processor

6.1 Functional overview

The SJA1105 contains the following functional modules (see the block diagrams in Figure 1 and Figure 2):

6.1.1 Auxiliary Configuration Unit (ACU)

This module contains the pin configuration and status registers. The host can configure the I/O pads of the chip (pull-up/-down, speed etc.) and monitor the product configuration and temperature sensor status via these registers.

6.1.2 Clock Generation Unit (CGU)

This module contains the oscillator and PLLs used to generate clocks for all internal blocks and a number of interface output clocks.

6.1.3 Reset Generation Unit (RGU)

This block ensures that the device transitions to a pre-defined state after power-up or an externally asserted reset.

6.1.4 Serial Peripheral Interface (SPI)

The host controller manages access to the internal configuration and programming space via the SPI.

6.1.5 Status and Control Unit (SCU)

This block contains the switch core status and configuration registers. The host processor accesses these registers via the SPI.

6.1.6 Configuration Stream Decoder/Configuration Controller (CSD/CC)

This block handles the distribution of the configuration stream from the host processor to the other modules and performs a CRC check on the configuration blocks.

6.1.7 xMII

This block is a wrapper and multiplexer for the MII interface options. The device supports MII, RMII and RGMII.

6.1.8 Dynamic Memory Management (DMM)/Frame Memory Controller (FMC)/ Frame Buffer Management (FBM)

These blocks deal with the storage and handling of frames in the memory buffer. The DMM provides memory handles for ingress frames and holds meta information related to the frames. The DMM releases frame handles for frames that are transmitted or dropped. The FMC converts frame handles into virtual memory addresses and the FBM optimizes the use of on-chip frame memory based on frame size.

6.1.9 Receive MAC (RXM)

The RXM loads the data from the xMII interface block and checks the IFG, the preamble, the SOF delimiter, the CRC and the frame length. It provides timestamps for clock synchronization frames, extracts frame metadata such as MAC addresses and VLAN information and drops runt and oversized frames. The RXM collects memory handles from the DMM and transfers frame data to the FMC block for writing to memory.

6.1.10 Input Queue (IQ)

The IQ arranges the frame processing order so that the switching fabric behaves in a deterministic manner. If two ports each receive the last byte of a complete frame in the same clock cycle, the lower port ID is processed first.

6.1.11 VLAN Lookup (VLAN_LU)

The forwarding limitations and tagging/untagging options are determined in the VLAN_LU block.

6.1.12 Address Lookup (L2ADDR_LU)

The forwarding information for frames based on the destination MAC address in combination with the VLAN ID are determined in this block. The lookup table is addressed using an 8-bit hash value computed from the destination MAC address and the VLAN ID. Up to four entries are supported per hash value. The table holds dynamically learned as well as statically configured entries. Dynamically learned entries can be configured to time-out. The address lookup process can be configured to use shared or independent address learning.

6.1.13 Policing (L2_POLICE)

Ingress policing rules are enforced in the L2_POLICE block. The transmission rate can be limited for any of the eight priority levels and for broadcast traffic at each port. Non-compliant traffic is dropped and is indicated by associated flags and counters.

6.1.14 Forwarding (L2_FORW)

The L2_FORW block forwards frames to the destination ports. It maintains a vector of reachable ports for unicast traffic for each ingress port. In addition, it maintains a vector of destination ports for broadcast traffic and for unknown multicast traffic. This block also maintains a memory partition account for traffic received per port and drops frames if there is insufficient space. This block also handles priority remapping and egress queue priority mapping.

6.1.15 Transmit MAC (TXM)

This block handles frame output via the xMII interface. It supports eight priority queues and implements strict-priority scheduling. The AVB block can interrupt the scheduling from specific priority queues in case shapers are allocated to queues. When a frame is selected for transmission, this block gets the frame data from the FMC using the memory handle of the frame. It passes the free memory handle back to the DMM once the frame has been transmitted. It also inserts VLAN tags into packet headers. It can be configured to perform the IEEE 1588v2 transparent clock update for synchronization frames.

6.1.16 Audio Video Bridging (AVB)

This block implements credit-based traffic shaping and interrupts transmission from priority queues in the TXM when necessary to ensure that shaping occurs. It also captures high-resolution timestamps for IEEE 802.1AS and IEEE 1588v2 operation. The host processor can adjust the IEEE 1588v2 hardware clock via this block.

6.1.17 Loopback Port (LBP)

This block uses an internal port to replicate a frame internally and change the VLAN tag to support ingress and egress retagging of traffic. The replicated frame-handling information is fed back to the IQ which processes the frame in the same way as a frame from a regular traffic port.

6.1.18 Virtual Link Lookup (VL_LU); SJA1105TEL only

The VL_LU block performs a lookup of time-triggered and rate-constrained traffic based on the configured Virtual Link Multicast addresses, the VLAN ID and the VLAN priority identifying time-triggered or rate-constrained traffic.

6.1.19 Virtual Link Policing (VL_POLICE); SJA1105TEL only

The VL_POLICE block executes policing functions based on the time-triggered Ethernet or rate-constrained traffic rule set. Policing mechanisms can be configured individually per flow (i.e. per virtual link). Time-triggered Ethernet policing verifies that a frame received by the switch was sent at the correct point in time by the neighboring node. Non-compliant frames are dropped and are indicated by associated flags and counters.

6.1.20 Virtual Link Forwarding (VL_FORW); SJA1105TEL only

The VL_FORW block forwards time-triggered or rate-constrained traffic to the destination ports. Time-triggered traffic is stored in this module until the running traffic schedule fires a transmit trigger for the respective Virtual Link. Rate-constrained traffic is immediately routed to the destination ports. All time-triggered frames are dropped if synchronization is lost.

6.1.21 Clock Synchronization Subsystem (CSS) and Schedule Engine (SCH); SJA1105TEL only

This block implements the clock synchronization protocol and executes the message schedules.

6.2 Media Independent Interfaces (xMII)

The SJA1105 xMII interfaces can be configured to support a wide variety of PHYs and host controllers. Each port can be configured for MAC-to-PHY or MAC-to-MAC communication. The following configurations are supported:

MII: 25 MHz clock for 100 Mbit/s or 2.5 MHz for 10 Mbit/s operation, 14 interface signals, full duplex only, 3.3 V (Ref. 5)

RMII: 50 MHz clock for 100 Mbit/s and 10 Mbit/s operation, 8 interface signals (reference clock can be an input to both devices or may be driven from MAC to PHY), full duplex only, 3.3 V specification (Ref. 6)

RGMII: 125 MHz clock (both edges) for 1000 Mbit/s, 25 MHz for 100 Mbit/s or 2.5 MHz for 10 Mbit/s operation, 12 interface signals; full duplex only, 2.5 V (Ref. 4)

Depending on how the switch is configured, the following interface signals are available at each of the five ports:

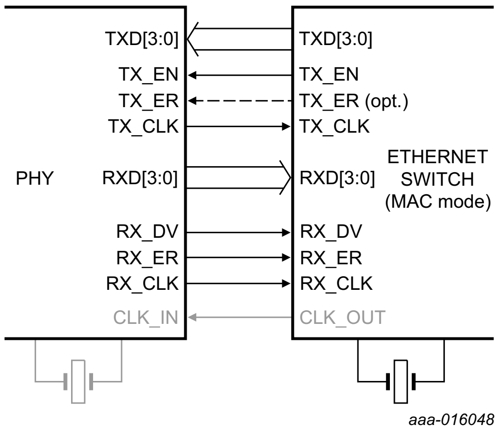
Table 5. MII pin multiplexing

MII (14 interface signals)	RMII (8 interface signals)	RGMII (12 interface signals)
TX_CLK	REF_CLK	TXC
TX_EN	TX_EN	TX_CTL
TX_ER	TX_ER	-
TXD0	TXD0	TXD0
TXD1	TXD1	TXD1
TXD2	-	TXD2
TXD3	-	TXD3
RX_CLK	-	RXC
RX_ER	RX_ER	-
RX_DV	CRS_DV	RX_CTL
RXD0	RXD0	RXD0
RXD1	RXD1	RXD1
RXD2	-	RXD2
RXD3	-	RXD3

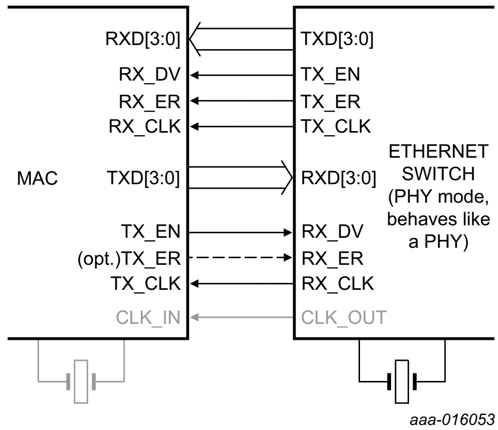
6.2.1 MII signaling and encoding

Figure 6 shows the PHY-MAC and MAC-MAC connections in an MII interface. Data is exchanged via 4-bit wide data nibbles TXD[3:0] and RXD[3:0]. Data transmission is synchronous with the transmit (TX_CLK) and receive (RX_CLK) clocks. For the PHY-MAC interface, both clock signals are provided by the PHY and are typically derived from an external crystal running at a nominal 25 MHz (±100 ppm) or from the CLK_OUT signal on the switch. When the Ethernet Switch is configured for MAC-MAC communication, the switch provides the clocks and acts like a PHY.

A HIGH level on TX_EN initiates data transmission; a HIGH level on RX_DV signals data reception.



a. PHY-MAC interface



b. MAC-MAC interface

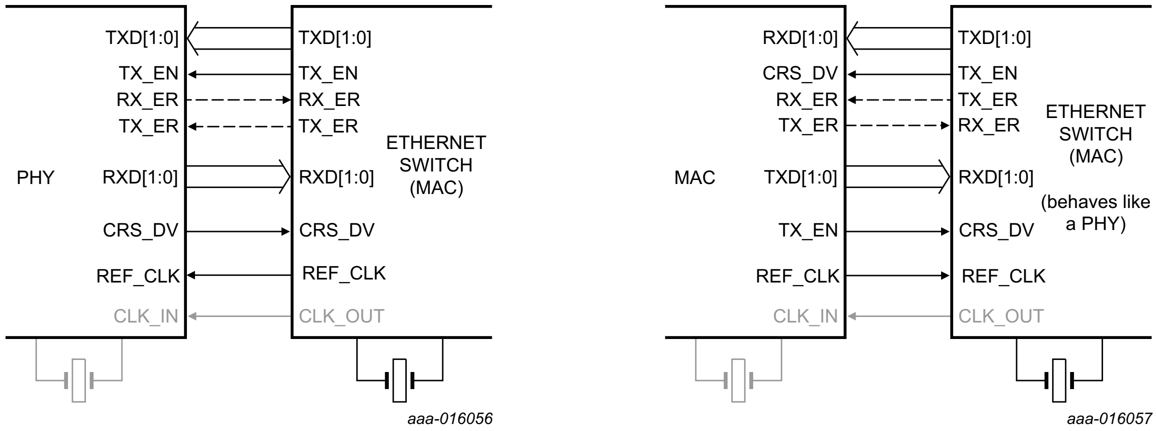
Fig 6. MII interface connections

6.2.2 RMII signaling and encoding

RMII data is exchanged via 2-bit data signals TXD[1:0] and RXD[1:0] as shown in Figure 7. Transmit and receive signals are synchronous with the shared reference clock, REF_CLK.

In the PHY-MAC configuration, the REF_CLK shared reference clock can be generated by the Ethernet switch. In the MAC-MAC configuration, the external MAC can supply the reference clock.

To achieve the same data rate as MII, the interface is clocked at a nominal 50 MHz (±50 ppm) for 100 Mbit/s and 10 Mbit/s operation.



a. PHY-MAC interface

b. MAC-MAC interface

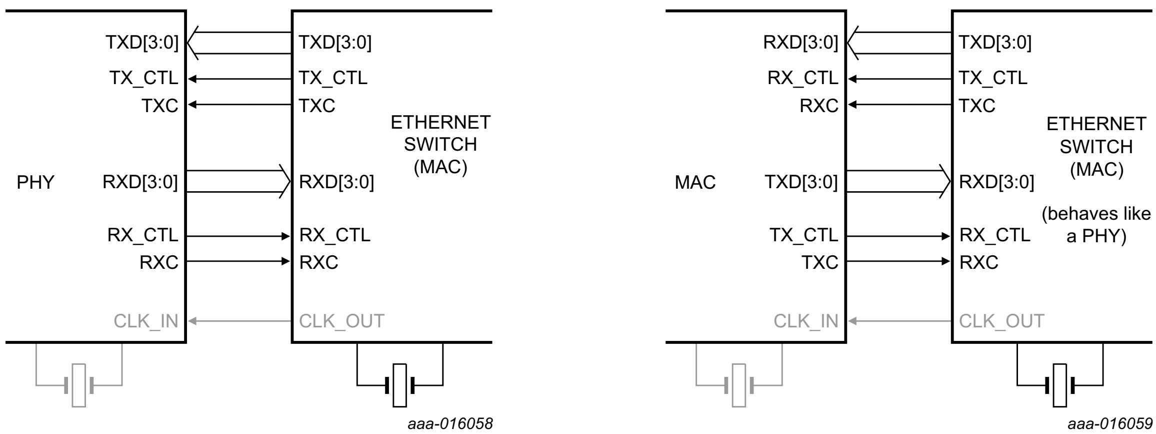
Fig 7. RMII interface connections

6.2.3 RGMII signaling and encoding

The PHY-MAC and MAC-MAC connections in an RGMII-configured interface are shown in Figure 8. The RGMII protocol is intended to be an alternative to the IEEE 802.3z GMII standard (not supported on the SJA1105). The objective is to reduce the number of pins needed to connect the MAC and PHY in a cost-effective and technology-independent way. RGMII has the added advantage over RMII in that it supports Gigabit operation.

In order to achieve a reduced pin count, the number of data signals and associated control signals is reduced. Control signals are multiplexed together and transmitted data is synchronized with both clock edges (double data rate).

RGMII is a symmetrical interface. For 1000 Mbit/s, 100 Mbit/s and 10 Mbit/s operation, the clocks operate at 125 MHz, 25 MHz and 2.5 MHz (±50 ppm) respectively. The TXC signal is always generated by the MAC. The PHY generates the RXC. Note that RGMII requires an external delay of between 1.5 ns and 2 ns on TXC and RXC.



a. PHY-MAC interface

b. MAC-MAC interface

Fig 8. RGMII interface connections

6.3 SPI interface

The SJA1105 provides an SPI bus slave as the host control interface. The host can control/configure the SJA1105 by accessing the configuration address space and the programming address space.

This interface acts as a slave in a synchronous serial data link that conforms with the SPI standard as defined in the SPI Block Guide from Motorola (Ref. 7). The interface operates in SPI Transfer mode 1 (CPOL = 0, CPHA = 1).

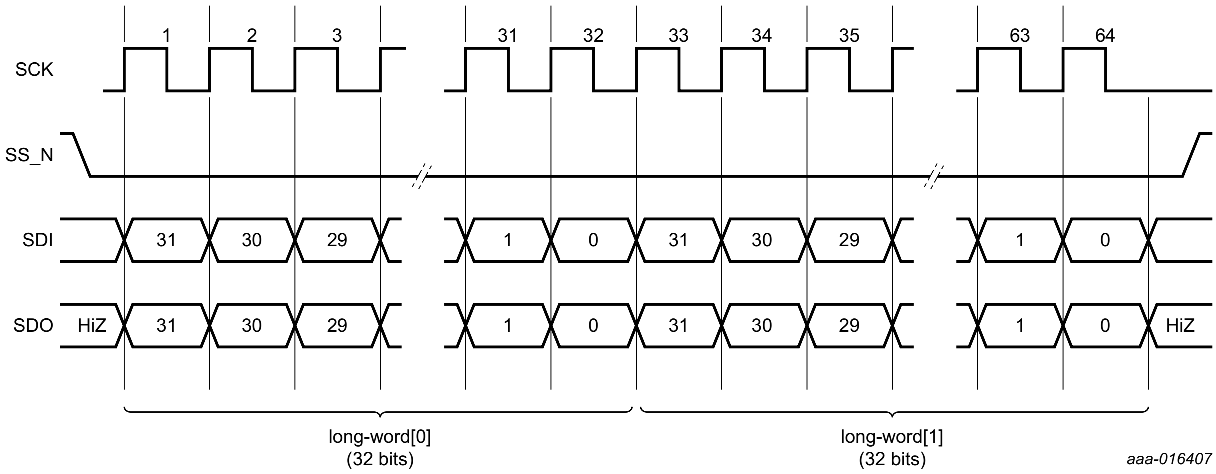


Fig 9. SPI transfer timing (example)

An example SPI timing diagram is shown in Figure 9. Data is captured on the falling edge of the clock and transmitted on the rising edge. Both master and slave must operate in the same mode.

When CGU registers are read, a 64 ns delay must be inserted between the control and data phases to allow the device to retrieve the data. Alternatively, the access can be performed at a frequency below 17.8 MHz. In addition, a read-after-write time of >130 ns between an SPI write and read transaction to the same register must be guaranteed. See the SJA1105 software user manuals (Ref. 8) for further details on the data format.

The number of SPI clock cycles must be between 64 and 2080 and be a multiple of 32. In order to ensure support for a wide a range of microcontrollers, the SPI interface can operate at a supply voltage of 3.3 V, 2.5 V or 1.8 V (determined by the voltage connected to VDDIO_HOST; see Section 11).

7. Limiting values

Table 6. Limiting values
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
$V_{DDA(osc)}$	oscillator analog supply voltage	on pin VDDA_OSC		–0.5	+1.6	V
$V_{DDA(PLL)}$	PLL analog supply voltage	on pin VDDA_PLL		–0.5	+1.6	V
V_{DDC}	core supply voltage	on pins VDD_CORE		–0.5	+1.6	V
$V_{DD(host)}$	host supply voltage	on pin VDDIO_HOST		–0.5	+5	V
$V_{DD(clk)}$	clock supply voltage	on pin VDDIO_CLO		–0.5	+5	V
$V_{DD(MII)}$	MII supply voltage	on pins VDDIO_MIIx		–0.5	+5	V
V_{ESD}	electrostatic discharge voltage	Human Body Model (HBM); 100 pF, 1.5 kΩ	[1]	–2000	+2000	V
		Charged Device Model (CDM)	[2]			
		corner balls		–750	+750	V
		other balls		–500	+500	V
T_j	junction temperature			–40	+125	°C
T_{stg}	storage temperature			–55	+150	°C

[1] According to AEC-Q100-002.

[2] According to AEC-Q100-011.

8. Thermal characteristics

Table 7. Thermal characteristics

Symbol	Parameter	Conditions	Typ	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	4-layer board (JESD51-9)	29	K/W
$R_{th(j-lead)}$	thermal resistance from junction to lead	4-layer board (JESD51-9)	15	K/W
Ψ_{j-top}	thermal characterization parameter from junction to top of package	4-layer board (JESD51-9)	0.33	K/W

9. Static characteristics

Table 8. Static characteristics

T_j = –40 °C to +125 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Supply voltages; see Figure 15						
Clock and host interface supply (pins VDDIO_CLO and VDDIO_HOST)						
$V_{DD(clk)}$	clock supply voltage	3.3 V signaling	3.00	3.30	3.60	V
		2.5 V signaling	2.30	2.50	2.70	V
		1.8 V signaling	1.65	1.80	1.95	V
$V_{DD(host)}$	host supply voltage	3.3 V signaling	3.00	3.30	3.60	V
		2.5 V signaling	2.30	2.50	2.70	V
		1.8 V signaling	1.65	1.80	1.95	V
MII interface supply (pins VDDIO_MII0 to VDDIO_MII4)						
$V_{DD(MII)}$	MII supply voltage	MII/RMII	3.00	3.30	3.60	V
		RGMII	2.30	2.50	2.70	V
Core, oscillator and PLL supply (pins VDD_CORE, VDDA_OSC and VDDA_PLL)						
V_{DDC}	core supply voltage	see Figure 15	1.14	1.20	1.30	V
$V_{DDA(osc)}$	oscillator analog supply voltage		1.10	1.20	1.30	V
$V_{DDA(PLL)}$	PLL analog supply voltage		1.10	1.20	1.30	V
Supply currents						
Clock and host interface supply (pins VDDIO_CLO and VDDIO_HOST)						
$I_{DD(host)}$	host supply current	$V_{DD(HOST)}$ = 3.30 V	-	-	2.8	mA
$I_{DD(clk)}$	clock supply current	$V_{VDD(CLK)}$ = 3.30 V	-	-	3.5	mA
MII interface supply (pins VDDIO_MII0 to VDDIO_MII4)						
$I_{DD(MII)}$	MII supply current	port set to RGMII, 1 Gbit/s				
		C_L = 18 pF	-	-	65.5	mA
		25 % load PRBS	-	14.3	-	mA
		100 % load PRBS	-	31.8	-	mA
		port set to RMII, 100 Mbit/s				
		C_L = 25 pF	-	-	15.5	mA
		25 % load PRBS	-	6.8	-	mA
		100 % load PRBS	-	8.5	-	mA
		port set to MII, 100 Mbit/s				
		C_L = 25 pF	-	-	11.5	mA
		25 % load PRBS	-	0.7	-	mA
		100 % load PRBS	-	2.4	-	mA

Table 8. Static characteristics *…continued*

T_j = –40 °C to +125 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Core, oscillator and PLL supply (pins VDD_CORE, VDDA_OSC and VDDA_PLL)						
I_{DDC}	core supply current	worst case	-	-	110	mA
		all ports set to RGMII, 1 Gbit/s				
		25 % PRBS	-	37.7	-	mA
		100 % PRBS	-	54.3	-	mA
		all ports set to MII/RMII, 100 Mbit/s				
		25 % PRBS	-	31.0	-	mA
		100 % PRBS	-	33.2	-	mA
$I_{DDA(PLL)}$	PLL analog supply current	PLL0 enabled; see Ref. 8	-	-	1.2	mA
		PLL0 and PLL1 enabled; see Ref. 8	-	-	2.4	mA
$I_{DDA(osc)}$	oscillator analog supply current		-	350	-	µA
$I_{startup(osc)}$	oscillator start-up current		0.2	1.0	2.5	mA
Power-On Reset (POR)						
$V_{trip(POR)}$	power-on reset trip voltage	HIGH level	0.65	0.76	1.01	V
		LOW level	0.60	0.72	0.91	V
pin RST_N[1]						
$V_{hys(i)}$	input hysteresis voltage		0.1 × $V_{VDD(HOST)}$	-	-	V
V_{IH}	HIGH-level input voltage	3.3 V signaling	2.0	-	$V_{VDD(HOST)}$ + 0.5	V
		2.5 V signaling	1.7	-	$V_{VDD(HOST)}$ + 0.5	V
		1.8 V signaling	0.65 × $V_{VDD(HOST)}$	-	$V_{VDD(HOST)}$ + 0.5	V
V_{IL}	LOW-level input voltage	3.3 V signaling	–0.5	-	+0.8	V
		2.5 V signaling	–0.5	-	+0.7	V
		1.8 V signaling	–0.5	-	+0.35 × $V_{VDD(HOST)}$	V
$R_{pu(weak)}$	weak pull-up resistance		40	50	57	kΩ
C_i	input capacitance		-	-	8.0	pF
Oscillator (pins OSC_IN and OSC_OUT)						
Crystal oscillator mode						
C_i	input capacitance	on pin OSC_IN	-	-	3.5	pF
C_{shunt}	shunt capacitance		-	-	7.0	pF
$C_{L(ext)}$	external load capacitance	on pin OSC_IN [2]	-	8	-	pF
		on pin OSC_OUT [2]	-	8	-	pF
Clock mode						
C_{dec}	decoupling capacitance		-	100	-	pF
$V_{i(OSC\_IN)}$	input voltage on pin OSC_IN	RMS value	0.20	-	$V_{DDA(OSC)}$	V

Table 8. Static characteristics *…continued*

T_j = −40 °C to +125 °C; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I/O pins (VDDIO_MII0 to VDDIO_MII4, SPI, JTAG, CLK_OUT, PTP_CLK)						
V_{IH}	HIGH-level input voltage	3.3 V signaling (supported for MII/RMII operation)	2.0	-	V_{DDx} + 0.5[3]	V
		2.5 V signaling (supported for RGMII operation)	1.7	-	V_{DDx}[3] + 0.5	V
		1.8 V signaling (not supported for MII, RMII or RGMII)	0.65 × V_{DDx}[3]	-	V_{DDx}[3] + 0.5	V
V_{IL}	LOW-level input voltage	3.3 V signaling	−0.5	-	+0.8	V
		2.5 V signaling	−0.5	-	+0.7	V
		1.8 V signaling	−0.5	-	+0.35 × V_{DDx}[3]	V
$V_{hys(i)}$	input hysteresis voltage		0.1 × V_{DDx}[3]	-	-	V
$R_{pu(weak)}$	weak pull-up resistance	V_{IO} = 0 V	40.0	50.0	57.0	kΩ
$R_{pd(weak)}$	weak pull-down resistance	V_{IO} = V_{DDx}	40.0	50.0	57.0	kΩ
I_{OSH}	HIGH-level short-circuit output current		-	-	−111.7	mA
I_{OSL}	LOW-level short-circuit output current		-	-	110.2	mA
C_i	input capacitance		-	-	5.0	pF
Z_o	output impedance		40.0	-	67.5	Ω

[1] Pins RST_N and TRST_N must be held LOW simultaneously to reset the device.

[2] Value is crystal dependent.

[3] Supply voltage on I/O pin x.

10. Dynamic characteristics

Table 9. Dynamic characteristics

T_j = −40 °C to +125 °C; capacitive load of 4 pF; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I/O pins (VDDIO_MII0 to VDDIO_MII4, SPI, JTAG, CLK_OUT, PTP_CLK)						
$t_{r(o)}$	output rise time	3.3 V signaling				
		high-speed mode	0.3	-	0.8	ns
		fast-speed mode	0.5	-	1.3	ns
		medium-speed mode	0.8	-	2.0	ns
		low-speed mode	1.4	-	2.7	ns
		2.5 V signaling				
		high-speed mode	0.4	-	1.1	ns
		fast-speed mode	0.6	-	1.7	ns
		medium-speed mode	1.1	-	2.4	ns
		low-speed mode	1.8	-	3.1	ns
		1.8 V signaling				
		high-speed mode	0.5	-	1.9	ns
		fast-speed mode	0.9	-	2.5	ns
		medium-speed mode	1.5	-	3.2	ns
		low-speed mode	2.3	-	4.1	ns
$t_{f(o)}$	output fall time	3.3 V signaling				
		high-speed mode	0.6	-	0.8	ns
		fast-speed mode	0.6	-	1.0	ns
		medium-speed mode	0.6	-	1.8	ns
		low-speed mode	1.2	-	2.7	ns
		2.5 V signaling				
		high-speed mode	0.5	-	0.9	ns
		fast-speed mode	0.5	-	1.4	ns
		medium-speed mode	1.0	-	2.3	ns
		low-speed mode	1.6	-	3.0	ns
		1.8 V signaling				
		high-speed mode	0.5	-	1.6	ns
		fast-speed mode	0.7	-	2.3	ns
		medium-speed mode	1.4	-	3.0	ns
		low-speed mode	2.0	-	3.9	ns
Oscillator (pins OSC_IN and OSC_OUT)						
Crystal oscillator mode[1]						
f_{xtal}	crystal frequency		-	25	-	MHz
$t_{startup}$	start-up time	25 MHz crystal; $C_{OSC\_IN} = C_{OSC\_OUT}$ = 8 pF	-	275	800	µs
δ	duty cycle		45	50	55	%

Table 9. Dynamic characteristics *...continued*

T_j = –40 °C to +125 °C; capacitive load of 4 pF; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$N_{cy(clk)startup}$	number of start-up clock cycles	until clock is stable; 25 MHz crystal; $C_{OSC\_IN} = C_{OSC\_OUT}$ = 8 pF	-	1000	-	-
Clock mode						
$f_{clk(i)}$	input clock frequency		-	25	-	MHz
$N_{cy(clk)startup}$	number of start-up clock cycles	until clock is stable	-	10	-	-
pin RST_N						
t_w	pulse width		5.0	-	-	μs
pin CLK_OUT						
f_{clk}	clock frequency		-	25	-	MHz
δ	duty cycle		40	50	60	%
pin PTP_CLK						
f_{clk}	clock frequency		-	100	-	kHz
δ	duty cycle		-	50	-	%
SPI: pins SS_N, SCK, SDI and SDO						
f_{clk}	clock frequency	[2]	0.1	-	25	MHz
δ	duty cycle		45	50	55	%
$t_{su(D)}$	data input set-up time	w.r.t. SCK sampling edge	12.4	-	-	ns
$t_{h(D)}$	data input hold time	w.r.t. SCK sampling edge	18	-	-	ns
$t_{d(clk-data)}$	clock to data delay time	w.r.t. SCK launching edge; high-speed mode; 25 pF load	0	-	14	ns
$t_{d(W-R)}$	write to read delay time		130	-	-	ns
$t_{d(addr-data)}$	address to data delay time		64	-	-	ns
JTAG: pins TRST_N, TDI, TCK, TMS and TDO						
f_{clk}	clock frequency		0.1	-	16	MHz
δ	duty cycle		40	50	60	%
t_w	pulse width	on pin TRST_N	100.0	-	-	ns
$t_{su(D)}$	data input set-up time	w.r.t. TCK sampling edge	4.0	-	-	ns
$t_{h(D)}$	data input hold time	w.r.t. TCK sampling edge	25	-	-	ns
$t_{d(clk-data)}$	clock to data delay time	w.r.t. TCK launching edge; high-speed mode; 25 pF load	-	-	20.0	ns
xMII ports						
port configured by host for MII MAC mode; pad speed selection: medium noise, fast speed						
f_{clk}	clock frequency	transmit (TX_CLK) and receive (RX_CLK) clocks; 100 Mbit/s operating speed	-	25	-	MHz
δ	duty cycle	of transmit and receive clocks	35	50	65	%
$t_{su(D)}$	data input set-up time	on pins RXDx, RX_DV and RX_ER w.r.t. rising edge on RX_CLK	10	-	-	ns
$t_{h(D)}$	data input hold time	on pins RXDx, RX_DV and RX_ER w.r.t. rising edge on RX_CLK	10	-	-	ns

Table 9. Dynamic characteristics *...continued*

T_j = −40 °C to +125 °C; capacitive load of 4 pF; all voltages are defined with respect to ground unless otherwise specified; positive currents flow into the IC.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$t_{d(clk-data)}$	clock to data delay time	on pins TXDx, TX_EN and TX_ER w.r.t. rising edge on TX_CLK	0	-	25	ns
port configured by host for MII PHY mode; pad speed selection: medium noise, fast speed						
$t_{su(D)}$	data input set-up time	on pins RXDx, RX_DV and RX_ER w.r.t. rising edge on RX_CLK	10	-	-	ns
$t_{h(D)}$	data input hold time	on pins RXDx, RX_DV and RX_ER w.r.t. rising edge on RX_CLK	0	-	-	ns
$t_{d(clk-data)}$	clock to data delay time	on pins TXDx, TX_EN and TX_ER w.r.t. rising edge on TX_CLK	12	-	25	ns
port configured by host for RMII mode; pad speed selection: medium noise, fast speed						
f_{clk}	clock frequency	reference clock (REF_CLK); 100 Mbit/s operating speed	-	50	-	MHz
δ	duty cycle	of reference clock	35	50	65	%
$t_{su(D)}$	data input set-up time	on pins RXDx, CRS_DV and RX_ER w.r.t. rising edge on REF_CLK	4	-	-	ns
$t_{h(D)}$	data input hold time	on pins RXDx, CRS_DV and RX_ER w.r.t. rising edge on REF_CLK	0	-	-	ns
$t_{d(clk-data)}$	clock to data delay time	on pins RXDx, CRS_DV and RX_ER w.r.t. rising edge on REF_CLK; fast speed I/O setting	2	-	10	ns
port configured by host for RGMII mode; pad speed selection: high noise, high speed						
f_{clk}	clock frequency	transmit (TXC) and receive (RXC) clocks				
		1 Gbit/s operating speed	-	125	-	MHz
		100 Mbit/s operating speed	-	25	-	MHz
		10 Mbit/s operating speed	-	2.5	-	MHz
δ	duty cycle	of transmit and receive clocks				
		1 Gbit/s operating speed	45	50	55	%
		100/10 Mbit/s operating speed	40	50	60	%
$t_{sk(o)}$	output skew time	at the transmitter w.r.t. edge on TXC	−0.5	-	+0.5	ns
$t_{sk(I)}$	input skew time	at the receiver w.r.t. edge on RXC [3]	1.0	-	2.6	ns

[1] A 100 ppm crystal is needed for MII and a 50 ppm crystal for RMII/RGMII.

[2] CGU configuration register read-access timing is stricter at 25 MHz (max); see Section 6.3.

[3] Implies that PCB board design requires the clock to be routed such that an additional trace delay of more than 1.5 ns and less than 2.0 ns is added to the associated clock signal or an external delay line is used.

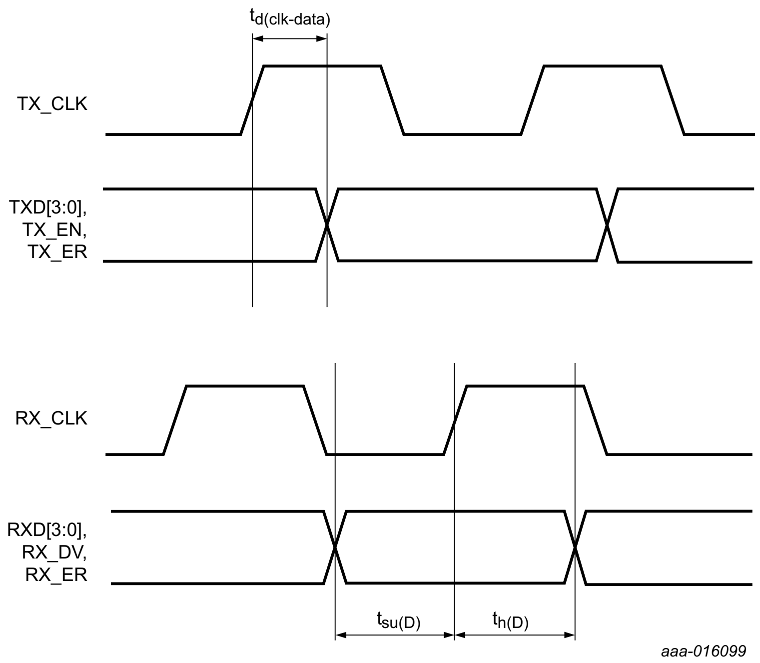


Fig 10. MII timing diagram

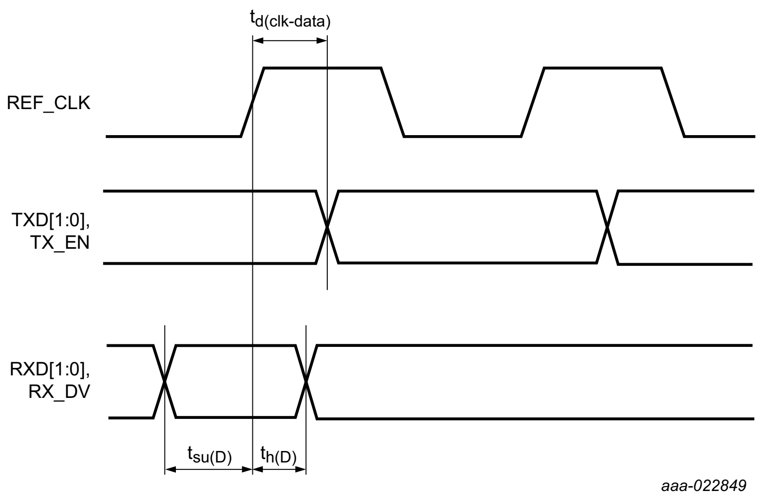


Fig 11. RMII timing diagram

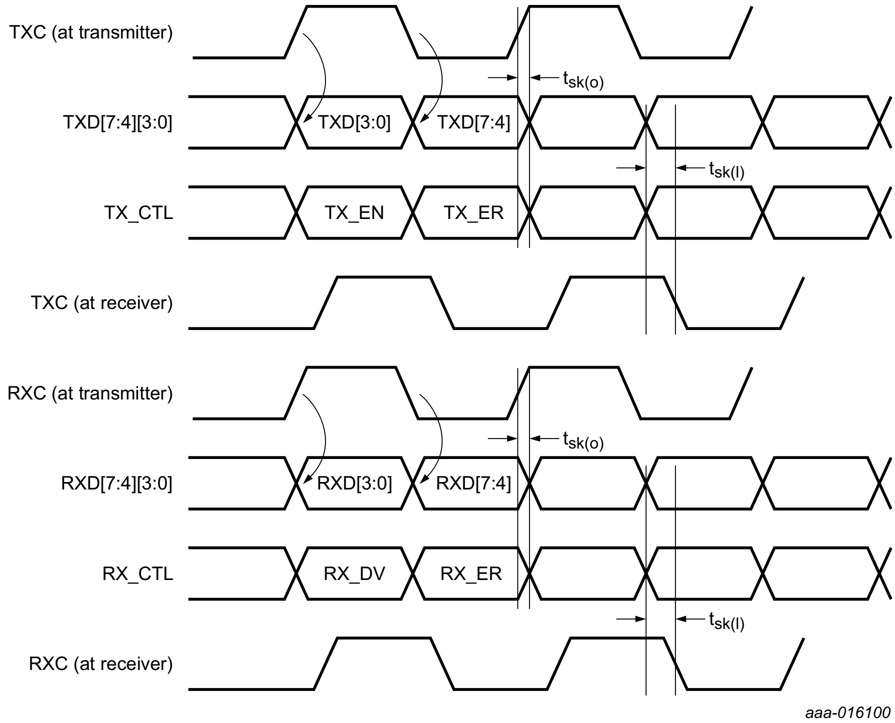
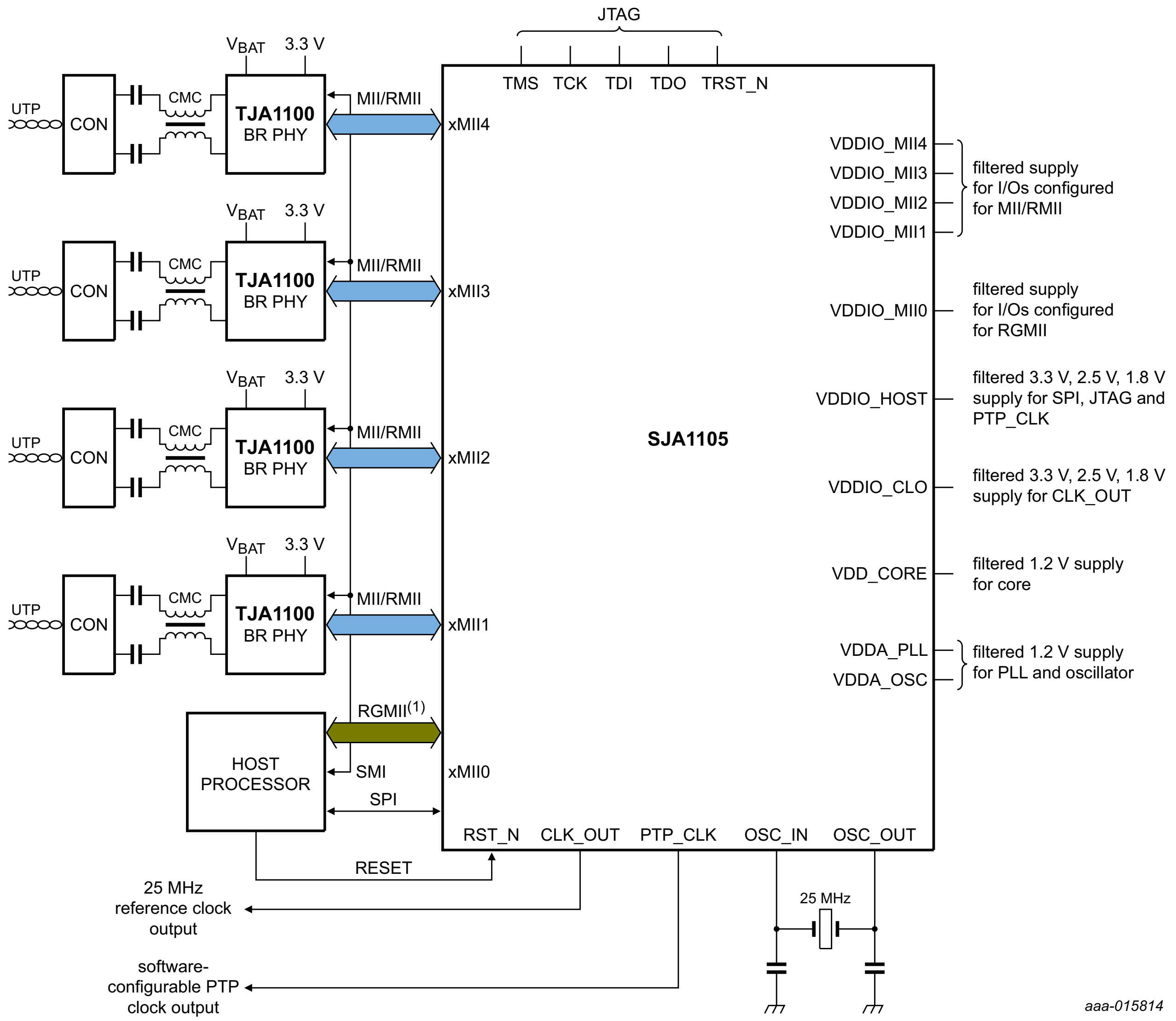


Fig 12. RGMII timing diagram

11. Application information

The SJA1105 features a programmable traffic interface. Each of the five ports can be individually configured for 10 Mbit/s or 100 Mbit/s MII/RMII/RGMII, or for 1 Gbit/s RGMII operation. A typical use case is illustrated in Figure 13.



(1) RGMII requires an external delay of between 1.5 ns and 2 ns on TXC and RXC.

Fig 13. Typical SJA1105 application circuit

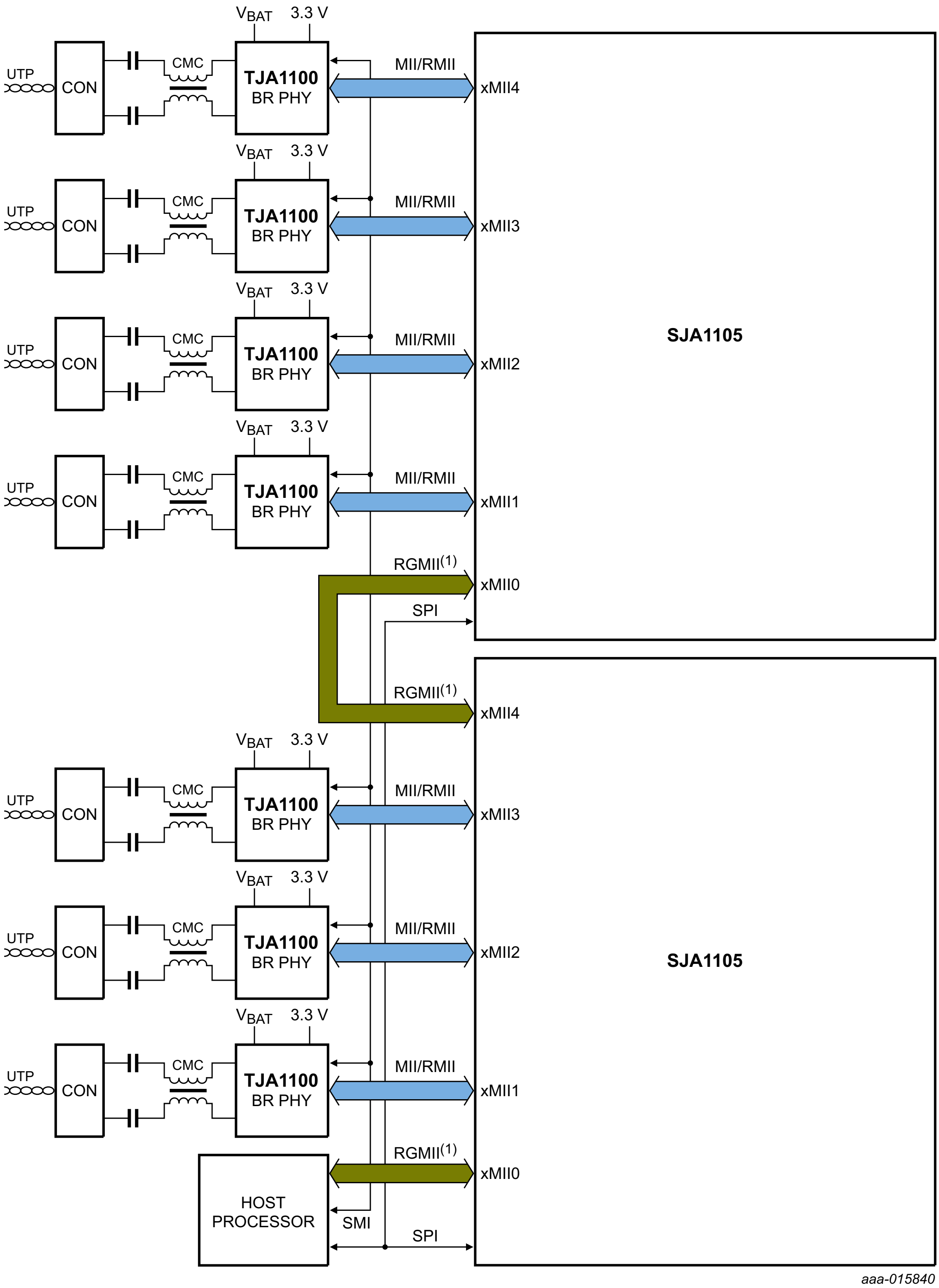
In this configuration, four TJA1100 BroadR-Reach PHYs are connected to the SJA1105 for MII/RMII operation while a host processor has RGMII connectivity with the SJA1105. The I/O supply voltage needed at a port depends on the selected configuration: 3.3 V for MII/RMII operation and 2.5 V for RGMII operation.

Port 1 to Port 4 are configured for MII/RMII operation, so a 3.3 V supply is connected to pins VDDIO_MII1 to VDDIO_MII4. A 2.5 V supply is connected to VDDIO_MII1 since it is configured for RGMII operation.

The SPI, JTAG and PTP_CLK interfaces are supplied via VDDIO_HOST. The 25 MHz clock output, CLK_OUT, is supplied from VDDIO_CLO. Both VDDIO_HOST and VDDIO_CLO accept a 1.8 V, 2.5 V or 3.3 V supply.

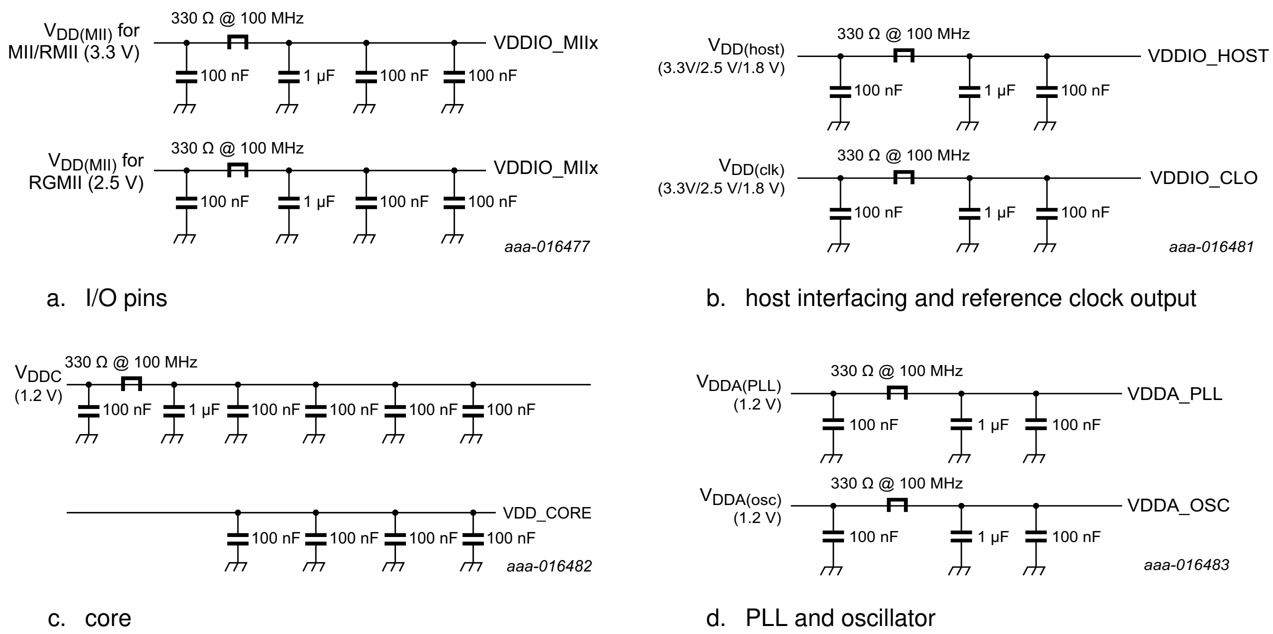
SJA1105 devices can be cascaded, as illustrated in Figure 14. Note that Ethernet connectivity to the host processor is only needed if the system has to support AVB operation or other bridge management protocols such as STP/RSTP. If such operations are not needed, all the ports can be used for data traffic.

In Crystal oscillator mode, the SJA1105 oscillator is used as a crystal oscillator with an external 25 MHz crystal and, typically, a 2 × 8 pF load. In Clock mode, the SJA1105 oscillator is used as a clock input with an external clock connected to input terminal OSC_IN with OSC_OUT left open.



(1) RGMII requires an external delay of between 1.5 ns and 2 ns on TXC and RXC.

Fig 14. Cascading SJA1105 devices



a. I/O pins

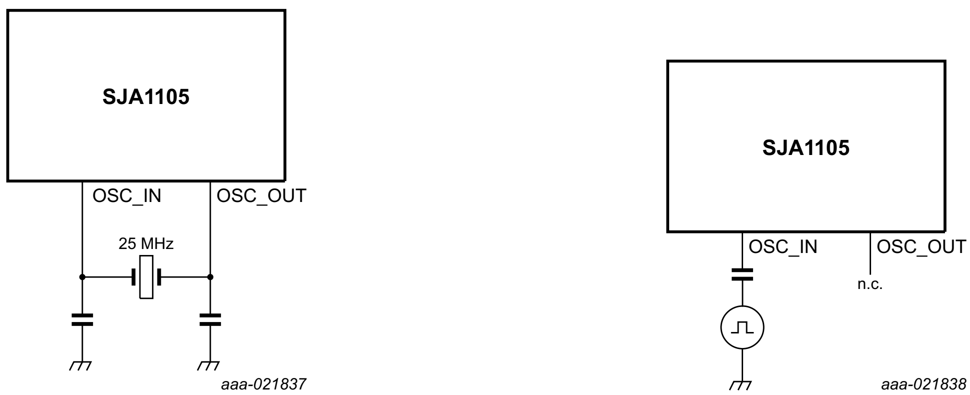
b. host interfacing and reference clock output

c. core

d. PLL and oscillator

PCB layout guidelines showing capacitor placement can be found in AH1604 '*SJA1105 Hardware Design Application Hints*'

Fig 15. Power supply filtering



a. Crystal oscillator mode

b. Clock mode

Fig 16. Device clocking

11.1 Application hints

Further information on the application of the SJA1105 can be found in NXP application hints AH1402 '*Application Hints - 5-port Ethernet Switch*', AH1601 '*Device Configuration Application Hints*', and AH1604 '*SJA1105 Hardware Design Application Hints*'.

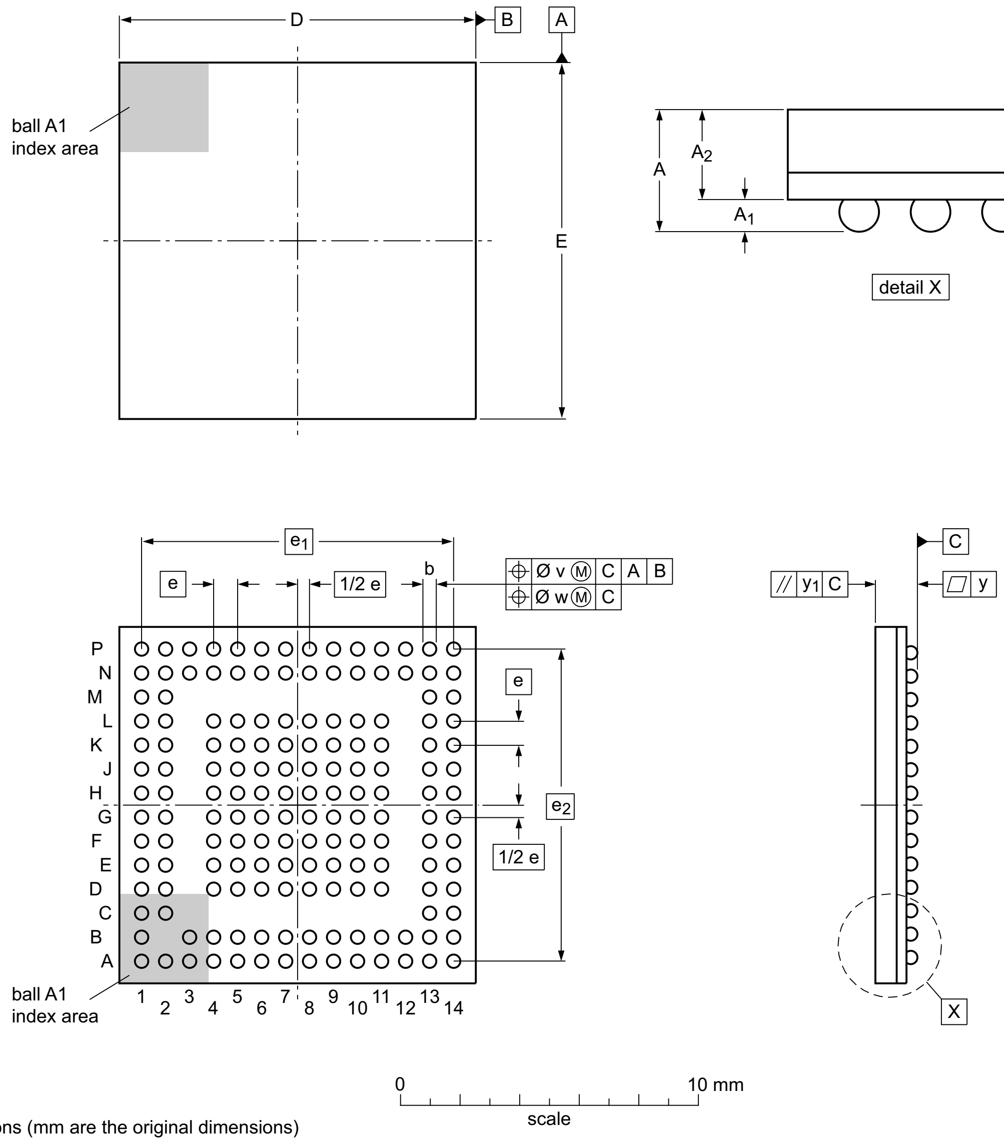
12. Test information

12.1 Quality information

This product has been qualified in accordance with the Automotive Electronics Council (AEC) standard *Q100 Rev-H - Failure mechanism based stress test qualification for integrated circuits*, and is suitable for use in automotive applications.

13. Package outline

LFBGA159: plastic low profile fine-pitch ball grid array package; 159 balls **SOT1427-1**



Dimensions (mm are the original dimensions)

Unit		A	A_1	A_2	b	D	E	e	e_1	e_2	v	w	y	y_1
mm	max	1.50	0.40	1.10	0.50	12.1	12.1							
	nom	1.35	0.35	1.00	0.45	12.0	12.0	0.80	10.4	10.4	0.15	0.08	0.12	0.10
	min	1.25	0.30	0.95	0.40	11.9	11.9							

sot1427-1_po

Outline version	References				European projection	Issue date
	IEC	JEDEC	JEITA			
SOT1427-1		MO-205				~~14-07-18~~ 14-07-26

Fig 17. Package outline SOT1427-1 (LFBGA159)

14. Handling information

All input and output pins are protected against ElectroStatic Discharge (ESD) under normal handling. When handling ensure that the appropriate precautions are taken as described in *JESD625-A* or equivalent standards.

15. Abbreviations

Table 10. Abbreviations

Abbreviation	Description
AVB	Audio Video Bridging
CMC	Common Mode Choke
CRC	Cyclic Redundancy Check
ECU	Electronic Control Unit
Gbit	Gigabit
IFG	InterFrame Gap
JTAG	Joint Test Action Group
LAN	Local Area Network
MAC	Medium Access Controller
Mbit	Megabit
MII	Media Independent Interface
NMOS	N-channel Metal-Oxide Silicon
OTP	One-Time Programmable
PHY	Physical Layer (of the interface)
PLL	Phase-Locked Loop
PMOS	P-channel Metal-Oxide Silicon
PRBS	Pseudo Random Binary Sequence
PTP	Precision Time Protocol
QoS	Quality of Service
RGMII	Reduced Gigabit Media Independent Interface
RMII	Reduced Media Independent Interface
RSTP	Rapid Spanning Tree Protocol
SMI	Serial Management Interface
SOF	Start Of Frame
SPI	Serial Peripheral Interface
SR	Stream Reservation (class)
STP	Spanning Tree Protocol
TAP	Test Access Port
TSN	Time-Sensitive Networking
TTEthernet	Time-Triggered Ethernet
UTP	Unshielded Twisted Pair
VL	Virtual Link
VLAN	Virtual LAN

16. References

[1] OPEN Alliance BroadR-Reach Physical Layer Transceiver Specification for Automotive Applications, V3.2, 24 June 2014

[2] TJA1100 OPEN Alliance BroadR-Reach PHY for Automotive Ethernet data sheet available from NXP Semiconductors

[3] IEEE 802.1BA - Audio Video Bridging (AVB) Systems

[4] Reduced Gigabit Media Independent Interface (RGMII), V1.3, 12 October 2000, V1.3, Broadcom Corporation, Hewlett Packard, Marvell

[5] IEEE Std. 802.3

[6] Reduced Media Independent Interface (RMII), March 20, 1998, RMII Consortium Copyright AMD Inc., Broadcom Corp., National Semiconductor Corp., and Texas Instruments Inc., 1997

[7] SPI Block Guide, V03.06, 04 February 2003, Motorola Inc.

[8] UM10851 SJA1105EL and UM10944 SJA1105TEL software user manuals available from NXP Semiconductors

17. Revision history

Table 11. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
SJA1105 v.1.1	20161107	Product data sheet	-	-

18. Legal information

18.1 Data sheet status

Document status[1][2]	Product status[3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

[1] Please consult the most recently issued document before initiating or completing a design.

[2] The term 'short data sheet' is explained in section "Definitions".

[3] The product status of device(s) described in this document may have changed since this document was published and may differ in case of multiple devices. The latest product status information is available on the Internet at URL http://www.nxp.com.

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