DS80PCI810EVM Evaluation Board

User's Guide

Literature Number: SNLU171
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Contents

List of Figures

List of Tables

Overview

The DS80PCI810EVM – SMA evaluation kit provides a complete high bandwidth platform to evaluate the PCIe signal conditioning features of the Texas Instruments DS80PCI810 repeater/redriver. The DS80PCI810EVM can be used for standard compliance testing, performance evaluation, and initial system prototyping. The SMA edge launch connectors used for the DS80PCI810EVM will interface to multiple system connector types via commercially available breakout cables, adaptors, and boards (not included). This flexible connectivity enables integrated system level testing between TI repeaters and 3rd party ASIC/FPGA host boards. For a functional description of the DS80PCI810, refer to the DS80PCI810 datasheet.

1.1 Features

- 8-Channel unidirectional repeater operating at rates up to 8 Gbps
- Linear equalization to support link training protocols
- EQ up to ~10 dB at 4 GHz
- Variable voltage range up to 1200 mVpp
- Linear output driver
- Programmable by pin selection (pin mode), EEPROM, or SMBus interface
- Single supply operation: V_{IN} = 3.3 V ± 10% or V_{DD} = 2.5 V ± 5%
- –40°C to +85°C operation
- 4 kV HBM ESD rating / 1 kV CDM ESD rating
- High speed signal flow–thru pin-out package: 54-pin QFN (10 mm x 5.5 mm, 0.5 mm pitch)

1.2 Applications

- FR-4 Backplane traces and high speed cable in serial Interfaces up to 8 Gbps
- PCIe Gen 1/2/3

1.3 Ordering Information

Table 1-1. Ordering Information

EVM ID	DEVICE ID	DEVICE PACKAGE
DS80PCI810EVM	DS80PCI810NJY	WQFN-54

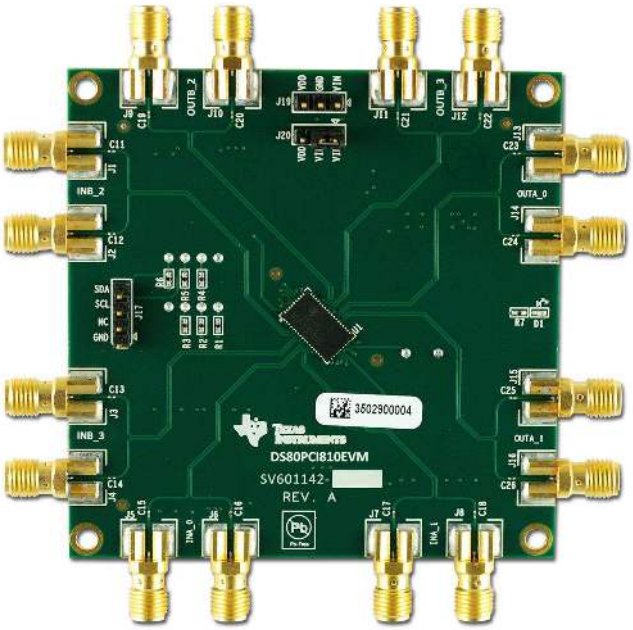


Figure 1-1. DS80PCI810EVM Front

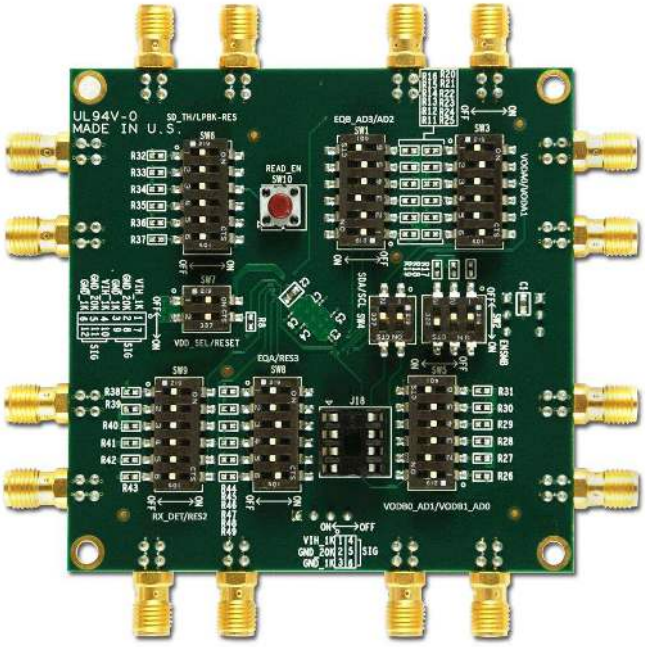


Figure 1-2. DS80PCI810EVM Back

4-Level IO Control

The channel settings and controls are configurable in pin mode for the DS80PCI810 via four logic levels (0, R, F, 1). The four logic levels correspond to the following voltages in Table 2-1.

Table 2-1. Description of 4-Level Voltage Inputs

Level	Setting	Internal Pin Voltage (3.3 V Mode)	Internal Pin Voltage (2.5 V Mode)
0	Tie 1kΩ to GND	0.10 V	0.08 V
R	Tie 20kΩ to GND	1/3 x VIN	1/3 x VDD
F	Float (leave pin open)	2/3 x VIN	2/3 x VDD
1	Tie 1kΩ to VIN or VDD	VIN – 0.05 V	VDD – 0.04 V

Typical 4-level input thresholds:

- Internal threshold between 0 and R = 0.2 * V_{IN} or V_{DD}
- Internal threshold between R and F = 0.5 * V_{IN} or V_{DD}
- Internal threshold between F and 1 = 0.8 * V_{IN} or V_{DD}

To set these 4-level voltage inputs, each input is controlled by a group of three switches in accordance with Figure 2-1. These switches are located on the back of the EVM. For switch modules that come in a set of six (such as SW3), switches 6-5-4 control one setting, and switches 3-2-1 control another.

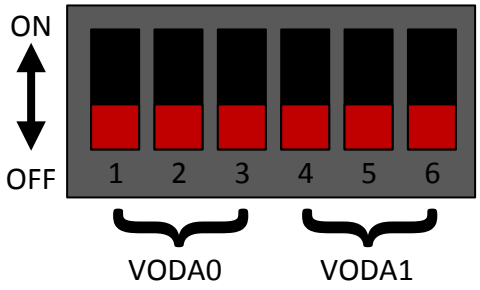


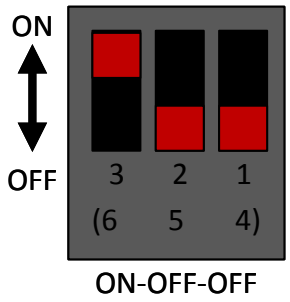
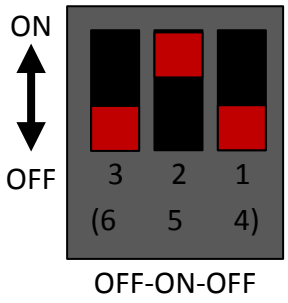
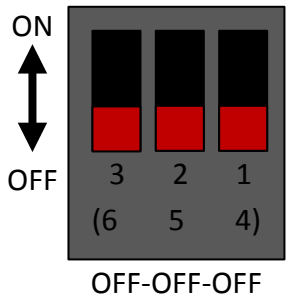
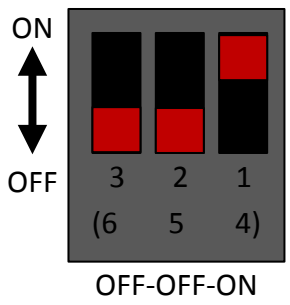
Figure 2-1. Switch Orientation for User Configuration

NOTE: The switches on the back of the EVM physically display the switch numbers in **ascending** order, as shown from the example in Figure 2-1. However, conventional notation of switch settings are typically given in **descending** order. Therefore, switch configurations for the EVM will appear in **descending** order for the rest of this User's Guide as a result of this notation convention.

The following switches are used to set the input condition for 4-level inputs: **SW1, SW2, SW3, SW5, SW6, SW8, and SW9**.

The switch configurations for each of the 4-level inputs are shown in Table 2-2. Note the notation in descending order.

Table 2-2. Switch Configuration

4-Level Input	Setting	Switch Settings (3-2-1 or 6-5-4)
0	Tie 1kΩ to GND	
R	Tie 20kΩ to GND	
F	Float (leave pin open)	
1	Tie 1kΩ to VIN or VDD	

NOTE: Since each 4-level input setting is controlled by a set of three adjacent switches, only one of the three switches can be in the **ON** position at any time.

DS80PCI810EVM Configuration Overview

The following tables describe the various connectors and user-controllable settings available on the DS80PCI810EVM. Since the device can operate in one of three modes (pin mode, SMBus slave mode, and SMBus master mode), note the switch description that matches the intended mode of operation. For more information about specific EQ, VOD, and SD_TH values, see the DS80PCI810 datasheet.

Table 3-1. Description of Connections

Component	Name	Function
J1, J2 J3, J4 J5, J6 J7, J8	IN_B2+, IN_B2- IN_B3+, IN_B3- IN_A0+, IN_A0- IN_A1+, IN_A1-	High-speed differential input pairs
J9, J10 J11, J12 J13, J14 J15, J16	OUT_B2+, OUT_B2- OUT_B3+, OUT_B3- OUT_A0+, OUT_A0- OUT_A1+, OUT_A1-	High-speed differential output pairs
J17	SDA, SCL	Optional SMBus access pins. See datasheet for additional information on SMBus.
J18	EEPROM	EEPROM slot for operation in master mode (optional)
J19	PWR	V_{IN} (3.3 V) or V_{DD} (2.5 V) for DC power
J20	VIH_SEL	Tie V_{IN} (3.3 V) or V_{DD} (2.5 V) to V_{IH} power (jumper required)

Table 3-2. Description of Switch Configuration and Settings

Component	Switch No.	Name and Description
SW1	6-5-4	[Pin and SMBus modes] AD2: ADDR[2] Note: In Pin mode, this must be tied to GND (6-5-4 = **ON**-OFF-OFF)
	3-2-1	[Pin mode] EQB: 4-level EQ setting for B-Channels [SMBus modes] AD3: ADDR[3]
SW2	3-2-1	ENSMB: Enable SMBus modes 3-2-1 = **ON**-OFF-OFF for pin mode 3-2-1 = OFF-OFF-**ON** for SMBus slave mode 3-2-1 = OFF-OFF-OFF for SMBus master mode (load configuration from EEPROM)
SW3	6-5-4	[Pin mode] VODA1: VOD Control [1] for A-Channels [SMBus modes] Set all switches to OFF. VOD is controlled individually via registers.
	3-2-1	[Pin mode] VODA0: VOD Control [0] for A-Channels [SMBus modes] Set all switches to OFF. VOD is controlled individually via registers.

Table 3-2. Description of Switch Configuration and Settings (continued)

Component	Switch No.	Name and Description
SW4	2	SCL **ON** for SMBus modes OFF for Pin mode
	1	SDA **ON** for SMBus modes OFF for Pin mode
SW5	6-5-4	[Pin mode] VODB1: VOD Control [1] for B-Channels [SMBus modes] AD1: ADDR[1]
	3-2-1	[Pin mode] VODB0: VOD Control [0] for B-Channels [SMBus modes] AD0: ADDR[0]
SW6	6-5-4	[Pin and SMBus modes] LPBK-RES (RES1): Reserved Note: Set all switches to OFF for normal operation.
	3-2-1	[Pin and SMBus slave mode] SD_TH: Signal detect assert/de-assert Threshold level for signal detect monitor [SMBus master mode] READ_EN: See description of Read Enable button on SW10.
SW7	2	RESET/PWDN **ON** to enable device OFF to disable device
	1	VDD_SEL **ON** for 3.3 V mode OFF for 2.5 V mode
SW8	6-5-4	[Pin and SMBus modes] RES3: Reserved Note: In Pin mode, this must be tied to GND (6-5-4 = **ON**-OFF-OFF)
	3-2-1	[Pin mode] EQA: 4-level EQ settings for A-Channels [SMBus modes] Set all switches to OFF. EQA is controlled individually via registers.
SW9	6-5-4	[Pin and SMBus modes] RES2: Reserved Note: Set all switches to OFF for normal operation.
	3-2-1	[Pin and SMBus modes] RX_DET: Enable or disable the internal 50Ω to VDD Input Termination. See datasheet for more information.
SW10	N/A	[SMBus master mode] READ_EN: Enable load from external EEPROM in master mode SW6: SD_TH (3-2-1) becomes the READ_EN pin. To start the loading at power up, set SW6 pin 3 to **ON** (pull to GND). To control the start manually, set SW6 pin 1 to **ON** (pull to VDD) and push the SW10 button for the high-to-low transition to start the loading. When loading is complete, the LED – D1 will turn off.

3.1 Quick Start Guide

1. Connect J19: V_{IN} = 3.3 V or V_{DD} = 2.5 V and GND.
   - For V_{IN} = 3.3 V: Set SW7 pin1 (VDD_SEL) to the **ON** position (enable internal LDO regulator) and float V_{DD} at J19.
   - For V_{IN} = 2.5 V: Set SW7 pin1 (VDD_SEL) to the OFF positions (disable internal LDO regulator) and float V_{IN} at J19.
2. Set Jumper J20 for V_{IH} connection to V_{IN} or V_{DD}.
   - For 3.3 V mode: V_{IH} tied to V_{IN} (see Figure 1-1)
   - For 2.5 V mode: V_{IH} tied to V_{DD} (see Figure 1-1)
3. Set the control switches for normal operation:

- SW6 – SD_TH = F (default signal detect threshold level): Set switches (3-2-1) = (OFF-OFF-OFF).
- SW6 – LPBK-RES = F (normal operation): Set switches (6-5-4) = (OFF-OFF-OFF).
- SW7 – RESET = 0 (enables the device): Set switch pin 2 to the **ON** position.
- SW9 – RX_DET = F (enables RX detection): Set switches (3-2-1) = (OFF-OFF-OFF).
- SW9 – RES2 = F (normal operation): Set switches (6-5-4) = (OFF-OFF-OFF).

4. Connect 50Ω SMA cables to the board depending on the desired input and output channels:
   - The input signals J1 to J8 can be connected from a pattern generator.
   - The output signals J9 to J16 can be connected to a scope.

Table 3-3. SMA Channel Connections

A/B Channels	Input Channel	Output Channel
B-Channels	J1: IN_B2+, J2: IN_B2-	J9: OUT_B2+, J10: OUT_B2-
	J3: IN_B3+, J4: IN_B3-	J11: OUT_B3+, J12: OUT_B3-
A-Channels	J5: IN_A0+, J6: IN_A0-	J13: OUT_A0+, J14: OUT_A0-
	J7: IN_A1+, J8: IN_A1-	J15: OUT_A1+, J16: OUT_A1-

5. Pin Mode – Set the input equalization level:
   - Set ENSMB = 0 (1 kΩ to GND) by using SW2 (3-2-1) = (**ON**-OFF-OFF).
   - Set SW4 switches 1 and 2 to the OFF positions so the SMBus signals are disconnected.
   - Refer to Table 2-1 for information on 3-switch settings for the 4-level input.
   - [Example] Set EQA to Level 3: SW8 (3-2-1) = (OFF-OFF-OFF) = EQA = F

Table 3-4. EQA and EQB Settings Available in Pin Mode

EQUALIZATION BOOST RELATIVE TO DC							
Level	EQA EQB	SW8 (3-2-1) SW1 (3-2-1)			dB at 1.5 GHz	dB at 2.5 GHz	dB at 4 GHz
		3	2	1			
1	0	**ON**	OFF	OFF	2.1	2.5	2.7
2	R	OFF	**ON**	OFF	4.0	5.1	6.4
3	F	OFF	OFF	OFF	5.5	7.0	8.3
4	1	OFF	OFF	**ON**	6.8	8.3	9.5

NOTE: For normal operation in pin mode, ensure that RES3 SW8 (6-5-4) = (**ON**-OFF-OFF) and AD2 SW1 (6-5-4) = (**ON**-OFF-OFF).

6. Pin mode: Set the output VOD level:
   - Set ENSMB = 0 (1 kΩ to GND) by using SW2 (3-2-1) = (**ON**-OFF-OFF).
   - Set SW4 switches 1 and 2 to the OFF positions so the SMBus signals are disconnected.
   - Refer to Table 2-1 for information on 3-switch settings for the 4-level input.
   - [Example] Set VODB[1:0] to Level 4: SW5 (6-5-4), (3-2-1) = (OFF-**ON**-OFF), (OFF-OFF-OFF) = VODB[1:0] = R, F

Table 3-5. VOD Output Settings available in Pin Mode

VOD GAIN RELATIVE TO VID = 1.2 V_{PP}									
Level	VODA[1:0] VODB[1:0]	SW3 (6-5-4), (3-2-1) SW5 (6-5-4), (3-2-1)						Input (V_{PP})	Output (V_{PP})
		6	5	4	3	2	1		
1	0, 0	**ON**	OFF	OFF	**ON**	OFF	OFF	1.2	0.65
2	0, R	**ON**	OFF	OFF	OFF	**ON**	OFF	1.2	0.71
3	0, F	**ON**	OFF	OFF	OFF	OFF	**ON**	1.2	0.77
4	R, F	OFF	**ON**	OFF	OFF	OFF	OFF	1.2	0.83
5	F, R	OFF	OFF	OFF	OFF	**ON**	OFF	1.2	0.90
6	1, 0	OFF	OFF	**ON**	**ON**	OFF	OFF	1.2	1.00

NOTE: The DS80PCI810 channels are designed to be linear, ideal for small to moderate levels of input attenuation or when TX FIR transparency is critical to system operation. There are two additional levels of VOD available in SMBus modes. Refer to the DS80PCI810 datasheet for more information.

7. SMBus slave mode – Set the EQ, VOD, VOD_DB level:
   - Set ENSMB = 1 (1 kΩ to VIH) by setting SW2 (3-2-1) = (OFF-OFF-**ON**).
   - Set SW4 switches 1 and 2 to the **ON** position so the SMBUS signals are connected.
   - Set SW3 switches 1 through 6 to the OFF position so they do not connect to the SDA and SCL line.
   - Set SW1 and SW5 to configure the AD[3:0] pins. AD[3:0]=0000 sets device slave address (+ write bit) = 0xB0.
   - Connect SDA, SCL and GND to J17.
   - All EQ, VOD, and VOD_DB levels can be set via SMBus registers in accordance to the register map in the DS80PCI810 datasheet.
8. SMBus master mode – Set the EQ, VOD, VOD_DB level:
   - Load a pre-programmed EEPROM in the J18 EEPROM slot. Note that the DS80PCI810 can only support EEPROM sizes ranging from 2K (256 Bytes) to 8K (1024 bytes). The EEPROM must also be capable of an operating frequency up to 1 MHz.
   - Set ENSMB = FLOAT by setting SW2 (3-2-1) = (OFF-OFF-OFF).
   - Set SW4 switches 1 and 2 to the **ON** position so the SMBUS signals are connected.
   - Set SW3 switches 1 through 6 to the OFF position so they do not connect to the SDA and SCL line.
   - Set SW1 and SW5 to configure the AD[3:0] pins. AD[3:0]=0000 sets device slave address (+ write bit) = 0xB0.
   - Set SW6 and SW10 in accordance to the desired EEPROM load behavior:
     - To start loading EEPROM at power up, set SW6 pin 3 to **ON** (pull to GND).
     - To control the start manually, set SW6 pin 1 to **ON** (pull to VDD) and push the SW10 button for the high-to-low transition to start loading EEPROM.
   - After a successful EEPROM load, the $\overline{\text{ALL\_DONE}}$ pin on the DS80PCI810 goes low and LED – D1 turns off. Afterwards, the DS80PCI810 releases control of the SDA/SCL line and all EQ, VOD, and VOD_DB levels become controllable via SMBus slave registers in accordance to the SMBus register map in the DS80PCI810 datasheet.

Bill of Materials

Table 4-1. Bill of Materials

Item	Qty	Reference	Digikey P/N	Manufacturer P/N	Description
1	1	PCB		SV601142	DS80PCI810EVM PCB
2	1	C1	445-4112-6-ND	C1608X5R0J106M080AB	CAP CER 10UF 6.3V 20% X5R 0603
3	1	C2	445-8144-6-ND	CGJ3E2X7R0J105K080AA	CAP CER 1.0UF 6.3V X7R 10% 0603
4	5	C3, C4, C5, C6, C7	445-4711-1-ND	C0603X5R0J104M	CAP CER .10UF 6.3V X5R 0201
5	16	C11, C12, C13, C14, C15, C16, C17, C18, C19, C20, C21, C22, C23, C24, C25, C26	587-2483-1-ND	LMK063BJ224MP-F	CAP CER .22UF 10V X5R 20% 0201
6	1	D1	511-1592-1-ND	SML-P12PTT86	LED GREEN 0.2MM 13MCD 0402 SMD
7	16	J1, J2, J3, J4, J5, J6, J7, J8, J9, J10, J11, J12, J13, J14, J15, J16	J801-ND	142-0761-881	CONN JACK SMA 50 OHMS PC MOUNT
8	1	J17	WM6504-ND	22-28-4043	CONN HEADER 4POS .100 VERT GOLD
9	2	J19, J20	WM6503-ND	22-28-4033	CONN HEADER 3POS .100 VERT GOLD
10	1	J18	3M5473-ND	4808-3004-CP	SOCKET IC OPEN FRAME 8POS .3"
11	31	R1, R2, R3, R4, R8, R11, R13, R14, R16, R17, R19, R20, R22, R23, R25, R26, R28, R29, R31, R32, R34, R35, R37, R38, R40, R41, R43, R44, R46, R47, R49	P1.00KLCT-ND	ERJ-2RKF1001X	RES 1.00K OHM 1/10W 1% 0402 SMD
12	1	R7	P220LCT-ND	ERJ-2RKF2200X	RES 220 OHM 1/10W 1% 0402 SMD
13	13	R12, R15, R18, R21, R24, R27, R30, R33, R36, R39, R42, R45, R48	P20.0KLCT-ND	ERJ-2RKF2002X	RES 20.0K OHM 1/10W 1% 0402 SMD
14	2	R5, R6	P4.70KLCT-ND	ERJ-2RKF4701X	RES 4.70K OHM 1/10W 1% 0402 SMD
15	6	SW1, SW3, SW5, SW6, SW8, SW9	CT2196MST-ND	219-6MST	SWITCH TAPE SEAL 6 POS SMD
16	1	SW2	CT2193MST-ND	219-3MST	SWITCH TAPE SEAL 3 POS SMD
17	2	SW4, SW7	CT2192MST-ND	219-2MST	SWITCH TAPE SEAL 2 POS SMD
18	1	SW10	P12225STB-ND	EVQ-21505R	SWITCH LT 6MM 160GF 5MM HEIGHT
19	1	U1		DS80PCI810NJY	BUFFER - REPEATER
20	1	N/A	S9001-ND	SPC02SYAN	CONN JUMPER SHORTING GOLD FLASH

Schematic

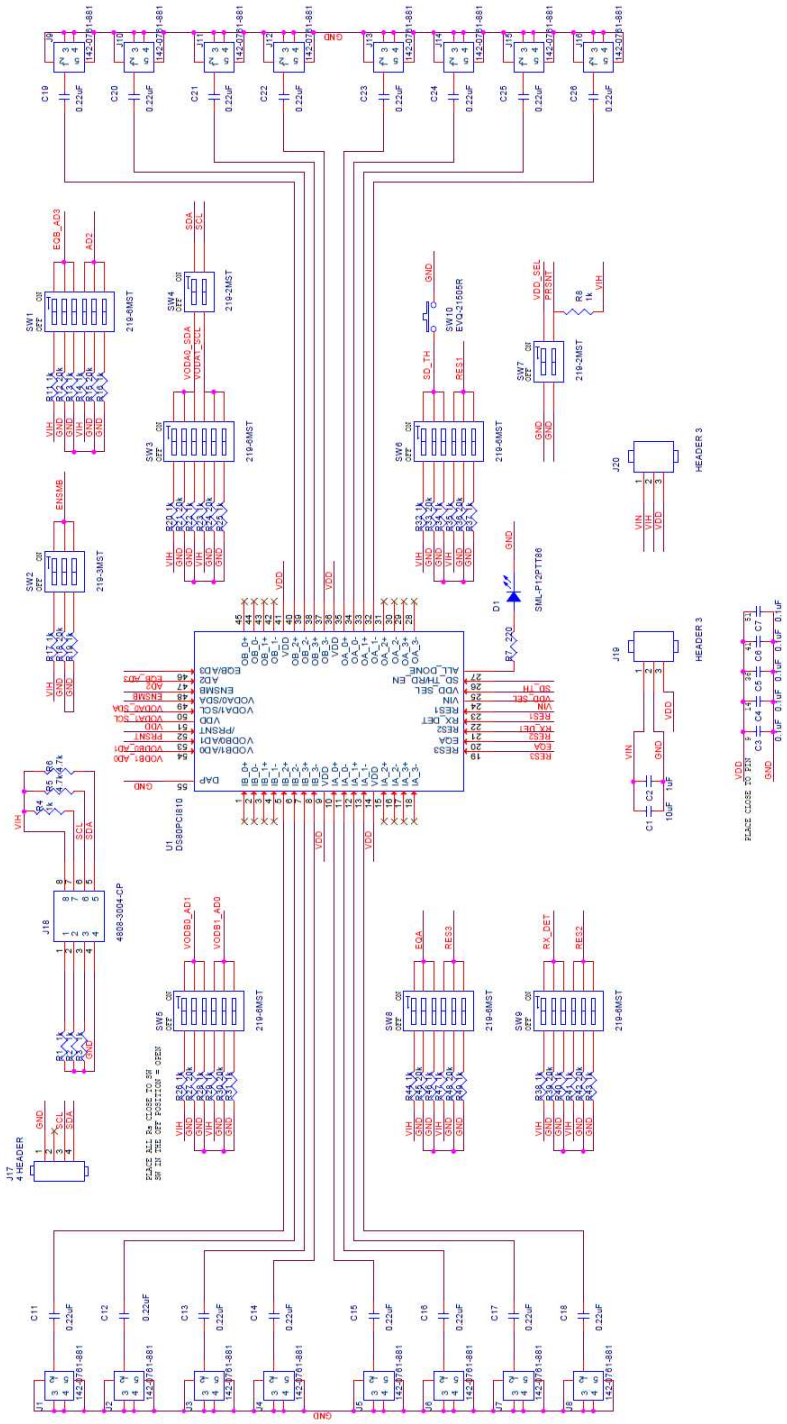


Figure 5-1. Schematic

EVM Layout

Figure 6-1 and Figure 6-2 show the DS80PCI810EVM layout. The evaluation board uses switches to control signal integrity settings. The DS80PCI810EVM allows access to the inner four buffer repeater channels while remaining both very compact and low power. The WQFN package offers an exposed thermal pad to enhance electrical and thermal performance. This must be soldered to the copper landing on the PWB.

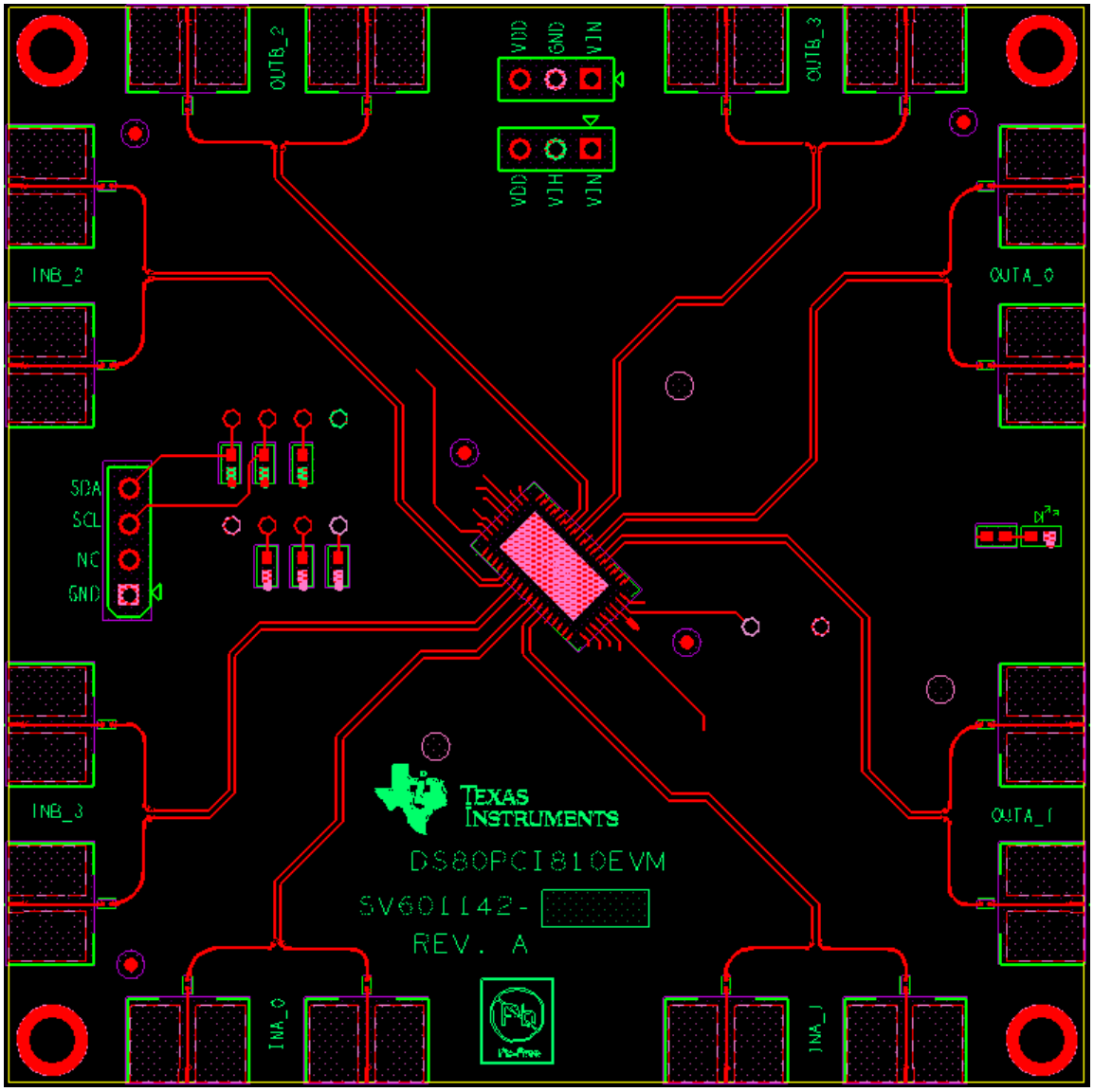


Figure 6-1. Top Assembly Layer

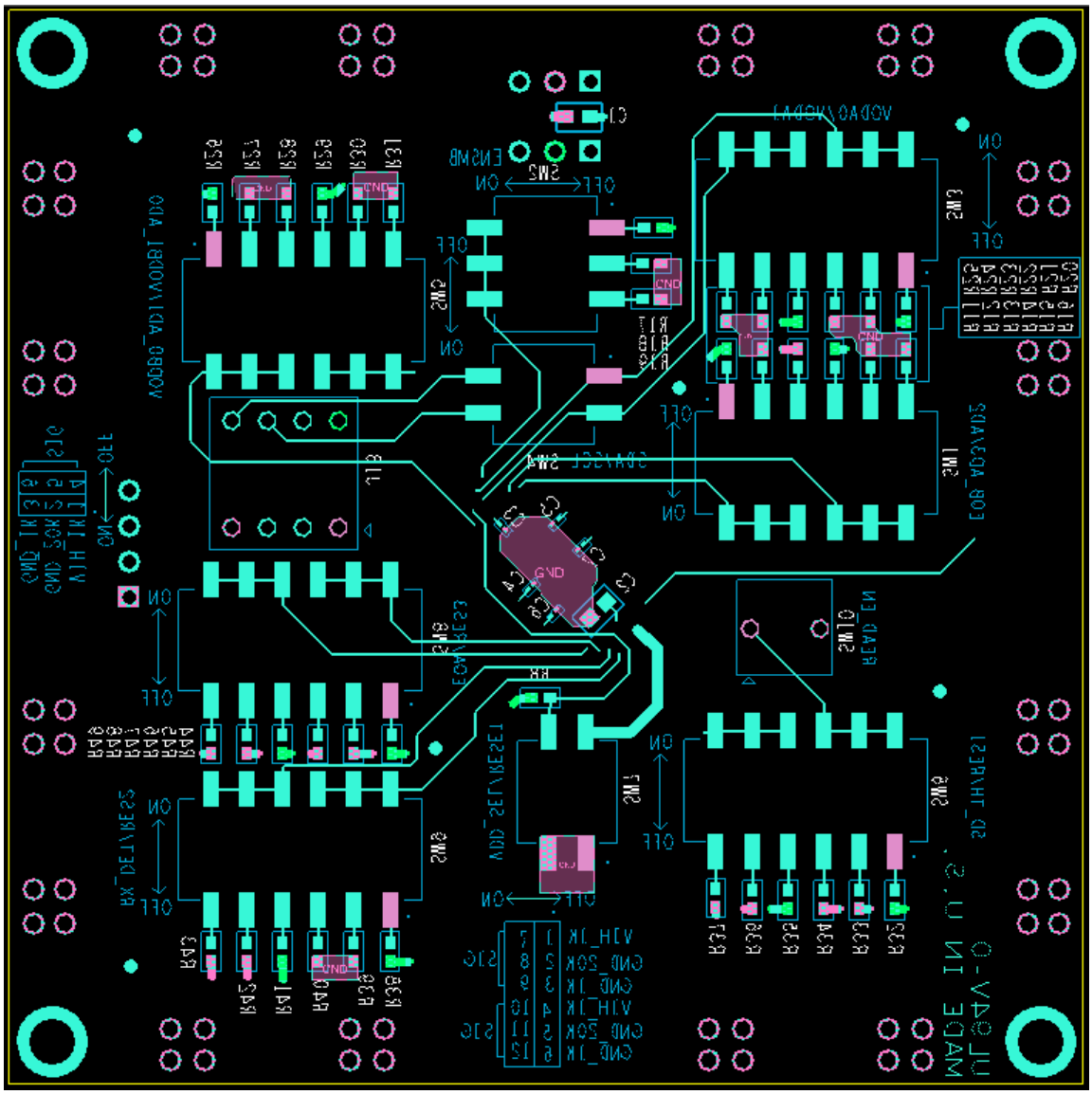


Figure 6-2. Bottom Assembly Layer

STANDARD TERMS AND CONDITIONS FOR EVALUATION MODULES

1. *Delivery:* TI delivers TI evaluation boards, kits, or modules, including any accompanying demonstration software, components, or documentation (collectively, an “EVM” or “EVMs”) to the User (“User”) in accordance with the terms and conditions set forth herein. Acceptance of the EVM is expressly subject to the following terms and conditions.

   1.1 EVMs are intended solely for product or software developers for use in a research and development setting to facilitate feasibility evaluation, experimentation, or scientific analysis of TI semiconductors products. EVMs have no direct function and are not finished products. EVMs shall not be directly or indirectly assembled as a part or subassembly in any finished product. For clarification, any software or software tools provided with the EVM (“Software”) shall not be subject to the terms and conditions set forth herein but rather shall be subject to the applicable terms and conditions that accompany such Software

   1.2 EVMs are not intended for consumer or household use. EVMs may not be sold, sublicensed, leased, rented, loaned, assigned, or otherwise distributed for commercial purposes by Users, in whole or in part, or used in any finished product or production system.

2 *Limited Warranty and Related Remedies/Disclaimers*:

   2.1 These terms and conditions do not apply to Software. The warranty, if any, for Software is covered in the applicable Software License Agreement.

   2.2 TI warrants that the TI EVM will conform to TI's published specifications for ninety (90) days after the date TI delivers such EVM to User. Notwithstanding the foregoing, TI shall not be liable for any defects that are caused by neglect, misuse or mistreatment by an entity other than TI, including improper installation or testing, or for any EVMs that have been altered or modified in any way by an entity other than TI. Moreover, TI shall not be liable for any defects that result from User's design, specifications or instructions for such EVMs. Testing and other quality control techniques are used to the extent TI deems necessary or as mandated by government requirements. TI does not test all parameters of each EVM.

   2.3 If any EVM fails to conform to the warranty set forth above, TI's sole liability shall be at its option to repair or replace such EVM, or credit User's account for such EVM. TI's liability under this warranty shall be limited to EVMs that are returned during the warranty period to the address designated by TI and that are determined by TI not to conform to such warranty. If TI elects to repair or replace such EVM, TI shall have a reasonable time to repair such EVM or provide replacements. Repaired EVMs shall be warranted for the remainder of the original warranty period. Replaced EVMs shall be warranted for a new full ninety (90) day warranty period.

3 *Regulatory Notices:*

   3.1 *United States*

      3.1.1 *Notice applicable to EVMs not FCC-Approved:*

      This kit is designed to allow product developers to evaluate electronic components, circuitry, or software associated with the kit to determine whether to incorporate such items in a finished product and software developers to write software applications for use with the end product. This kit is not a finished product and when assembled may not be resold or otherwise marketed unless all required FCC equipment authorizations are first obtained. Operation is subject to the condition that this product not cause harmful interference to licensed radio stations and that this product accept harmful interference. Unless the assembled kit is designed to operate under part 15, part 18 or part 95 of this chapter, the operator of the kit must operate under the authority of an FCC license holder or must secure an experimental authorization under part 5 of this chapter.

      3.1.2 *For EVMs annotated as FCC – FEDERAL COMMUNICATIONS COMMISSION Part 15 Compliant:*

      CAUTION

      This device complies with part 15 of the FCC Rules. Operation is subject to the following two conditions: (1) This device may not cause harmful interference, and (2) this device must accept any interference received, including interference that may cause undesired operation.

      Changes or modifications not expressly approved by the party responsible for compliance could void the user's authority to operate the equipment.

      FCC Interference Statement for Class A EVM devices

      NOTE: This equipment has been tested and found to comply with the limits for a Class A digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference when the equipment is operated in a commercial environment. This equipment generates, uses, and can radiate radio frequency energy and, if not installed and used in accordance with the instruction manual, may cause harmful interference to radio communications. Operation of this equipment in a residential area is likely to cause harmful interference in which case the user will be required to correct the interference at his own expense.

FCC Interference Statement for Class B EVM devices

NOTE: This equipment has been tested and found to comply with the limits for a Class B digital device, pursuant to part 15 of the FCC Rules. These limits are designed to provide reasonable protection against harmful interference in a residential installation. This equipment generates, uses and can radiate radio frequency energy and, if not installed and used in accordance with the instructions, may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment does cause harmful interference to radio or television reception, which can be determined by turning the equipment off and on, the user is encouraged to try to correct the interference by one or more of the following measures:

- *Reorient or relocate the receiving antenna.*
- *Increase the separation between the equipment and receiver.*
- *Connect the equipment into an outlet on a circuit different from that to which the receiver is connected.*
- *Consult the dealer or an experienced radio/TV technician for help.*

3.2 *Canada*

3.2.1 *For EVMs issued with an Industry Canada Certificate of Conformance to RSS-210*

Concerning EVMs Including Radio Transmitters:

This device complies with Industry Canada license-exempt RSS standard(s). Operation is subject to the following two conditions: (1) this device may not cause interference, and (2) this device must accept any interference, including interference that may cause undesired operation of the device.

Concernant les EVMs avec appareils radio:

Le présent appareil est conforme aux CNR d'Industrie Canada applicables aux appareils radio exempts de licence. L'exploitation est autorisée aux deux conditions suivantes: (1) l'appareil ne doit pas produire de brouillage, et (2) l'utilisateur de l'appareil doit accepter tout brouillage radioélectrique subi, même si le brouillage est susceptible d'en compromettre le fonctionnement.

Concerning EVMs Including Detachable Antennas:

Under Industry Canada regulations, this radio transmitter may only operate using an antenna of a type and maximum (or lesser) gain approved for the transmitter by Industry Canada. To reduce potential radio interference to other users, the antenna type and its gain should be so chosen that the equivalent isotropically radiated power (e.i.r.p.) is not more than that necessary for successful communication. This radio transmitter has been approved by Industry Canada to operate with the antenna types listed in the user guide with the maximum permissible gain and required antenna impedance for each antenna type indicated. Antenna types not included in this list, having a gain greater than the maximum gain indicated for that type, are strictly prohibited for use with this device.

Concernant les EVMs avec antennes détachables

Conformément à la réglementation d'Industrie Canada, le présent émetteur radio peut fonctionner avec une antenne d'un type et d'un gain maximal (ou inférieur) approuvé pour l'émetteur par Industrie Canada. Dans le but de réduire les risques de brouillage radioélectrique à l'intention des autres utilisateurs, il faut choisir le type d'antenne et son gain de sorte que la puissance isotrope rayonnée équivalente (p.i.r.e.) ne dépasse pas l'intensité nécessaire à l'établissement d'une communication satisfaisante. Le présent émetteur radio a été approuvé par Industrie Canada pour fonctionner avec les types d'antenne énumérés dans le manuel d'usage et ayant un gain admissible maximal et l'impédance requise pour chaque type d'antenne. Les types d'antenne non inclus dans cette liste, ou dont le gain est supérieur au gain maximal indiqué, sont strictement interdits pour l'exploitation de l'émetteur

3.3 *Japan*

3.3.1 *Notice for EVMs delivered in Japan:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page 日本国内に輸入される評価用キット、ボードについては、次のところをご覧ください。
http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_01.page

3.3.2 *Notice for Users of EVMs Considered "Radio Frequency Products" in Japan:* EVMs entering Japan may not be certified by TI as conforming to Technical Regulations of Radio Law of Japan.

If User uses EVMs in Japan, not certified to Technical Regulations of Radio Law of Japan, User is required by Radio Law of Japan to follow the instructions below with respect to EVMs:

1. Use EVMs in a shielded room or any other test facility as defined in the notification #173 issued by Ministry of Internal Affairs and Communications on March 28, 2006, based on Sub-section 1.1 of Article 6 of the Ministry's Rule for Enforcement of Radio Law of Japan,
2. Use EVMs only after User obtains the license of Test Radio Station as provided in Radio Law of Japan with respect to EVMs, or
3. Use of EVMs only after User obtains the Technical Regulations Conformity Certification as provided in Radio Law of Japan with respect to EVMs. Also, do not transfer EVMs, unless User gives the same notice above to the transferee. Please note that if User does not follow the instructions above, User will be subject to penalties of Radio Law of Japan.

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2. 実験局の免許を取得後ご使用いただく。
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3.3.3 *Notice for EVMs for Power Line Communication:* Please see http://www.tij.co.jp/lsds/ti_ja/general/eStore/notice_02.page

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4 *EVM Use Restrictions and Warnings:*

4.1 EVMS ARE NOT FOR USE IN FUNCTIONAL SAFETY AND/OR SAFETY CRITICAL EVALUATIONS, INCLUDING BUT NOT LIMITED TO EVALUATIONS OF LIFE SUPPORT APPLICATIONS.

4.2 User must read and apply the user guide and other available documentation provided by TI regarding the EVM prior to handling or using the EVM, including without limitation any warning or restriction notices. The notices contain important safety information related to, for example, temperatures and voltages.

4.3 *Safety-Related Warnings and Restrictions:*

4.3.1 User shall operate the EVM within TI's recommended specifications and environmental considerations stated in the user guide, other available documentation provided by TI, and any other applicable requirements and employ reasonable and customary safeguards. Exceeding the specified performance ratings and specifications (including but not limited to input and output voltage, current, power, and environmental ranges) for the EVM may cause personal injury or death, or property damage. If there are questions concerning performance ratings and specifications, User should contact a TI field representative prior to connecting interface electronics including input power and intended loads. Any loads applied outside of the specified output range may also result in unintended and/or inaccurate operation and/or possible permanent damage to the EVM and/or interface electronics. Please consult the EVM user guide prior to connecting any load to the EVM output. If there is uncertainty as to the load specification, please contact a TI field representative. During normal operation, even with the inputs and outputs kept within the specified allowable ranges, some circuit components may have elevated case temperatures. These components include but are not limited to linear regulators, switching transistors, pass transistors, current sense resistors, and heat sinks, which can be identified using the information in the associated documentation. When working with the EVM, please be aware that the EVM may become very warm.

4.3.2 EVMs are intended solely for use by technically qualified, professional electronics experts who are familiar with the dangers and application risks associated with handling electrical mechanical components, systems, and subsystems. User assumes all responsibility and liability for proper and safe handling and use of the EVM by User or its employees, affiliates, contractors or designees. User assumes all responsibility and liability to ensure that any interfaces (electronic and/or mechanical) between the EVM and any human body are designed with suitable isolation and means to safely limit accessible leakage currents to minimize the risk of electrical shock hazard. User assumes all responsibility and liability for any improper or unsafe handling or use of the EVM by User or its employees, affiliates, contractors or designees.

4.4 User assumes all responsibility and liability to determine whether the EVM is subject to any applicable international, federal, state, or local laws and regulations related to User's handling and use of the EVM and, if applicable, User assumes all responsibility and liability for compliance in all respects with such laws and regulations. User assumes all responsibility and liability for proper disposal and recycling of the EVM consistent with all applicable international, federal, state, and local requirements.

5. *Accuracy of Information:* To the extent TI provides information on the availability and function of EVMs, TI attempts to be as accurate as possible. However, TI does not warrant the accuracy of EVM descriptions, EVM availability or other information on its websites as accurate, complete, reliable, current, or error-free.

6. *Disclaimers:*

   6.1 EXCEPT AS SET FORTH ABOVE, EVMS AND ANY WRITTEN DESIGN MATERIALS PROVIDED WITH THE EVM (AND THE DESIGN OF THE EVM ITSELF) ARE PROVIDED "AS IS" AND "WITH ALL FAULTS." TI DISCLAIMS ALL OTHER WARRANTIES, EXPRESS OR IMPLIED, REGARDING SUCH ITEMS, INCLUDING BUT NOT LIMITED TO ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF ANY THIRD PARTY PATENTS, COPYRIGHTS, TRADE SECRETS OR OTHER INTELLECTUAL PROPERTY RIGHTS.

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7. *USER'S INDEMNITY OBLIGATIONS AND REPRESENTATIONS.* USER WILL DEFEND, INDEMNIFY AND HOLD TI, ITS LICENSORS AND THEIR REPRESENTATIVES HARMLESS FROM AND AGAINST ANY AND ALL CLAIMS, DAMAGES, LOSSES, EXPENSES, COSTS AND LIABILITIES (COLLECTIVELY, "CLAIMS") ARISING OUT OF OR IN CONNECTION WITH ANY HANDLING OR USE OF THE EVM THAT IS NOT IN ACCORDANCE WITH THESE TERMS AND CONDITIONS. THIS OBLIGATION SHALL APPLY WHETHER CLAIMS ARISE UNDER STATUTE, REGULATION, OR THE LAW OF TORT, CONTRACT OR ANY OTHER LEGAL THEORY, AND EVEN IF THE EVM FAILS TO PERFORM AS DESCRIBED OR EXPECTED.

8. *Limitations on Damages and Liability:*

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9. *Return Policy*. Except as otherwise provided, TI does not offer any refunds, returns, or exchanges. Furthermore, no return of EVM(s) will be accepted if the package has been opened and no return of the EVM(s) will be accepted if they are damaged or otherwise not in a resalable condition. If User feels it has been incorrectly charged for the EVM(s) it ordered or that delivery violates the applicable order, User should contact TI. All refunds will be made in full within thirty (30) working days from the return of the components(s), excluding any postage or packaging costs.

10. *Governing Law:* These terms and conditions shall be governed by and interpreted in accordance with the laws of the State of Texas, without reference to conflict-of-laws principles. User agrees that non-exclusive jurisdiction for any dispute arising out of or relating to these terms and conditions lies within courts located in the State of Texas and consents to venue in Dallas County, Texas. Notwithstanding the foregoing, any judgment may be enforced in any United States or foreign court, and TI may seek injunctive relief in any United States or foreign court.

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