HARRIS

RFP15N08L

N-Channel Logic Level Power Field-Effect Transistor

August 1991

Features

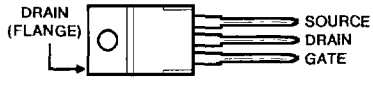
- 15A, 80V
- $R_{DS(ON)}$: 0.14Ω
- Design Optimized for 5 Volt Gate Drive
- Can be Driven Directly from Q-MOS, N-MOS, TTL Circuits
- SOA is Power-Dissipation Limited
- +175°C Rated Junction Temperature
- Logic Level Gate
- High Input Impedance

Description

The RFP15N08L is an n-channel enhancement mode silicon gate power field effect transistor specifically designed for use with logic level (5 volt) driving sources in applications such as programmable controllers, automotive switching, and solonoid drivers. This performance is accomplished through a special gate oxide design which provides full rated conduction at gate biases in the 3-5 volt range, thereby facilitating true on-off power control from logic circuit supply voltages.

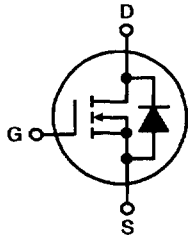
Package

TO-220AB
TOP VIEW



Terminal Diagram

N-CHANNEL ENHANCEMENT MODE



Absolute Maximum Ratings (T_C = +25°C), Unless Otherwise Specified

		RFP15N08L	UNITS
Drain-Source Voltage	V_{DSS}	80	V
Drain-Gate Voltage	V_{DGR}	80	V
Gate-Source Voltage	V_{GS}	±10	V
Drain Current, RMS Continuous	I_D	15	A
Pulsed	I_{DM}	40	A
Power Dissipation Total @ T_C = +25°C	P_D	72	W
Power Dissipation Derating T_C = +25°C		0.48	W/°C
Operating and Storage Junction Temperature Range	T_j, T_{STG}	-55 to +175	°C

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PREVIEW PRODUCTS

CAUTION: These devices are sensitive to electrostatic discharge. Proper I.C. handling procedures should be followed.

File Number **2840**

Electrical Characteristics At Case Temperature (T_C = +25°C), Unless Otherwise Specified

PARAMETERS	SYMBOL	TEST CONDITIONS		LIMITS MIN	LIMITS MAX	UNITS
Drain-Source Breakdown Voltage	BV_{DSS}	I_D = 1mA	V_{GS} = 0V	80	-	V
Gate Threshold Voltage	$V_{GS(TH)}$	V_{GS} = V_{DS}	I_D = 1mA	1	2.5	V
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 65V		-	1	µA
		V_{DS} = 65V	at T_C = +125°C	-	50	µA
Gate-Source Leakage Current	I_{GSS}	V_{GS} = ±10V	V_{DS} = 0V	-	100	nA
Drain-Source On Voltage	$V_{DS(ON)}$	I_D = 7.5A	V_{GS} = 5V	-	1.05	V
		I_D = 15A	V_{GS} = 5V	-	3.0	V
On Resistance	$R_{DS(ON)}$	I_D = 7.5A	V_{GS} = 5V	-	0.14	Ω
Total Gate Charge	$Q_{G(TOTAL)}$	V_{GS} = 0-10V	V_{DD} = 64V	-	80	nC
Gate Charge at 5V	$Q_{G(5)}$	V_{GS} = 0-5V	I_D = 15A	-	45	nC
Threshold Gate Charge	$Q_{G(TH)}$	V_{GS} = 0-1V	R_L = 4.27Ω	-	3	nC
Plateau Voltage	$V_{(PLATEAU)}$	I_D =15A	V_{DS} =15V	-	4.5	V
Turn-On Delay Time	$t_{D(ON)}$	V_{DD} = 40V	I_D = 7.5A	-	40	ns
Rise Time	t_r	R_G = 6.25Ω	V_{GS} = 5V	-	325	ns
Turn-Off Delay Time	$t_{D(OFF)}$			-	325	ns
Fall Time	t_f			-	325	ns
Thermal Resistance Junction to Case	$R\theta_{JC}$	-		-	2.083	°C/W

Source-Drain Diode Ratings and Characteristics

PARAMETERS	SYMBOL	TEST CONDITIONS	LIMITS MIN	LIMITS MAX	UNITS
Forward Voltage	V_{SD}	I_{SD} = 7.5A	-	1.4	V
Reverse Recovery Time	T_{RR}	I_F = 4A, di_f/dt = 100a/µs	-	225(typ)	ns