T-46-23-10

CY7C191
CY7C192

CYPRESS SEMICONDUCTOR

65,536 x 4 Static R/W RAM Separate I/O

Features

- Automatic power-down when deselected
- Transparent write (7C191)
- CMOS for optimum speed/power
- High speed
  — t_{AA} = 25 ns
- Low active power
  — 880 mW
- Low standby power
  — 220 mW
- TTL-compatible inputs and outputs
- Capable of withstanding greater than 2001V electrostatic discharge

Functional Description

The CY7C191 and CY7C192 are high-performance CMOS static RAMs organized as 65,536 x 4 bits with separate I/O. Easy memory expansion is provided by active LOW chip enable ($\overline{CE}$) and three-state drivers. They have an automatic power-down feature, reducing the power consumption by 75% when deselected.

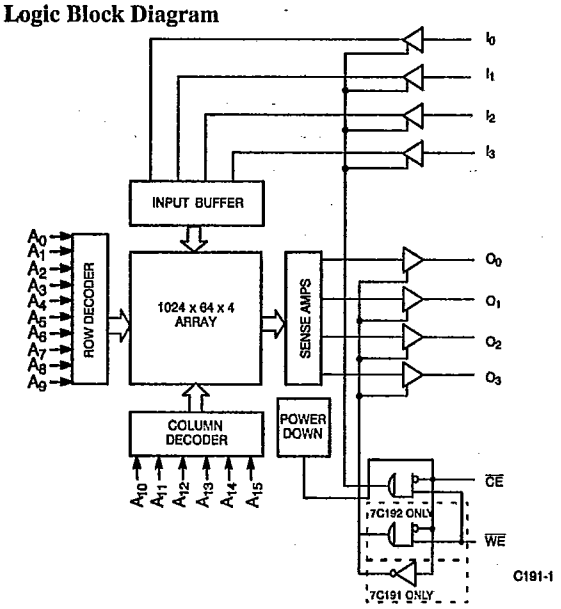
Writing to the device is accomplished when the chip enable ($\overline{CE}$) and write enable ($\overline{WE}$) inputs are both LOW. Data on the four input pins (I_0 through I_3) is written into the memory location specified on the address pins (A_0 through A_{15}).

Reading the device is accomplished by taking the chip enable ($\overline{CE}$) LOW while the write enable ($\overline{WE}$) remains HIGH. Under these conditions the contents of the memory location specified on the address pins will appear on the four data output pins.

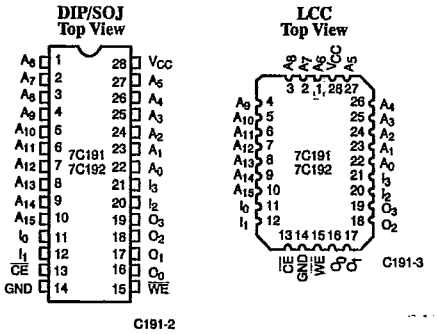
The output pins stay in high-impedance state when write enable ($\overline{WE}$) is LOW (7C192 only), or chip enable ($\overline{CE}$) is HIGH.

A die coat is used to insure alpha immunity.

Logic Block Diagram



Pin Configurations



Selection Guide

		7C191–12 7C192–12	7C191–15 7C192–15	7C191–20 7C192–20	7C191–25 7C192–25	7C191–35 7C192–35	7C191–45 7C192–45
Maximum Access Time (ns)		12	15	20	25	35	45
Maximum Operating Current (mA)	Commercial	160	150	140	120	120	120
	Military		160	150	130	130	130
Maximum Standby Current (mA)		40	40	40	35	35	35

Shaded area contains advanced information.

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential (Pin 28 to Pin 14) ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +7.0V

DC Input Voltage ..... −3.0V to +7.0V

Output Current into Outputs (LOW) ..... 20 mA

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature[1]	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Military	−55°C to +125°C	5V ± 10%

SRAMs

Electrical Characteristics Over the Operating Range[2]

Parameters	Description	Test Conditions		7C191−12 7C192−12 Min.	7C191−12 7C192−12 Max.	7C191−15 7C192−15 Min.	7C191−15 7C192−15 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−0.5	0.8	−0.5	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	µA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	µA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		160		150	mA
			Mil				160	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			40		40	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0			20		20	mA

Shaded area contains advanced information.

Notes:

1. T_A is the "instant on" case temperature.
2. See the last page of this specification for Group A subgroup testing information.
3. Not more than 1 output should be shorted at one time. Duration of the short circuit should not exceed 30 seconds.
4. Tested initially and after any design or process changes that may affect these parameters.

Electrical Characteristics Over the Operating Range[2] (continued)

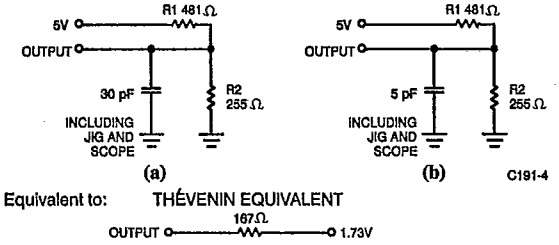
Parameters	Description	Test Conditions		7C191–20 7C192–20 Min.	7C191–20 7C192–20 Max.	7C191–25, 35, 45 7C192–25, 35, 45 Min.	7C191–25, 35, 45 7C192–25, 35, 45 Max.	Units
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 8.0 mA			0.4		0.4	V
V_{IH}	Input HIGH Voltage			2.2	V_{CC}	2.2	V_{CC}	V
V_{IL}	Input LOW Voltage			−0.5	0.8	−3.0	0.8	V
I_{IX}	Input Load Current	GND ≤ V_I ≤ V_{CC}		−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_O ≤ V_{CC}, Output Disabled		−10	+10	−10	+10	μA
I_{OS}	Output Short Circuit Current[3]	V_{CC} = Max., V_{OUT} = GND			−350		−350	mA
I_{CC}	V_{CC} Operating Supply Current	V_{CC} = Max., I_{OUT} = 0 mA, f = f_{MAX} = $1/t_{RC}$	Com'l		140		120	mA
			Mil		150		130	
I_{SB1}	Automatic $\overline{CE}$ Power-Down Current—TTL Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{IH}, V_{IN} ≥ V_{IH} or V_{IN} ≤ V_{IL}, f = f_{MAX}			40		35	mA
I_{SB2}	Automatic $\overline{CE}$ Power-Down Current—CMOS Inputs	Max. V_{CC}, $\overline{CE}$ ≥ V_{CC} − 0.3V, V_{IN} ≥ V_{CC} − 0.3V or V_{IN} ≤ 0.3V, f = 0			20		20	mA

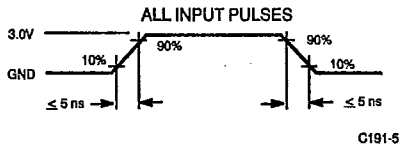
Shaded area contains advanced information.

Capacitance[4]

Parameters	Description	Test Conditions	Max.	Units
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

AC Test Loads and Waveforms





SRAMs

Switching Characteristics Over the Operating Range[2,5]

Parameters	Description	7C191–12 7C192–12		7C191–15 7C192–15		7C191–20 7C192–20		7C191–25 7C192–25		7C191–35 7C192–35		7C191–45 7C192–45		Units
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
READ CYCLE														
t_{RC}	Read Cycle Time	12		15		20		25		35		45		ns
t_{AA}	Address to Data Valid		12		15		20		25		35		45	ns
t_{OHA}	Output Hold from Address Change	3		3		3		3		3		3		ns
t_{ACE}	$\overline{CE}$ LOW to Data Valid		12		15		20		25		35		45	ns
t_{LZCE}	$\overline{CE}$ LOW to Low Z[6]	3		3		3		3		3		3		ns
t_{HZCE}	$\overline{CE}$ HIGH to High Z[6,7]		7		8		10		13		15		20	ns
t_{PU}	$\overline{CE}$ LOW to Power-Up	0		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ HIGH to Power-Down		12		15		20		25		35		45	ns
WRITE CYCLE[8]														
t_{WC}	Write Cycle Time	12		15		20		25		35		45		ns
t_{SCE}	$\overline{CE}$ LOW to Write End	9		10		15		20		30		40		ns
t_{AW}	Address Set-Up to Write End	9		10		15		20		25		35		ns
t_{HA}	Address Hold from Write End	0		0		0		0		0		0		ns
t_{SA}	Address Set-Up to Write Start	0		0		0		0		0		0		ns
t_{PWE}	$\overline{WE}$ Pulse Width	9		10		15		20		25		30		ns
t_{SD}	Data Set-Up to Write End	7		8		10		15		17		20		ns
t_{HD}	Data Hold from Write End	0		0		0		0		0		0		ns
t_{LZWE}	$\overline{WE}$ HIGH to Low Z (7C192)[6]	3		3		3		3		3		3		ns
t_{HZWE}	$\overline{WE}$ LOW to High Z (7C192)[6,7]		7		7		10		13		15		20	ns
t_{AWE}	$\overline{WE}$ LOW to Data Valid (7C191)		12		15		20		25		30		35	ns
t_{ADV}	Data Valid to Output Valid (7C191)		12		15		20		20		30		35	ns

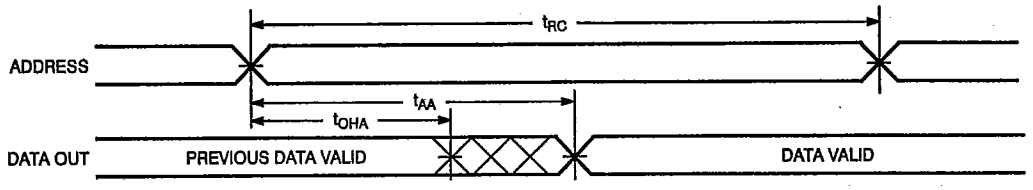
Shaded area contains advanced information.

Notes:

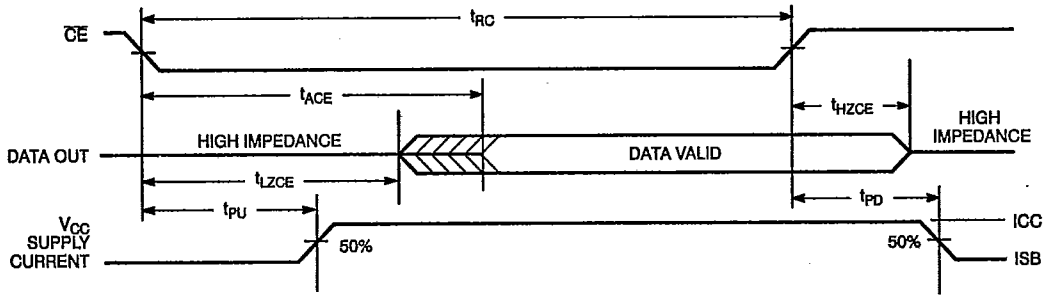
5. Test conditions assume signal transition time of 5 ns or less, timing reference levels of 1.5V, input pulse levels of 0 to 3.0V, and output loading of the specified I_{OL}/I_{OH} and 30-pF load capacitance.
6. At any given temperature and voltage condition, t_{HZCE} is less than t_{LZCE}, t_{HZWE} is less than t_{LZWE} for any given device. These parameters are guaranteed and not 100% tested.
7. t_{HZCE} and t_{HZWE} are specified with C_L = 5 pF as in part (b) of AC Test Loads. Transition is measured ±500 mV from steady state voltage.
8. The internal write time of the memory is defined by the overlap of $\overline{CE}$ LOW and $\overline{WE}$ LOW. Both signals must be LOW to initiate a write and either signal can terminate a write by going HIGH. The data input set-up and hold timing should be referenced to the rising edge of the signal that terminates the write.
9. $\overline{WE}$ is HIGH for read cycle.
10. Device is continuously selected, $\overline{CE}$ = V_{IL}.
11. Address valid prior to or coincident with $\overline{CE}$ transition LOW.
12. If $\overline{CE}$ goes HIGH simultaneously with $\overline{WE}$ HIGH, the output remains in a high-impedance state (7C192 only).

Switching Waveforms

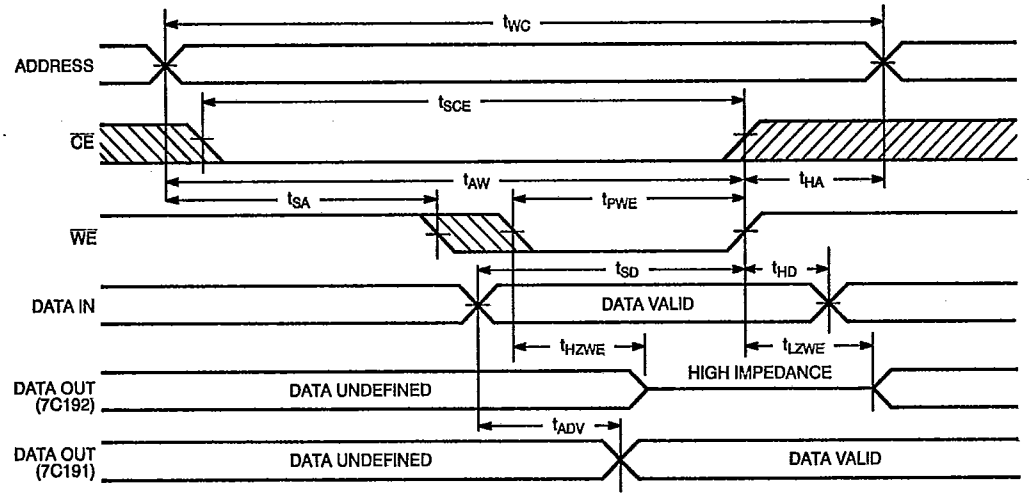
Read Cycle No. 1[9, 10]



Read Cycle No. 2[9, 11]

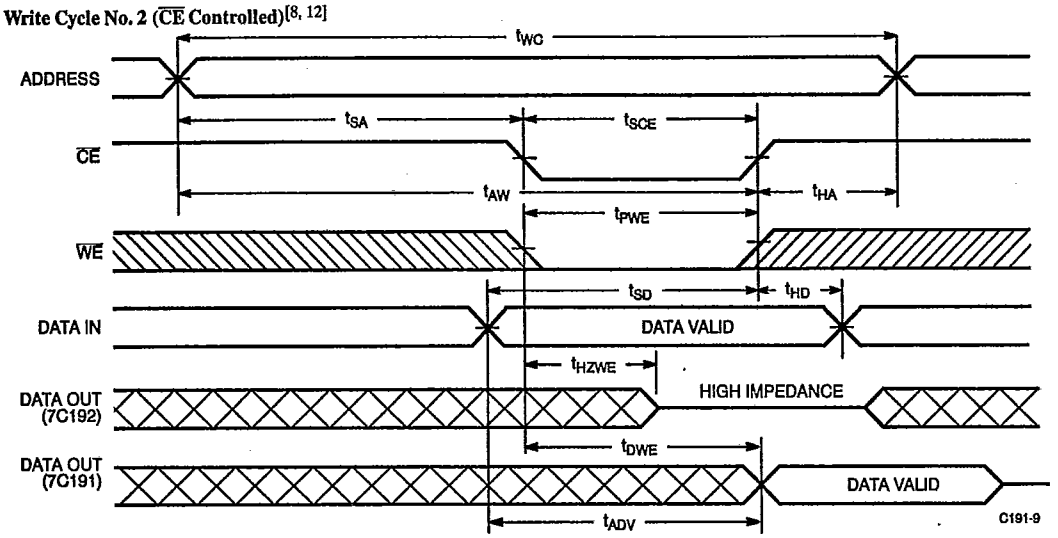


Write Cycle No. 1 ($\overline{WE}$ Controlled)[8]

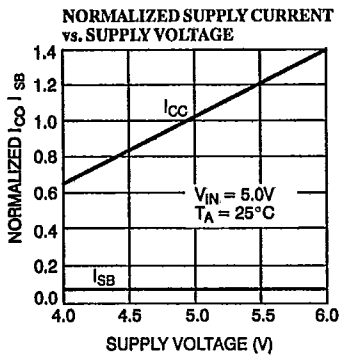


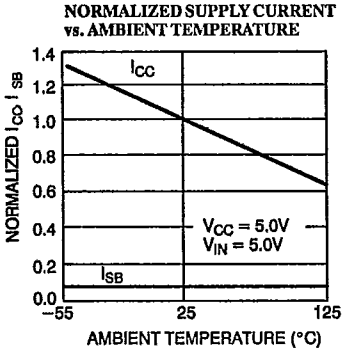
Switching Waveforms (continued)

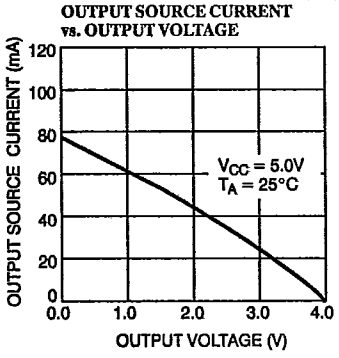
Write Cycle No. 2 ($\overline{CE}$ Controlled)[8, 12]

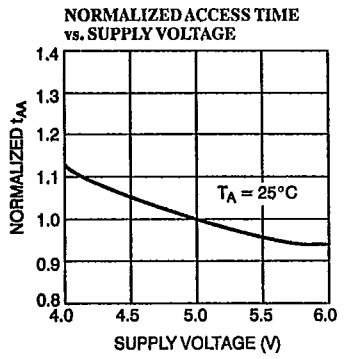


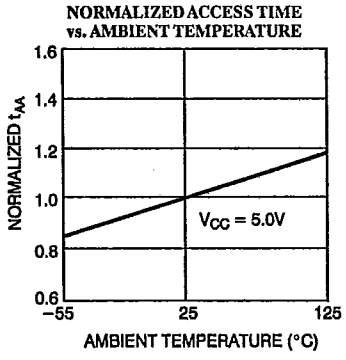
Typical DC and AC Characteristics

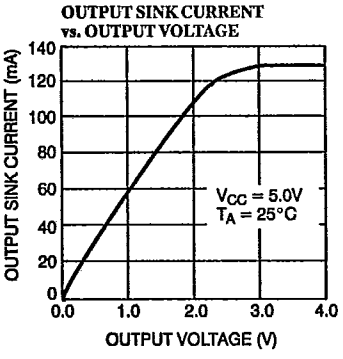






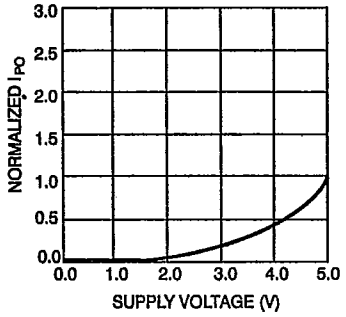




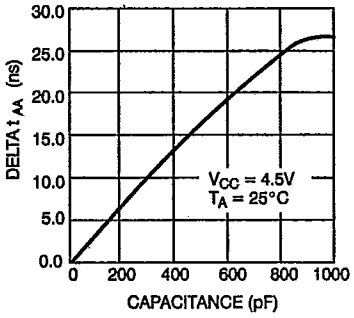


Typical DC and AC Characteristics (continued)

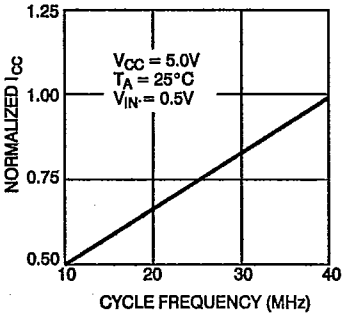
TYPICAL POWER-ON CURRENT vs. SUPPLY VOLTAGE



TYPICAL ACCESS TIME CHANGE vs. OUTPUT LOADING



NORMALIZED I_{CC} vs. CYCLE TIME



Ordering Information

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7C191–12DC	D22	Commercial
	CY7C191–12LC	L54	
	CY7C191–12PC	P21	
	CY7C191–12VC	V21	
15	CY7C191–15DC	D22	Commercial
	CY7C191–15LC	L54	
	CY7C191–15PC	P21	
	CY7C191–15VC	V21	
	CY7C191–15DMB	D22	Military
	CY7C191–15KMB	K74	
	CY7C191–15LMB	L54	
20	CY7C191–20DC	D22	Commercial
	CY7C191–20LC	L54	
	CY7C191–20PC	P21	
	CY7C191–20VC	V21	
	CY7C191–20DMB	D22	Military
	CY7C191–20KMB	K74	
	CY7C191–20LMB	L54	

Shaded area contains advanced information.

Speed (ns)	Ordering Code	Package Type	Operating Range
25	CY7C191–25DC	D22	Commercial
	CY7C191–25LC	L54	
	CY7C191–25PC	P21	
	CY7C191–25VC	V21	
	CY7C191–25DMB	D22	Military
	CY7C191–25KMB	K74	
	CY7C191–25LMB	L54	
35	CY7C191–35DC	D22	Commercial
	CY7C191–35LC	L54	
	CY7C191–35PC	P21	
	CY7C191–35VC	V21	
	CY7C191–35DMB	D22	Military
	CY7C191–35KMB	K74	
	CY7C191–35LMB	L54	
45	CY7C191–45DC	D22	Commercial
	CY7C191–45LC	L54	
	CY7C191–45PC	P21	
	CY7C191–45VC	V21	
	CY7C191–45DMB	D22	Military
	CY7C191–45KMB	K74	
	CY7C191–45LMB	L54	

Ordering Information (continued)

Speed (ns)	Ordering Code	Package Type	Operating Range
12	CY7C192–12DC	D22	Commercial
	CY7C192–12LC	L54	
	CY7C192–12PC	P21	
	CY7C192–12VC	V21	
15	CY7C192–15DC	D22	Commercial
	CY7C192–15LC	L54	
	CY7C192–15PC	P21	
	CY7C192–15VC	V21	
	CY7C192–15DMB	D22	Military
	CY7C192–15KMB	K74	
	CY7C192–15LMB	L54	
20	CY7C192–20DC	D22	Commercial
	CY7C192–20LC	L54	
	CY7C192–20PC	P21	
	CY7C192–20VC	V21	
	CY7C191–20DMB	D22	Military
	CY7C191–20KMB	K74	
	CY7C191–20LMB	L54	
25	CY7C192–25DC	D22	Commercial
	CY7C192–25LC	L54	
	CY7C192–25PC	P21	
	CY7C192–25VC	V21	
	CY7C192–25DMB	D22	Military
	CY7C192–25KMB	K74	
	CY7C192–25LMB	L54	
35	CY7C192–35DC	D22	Commercial
	CY7C192–35LC	L54	
	CY7C192–35PC	P21	
	CY7C192–35VC	V21	
	CY7C192–35DMB	D22	Military
	CY7C192–35KMB	K74	
	CY7C192–35LMB	L54	
45	CY7C192–45DC	D22	Commercial
	CY7C192–45LC	L54	
	CY7C192–45PC	P21	
	CY7C192–45VC	V21	
	CY7C192–45DMB	D22	Military
	CY7C192–45KMB	K74	
	CY7C192–45LMB	L54	

Shaded area contains advanced information.

MILITARY SPECIFICATIONS

Group A Subgroup Testing

DC Characteristics

Parameters	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL} Max.	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB1}	1, 2, 3
I_{SB2}	1, 2, 3

Switching Characteristics

Parameters	Subgroups
READ CYCLE	
t_{RC}	7, 8, 9, 10, 11
t_{AA}	7, 8, 9, 10, 11
t_{OHA}	7, 8, 9, 10, 11
t_{ACE}	7, 8, 9, 10, 11
WRITE CYCLE	
t_{WC}	7, 8, 9, 10, 11
t_{SCE}	7, 8, 9, 10, 11
t_{AW}	7, 8, 9, 10, 11
t_{HA}	7, 8, 9, 10, 11
t_{SA}	7, 8, 9, 10, 11
t_{PWE}	7, 8, 9, 10, 11
t_{SD}	7, 8, 9, 10, 11
t_{HD}	7, 8, 9, 10, 11
t_{AWE}[13]	7, 8, 9, 10, 11
t_{ADV}[13]	7, 8, 9, 10, 11

Note:
13. 7C191 only

Document #: 38–00076–G