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NVT224

dbCOOL™ Remote Thermal Monitor and Fan Controller

The NVT224 dbCOOL controller is a thermal monitor and multiple PWM fan controller for noise−sensitive or power−sensitive applications requiring active system cooling. The NVT224 can drive a fan using either a low or high frequency drive signal, monitor the temperature of up to two remote sensor diodes plus its own internal temperature, and measure and control the speed of up to four fans so that they operate at the lowest possible speed for minimum acoustic noise.

The automatic fan speed control loop optimizes fan speed for a given temperature. The effectiveness of the system's thermal solution can be monitored using the $\overline{\text{THERM}}$ input. The NVT224 also provides critical thermal protection to the system using the bidirectional $\overline{\text{THERM}}$ pin as an output to prevent system or component overheating.

The NVT224 has been through Automotive Qualification according to AEC−Q100 Grade 1 standards.

Features

- Controls and Monitors Up to 4 Fans
- High and Low Frequency Fan Drive Signal
- 1 On−Chip and 2 Remote Temperature Sensors
- Extended Temperature Measurement Range, Up to 191°C
- Automatic Fan Speed Control Mode Controls System Cooling Based on Measured Temperature
- Enhanced Acoustic Mode Dramatically Reduces User Perception of Changing Fan Speeds
- Thermal Protection Feature via $\overline{\text{THERM}}$ Output
- Monitors Performance Impact of Intel Pentium® 4 Processor
- Thermal Control Circuit via $\overline{\text{THERM}}$ Input
- 3−Wire and 4−Wire Fan Speed Measurement
- Limit Comparison of All Monitored Values
- Meets SMBus 2.0 Electrical Specifications (Fully SMBus 1.1 Compliant)
- Automotive Qualification According to AEC−Q100 Grade 1
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

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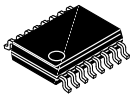
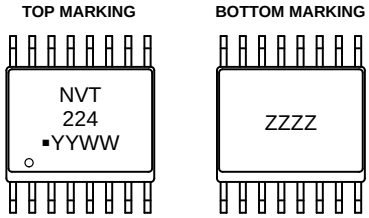


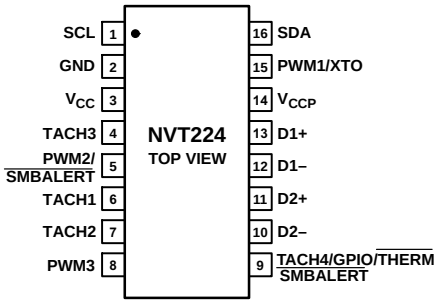
QSOP−16
CASE 492

MARKING DIAGRAMS



NVT224 = Specific Device Code
▪ = Pb−Free Package
YY = Year
WW = Work Week
ZZZZ = Assembly Lot Code

PIN ASSIGNMENT



ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 57 of this data sheet.

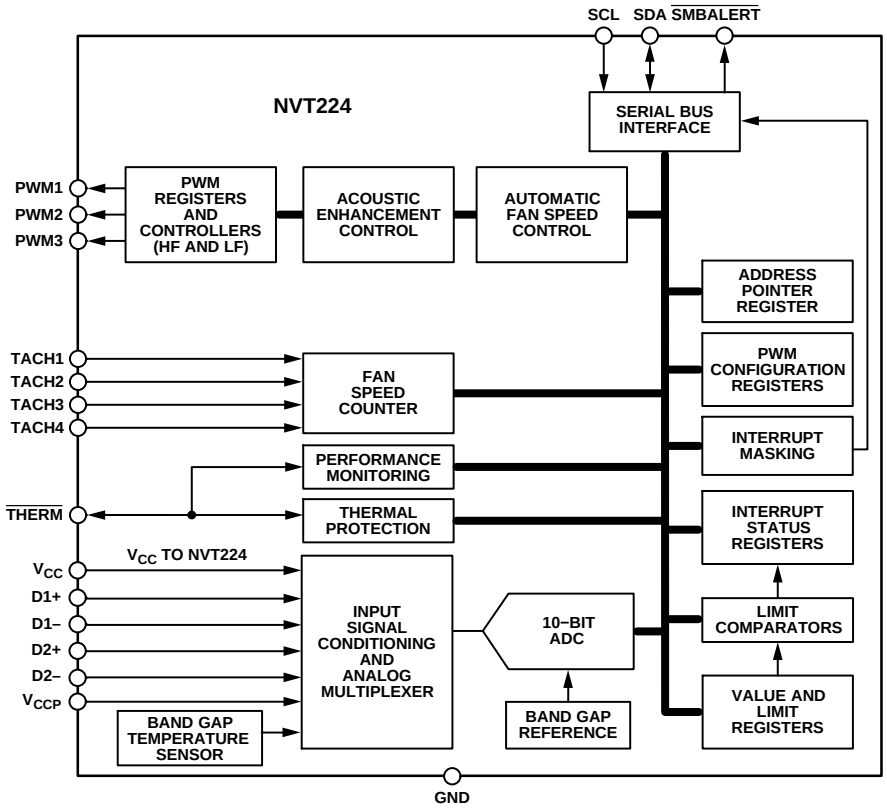


Figure 1. Functional Block Diagram

ABSOLUTE MAXIMUM RATINGS

Parameter	Rating	Unit
Positive Supply Voltage (V_{CC})	3.6	V
Voltage on Any Input or Output Pin	−0.3 to +3.6	V
Input Current at Any Pin	±5	mA
Package Input Current	±20	mA
Maximum Junction Temperature (T_{JMAX})	150	°C
Storage Temperature Range	−65 to +150	°C
Lead Temperature, Soldering IR Reflow Peak Temperature Lead Temperature (Soldering, 10 sec)	 260 300	°C
ESD Rating Human Body Model Machine Model Charged Device Model	 1000 100 1000	V

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

NOTE: This device is ESD sensitive. Use standard ESD precautions when handling.

THERMAL CHARACTERISTICS

Package Type	θ_{JA}	θ_{JC}	Unit
16−lead QSOP	150	39	°C/W

1. θ_{JA} is specified for the worst−case conditions, that is, a device soldered in a circuit board for surface−mount packages.

PIN ASSIGNMENT

Pin No.	Mnemonic	Description
1	SCL	Digital Input (Open Drain). SMBus serial clock input. Requires SMBus pullup.
2	GND	Ground Pin.
3	VCC	Power Supply. VCC is also monitored through this pin.
4	TACH3	Digital Input (Open Drain). Fan tachometer input to measure speed of Fan 3.
5	PWM2	PWM2: Digital Output (Open Drain). Requires 10 kΩ typical pullup. Pulse−width modulated output to control Fan 2 speed. Can be configured as a high or low frequency drive.
	$\overline{\text{SMBALERT}}$	$\overline{\text{SMBALERT}}$: Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out−of−limit conditions.
6	TACH1	Digital Input (Open Drain). Fan tachometer input to measure the speed of Fan 1.
7	TACH2	Digital Input (Open Drain). Fan tachometer input to measure the speed of Fan 2.
8	PWM3	Digital I/O (Open Drain). Pulse−width modulated output to control the speed of Fan 3 and Fan 4. Requires 10 kΩ typical pullup. Can be configured as a high or low frequency drive.
9	TACH4 $\overline{\text{THERM}}$	TACH4: Digital Input (Open Drain). Fan tachometer input to measure the speed of Fan 4. $\overline{\text{THERM}}$: Digital I/O (Open Drain). Alternatively, this pin can be reconfigured as a bidirectional $\overline{\text{THERM}}$ pin that can be used to time and monitor assertions on the $\overline{\text{THERM}}$ input. For example, the pin can be connected to the $\overline{\text{PROCHOT}}$ output of an Intel Pentium 4 processor or to the output of a trip point temperature sensor. This pin can be used as an output to signal overtemperature conditions.
	GPIO $\overline{\text{SMBALERT}}$	GPIO: General−Purpose Open Drain Digital I/O. $\overline{\text{SMBALERT}}$: Digital Output (Open Drain). This pin can be reconfigured as an $\overline{\text{SMBALERT}}$ interrupt output to signal out−of−limit conditions.
10	D2−	Cathode Connection to Second Thermal Diode.
11	D2+	Anode Connection to Second Thermal Diode.
12	D1−	Cathode Connection to First Thermal Diode.
13	D1+	Anode Connection to First Thermal Diode.
14	VCCP	Analog Input. Monitors processor core voltage (0 V to 3.0 V).
15	PWM1	Digital Output (Open Drain). Pulse−width modulated output to control Fan 1 speed. Requires 10 kΩ typical pullup.
	XTO	Also functions as the output from the XNOR tree in XNOR test mode.
16	SDA	Digital I/O (Open Drain). SMBus bidirectional serial data. Requires 10 kΩ typical pullup.

ELECTRICAL CHARACTERISTICS $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted. (Note 1)

Parameter	Conditions	Min	Typ	Max	Unit
Power Supply					
Supply Voltage		3.0	3.3	3.6	V
Supply Current, I_{CC}	Interface inactive, ADC active		1.5	3.0	mA
Temperature−to−Digital Converter					
Local Sensor Accuracy Resolution	$0°C \le T_A \le 85°C$ $-40°C \le T_A \le +125°C$		±0.5 0.25	±1.5 ±2.5	°C
Remote Diode Sensor Accuracy Resolution	$0°C \le T_A \le 85°C$ $-40°C \le T_A \le +125°C$		±0.5 0.25	1.5 ±2.5	°C
Remote Sensor Source Current	High level Low level		180 11		μA
ANALOG−TO−DIGITAL CONVERTER (INCLUDING MUX AND ATTENUATORS)					
Total Unadjusted Error (TUE)				±2	%
Differential Non−linearity (DNL)	8 bits			±1	LSB
Power Supply Sensitivity			±0.1		%/V
Conversion Time (Voltage Input)	Averaging enabled		11		ms
Conversion Time (Local Temperature)	Averaging enabled		12		ms
Conversion Time (Remote Temperature)	Averaging enabled		38		ms
Total Monitoring Cycle Time	Averaging enabled Averaging disabled		145 19		ms
Input Resistance	For V_{CCP} channel	70	120		kΩ
FAN RPM−TO−DIGITAL CONVERTER					
Accuracy	$0°C \le T_A \le 70°C$ $-40°C \le T_A \le +120°C$			±6 ±10	%
Full−Scale Count				65,535	
Nominal Input RPM	Fan count = 0xBFFF Fan count = 0x3FFF Fan count = 0x0438 Fan count = 0x021C		109 329 5000 10,000		RPM
OPEN−DRAIN DIGITAL OUTPUTS (PWM1 TO PWM3, XTO)					
Current Sink, I_{OL}				8.0	mA
Output Low Voltage, V_{OL}	$I_{OUT} = -8.0$ mA			0.4	V
High Level Output Current, I_{OH}	$V_{OUT} = V_{CC}$		0.1	20	μA
OPEN−DRAIN SERIAL DATA BUS OUTPUT (SDA)					
Output Low Voltage, V_{OL}	$I_{OUT} = -4.0$ mA			0.4	V
High Level Output Current, I_{OH}	$V_{OUT} = V_{CC}$		0.1	1.0	μA
SMBus DIGITAL INPUTS (SCL, SDA)					
Input High Voltage, V_{IH}		2.0			V
Input Low Voltage, V_{IL}				0.4	V
Hysteresis			500		mV
DIGITAL INPUT LOGIC LEVELS (TACH INPUTS)					
Input High Voltage, V_{IH}	Maximum input voltage	2.0		3.6	V
Input Low Voltage, V_{IL}	Minimum input voltage	−0.3		0.8	V
Hysteresis			0.5		V p−p

1. All voltages are measured with respect to GND, unless otherwise specified. Typicals are at $T_A = 25°C$ and represent the most likely parametric norm. Logic inputs accept input high voltages of up to V_{MAX}, even when the device is operating down to V_{MIN}. Timing specifications are tested at logic levels of $V_{IL} = 0.8$ V for a falling edge and $V_{IH} = 2.0$ V for a rising edge.
2. SMBus timing specifications are guaranteed by design and are not production tested.

ELECTRICAL CHARACTERISTICS $T_A = T_{MIN}$ to T_{MAX}, $V_{CC} = V_{MIN}$ to V_{MAX}, unless otherwise noted. (Note 1)

Parameter	Conditions	Min	Typ	Max	Unit
DIGITAL INPUT LOGIC LEVELS ($\overline{\text{THERM}}$) ADTL+					
Input High Voltage, V_{IH}		0.75 x V_{CC}			V
Input Low Voltage, V_{IL}				0.8	V
DIGITAL INPUT CURRENT					
Input High Current, I_{IH}	$V_{IN} = V_{CC}$		±1		μA
Input Low Current, I_{IL}	$V_{IN} = 0$ V		±1		μA
Input Capacitance, C_{IN}			5		pF
SERIAL BUS TIMING	See Note 2 and Figure 2				
Clock Frequency, f_{SCLK}		10		400	kHz
Glitch Immunity, t_{SW}				50	ns
Bus Free Time, t_{BUF}		4.7			μs
SCL Low Time, t_{LOW}		4.7			μs
SCL High Time, t_{HIGH}		4.0		50	μs
SCL, SDA Rise Time, t_R				1000	ns
SCL, SDA Fall Time, t_F				300	ns
Data Setup Time, $t_{SU: DAT}$		250			ns
Detect Clock Low Timeout, $t_{TIMEOUT}$	Can be optionally disabled	15		35	ms

1. All voltages are measured with respect to GND, unless otherwise specified. Typicals are at $T_A = 25°C$ and represent the most likely parametric norm. Logic inputs accept input high voltages of up to V_{MAX}, even when the device is operating down to V_{MIN}. Timing specifications are tested at logic levels of $V_{IL} = 0.8$ V for a falling edge and $V_{IH} = 2.0$ V for a rising edge.
2. SMBus timing specifications are guaranteed by design and are not production tested.

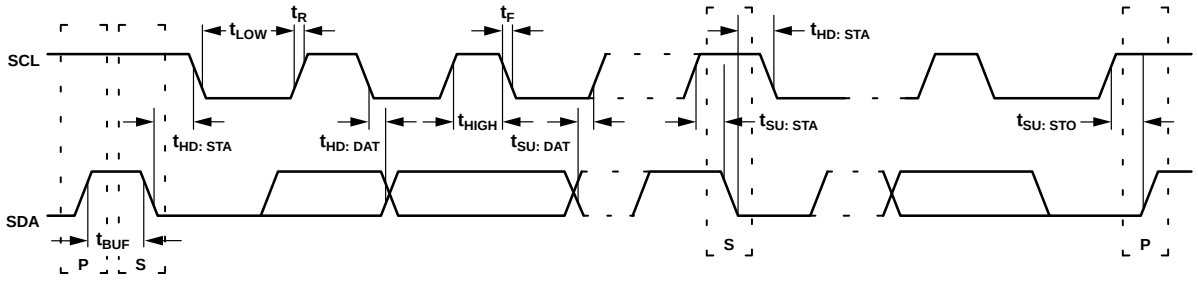


Figure 2. Serial Bus Timing Diagram

TYPICAL PERFORMANCE CHARACTERISTICS

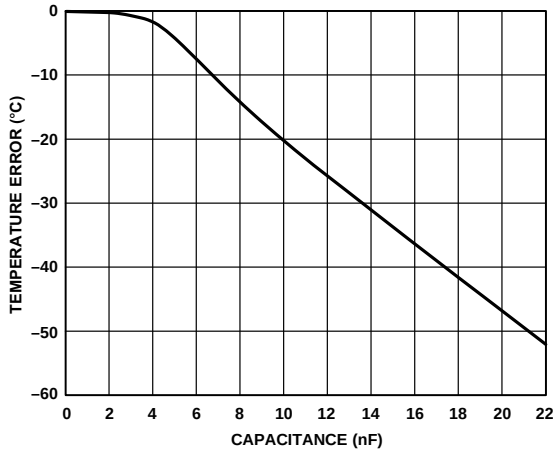


Figure 3. Temperature Error vs. Capacitance Between D+ and D−

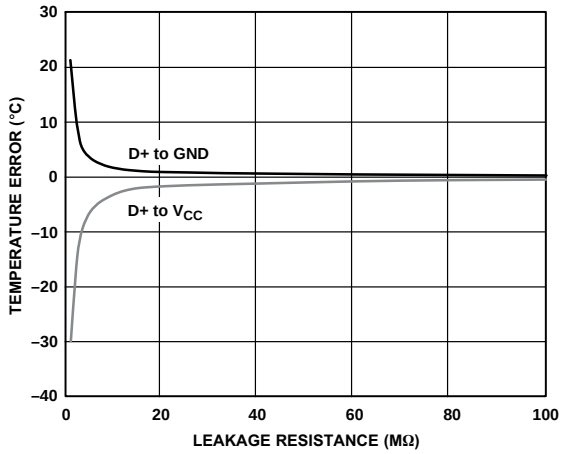


Figure 4. Remote Temperature Error vs. PCB Resistance

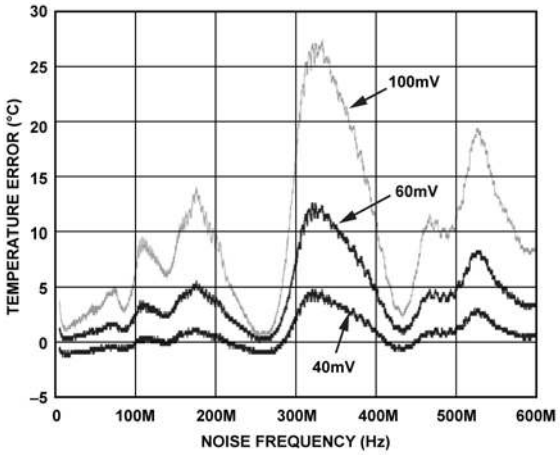


Figure 5. Remote Temperature Error vs. Common−Mode Noise Frequency

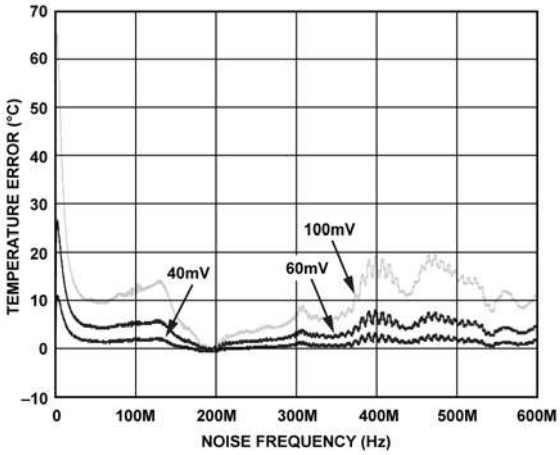


Figure 6. Remote Temperature Error vs. Differential Mode Noise Frequency

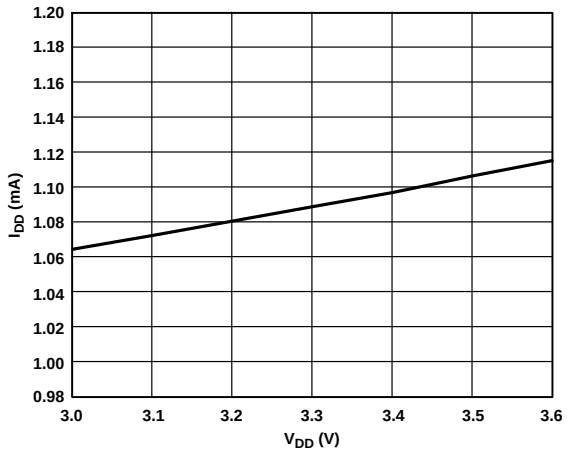


Figure 7. Normal I_{DD} vs. Power Supply

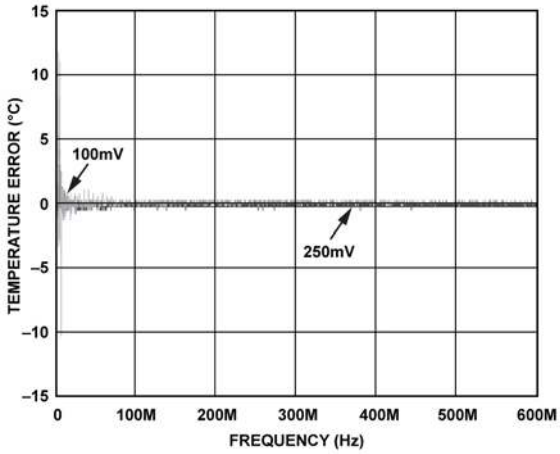


Figure 8. Internal Temperature Error vs. Power Supply Noise

TYPICAL PERFORMANCE CHARACTERISTICS

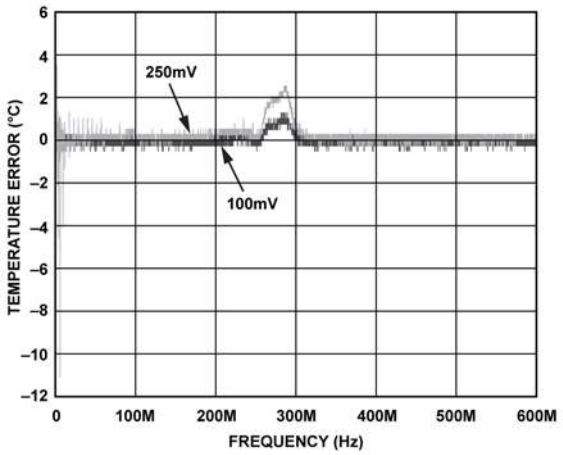


Figure 9. Remote Temperature Error vs. Power Supply Noise Frequency

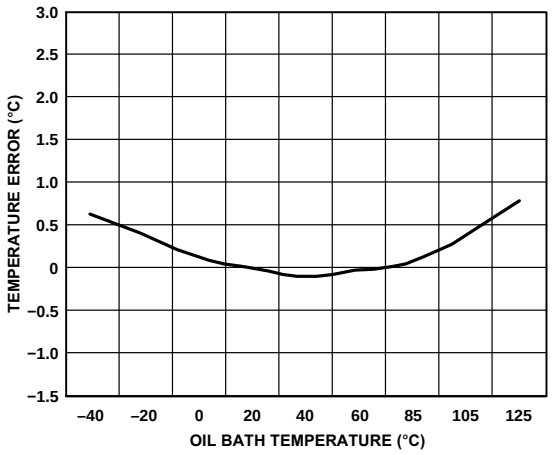


Figure 10. Internal Temperature Error vs. NVT224 Temperature

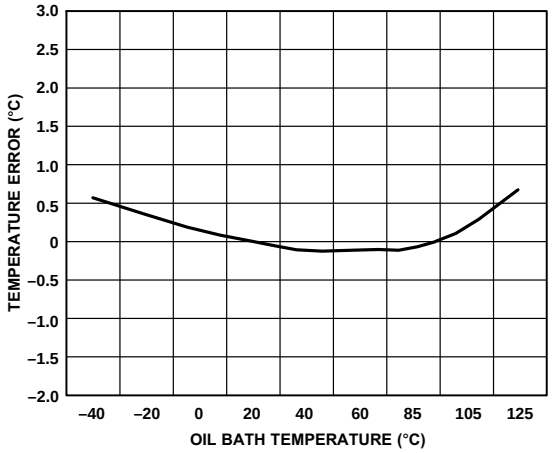


Figure 11. Remote Temperature Error vs. NVT224 Temperature

Product Description

The NVT224 is a complete thermal monitor and multiple fan controller for any system requiring thermal monitoring and cooling. The device communicates with the system via a serial system management bus. The serial bus controller has a serial data line for reading and writing addresses and data (Pin 16), and an input line for the serial clock (Pin 1). All control and programming functions for the NVT224 are performed over the serial bus. In addition, a pin can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out−of−limit conditions.

Quick Comparison Between ADT7473 and NVT224

- The ADT7473 supports advanced dynamic T_{MIN} features while the NVT224 does not.
- Acoustic smoothing is improved on the NVT224.
- $\overline{\text{THERM}}$ can be selected as an output only on the NVT224.
- The NVT224 has two additional configuration registers.
- The NVT224 has other minor register changes.

The NVT224 is similar to the ADT7473 in that it is powered by a supply no greater than 3.6 V. Exceeding this specification results in irreversible damage to the NVT224. Signal pins (TACH/PWM) should be pulled up or clamped to 3.6 V maximum. See the Specifications Section for more information.

Recommended Implementation

Configuring the NVT224 as shown in Figure 12 allows the system designer to use the following features:

- Two PWM outputs for fan control of up−to−three fans (the front and rear chassis fans are connected in parallel).
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 3.
- CPU temperature measured using the Remote 1 temperature channel.
- Ambient temperature measured through the Remote 2 temperature channel.
- Bidirectional $\overline{\text{THERM}}$ pin. This feature allows Intel Pentium 4 $\overline{\text{PROCHOT}}$ monitoring and can function as an overtemperature $\overline{\text{THERM}}$ output. The $\overline{\text{THERM}}$ pin can alternatively be programmed as an $\overline{\text{SMBALERT}}$ system interrupt output.

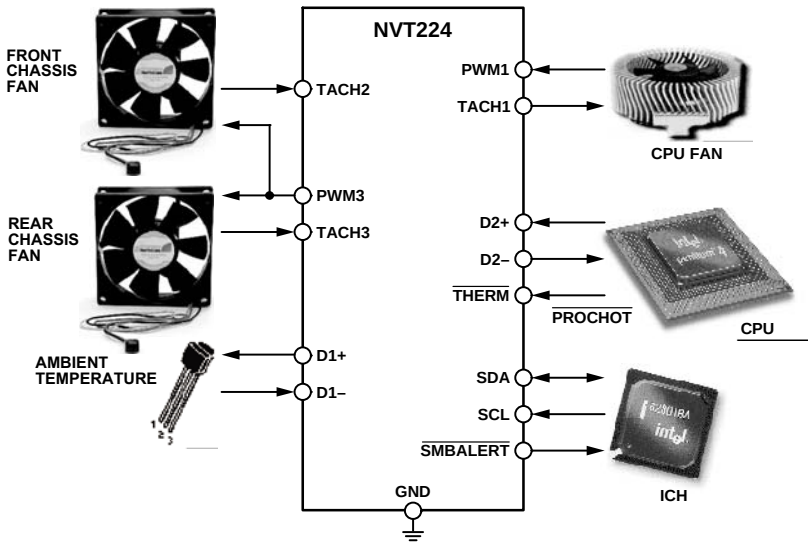


Figure 12. NVT224 Configuration

Serial Bus Interface

On PCs and servers, control of the NVT224 is carried out using the SMBus. The NVT224 is connected to this bus as a slave device under the control of a master controller, which is usually (but not necessarily) the ICH.

The NVT224 has a fixed 7−bit serial bus address of 0101110 or 0x2E. The read/write bit must be added to get the 8−bit address (01011100 or 0x5C). Data is sent over the serial bus in sequences of nine clock pulses, that is, eight bits of data followed by an acknowledge bit from the slave device. Transitions on the data line must occur during the low period of the clock signal and remain stable during the high period because a low−to−high transition when the clock is high may be interpreted as a stop signal. The number of data bytes that can be transmitted over the serial bus in a single read or write operation is limited only by what the master and slave devices can handle.

When all data bytes are read or written, stop conditions are established. In write mode, the master pulls the data line high during the tenth clock pulse to assert a stop condition. In read mode, the master device overrides the acknowledge bit by pulling the data line high during the low period before the ninth clock pulse; this is known as no acknowledge. The master takes the data line low during the low period before

the tenth clock pulse, and then high during the tenth clock pulse to assert a stop condition.

Any number of bytes of data can be transferred over the serial bus in one operation, but it is not possible to mix read and write in one operation because the type of operation is determined at the beginning and cannot subsequently be changed without starting a new operation.

In the NVT224, write operations contain either one or two bytes, and read operations contain one byte. To write data to one of the device data registers or read data from it, the address pointer register must be set so that the correct data register is addressed, and then data can be written to that register or read from it. The first byte of a write operation always contains an address that is stored in the address pointer register. If data is to be written to the device, the write operation contains a second data byte that is written to the register selected by the address pointer register.

This write operation is shown in Figure 13. The device address is sent over the bus, and then R/$\overline{W}$ is set to 0. This is followed by two data bytes. The first data byte is the address of the internal data register to write to, which is stored in the address pointer register. The second data byte is the data to write to the internal data register.

When reading data from a register, there are two possibilities:

- If the NVT224 address pointer register value is unknown or not the desired value, it must first be set to the correct value before data can be read from the desired data register. This is done by performing a write to the NVT224 as before, but only the data byte containing the register address is sent, because no data is written to the register see Figure 14.
  A read operation is then performed consisting of the serial bus address; the R/$\overline{W}$ bit set to 1, followed by the data byte read from the data register see Figure 15.
- If the address pointer register is known to be already at the desired address, data can be read from the corresponding data register without first writing to the address pointer register see Figure 15.

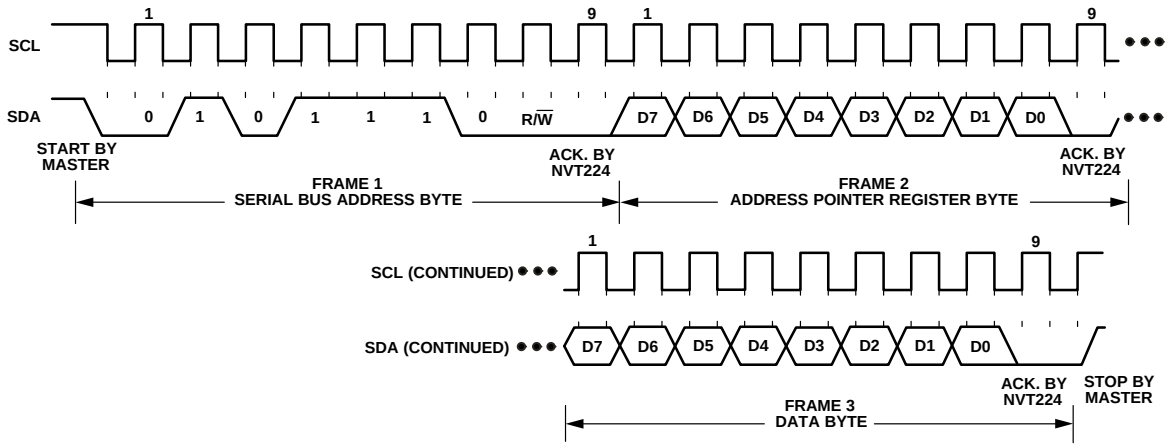


Figure 13. Writing a Register Address to the Address Pointer Register, then Writing Data to the Selected Register

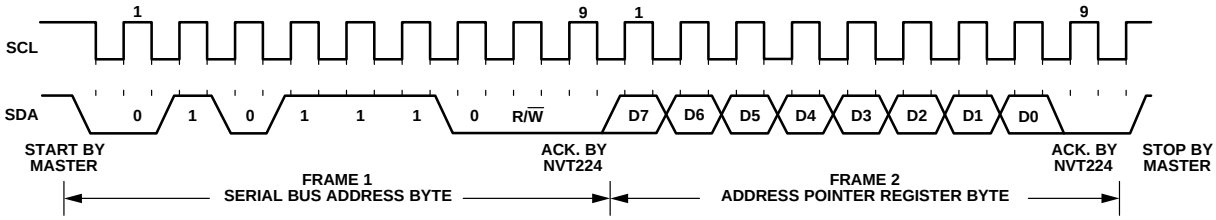


Figure 14. Writing to the Address Pointer Register Only

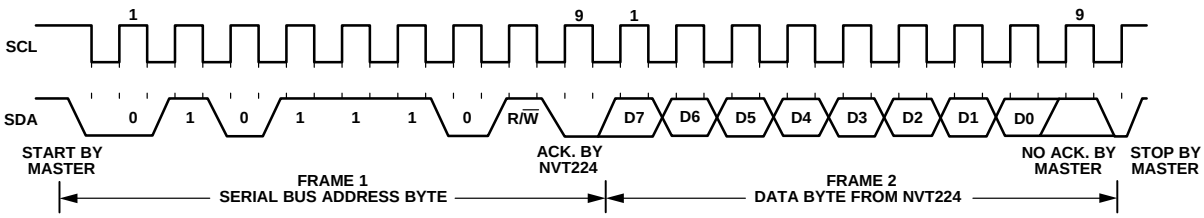


Figure 15. Reading Data from a Previously Selected Register

It is possible to read a data byte from a data register without first writing to the address pointer register if the address pointer register is already at the correct value. However, it is not possible to write data to a register without writing to the address pointer register because the first data byte of a write is always written to the address pointer register.

In addition to supporting the send byte and receive byte protocols, the NVT224 also supports the read byte protocol (for more information, see System Management Bus Specifications Rev. 2.0, available from Intel).

If several read or write operations must be performed in succession, the master can send a repeat start condition instead of a stop condition to begin a new operation.

Write Operations

The SMBus specification defines several protocols for different types of read and write operations. The ones used in the NVT224 are discussed in this section. The following abbreviations are used in the diagrams:

S—Start
P—Stop
R—Read
W—Write
A—Acknowledge
$\overline{A}$—No acknowledge

The NVT224 uses the following SMBus write protocols.

Send Byte

In this operation, the master device sends a single command byte to a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master asserts a stop condition on SDA and the transaction ends.

For the NVT224, the send byte protocol is used to write a register address to RAM for a subsequent single−byte read from the same address. This operation is shown in Figure 16.

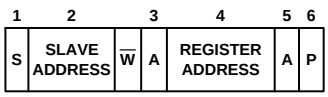


Figure 16. Setting a Register Address for Subsequent Read

If the master is required to read data from the register immediately after setting up the address, it can assert a repeat start condition immediately after the final ACK and carry out a single−byte read without asserting an intermediate stop condition.

Write Byte

In this operation, the master device sends a command byte and one data byte to the slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the write bit (low).
3. The addressed slave device asserts ACK on SDA.
4. The master sends a command code.
5. The slave asserts ACK on SDA.
6. The master sends a data byte.
7. The slave asserts ACK on SDA.
8. The master asserts a stop condition on SDA and the transaction ends.

The byte write operation is shown in Figure 17.

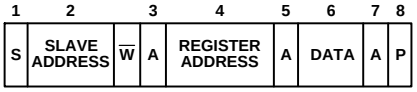


Figure 17. Single−Byte Write to a Register

Read Operations

The NVT224 uses the following SMBus read protocols.

Receive Byte

This operation is useful when repeatedly reading a single register. The register address must be set up previously. In this operation, the master device receives a single byte from a slave device as follows:

1. The master device asserts a start condition on SDA.
2. The master sends the 7−bit slave address followed by the read bit (high).
3. The addressed slave device asserts ACK on SDA.
4. The master receives a data byte.
5. The master asserts NO ACK on SDA.
6. The master asserts a stop condition on SDA, and the transaction ends.

In the NVT224, the receive byte protocol is used to read a single byte of data from a register whose address has previously been set by a send byte or write byte operation. This operation is shown in Figure 18.

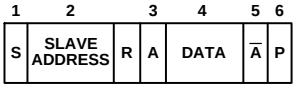


Figure 18. Single−Byte Read from a Register

Alert Response Address

Alert response address (ARA) is a feature of SMBus devices that allows an interrupting device to identify itself to the host when multiple devices exist on the same bus.

The $\overline{\text{SMBALERT}}$ output can be used as either an interrupt output or an $\overline{\text{SMBALERT}}$. One or more outputs can be

connected to a common $\overline{\text{SMBALERT}}$ line connected to the master. If a device's $\overline{\text{SMBALERT}}$ line goes low, the following events occur:

1. $\overline{\text{SMBALERT}}$ is pulled low.
2. The master initiates a read operation and sends the alert response address (ARA = 0001 100). This general call address must not be used as a specific device address.
3. The device whose $\overline{\text{SMBALERT}}$ output is low responds to the alert response address, and the master reads its device address. The address of the device is now known and can be interrogated in the usual way.
4. If more than one device's $\overline{\text{SMBALERT}}$ output is low, the one with the lowest device address has priority in accordance with normal SMBus arbitration.
5. Once the NVT224 has responded to the alert response address, the master must read the status registers, and the $\overline{\text{SMBALERT}}$ is cleared only if the error condition has gone away.

SMBus Timeout

The NVT224 includes an SMBus timeout feature. If there is no SMBus activity for 35 ms, the NVT224 assumes that the bus is locked and releases the bus. This prevents the device from locking or holding the SMBus expecting data. Some SMBus controllers cannot handle the SMBus timeout feature, so it can be disabled.

Configuration Register 1 (0x40)

Bit 6 TODIS = 0; SMBus timeout enabled (default).

Bit 6 TODIS = 1; SMBus timeout disabled.

Virus Protection

To prevent rogue programs or viruses from accessing critical NVT224 register settings, the lock bit can be set. Setting Bit 1 of Configuration Register 1 (0x40) sets the lock bit and locks critical registers. In this mode, certain registers can no longer be written to until the NVT224 is powered down and powered up again. For more information on which registers are locked, see the Register Tables section.

Voltage Measurement Input

The NVT224 has one external voltage measurement channel. It can also measure its own supply voltage, V_{CC}. Pin 14 can measure V_{CCP}. The V_{CC} supply voltage measurement is carried out through the V_{CC} pin (Pin 3). The V_{CCP} input can be used to monitor a chipset supply voltage in computer systems.

Analog−to−Digital Converter

All analog inputs are multiplexed into the on−chip, successive approximation, analog−to−digital converter. This has a resolution of 10 bits. The basic input range is 0 V to 2.25 V, but the input has built−in attenuators to allow measurement of V_{CCP} without any external components. To allow for the tolerance of the supply voltage, the ADC produces an output of 3/4 full scale (decimal 768 or 300 hex) for the nominal input voltage and so has adequate headroom to deal with overvoltages.

Input Circuitry

The internal structure for the V_{CCP} analog input is shown in Figure 19. The input circuit consists of an input protection diode, an attenuator, and a capacitor to form a first−order, low−pass filter that gives the input immunity to high frequency noise.

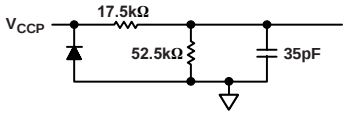


Figure 19. Structure of Analog Inputs

Voltage Measurement Registers

Register 0x21, V_{CCP} Reading = 0x00 default

Register 0x22, V_{CC} Reading = 0x00 default

V_{CCP} Limit Registers

Associated with the V_{CCP} measurement channel is a high and low limit register. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts.

Register 0x46, V_{CCP} Low Limit = 0x00 default

Register 0x47, V_{CCP} High Limit = 0xFF default

Table 2 shows the input ranges of the analog inputs and output codes of the 10−bit ADC.

When the ADC is running, it samples and converts a voltage input in 711 μs and averages 16 conversions to reduce noise; a measurement takes nominally 11.38 ms.

Extended Resolution Registers

Voltage measurements can be made with higher accuracy using the extended resolution registers (0x76 and 0x77). Whenever the extended resolution registers are read, the corresponding data in the voltage measurement registers is locked until their data is read. That is, if extended resolution is required, then the extended resolution register must be read first, immediately followed by the appropriate voltage measurement register.

Additional ADC Functions for Voltage Measurements

A number of other functions are available on the NVT224 to offer the system designer increased flexibility.

Turn−Off Averaging

For each voltage measurement read from a value register, 16 readings have been made internally, and the results averaged, before being placed into the value register. For instances where faster conversions are needed, setting Bit 4 of Configuration Register 2 (0x73) turns averaging off.

This effectively gives a reading 16 times faster (711 μs), but the reading may be noisier.

Bypass Voltage Input Attenuator

Setting Bit 5 of Configuration Register 2 (0x73) removes the attenuation circuitry from the V_{CCP} input. This allows the user to directly connect external sensors or to rescale the analog voltage measurement inputs for other applications. The input range of the ADC without the attenuators is 0 V to 2.25 V.

Single−Channel ADC Conversion

Setting Bit 6 of Configuration Register 2 (0x73) places the NVT224 into single−channel ADC conversion mode. In this mode, the NVT224 can be made to read a single voltage channel only. If the internal NVT224 clock is used, the selected input is read every 711 μs. The appropriate ADC channel is selected by writing to Bits [7:5] of the TACH1 minimum high byte register (0x55).

Table 1. Single−Channel ADC Conversion

Register 0x55, Bits [7:5]	Channel Selected
001	V_{CCP}
010	V_{CC}
101	Remote 1 Temperature
110	Local Temperature
111	Remote 2 Temperature

Configuration Register 2 (0x73)

Bit 4 = 1; averaging off.

Bit 5 = 1; bypass input attenuators.

Bit 6 = 1; single−channel convert mode.

TACH1 Minimum High Byte (0x55)

Bits [7:5] select the ADC channel for single−channel convert mode.

Table 2. 10−Bit ADC Output Code vs. V_{IN}

ADC Output			
V_{CC} (3.3 V_{IN}) (Note 1)	**V_{CCP}**	**Decimal**	**Binary (10 Bits)**
<0.0042	<0.00293	0	00000000 00
0.0042 to 0.0085	0.0293 to 0.0058	1	00000000 01
0.0085 to 0.0128	0.0058 to 0.0087	2	00000000 10
0.0128 to 0.0171	0.0087 to 0.0117	3	00000000 11
0.0171 to 0.0214	0.0117 to 0.0146	4	00000001 00
0.0214 to 0.0257	0.0146 to 0.0175	5	00000001 01
0.0257 to 0.0300	0.0175 to 0.0205	6	00000001 10
0.0300 to 0.0343	0.0205 to 0.0234	7	00000001 11
0.0343 to 0.0386	0.0234 to 0.0263	8	00000010 00
–	–	–	–
1.100 to 1.1042	0.7500 to 0.7529	256 (1/4 scale)	01000000 00
–	–	–	–
2.200 to 2.2042	1.5000 to 1.5029	512 (1/2 scale)	10000000 00
–	–	–	–
3.300 to 3.3042	2.2500 to 2.2529	768 (3/4 scale)	11000000 00
–	–	–	–
4.3527 to 4.3570	2.9677 to 2.9707	1013	11111101 01
4.3570 to 4.3613	2.9707 to 2.9736	1014	11111101 10
4.3613 to 4.3656	2.9736 to 2.9765	1015	11111101 11
4.3656 to 4.3699	2.9765 to 2.9794	1016	11111110 00
4.3699 to 4.3742	2.9794 to 2.9824	1017	11111110 01
4.3742 to 4.3785	2.9824 to 2.9853	1018	11111110 10
4.3785 to 4.3828	2.9853 to 2.9882	1019	11111110 11
4.3828 to 4.3871	2.9882 to 2.9912	1020	11111111 00
4.3871 to 4.3914	2.9912 to 2.9941	1021	11111111 01
4.3914 to 4.3957	2.9941 to 2.9970	1022	11111111 10
>4.3957	>2.9970	1023	11111111 11

1. The V_{CC} output codes listed assume that V_{CC} is 3.3 V and that V_{CC} should never exceed 3.6 V.

Temperature Measurement Method

Local Temperature Measurement

The NVT224 contains an on−chip band gap temperature sensor whose output is digitized by the on−chip, 10−bit ADC. The 8−bit MSB temperature data is stored in the temperature registers (0x25, 0x26, and 0x27). Because both positive and negative temperatures can be measured, the temperature data is stored in Offset 64 format or twos complement format, as shown in Table 3 and Table 4.

Theoretically, the temperature sensor and ADC can measure temperatures from −128°C to +127°C (or −64°C to +191°C in the extended temperature range) with a resolution of 0.25°C.

However, this exceeds the operating temperature range of the device, so local temperature measurements outside the NVT224 operating temperature range are not possible.

Remote Temperature Measurement

The NVT224 can measure the temperature of two remote diode sensors or diode−connected transistors connected to Pin 10 and Pin 11 or to Pin 12 and Pin 13.

The forward voltage of a diode or diode−connected transistor operated at a constant current exhibits a negative temperature coefficient of about –2 mV/°C. Because the absolute value of V_{BE} varies from device to device and individual calibration is required to null this out, the technique is unsuitable for mass production.

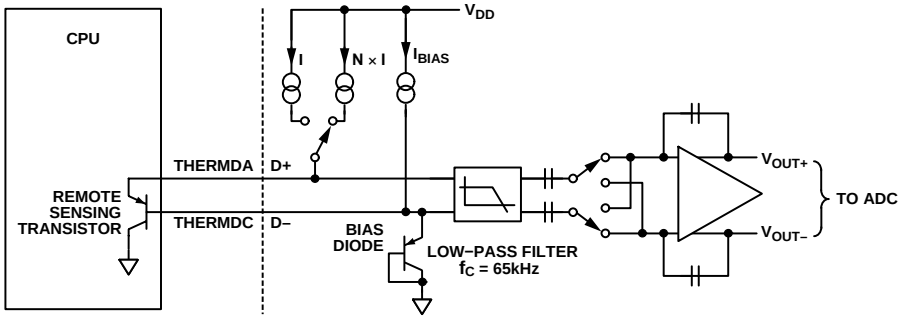


Figure 20. Signal Conditioning for Remote Diode Temperature Sensors

The technique used in the NVT224 is to measure the change in V_{BE} when the device is operated at two different currents.

This is given by:

$$\Delta V_{BE} = kT/q \times \ln(N) \quad \text{(eq. 1)}$$

where:

k is Boltzmann's constant.

q is the charge on the carrier.

T is the absolute temperature in Kelvin.

N is the ratio of the two currents.

Figure 20 shows the input signal conditioning used to measure the output of a remote temperature sensor. This figure shows the external sensor as a substrate transistor, provided for temperature monitoring on some microprocessors. It could also be a discrete transistor such as a 2N3904/2N3906.

If a discrete transistor is used, the collector is not grounded and should be linked to the base. If a PNP transistor is used, the base is connected to the D input and the emitter to the D+ input. If an NPN transistor is used, the emitter is connected to the D input and the base to the D+ input. Figure 21 and Figure 22 show how to connect the NVT224 to an NPN or PNP transistor for temperature measurement. To prevent ground noise from interfering with the measurement, the more negative terminal of the sensor is not referenced to ground but is biased above ground by an internal diode at the D input.

To measure ΔV_{BE}, the sensor is switched between operating currents of I and N x I. The resulting waveform is passed through a 65 kHz low−pass filter to remove noise and to a chopper stabilized amplifier that performs the functions of amplification and rectification of the waveform to produce a dc voltage proportional to ΔV_{BE}. This voltage is measured by the ADC to give a temperature output in 10−bit, twos complement format. To further reduce the effects of noise, digital filtering is performed by averaging the results of 16 measurement cycles.

A remote temperature measurement takes nominally 38 ms. The results of remote temperature measurements are stored in 10−bit, twos complement format, as shown in Table 3. The extra resolution for the temperature measurements is held in the Extended Resolution Register 2 (0x77). This gives temperature readings with a resolution of 0.25°C.

Noise Filtering

For temperature sensors operating in noisy environments, previous practice was to place a capacitor across the D+ pin and D− pin to help combat the effects of noise. However, large capacitance's affect the accuracy of the temperature measurement, leading to a recommended maximum capacitor value of 1000 pF.

This capacitor reduces the noise but does not eliminate it. Sometimes, this sensor noise is a problem in a very noisy environment. In most cases, a capacitor is not required

because differential inputs, by their very nature, have a high immunity to noise.

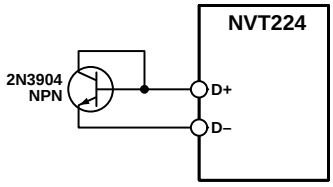


Figure 21. Measuring Temperature Using an NPN Transistor

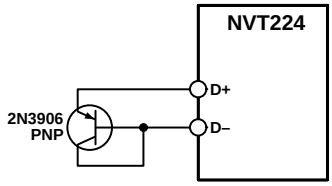


Figure 22. Measuring Temperature Using a PNP Transistor

Factors Affecting Diode Accuracy

Remote Sensing Diode

The NVT224 is designed to work with either substrate transistors built into processors or with discrete transistors. Substrate transistors are generally PNP types with the collector connected to the substrate. Discrete types can be either PNP or NPN transistors connected as a diode (base−shorted to the collector). If an NPN transistor is used, the collector and base are connected to D+ and the emitter to D−. If a PNP transistor is used, the collector and base are connected to D− and the emitter is connected to D+.

To reduce the error due to variations in both substrate and discrete transistors, a number of factors should be taken into consideration:

- The ideality factor, n_f, of the transistor is a measure of the deviation of the thermal diode from ideal behavior. The NVT224 is trimmed for an n_f value of 1.008. Use the following equation to calculate the error introduced at a temperature, T (°C), when using a transistor whose n_f does not equal 1.008. See the processor data sheet for the n_f values.

$$\Delta T = (n_f - 1.008) \times (273.15\ k + T) \qquad \text{(eq. 2)}$$

  To factor this in, the user can write the ΔT value to the offset register. The NVT224 automatically adds it to or subtracts it from the temperature measurement.
- Some CPU manufacturers specify the high and low current levels of the substrate transistors. The high current level of the NVT224, I_{HIGH}, is 180 μA and the low level current, I_{LOW}, is 11 μA. If the NVT224 current levels do not match the current levels specified by the CPU manufacturer, it might be necessary to remove an offset. The CPU's data sheet advises whether this offset needs to be removed and how to calculate it. This offset can be programmed to the offset register. If more than one offset must be considered, the algebraic sum of these offsets must be programmed to the offset register.

If a discrete transistor is used with the NVT224, the best accuracy is obtained by choosing devices according to the following criteria:

- Base−emitter voltage greater than 0.25 V at 11 μA, at the highest operating temperature.
- Base−emitter voltage less than 0.95 V at 180 μA, at the lowest operating temperature.
- Base resistance less than 100 Ω.
- Small variation in h_{FE} (approximately 50 to 150) that indicates tight control of V_{BE} characteristics.

Transistors, such as 2N3904, 2N3906, or equivalents in SOT−23 packages, are suitable devices to use.

Table 3. Twos Complement Temperature Data Format

Temperature	Digital Output (10−Bit) (Note 1)
–128°C	1000 0000 **00** (diode fault)
–63°C	1100 0001 **00**
–50°C	1100 1110 **00**
–25°C	1110 0111 **00**
–10°C	1111 0110 **00**
0°C	0000 0000 **00**
10.25°C	0000 1010 **01**
25.5°C	0001 1001 **10**
50.75°C	0011 0010 **11**
75°C	0100 1011 **00**
100°C	0110 0100 **00**
125°C	0111 1101 **00**
127°C	0111 1111 **00**

1. Bold numbers denote 2 LSBs of measurement in the Extended Resolution Register 2 (0x77) with 0.25°C resolution.

Table 4. Extended Range, Temperature Data Format

Temperature	Digital Output (10−Bit) (Note 1)
–64°C	0000 0000 **00** (diode fault)
–63°C	0000 0001 **00**
–1°C	0011 1111 **00**
0°C	0100 0000 **00**
1°C	0100 0001 **00**
10°C	0100 1010 **00**
25°C	0101 1001 **00**
50°C	0111 0010 **00**
75°C	1000 1001 **00**
100°C	1010 0100 **00**
125°C	1011 1101 **00**
191°C	1111 1111 **00**

1. Bold numbers denote 2 LSBs of measurement in the Extended Resolution Register 2 (0x77) with 0.25°C resolution.

Nulling Out Temperature Errors

As CPUs run faster, it is more difficult to avoid high frequency clocks when routing the D+/D– traces around a system board. Even when recommended layout guidelines are followed, some temperature errors can still be attributable to noise coupled onto the D+/D– lines. Constant high frequency noise usually attenuates, or increases, temperature measurements by a linear, constant value.

The NVT224 has two temperature offset registers, Register 0x70 and Register 0x72, for the Remote 1 and Remote 2 temperature channels. By doing a one−time calibration of the system, the user can determine the offset caused by system board noise and null it out using the offset registers. The offset registers automatically add a twos complement 8−bit reading to every temperature measurement.

Changing Bit 1 of Configuration Register 5 (0x7C) changes the resolution and therefore the range of the temperature offset as either having a range of –63°C to +127°C, with a resolution of 1°C, or having a range of −63°C to +64°C, with a resolution of 0.5°C. This temperature offset can be used to compensate for linear temperature errors introduced by noise.

Temperature Offset Registers

Register 0x70, Remote 1 Temperature Offset = 0x00 (0°C default)

Register 0x71, Local Temperature Offset = 0x00 (0°C default)

Register 0x72, Remote 2 Temperature Offset = 0x00 (0°C default)

ADT7463/NVT224 Backwards Compatible Mode

By setting Bit 0 of Configuration Register 5 (0x7C), all temperature measurements are stored in the zone temperature value registers (0x25, 0x26, and 0x27) in twos complement in the range −128°C to +127°C. The temperature limits must be reprogrammed in twos complement.

If a twos complement temperature below −128°C is entered, the temperature is clamped to −128°C. In this mode, the diode fault condition remains −128°C = 1000 0000, while in the extended temperature range (−64°C to +191°C), the fault condition is represented by −64°C = 0000 0000.

Temperature Measurement Registers

Register 0x25, Remote 1 Temperature
Register 0x26, Local Temperature
Register 0x27, Remote 2 Temperature
Register 0x77, Extended Resolution 2 = 0x00 default
Bits [7:6] TDM2, Remote 2 Temperature LSBs.
Bits [5:4] LTMP, Local Temperature LSBs.
Bits [3:2] TDM1, Remote 1 Temperature LSBs.

Temperature Measurement Limit Registers

Associated with each temperature measurement channel are high and low limit registers. Exceeding the programmed high or low limit causes the appropriate status bit to be set. Exceeding either limit can also generate $\overline{\text{SMBALERT}}$ interrupts (depending on the way the interrupt mask register is programmed and assuming that $\overline{\text{SMBALERT}}$ is set as an output on the appropriate pin).

Register 0x4E, Remote 1 Temperature Low Limit = 0x81 default

Register 0x4F, Remote 1 Temperature High Limit = 0x7F default

Register 0x50, Local Temperature Low Limit = 0x81 default

Register 0x51, Local Temperature High Limit = 0x7F default

Register 0x52, Remote 2 Temperature Low Limit = 0x81 default

Register 0x53, Remote 2 Temperature High Limit = 0x7F default

Reading Temperature from the NVT224

It is important to note that temperature can be read from the NVT224 as an 8−bit value (with 1°C resolution) or as a 10−bit value (with 0.25°C resolution). If only 1°C resolution is required, the temperature readings can be read back at any time and in no particular order.

If the 10−bit measurement is required, this involves a two−register read for each measurement. The Extended Resolution Register 2 (0x77) should be read first. This causes all temperature reading registers to be frozen until all temperature reading registers have been read from. This prevents an MSB reading from being updated while its two LSBs are being read and vice versa.

Additional ADC Functions for Temperature Measurement

A number of other functions are available on the NVT224 to offer the system designer increased flexibility.

Turn−Off Averaging

For each temperature measurement read from a value register, 16 readings have actually been made internally, and the results averaged, before being placed into the value register. Sometimes it is necessary to take a very fast measurement. Setting Bit 4 of Configuration Register 2 (0x73) turns averaging off. The default round−robin cycle time takes 146.5 ms.

Table 5. Conversion Time with Averaging Disabled

Channel	Measurement Time (ms)
Voltage Channels	0.7
Remote Temperature 1	7
Remote Temperature 2	7
Local Temperature	1.3

When Bit 7 of Configuration Register 6 (0x10) is set, the default round−robin cycle time increases to 240 ms.

Table 6. Conversion Time with Averaging Enabled

Channel	Measurement Time (ms)
Voltage Channels	11
Remote Temperature 1	39
Remote Temperature 2	39
Local Temperature	12

Single−Channel ADC Conversions

Setting Bit 6 of Configuration Register 2 (0x73) places the NVT224 into single−channel ADC conversion mode. In this mode, the NVT224 can be made to read a single temperature channel only. The appropriate ADC channel is selected by writing to Bits [7:5] of the TACH1 minimum high byte register (0x55).

Table 7. Programming Single−Channel ADC Mode for Temperatures

Register 0x55, Bits [7:5]	Channel Selected
101	Remote 1 Temperature
110	Local Temperature
111	Remote 2 Temperature

Configuration Register 2 (0x73)

Bit 4 = 1, averaging off.

Bit 6 = 1, single−channel convert mode.

TACH1 Minimum High Byte Register (0x55)

Bits [7:5] select the ADC channel for single−channel convert mode.

Overtemperature Events

Overtemperature events on any of the temperature channels can be detected and dealt with automatically in automatic fan speed control mode. Register 0x6A to Register 0x6C are the $\overline{\text{THERM}}$ temperature limit registers. When a temperature exceeds its $\overline{\text{THERM}}$ temperature limit, all PWM outputs run at the maximum PWM duty cycle (Register 0x38, Register 0x39, and Register 0x3A). This effectively runs the fans at the fastest allowed speed.

The fans run at this speed until the temperature drops below $\overline{\text{THERM}}$ minus hysteresis. This can be disabled by setting the boost bit in Configuration Register 3 (0x78), Bit 2. The hysteresis value for the $\overline{\text{THERM}}$ temperature limit is the value programmed into Register 0x6D and Register 0x6E (hysteresis registers). The default hysteresis value is 4°C.

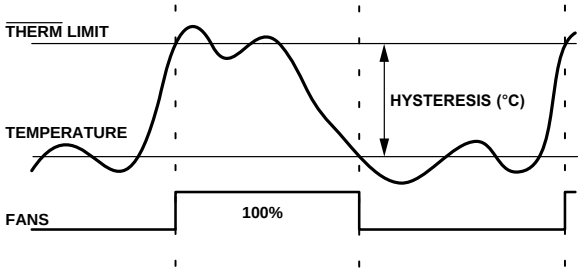


Figure 23. $\overline{\text{THERM}}$ Temperature Limit Operation

$\overline{\text{THERM}}$ can be disabled on specific temperature channels using Bits [7:5] of Configuration Register 5 (0x7C). $\overline{\text{THERM}}$ can also be disabled by:

- In Offset 64 mode, writing −64°C to the appropriate $\overline{\text{THERM}}$ Temperature Limit.
- In twos complement mode, writing −128°C to the appropriate $\overline{\text{THERM}}$ Temperature Limit.

Limits, Status Registers, and Interrupts

Limit Values

Associated with each measurement channel on the NVT224 are high and low limits. These can form the basis of system status monitoring; a status bit can be set for any out−of−limit condition and detected by polling the device. Alternatively, $\overline{\text{SMBALERT}}$ interrupts can be generated to flag out−of−limit conditions to a processor or microcontroller.

8−Bit Limits

The following is a list of 8−bit limits on the NVT224.

Voltage Limit Registers

Register 0x46, V_{CCP} Low Limit = 0x00 default

Register 0x47, V_{CCP} High Limit = 0xFF default

Register 0x48, V_{CC} Low Limit = 0x00 default

Register 0x49, V_{CC} High Limit = 0xFF default

Temperature Limit Registers

Register 0x4E, Remote 1 Temperature Low Limit = 0x81 default

Register 0x4F, Remote 1 Temperature High Limit = 0x7F default

Register 0x6A, Remote 1 $\overline{\text{THERM}}$ Temperature Limit = 0x64 default

Register 0x50, Local Temperature Low Limit = 0x81 default

Register 0x51, Local Temperature High Limit = 0x7F default

Register 0x6B, Local $\overline{\text{THERM}}$ Temperature Limit = 0x64 default

Register 0x52, Remote 2 Temperature Low Limit = 0x81 default

Register 0x53, Remote 2 Temperature High Limit = 0x7F default

Register 0x6C, Remote 2 $\overline{\text{THERM}}$ Temperature Limit = 0x64 default

$\overline{\text{THERM}}$ Limit Register

Register 0x7A, $\overline{\text{THERM}}$ Timer Limit = 0x00 default

16−Bit Limits

The fan TACH measurements are 16−bit results. The fan TACH limits are also 16 bits, consisting of a high byte and low byte. Because fans running under speed or stalled are normally the only conditions of interest, only high limits exist for fan TACHs. Because the fan TACH period is

actually being measured, exceeding the limit indicates a slow or stalled fan.

Fan Limit Registers

Register 0x54, TACH1 Minimum Low Byte = 0xFF default

Register 0x55, TACH1 Minimum High Byte = 0xFF default

Register 0x56, TACH2 Minimum Low Byte = 0xFF default

Register 0x57, TACH2 Minimum High Byte = 0xFF default

Register 0x58, TACH3 Minimum Low Byte = 0xFF default

Register 0x59, TACH3 Minimum High Byte = 0xFF default

Register 0x5A, TACH4 Minimum Low Byte = 0xFF default

Register 0x5B, TACH4 Minimum High Byte = 0xFF default

Out−of−Limit Comparisons

Once all limits have been programmed, the NVT224 can be enabled for monitoring. The NVT224 measures all voltage and temperature measurements in round−robin format and sets the appropriate status bit for out−of−limit conditions. TACH measurements are not part of this round−robin cycle. Comparisons are done differently, depending on whether the measured value is being compared to a high or low limit.

High Limit > Comparison Performed

Low Limit ≤ Comparison Performed

Voltage and temperature channels use a window comparator for error detecting and, therefore, have high and low limits. Fan speed measurements use only a low limit. This fan limit is needed only in manual fan control mode.

Analog Monitoring Cycle Time

The analog monitoring cycle begins when a 1 is written to the start bit (Bit 0) of Configuration Register 1 (0x40). By default, the NVT224 powers up with this bit set. The ADC measures each analog input in turn and, as each measurement is completed, the result is automatically stored in the appropriate value register. This round−robin monitoring cycle continues unless disabled by writing a 0 to Bit 0 of Configuration Register 1.

As the ADC is normally left to free−run in this manner, the time taken to monitor all the analog inputs is normally not of interest, because the most recently measured value of any input can be read out at any time.

For applications where the monitoring cycle time is important, it can easily be calculated. The total number of channels measured is

- One dedicated supply voltage input (V_{CCP} pin)
- Supply voltage (V_{CC} pin)
- Local temperature
- Two remote temperatures

As mentioned previously, the ADC performs round−robin conversions. The total monitoring cycle time for averaged voltage and temperature monitoring is 146 ms. The total monitoring cycle time for voltage and temperature monitoring with averaging disabled is 19 ms. The NVT224 is a derivative of the ADT7467. As a result, the total conversion time in the NVT224 is the same as the total conversion time of the ADT7467.

Fan TACH measurements are made in parallel and are not synchronized with the analog measurements in any way.

Interrupt Status Registers

The results of limit comparisons are stored in Interrupt Status Register 1 and Interrupt Status Register 2. The status register bit for each channel reflects the status of the last measurement and limit comparison on that channel. If a measurement is within limits, the corresponding status register bit is cleared to 0. If the measurement is out−of−limits, the corresponding status register bit is set to 1.

The state of the various measurement channels can be polled by reading the status registers over the serial bus. In Bit 7 (OOL) of Interrupt Status Register 1 (0x41), 1 means that an out−of−limit event has been flagged in Interrupt Status Register 2. This means that the user needs only to read Interrupt Status Register 2 when this bit is set. Alternatively, Pin 5 or Pin 9 can be configured as an $\overline{\text{SMBALERT}}$ output. This automatically notifies the system supervisor of an out−of−limit condition. Reading the status registers clears the appropriate status bit as long as the error condition that caused the interrupt has cleared.

Status register bits are sticky. Whenever a status bit is set, indicating an out−of−limit condition, it remains set even if the event that caused it has gone away (until read). The only way to clear the status bit is to read the status register after the event has gone away. Interrupt status mask registers (0x74 and 0x75) allow individual interrupt sources to be masked from causing an $\overline{\text{SMBALERT}}$. However, if one of these masked interrupt sources goes out−of−limit, its associated status bit is set in the interrupt status registers.

Interrupt Status Register 1 (0x41)

Bit 7 (OOL) = 1, denotes that a bit in Status Register 2 is set and that Interrupt Status Register 2 should be read.

Bit 6 (R2T) = 1, Remote 2 temperature high or low limit has been exceeded.

Bit 5 (LT) = 1, local temperature high or low limit has been exceeded.

Bit 4 (R1T) = 1, Remote 1 temperature high or low limit has been exceeded.

Bit 2 (V_{CC}) = 1, V_{CC} high or low limit has been exceeded.

Bit 1 (V_{CCP}) = 1, V_{CCP} high or low limit has been exceeded.

Interrupt Status Register 2 (0x42)

Bit 7 (D2) = 1, indicates an open or short on D2+/D2– inputs.

Bit 6 (D1) = 1, indicates an open or short on D1+/D1– inputs.

Bit 5 (F4P) = 1, indicates that Fan 4 has dropped below minimum speed. Alternatively, indicates that the $\overline{\text{THERM}}$ limit has been exceeded, if the $\overline{\text{THERM}}$ function is used.

Bit 4 (FAN3) = 1, indicates that Fan 3 has dropped below minimum speed.

Bit 3 (FAN2) = 1, indicates that Fan 2 has dropped below minimum speed.

Bit 2 (FAN1) = 1, indicates that Fan 1 has dropped below minimum speed.

Bit 1 (OVT) = 1, indicates that a $\overline{\text{THERM}}$ overtemperature limit has been exceeded.

$\overline{\text{SMBALERT}}$ Interrupt Behavior

The NVT224 can be polled for status, or an $\overline{\text{SMBALERT}}$ interrupt can be generated for out−of−limit conditions. Note how the $\overline{\text{SMBALERT}}$ output and status bits behave when writing interrupt handler software.

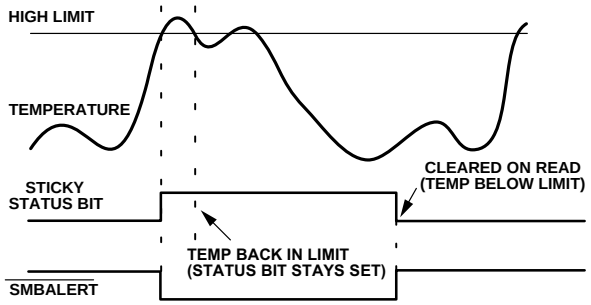


Figure 24. $\overline{\text{SMBALERT}}$ and Status Bit Behavior

Figure 24 shows how the $\overline{\text{SMBALERT}}$ output and sticky status bits behave. Once a limit is exceeded, the corresponding status bit is set to 1. The status bit remains set until the error condition subsides and the status register is read. The status bits are referred to as sticky because they remain set until read by software. This ensures that an out−of−limit event cannot be missed if software is polling the device periodically. Note that the $\overline{\text{SMBALERT}}$ output remains low for the entire duration that a reading is out−of−limit and until the interrupt status register has been read. This has implications for how software handles the interrupt.

Handling $\overline{\text{SMBALERT}}$ Interrupts

To prevent the system from being tied up servicing interrupts, it is recommended to handle the $\overline{\text{SMBALERT}}$ interrupt as follows:

1. Detect the $\overline{\text{SMBALERT}}$ assertion.
2. Enter the interrupt handler.
3. Read the status registers to identify the interrupt source.
4. Mask the interrupt source by setting the appropriate mask bit in the interrupt mask registers (0x74 and 0x75).
5. Take the appropriate action for a given interrupt source.
6. Exit the interrupt handler.
7. Periodically poll the status registers. If the interrupt status bit has cleared, reset the corresponding interrupt mask bit to 0. This causes the $\overline{\text{SMBALERT}}$ output and status bits to behave as shown in Figure 25.

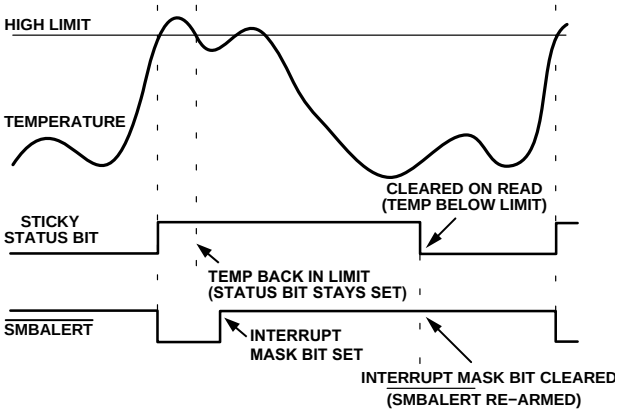


Figure 25. How Masking the Interrupt Source Affects $\overline{\text{SMBALERT}}$ Output

Masking Interrupt Sources

Interrupt Mask Register 1 (0x74) and Interrupt Mask Register 2 (0x75) allow individual interrupt sources to be masked out to prevent $\overline{\text{SMBALERT}}$ interrupts. Note that masking an interrupt source prevents only the $\overline{\text{SMBALERT}}$ output from being asserted; the appropriate status bit is set normally.

Interrupt Mask Register 1 (0x74)

Bit 7 (OOL) = 1, masks $\overline{\text{SMBALERT}}$ for any alert condition flagged in Interrupt Status Register 2.

Bit 6 (R2T) = 1, masks $\overline{\text{SMBALERT}}$ for Remote 2 Temperature.

Bit 5 (LT) = 1, masks $\overline{\text{SMBALERT}}$ for Local Temperature.

Bit 4 (R1T) = 1, masks $\overline{\text{SMBALERT}}$ for Remote 1 Temperature.

Bit 2 (V_{CC}) = 1, masks $\overline{\text{SMBALERT}}$ for V_{CC} Channel.

Bit 1 (V_{CCP}) = 1, masks $\overline{\text{SMBALERT}}$ for V_{CCP} Channel.

Interrupt Mask Register 2 (0x75)

Bit 7 (D2) = 1, masks $\overline{\text{SMBALERT}}$ for Diode 2 errors.

Bit 6 (D1) = 1, masks $\overline{\text{SMBALERT}}$ for Diode 1 errors.

Bit 5 (F4P) = 1, masks $\overline{\text{SMBALERT}}$ for Fan 4 failure.

If the TACH4 pin is being used as the $\overline{\text{THERM}}$ input, this bit masks $\overline{\text{SMBALERT}}$ for a $\overline{\text{THERM}}$ event.

Bit 4 (FAN3) = 1, masks $\overline{\text{SMBALERT}}$ for Fan 3.

Bit 3 (FAN2) = 1, masks $\overline{\text{SMBALERT}}$ for Fan 2.

Bit 2 (FAN1) = 1, masks $\overline{\text{SMBALERT}}$ for Fan 1.

Bit 1 (OVT) = 1, masks $\overline{\text{SMBALERT}}$ for overtemperature (exceeding $\overline{\text{THERM}}$ limits).

Enabling the $\overline{\text{SMBALERT}}$ Interrupt Output

The $\overline{\text{SMBALERT}}$ interrupt function is disabled by default. Pin 5 or Pin 9 can be reconfigured as an $\overline{\text{SMBALERT}}$ output to signal out−of−limit conditions.

Table 8. Configuring Pin 5 as $\overline{\text{SMBALERT}}$ Output

Register	Bit Setting
Configuration Register 3 (0x78)	[0] $\overline{\text{ALERT}}$ Enable = 1

Assigning $\overline{\text{THERM}}$ Functionality to a Pin

Pin 9 on the NVT224 has four possible functions: $\overline{\text{SMBALERT}}$, $\overline{\text{THERM}}$, GPIO, and TACH4. The user chooses the required functionality by setting Bit 0 and Bit 1 of Configuration Register 4 (0x7D).

Table 9. Pin 9 Configuration

Bit 1	Bit 0	Function
0	0	TACH4
0	1	$\overline{\text{THERM}}$
1	0	$\overline{\text{SMBALERT}}$
1	1	GPIO

Once Pin 9 is configured as $\overline{\text{THERM}}$, it must be enabled (Bit 1, Configuration Register 3 (0x78)).

$\overline{\text{THERM}}$ as an Input

When $\overline{\text{THERM}}$ is configured as an input, the user can time assertions on the $\overline{\text{THERM}}$ pin. This can be useful for connecting to the $\overline{\text{PROCHOT}}$ output of a CPU to gauge system performance.

The user can also set up the NVT224 so that, when the $\overline{\text{THERM}}$ pin is driven low externally, the fans run at 100%. The fans run at 100% for the duration of the time that the $\overline{\text{THERM}}$ pin is pulled low. This is done by setting the BOOST bit (Bit 2) in Configuration Register 3 (0x78) to 1. This works only if the fan is already running, for example, in manual mode when the current duty cycle is above 0x00 or in automatic mode when the temperature is above T_{MIN}. If the temperature is below T_{MIN} or if the duty cycle in manual mode is set to 0x00, pulling the $\overline{\text{THERM}}$ low externally has no effect. See Figure 26 for more information.

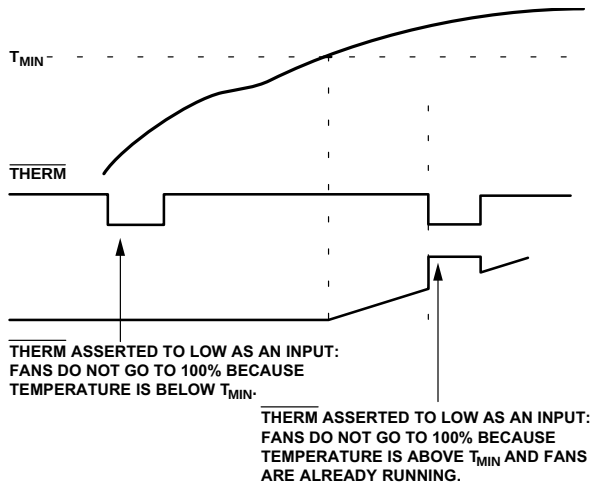


Figure 26. Asserting $\overline{\text{THERM}}$ Low as an Input in Automatic Fan Speed Control Mode

$\overline{\text{THERM}}$ Timer

The NVT224 has an internal timer to measure $\overline{\text{THERM}}$ assertion time. For example, the $\overline{\text{THERM}}$ input can be connected to the $\overline{\text{PROCHOT}}$ output of a Pentium 4 CPU to measure system performance. The $\overline{\text{THERM}}$ input can also be connected to the output of a trip point temperature sensor.

The timer is started on the assertion of the NVT224's $\overline{\text{THERM}}$ input and stopped when $\overline{\text{THERM}}$ is un−asserted. The timer counts $\overline{\text{THERM}}$ times cumulatively, that is, the timer resumes counting on the next $\overline{\text{THERM}}$ assertion. The $\overline{\text{THERM}}$ timer continues to accumulate $\overline{\text{THERM}}$ assertion times until the timer is read (it is cleared on read) or until it reaches full scale. If the counter reaches full scale, it stops at that reading until cleared.

The 8−bit $\overline{\text{THERM}}$ timer status register (0x79) is designed so that the Bit 0 is set to 1 on the first $\overline{\text{THERM}}$ assertion. Once the cumulative $\overline{\text{THERM}}$ assertion time has exceeded 45.52 ms, Bit 1 of the $\overline{\text{THERM}}$ timer is set and Bit 0 becomes the LSB of the timer with a resolution of 22.76 ms, see Figure 27.

When using the $\overline{\text{THERM}}$ timer, be aware of the following. After a $\overline{\text{THERM}}$ timer read (Register 0x79), the following happens:

1. The contents of the timer are cleared on read.
2. The F4P bit (Bit 5) of Interrupt Status Register 2 needs to be cleared (assuming that the $\overline{\text{THERM}}$ timer limit has been exceeded).

If the $\overline{\text{THERM}}$ timer is read during a $\overline{\text{THERM}}$ assertion, the following happens:

3. The contents of the timer are cleared.
4. Bit 0 of the $\overline{\text{THERM}}$ timer is set to 1 (because a $\overline{\text{THERM}}$ assertion is occurring).
5. The $\overline{\text{THERM}}$ timer increments from zero.
6. If the $\overline{\text{THERM}}$ timer limit (Register 0x7A) = 0x00, the F4P bit is set.

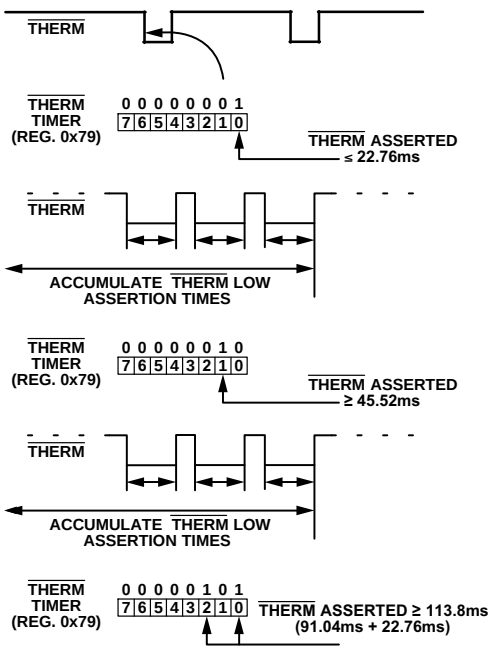


Figure 27. Understanding the $\overline{\text{THERM}}$ Timer

Generating SMBALERT Interrupts from A THERM Timer Events

The NVT224 can generate SMBALERTs when a programmable THERM timer limit has been exceeded. This allows the system designer to ignore brief, infrequent THERM assertions, while capturing longer THERM timer events. Register 0x7A is the THERM timer limit register. This 8−bit register allows a limit from 0 seconds (first THERM assertion) to 5.825 seconds to be set before an SMBALERT is generated. The THERM timer value is compared with the contents of the THERM timer limit register.

If the THERM timer value exceeds the THERM timer limit value, then the F4P bit (Bit 5) of Interrupt Status Register 2 is set, and an SMBALERT is generated. Note that the F4P bit (Bit 5) of Interrupt Mask Register 2 (0x75) masks out SMBALERTs if this bit is set to 1, although the F4P bit of Interrupt Status Register 2 is still set if the THERM timer limit is exceeded.

Figure 28 is a functional block diagram of the THERM timer, limit, and associated circuitry. Writing a value of 0x00 to the THERM timer limit register (0x7A) causes SMBALERT to be generated on the first THERM assertion. A THERM timer limit value of 0x01 generates an SMBALERT once cumulative THERM assertions exceed 45.52 ms.

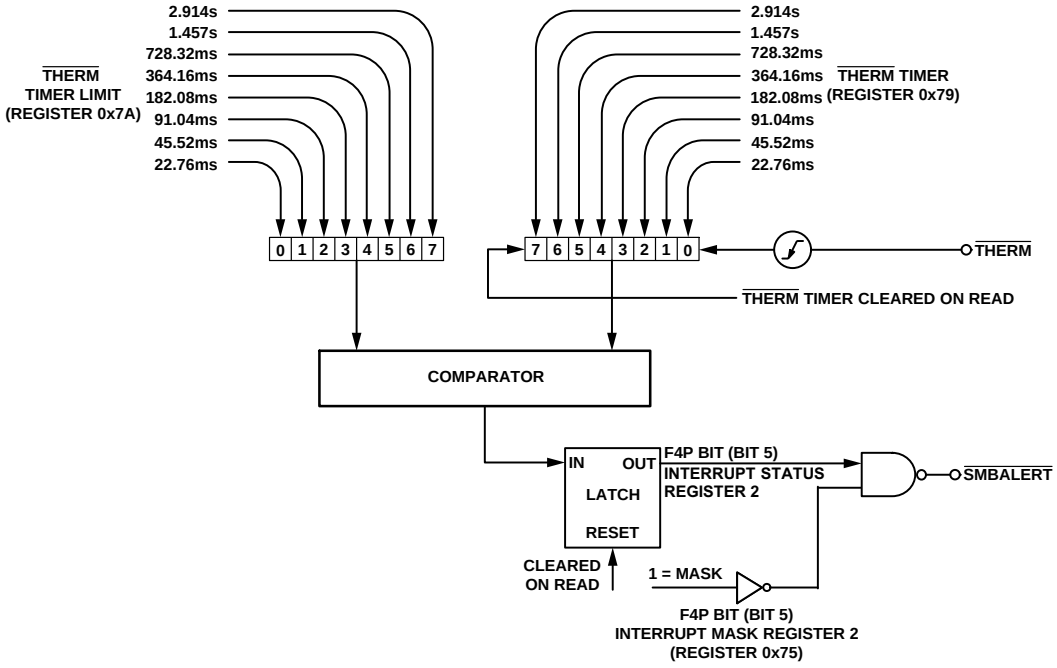


Figure 28. Functional Block Diagram of the NVT224 THERM Monitoring Circuitry

Configuring the THERM Behavior

1. Configure the relevant pin as the THERM timer input. Setting Bit 1 (THERM) of Configuration Register 3 (0x78) enables the THERM timer monitoring functionality. This is disabled on Pin 9 by default.
   Setting Bit 0 and Bit 1 (PIN9FUNC) of Configuration Register 4 (0x7D) enables THERM timer/output functionality on Pin 9 (Bit 1, THERM, of Configuration Register 3, must also be set). Pin 9 can also be used as TACH4.
2. Select the desired fan behavior for THERM timer events.
   Assuming that the fans are running, setting Bit 2 (BOOST bit) of Configuration Register 3 (0x78) causes all fans to run at 100% duty cycle whenever THERM is asserted. This allows fail−safe system cooling. If this bit is 0, the fans run at their current settings and are not affected by THERM events. If the fans are not already running when THERM is asserted, the fans do not run to full speed.
3. Select whether THERM timer events should generate SMBALERT interrupts.
   Bit 5 (F4P) of Interrupt Mask Register 2 (0x75), when set, masks out SMBALERTs when the THERM timer limit value is exceeded. This bit should be cleared if SMBALERTs based on THERM events are required.
4. Select a suitable THERM limit value.
   This value determines whether an SMBALERT is generated on the first THERM assertion or only if a cumulative THERM assertion time limit is exceeded. A value of 0x00 causes an SMBALERT to be generated on the first THERM assertion.
5. Select a THERM monitoring time.
   This value specifies how often OS− or BIOS−level software checks the THERM timer. For example, BIOS could read the THERM timer once an hour to determine the cumulative THERM assertion time. If, for example, the total THERM assertion time is <22.76 ms in Hour 1, >182.08 ms in Hour 2, and >2.914 s in Hour 3, this can indicate that system

performance is degrading significantly because THERM is asserting more frequently on an hourly basis.

Alternatively, OS− or BIOS−level software can time−stamp when the system is powered on. If an SMBALERT is generated due to the THERM timer limit being exceeded, another time−stamp can be taken. The difference in time can be calculated for a fixed THERM timer limit time. For example, if it takes one week for a THERM timer limit of 2.914 seconds to be exceeded and the next time it takes only one hour, this is an indication of a serious degradation in system performance.

Configuring the THERM Pin as an Output

In addition to monitoring THERM as an input, the NVT224 can optionally drive THERM low as an output. In cases where PROCHOT is bidirectional, THERM can be used to throttle the processor by asserting PROCHOT. The user can pre−program system−critical thermal limits. If the temperature exceeds a thermal limit by 0.25°C, THERM asserts low. If the temperature is still above the thermal limit on the next monitoring cycle, THERM stays low. THERM remains asserted low until the temperature is equal to or below the thermal limit. Because the temperature for that channel is measured only once for every monitoring cycle, after THERM asserts, it is guaranteed to remain low for at least one monitoring cycle.

The THERM pin can be configured to assert low if the Remote 1, local, or Remote 2 THERM temperature limit is exceeded by 0.25°C. The THERM temperature limit registers are at Register 0x6A, Register 0x6B, and Register 0x6C. Setting Bit 3 of Register 0x5F, Register 0x60, and Register 0x61 enables the THERM output feature for the Remote 1, local, and Remote 2 temperature channels, respectively. Figure 29 shows how the THERM pin asserts low as an output in the event of a critical over temperature.

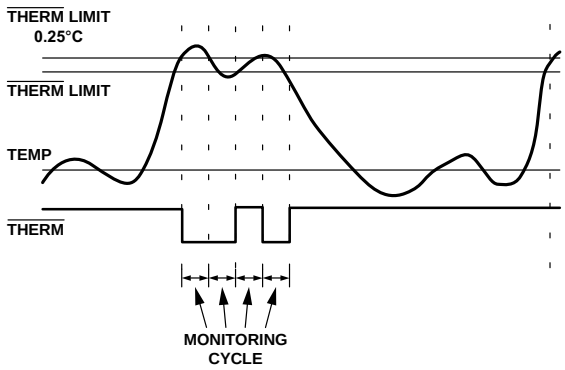


Figure 29. Asserting THERM as an Output, Based on Tripping THERM Limits

An alternative method of disabling THERM is to program the THERM temperature limit to 64°C or less in Offset 64 mode, or 128°C or less in twos complement mode; that is, for THERM temperature limit values less than 64°C or 128°C, respectively, THERM is disabled.

Enabling and Disabling THERM on Individual Channels

THERM can be enabled/disabled for individual or combinations of temperature channels using Bits [7:5] of Configuration Register 5 (0x7C).

THERM Hysteresis

Setting Bit 0 of Configuration Register 7 (0x11) disables THERM hysteresis.

If THERM hysteresis is enabled and THERM is disabled (Bit 2 of Configuration Register 4, 0x7D), the THERM pin does not assert low when a THERM event occurs. If THERM hysteresis is disabled and THERM is disabled (Bit 2 of Configuration Register 4, 0x7D, and assuming the appropriate pin is configured as THERM), the THERM pin asserts low when a THERM event occurs.

If THERM and THERM hysteresis are both enabled, the THERM output asserts as expected.

THERM Operation in Manual Mode

In manual mode, THERM events do not cause fans to go to full speed, unless Bit 3 of Configuration Register 6 (0x10) is set to 1.

Additionally, Bit 3 of Configuration Register 4 (0x7D) can be used to select PWM speed on THERM event (100% or maximum PWM).

Bit 2 in Configuration Register 4 (0x7D) can be set to disable THERM events from affecting the fans.

Fan Drive Using PWM Control

The NVT224 uses pulse−width modulation (PWM) to control fan speed. This relies on varying the duty cycle (or on/off ratio) of a square wave applied to the fan to vary the fan speed. The external circuitry required to drive a fan using PWM control is extremely simple. For 4−wire fans, the PWM drive may need only a pullup resistor. In many cases, the 4−wire fan PWM input has a built−in pullup resistor.

The NVT224 PWM frequency can be set to a selection of low frequencies or a single high PWM frequency. The low frequency options are usually used for 3−wire fans, while the high frequency option is usually used with 4−wire fans.

For 3−wire fans, a single N−channel MOSFET is the only drive device required. The specifications of the MOSFET depend on the maximum current required by the fan being driven. Typical notebook fans draw a nominal 170 mA, so SOT devices can be used where board space is a concern. In desktops, fans can typically draw 250 mA to 300 mA each. If several fans are driven in parallel from a single PWM output or drive larger server fans, the MOSFET must handle the higher current requirements.

The only other stipulation is that the MOSFET should have a gate voltage drive, V_{GS} < 3.3 V, for direct interfacing to the PWM output pin. The MOSFET should also have a low on resistance to ensure that there is not significant voltage drop across the FET, which would reduce the voltage applied across the fan and, therefore, the maximum operating speed of the fan.

Figure 30 shows how to drive a 3−wire fan using PWM control.

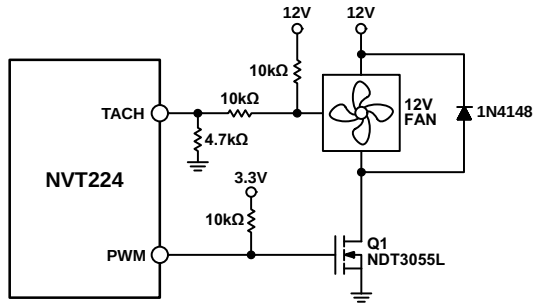


Figure 30. Driving a 3−Wire Fan Using an N−Channel MOSFET

Figure 30 uses a 10 kΩ pullup resistor for the TACH signal. This assumes that the TACH signal is an open−collector from the fan. In all cases, the TACH signal from the fan must be kept below 3.6 V maximum to prevent damaging the NVT224. If in doubt as to whether the fan used has an open−collector or totem pole TACH output, use one of the input signal conditioning circuits shown in the Fan Speed Measurement section.

Figure 31 shows a fan drive circuit using an NPN transistor such as a general−purpose MMBT2222. While these devices are inexpensive, they tend to have much lower current handling capabilities and higher on resistance than MOSFETs. When choosing a transistor, care should be taken to ensure that it meets the fan's current requirements.

Ensure that the base resistor is chosen so that the transistor is saturated when the fan is powered on.

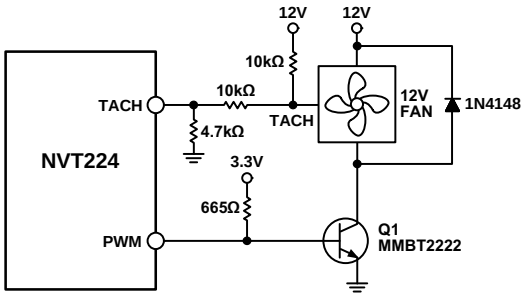


Figure 31. Driving a 3−Wire Fan Using an NPN Transistor

Because 4−wire fans are powered continuously, the fan speed is not switched on or off as with previous PWM driven/powered fans. This enables it to perform better than 3−wire fans, especially for high frequency applications. Figure 32 shows a typical drive circuit for 4−wire fans.

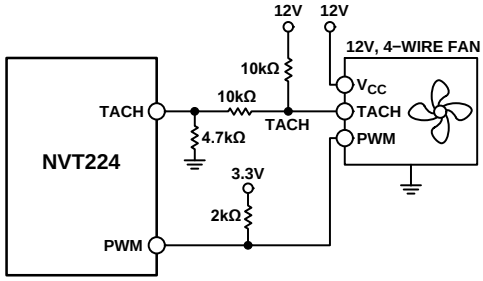


Figure 32. Driving a 4−Wire Fan

Driving Two Fans from PWM3

The NVT224 has four TACH inputs available for fan speed measurement but only three PWM drive outputs. If a fourth fan is used in the system, it should be driven from the PWM3 output in parallel with the third fan. Figure 33 shows how to drive two fans in parallel using low cost NPN transistors. Figure 34 shows the equivalent circuit using a MOSFET.

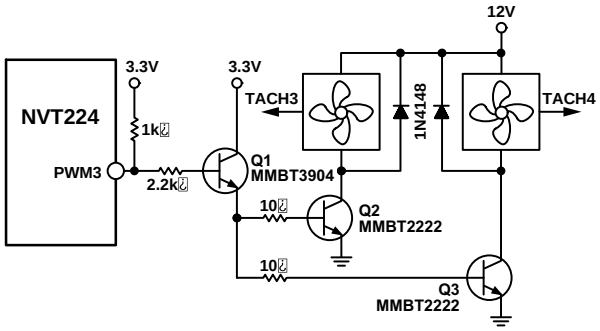


Figure 33. Interfacing Two Fans in Parallel to the PWM3 Output Using Low Cost NPN Transistors

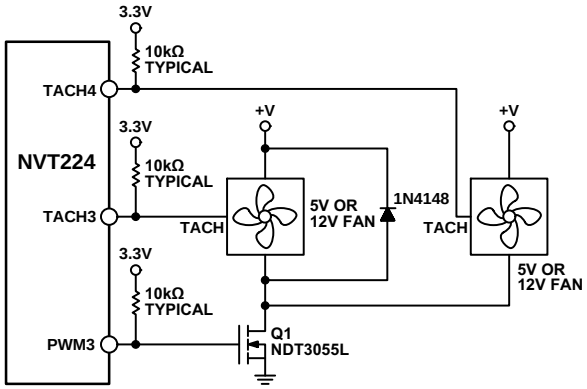


Figure 34. Interfacing Two Fans in Parallel to the PWM3 Output Using a Single N−Channel MOSFET

Because the MOSFET can handle up to 3.5 A, it is simply a matter of connecting another fan directly in parallel with the first. Care should be taken in designing drive circuits with transistors and FETs to ensure that the PWM pins are not required to source current and that they sink less than the 8 mA maximum current specified on the data sheet.

Driving up to Three Fans from PWM3

TACH measurements for fans are synchronized to particular PWM channels; for example, TACH1 is synchronized to PWM1. TACH3 and TACH4 are both synchronized to PWM3, so PWM3 can drive two fans. Alternatively, PWM3 can be programmed to synchronize TACH2, TACH3, and TACH4 to the PWM3 output. This allows PWM3 to drive two or three fans. In this case, the drive circuitry looks the same, as shown in Figure 33 and Figure 34. The SYNC bit in Register 0x62 enables this function.

Synchronization is not required in high frequency mode when used with 4−wire fans.

Bit 4 (SYNC) Enhanced Acoustics Register 1 (0x62)

SYNC = 1, synchronizes TACH2, TACH3, and TACH4 to PWM3.

TACH Inputs

Pin 4, Pin 6, Pin 7, and Pin 9, when configured as TACH inputs, are open−drain TACH inputs intended for fan speed measurement.

Signal conditioning in the NVT224 accommodates the slow rise and fall times typical of fan tachometer outputs. The maximum input signal range is 0 V to 3.6 V. In the event these inputs are supplied from fan outputs that exceed 0 V to 3.6 V, either resistive attenuation of the fan signal or diode clamping must be included to keep inputs within an acceptable range.

Figure 35 to Figure 38 show circuits for most common fan TACH outputs. If the fan TACH output has a resistive pullup to V_{CC}, it can be connected directly to the fan input, as shown in Figure 35.

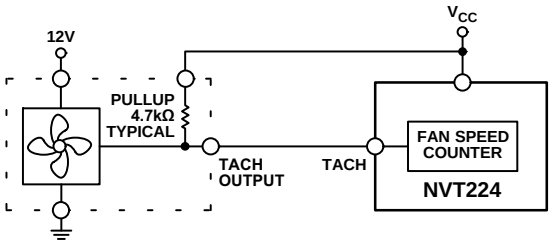


Figure 35. Fan with TACH Pullup to V_{CC}

If the fan output has a resistive pullup to 12 V, or other voltage greater than 3.6 V, the fan output can be clamped with a Zener diode, as shown in Figure 36. The Zener diode voltage should be chosen so that it is greater than V_{IH} of the TACH input but less than 3.6 V, allowing for the voltage tolerance of the Zener. A value between 3.0 V and 3.6 V is suitable.

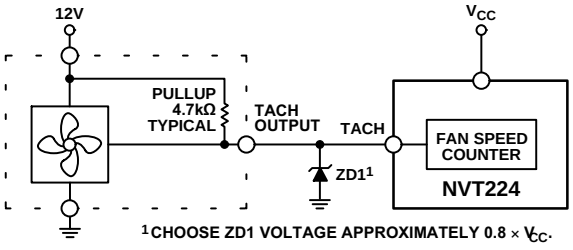


Figure 36. Fan with TACH Pullup to Voltage > 3.6 V (example, 12 V) Clamped with Zener Diode

If the fan has a strong pullup (less than 1 kΩ) to 12 V or a totem−pole output, then a series resistor can be added to limit the Zener current, as shown in Figure 37.

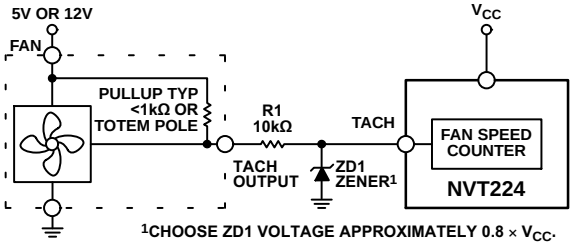


Figure 37. Fan with Strong TACH Pullup to > V_{CC} or Totem−Pole Output, Clamped with Zener and Resistor

Alternatively, a resistive attenuator can be used, as shown in Figure 38. R1 and R2 should be chosen such that:

$$2.0\ V < V_{PULLUP} \times R2/(R_{PULLUP} + R1 + R2) < 3.6\ V \quad \text{(eq. 3)}$$

The fan inputs can have an input resistance of 160 kΩ to 5.1 kΩ to ground, which should be taken into account when calculating resistor values.

With a pullup voltage of 12 V and pullup resistor less than 1 kΩ, suitable values for R1 and R2 would be 100 kΩ and 33 kΩ, respectively. This gives a high input voltage of 2.95 V.

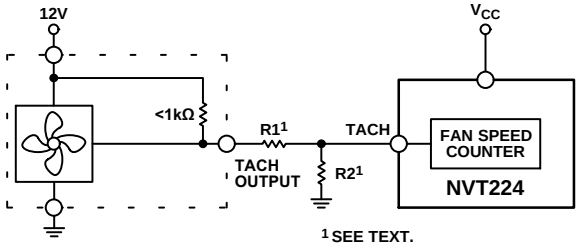


Figure 38. Fan with Strong TACH pullup to > V_{CC} or Totem−Pole Output, Attenuated with R1/R2

Fan Speed Measurement

The fan counter does not count the fan TACH output pulses directly because the fan speed could be less than 1000 RPM and it would take several seconds to accumulate a reasonably large and accurate count. Instead, the period of the fan revolution is measured by gating an on−chip 90 kHz oscillator into the input of a 16−bit counter for N periods of the fan TACH output (see Figure 39), so the accumulated count is actually proportional to the fan tachometer period and inversely proportional to the fan speed.

N, the number of pulses counted, is determined by the settings of Register 0x7B (TACH Pulses per Revolution register). This register contains two bits for each fan, allowing one, two (default), three, or four TACH pulses to be counted.

Measuring Fan TACH

When the NVT224 starts up, TACH measurements are locked. In effect, an internal read of the low byte has been

made for each TACH input. The net result of this is that all TACH readings are locked until the high byte is read from the corresponding TACH registers. All TACH related interrupts are also ignored until the appropriate high byte is read.

Once the corresponding high byte has been read, TACH measurements are unlocked and interrupts are processed as normal.

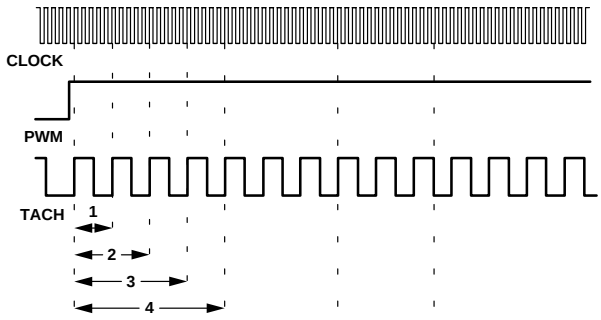


Figure 39. Fan Speed Measurement

Fan Speed Measurement Registers

The fan tachometer readings are 16−bit values consisting of a 2−byte read from the NVT224.

Register 0x28, TACH1 Low Byte = 0x00 default

Register 0x29, TACH1 High Byte = 0x00 default

Register 0x2A, TACH2 Low Byte = 0x00 default

Register 0x2B, TACH2 High Byte = 0x00 default

Register 0x2C, TACH3 Low Byte = 0x00 default

Register 0x2D, TACH3 High Byte = 0x00 default

Register 0x2E, TACH4 Low Byte = 0x00 default

Register 0x2F, TACH4 High Byte = 0x00 default

Reading Fan Speed from the NVT224

The measurement of fan speeds involves a 2−register read for each measurement. The low byte should be read first. This causes the high byte to be frozen until both high and low byte registers have been read, preventing erroneous TACH readings. The fan tachometer reading registers report back the number of 11.11 μs period clocks (90 kHz oscillator) gated to the fan speed counter, from the rising edge of the first fan TACH pulse to the rising edge of the third fan TACH pulse (assuming two pulses per revolution are being counted). Because the device is essentially measuring the fan TACH period, the higher the count value, the slower the fan is actually running. A 16−bit fan tachometer reading of 0xFFFF indicates that the fan either has stalled or is running very slowly (<100 RPM).

High Limit > Comparison Performed

Because the actual fan TACH period is being measured, falling below a fan TACH limit by 1 sets the appropriate status bit and can be used to generate an $\overline{\text{SMBALERT}}$.

Fan TACH Limit Registers

The fan TACH limit registers are 16−bit values consisting of two bytes.

Register 0x54, TACH1 Minimum Low Byte = 0xFF default

Register 0x55, TACH1 Minimum High Byte = 0xFF default

Register 0x56, TACH2 Minimum Low Byte = 0xFF default

Register 0x57, TACH2 Minimum High Byte = 0xFF default

Register 0x58, TACH3 Minimum Low Byte = 0xFF default

Register 0x59, TACH3 Minimum High Byte = 0xFF default

Register 0x5A, TACH4 Minimum Low Byte = 0xFF default

Register 0x5B, TACH4 Minimum High Byte = 0xFF default

Fan Speed Measurement Rate

The fan TACH readings are normally updated once every second. The FAST bit (Bit 3) of Configuration Register 3 (0x78), when set, updates the fan TACH readings every 250 ms.

If any of the fans are not being driven by a PWM channel but are powered directly from 5.0 V or 12 V, their associated dc bit in Configuration Register 3 should be set. This allows TACH readings to be taken on a continuous basis for fans connected directly to a dc source. For optimal results, the associated dc bit should always be set when using 4−wire fans.

Calculating Fan Speed

Assuming a fan with a two pulses per revolution (and two pulses per revolution being measured), fan speed is calculated by the following:

Fan Speed (RPM) = (90,000 x 60)/Fan TACH Reading where Fan TACH Reading is the 16−bit fan tachometer reading.

Example

TACH1 High Byte (Register 0x29) = 0x17

TACH1 Low Byte (Register 0x28) = 0xFF

What is Fan 1 speed in RPM?

Fan 1 TACH Reading = 0x17FF = 6143 (decimal)
RPM = (f x 60)/Fan 1 TACH Reading
RPM = (90,000 x 60)/6143
Fan Speed = 879 RPM

Fan Pulses per Revolution

Different fan models can output either 1, 2, 3, or 4 TACH pulses per revolution. Once the number of fan TACH pulses has been determined, it can be programmed into the TACH Pulses per Revolution register (Register 0x7B) for each fan.

Alternatively, this register can be used to determine the number or pulses per revolution output by a given fan. By plotting fan speed measurements at 100% speed with different pulses per revolution setting, the smoothest graph with the lowest ripple determines the correct pulses per revolution value.

TACH Pulses per Revolution Register

Bits [1:0] Fan 1 default = 2 pulses per revolution.

Bits [3:2] Fan 2 default = 2 pulses per revolution.

Bits [5:4] Fan 3 default = 2 pulses per revolution.

Bits [7:6] Fan 4 default = 2 pulses per revolution.

00 = 1 pulse per revolution
01 = 2 pulses per revolution
10 = 3 pulses per revolution
11 = 4 pulses per revolution

Fan Spin−Up

The NVT224 has a unique fan spin−up function. It spins the fan at 100% PWM duty cycle until two TACH pulses are detected on the TACH input. Once two TACH pulses have been detected, the PWM duty cycle goes to the expected running value, for example, 33%. The advantage is that fans have different spin−up characteristics and take different times to overcome inertia. The NVT224 runs the fans just fast enough to overcome inertia and is quieter on spin−up than fans programmed to spin up for a given spin−up time.

Fan Startup Timeout

To prevent the generation of false interrupts as a fan spins up (because it is below running speed), the NVT224 includes a fan startup timeout function. During this time, the NVT224 looks for two TACH pulses. If two TACH pulses are not detected, an interrupt is generated. Using Configuration Register 1 (0x40), Bit 5 (FSPDIS), this functionality can be changed (see the Disabling Fan Startup Timeout section).

PWM1, PWM2, PWM3 Configuration Registers (0x5C, 0x5D, and 0x5E)

Bits [2:0] SPIN, startup timeout for PWM1 = 0x5C, PWM2 = 0x5D, and PWM3 = 0x5E.

000 = No startup timeout
001 = 100 ms
010 = 250 ms default
011 = 400 ms
100 = 667 ms
101 = 1 sec
110 = 2 sec
111 = 4 sec

Disabling Fan Startup Timeout

Although fan startup makes fan spin−ups much quieter than fixed−time spin−ups, the option exists to use fixed spin−up times. Setting Bit 5 (FSPDIS) to 1 in Configuration Register 1 (0x40) disables the spin−up for two TACH pulses. Instead, the fan spins up for the fixed time as selected in Register 0x5C to Register 0x5E.

PWM Logic State

The PWM outputs can be programmed high for 100% duty cycle (non−inverted) or low for 100% duty cycle (inverted).

PWM1 Configuration Register (0x5C)

Bit 4 INV
0 = Logic high for 100% PWM duty cycle.
1 = Logic low for 100% PWM duty cycle.

PWM2 Configuration Register (0x5D)

Bit 4 INV
0 = Logic high for 100% PWM duty cycle.
1 = Logic low for 100% PWM duty cycle.

PWM3 Configuration Register (0x5E)

Bit 4 INV
0 = Logic high for 100% PWM duty cycle.
1 = Logic low for 100% PWM duty cycle.

Low Frequency Mode PWM Drive Frequency

The PWM drive frequency can be adjusted for the application. Register 0x5F to Register 0x61 configure the PWM frequency for PWM1 to PWM3, respectively. In high frequency mode, the PWM drive frequency is always 22.5 kHz.

High Frequency Mode PWM Drive

Setting Bit 3 of Register 0x5F, Register 0x60, and Register 0x61 enables high frequency mode for Fan 1, Fan 2, and Fan 3, respectively.

PWM Frequency Registers (0x5F to 0x61)

Bits [2:0] FREQ

000 = 11.0 Hz
001 = 14.7 Hz
010 = 22.1 Hz
011 = 29.4 Hz
100 = 35.3 Hz default
101 = 44.1 Hz
110 = 58.8 Hz
111 = 88.2 Hz

Fan Speed Control

The NVT224 controls fan speed using automatic mode and manual mode as follows:

- In automatic fan speed control mode, fan speed is automatically varied with temperature and without CPU intervention, once initial parameters are set up. The advantage of this is, if the system hangs, the user is guaranteed that the system is protected from overheating. For more information about how to program the automatic fan speed control loop, see the Programming the Automatic Fan Speed Control Loop section.
- In manual fan speed control mode, the NVT224 allows the duty cycle of any PWM output to be manually adjusted. This can be useful if the user wants to change fan speed at the software level or adjust PWM duty cycle output for test purposes. Bits [7:5] of Register 0x5C to Register 0x5E (PWM configuration) control the behavior of each PWM output.

PWM Configuration Registers (0x5C to 0x5E)

Bits [7:5] BHVR

111 = manual mode.

Once under manual control, each PWM output can be manually updated by writing to Register 0x30 to Register 0x32 (PWMx current duty cycle registers).

Programming the PWM Current Duty Cycle Registers

The PWM current duty cycle registers are 8−bit registers that allow the PWM duty cycle for each output to be set anywhere from 0% to 100% in steps of 0.39%.

The value to be programmed into the PWM_{MIN} register is given by:

Value (decimal) = PWM_{MIN} /0.39

Example 1: For a PWM duty cycle of 50%,

Value (decimal) = 50/0.39 = 128 (decimal)

Value = 128 (decimal) or 0x80 (hex)

Example 2: For a PWM duty cycle of 33%,

Value (decimal) = 33/0.39 = 85 (decimal)

Value = 85 (decimal) or 0x54 (hex)

PWM Current Duty Cycle Registers

Register 0x30, PWM1 Current Duty Cycle = 0x00 (0% default)

Register 0x31, PWM2 Current Duty Cycle = 0x00 (0% default)

Register 0x32, PWM3 Current Duty Cycle = 0x00 (0% default)

By reading the PWMx current duty cycle registers, the user can keep track of the current duty cycle on each PWM output, even when the fans are running in automatic fan speed control mode or acoustic enhancement mode. See the Programming the Automatic Fan Speed Control Loop section for details.

Operating from 3.3 V Standby

The NVT224 has been specifically designed to operate from a 3.3 V STBY supply. In computers that support S3 and S5 states, the core voltage of the processor is lowered in these states. When monitoring $\overline{\text{THERM}}$, the $\overline{\text{THERM}}$ timer should be disabled during these states.

Standby Mode

The NVT224 has been specifically designed to respond to the STBY supply. In computers that support S3 and S5 states, the core voltage of the processor is lowered in these states. When monitoring $\overline{\text{THERM}}$, the $\overline{\text{THERM}}$ timer should be disabled during these states.

When the V_{CCP} voltage drops below the V_{CCP} low limit, the following occurs:

1. Status Bit 1 (V_{CCP}) in Status Register 1 is set.
2. $\overline{\text{SMBALERT}}$ is generated, if enabled.
3. $\overline{\text{THERM}}$ monitoring is disabled. The $\overline{\text{THERM}}$ timer should hold its value prior to the S3 or S5 state.

Once the core voltage, V_{CCP}, goes above the V_{CCP} low limit, everything is re−enabled and the system resumes normal operation.

XNOR Tree Test Mode

The NVT224 includes an XNOR tree test mode. This mode is useful for in−circuit test equipment at board−level testing. By applying stimulus to the pins included in the XNOR tree, it is possible to detect opens or shorts on the system board.

Figure 40 shows the signals that are exercised in the XNOR tree test mode. The XNOR tree test is invoked by setting Bit 0 (XEN) of the XNOR tree test enable register (0x6F).

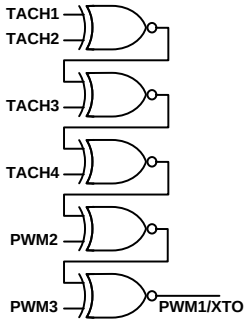


Figure 40. XNOR Tree Test

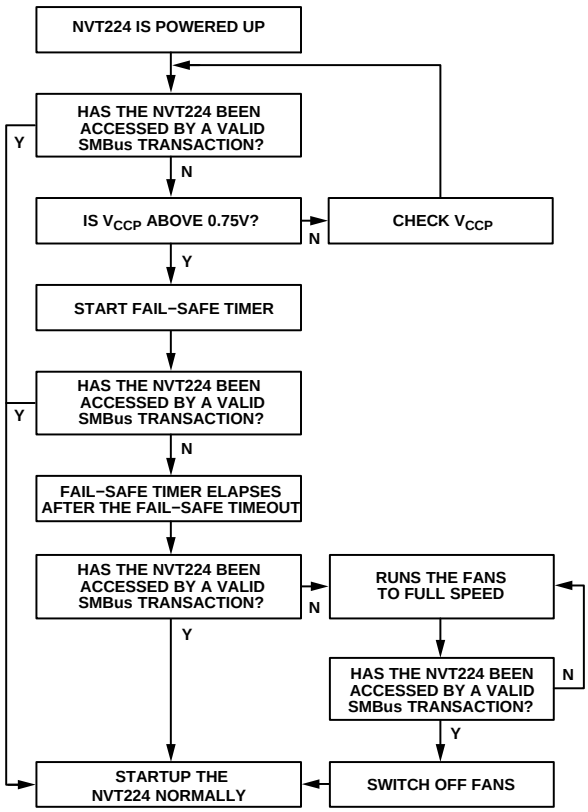


Figure 41. Power−On Flow Chart

Power−On Default

When the NVT224 is powered up, it polls the V_{CCP} input.

If V_{CCP} stays below 0.75 V (the system CPU power rail is not powered up), the NVT224 assumes the functionality of the default registers after the NVT224 is addressed via any valid SMBus transaction.

If V_{CC} goes high (the system processor power rail is powered up), a fail−safe timer begins to count down. If the NVT224 is not addressed by any valid SMBus transactions before the fail−safe timeout (4.6 seconds) lapses, the NVT224 drives the fans to full speed. If the NVT224 is addressed by a valid SMBus transaction after this point, the fans stop, and the NVT224 assumes its default settings and begins normal operation.

If V_{CCP} goes high (the system processor power rail is powered up), then a fail−safe timer begins to count down. If the NVT224 is addressed by a valid SMBus transaction before the fail−safe timeout (4.6 seconds) lapses, then the NVT224 operates normally, assuming the functionality of all the default registers. See the flow chart in Figure 41.

Programming the Automatic Fan Speed Control Loop

To more efficiently understand the automatic fan speed control loop, it is strongly recommended to use the NVT224 evaluation board and software while reading this section.

This section provides the system designer with an understanding of the automatic fan control loop, and provides step−by−step guidance on effectively evaluating and selecting critical system parameters. To optimize the system characteristics, the designer needs to give some thought to system configuration, including the number of fans, where they are located, and what temperatures are being measured in the particular system.

The mechanical or thermal engineer who is tasked with the system thermal characterization should also be involved at the beginning of this process.

Automatic Fan Control Overview

The NVT224 can automatically control the speed of fans based upon the measured temperature. This is done independently of CPU intervention once initial parameters are set up.

The NVT224 has a local temperature sensor and two remote temperature channels that can be connected to a CPU on−chip thermal diode (available on Intel Pentium class and other CPUs). These three temperature channels can be used as the basis for automatic fan speed control to drive fans using pulse−width modulation (PWM).

Automatic fan speed control reduces acoustic noise by optimizing fan speed according to accurately measured temperature. Reducing fan speed can also decrease system current consumption.

The automatic fan speed control mode is very flexible owing to the number of programmable parameters, including T_{MIN} and T_{RANGE}. The T_{MIN} and T_{RANGE} values for a temperature channel, and, therefore, for a given fan are critical because they define the thermal characteristics of the system. The thermal validation of the system is one of the most important steps in the design process, so select these values carefully.

Figure 42 gives a top−level overview of the automatic fan control circuitry on the NVT224. From a systems level perspective, up to three system temperatures can be monitored and used to control three PWM outputs. The three PWM outputs can be used to control up to four fans. The NVT224 allows the speed of four fans to be monitored. Each temperature channel has a thermal calibration block, allowing the designer to individually configure the thermal characteristics of each temperature channel.

For example, the designer can decide to run the CPU fan when CPU temperature increases above 60°C and a chassis fan when the local temperature increases above 45°C. At this stage, the designer has not assigned these thermal calibration settings to a particular fan drive (PWM) channel. The right side of Figure 42 shows controls that are fan−specific. The designer has individual control over parameters such as minimum PWM duty cycle, fan speed failure thresholds, and even ramp control of the PWM outputs. Automatic fan control, then, ultimately allows graceful fan speed changes that are less perceptible to the system user.

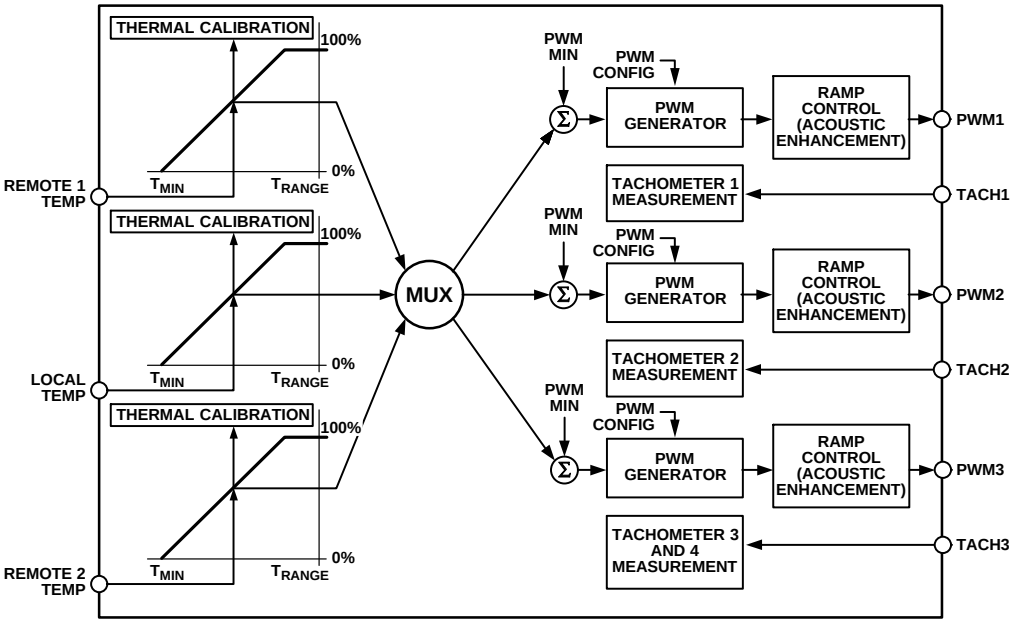


Figure 42. Automatic Fan Control Block Diagram

Step 1: Hardware Configuration

During system design, the motherboard sensing and control capabilities should be addressed early in the design stages. Decisions about how these capabilities are used should involve the system thermal/mechanical engineer. Ask the following questions:

1. What NVT224 functionality will be used?
   - PWM2 or $\overline{\text{SMBALERT}}$?
   - TACH4 fan speed measurement or overtemperature $\overline{\text{THERM}}$ function?

     The NVT224 offers multifunctional pins that can be reconfigured to suit different system requirements and physical layouts. These multifunction pins are software programmable.
2. How many fans will be supported in the system, three or four? This influences the choice of whether to use the TACH4 pin or to reconfigure it for the $\overline{\text{THERM}}$ function.
3. s the CPU fan to be controlled using the NVT224 or will it run at full speed 100% of the time?
   If run at 100%, this frees up a PWM output, but the system is louder.
4. Where will the NVT224 be physically located in the system?
   This influences the assignment of the temperature measurement channels to particular system thermal zones. For example, locating the NVT224 close to the VRM controller circuitry allows the VRM temperature to be monitored using the local temperature channel.

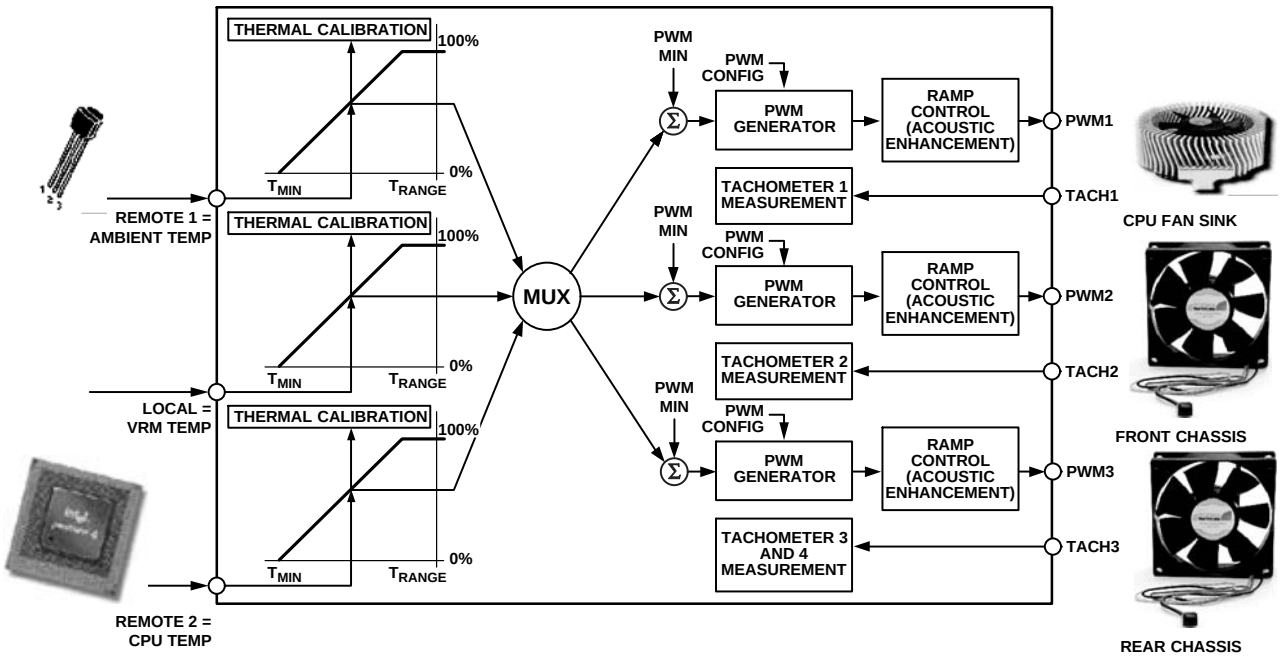


Figure 43. Hardware Configuration Example

Recommended Implementation 1

Configuring the NVT224 as in Figure 44 provides the system designer with the following features:

- Two PWM outputs for fan control of up to three fans. (The front and rear chassis fans are connected in parallel.)
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 3.
- CPU core voltage measurement (V_{CORE}).
- VRM temperature using local temperature sensor.
- CPU temperature measured using the Remote 1 temperature channel.
- Ambient temperature measured through the Remote 2 temperature channel.
- Bidirectional $\overline{\text{THERM}}$ pin, which allows the monitoring of $\overline{\text{PROCHOT}}$ output from an Intel Pentium 4 processor, for example, or can be used as an overtemperature $\overline{\text{THERM}}$ output.
- $\overline{\text{SMBALERT}}$ system interrupt output.

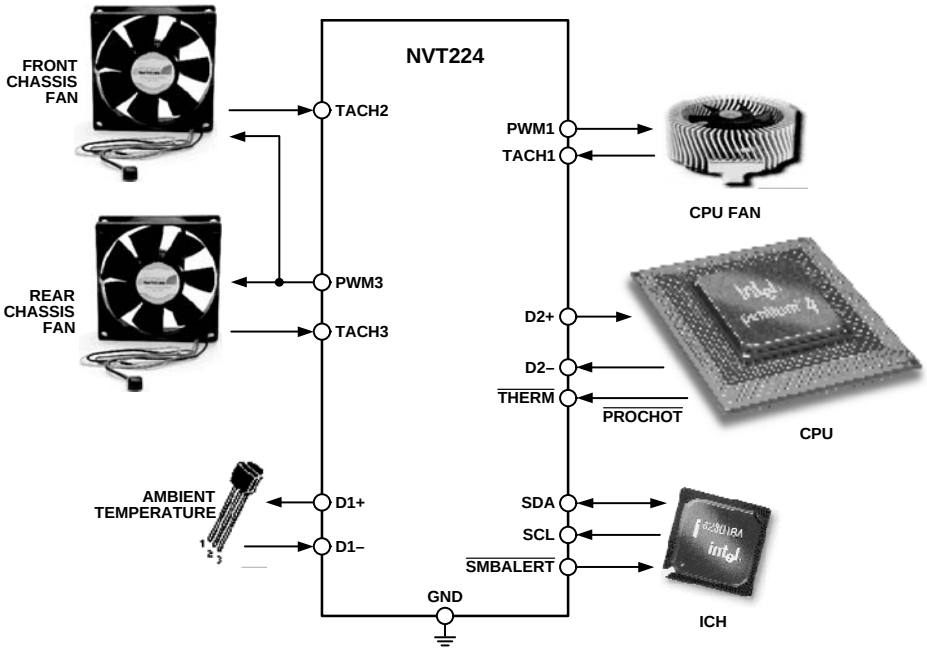


Figure 44. Recommended Implementation 1

Recommended Implementation 2

Configuring the NVT224 as in Figure 45 provides the system designer with the following features:

- Three PWM outputs for fan control of up to three fans. (All three fans can be individually controlled.)
- Three TACH fan speed measurement inputs.
- V_{CC} measured internally through Pin 3.
- CPU core voltage measurement (V_{CORE}).
- CPU temperature measured using the Remote 1 temperature channel.
- Ambient temperature measured through the Remote 2 temperature channel.
- Bidirectional $\overline{\text{THERM}}$ pin that allows the monitoring of $\overline{\text{PROCHOT}}$ output from an Intel Pentium 4 processor, for example, or can be used as an overtemperature $\overline{\text{THERM}}$ output.

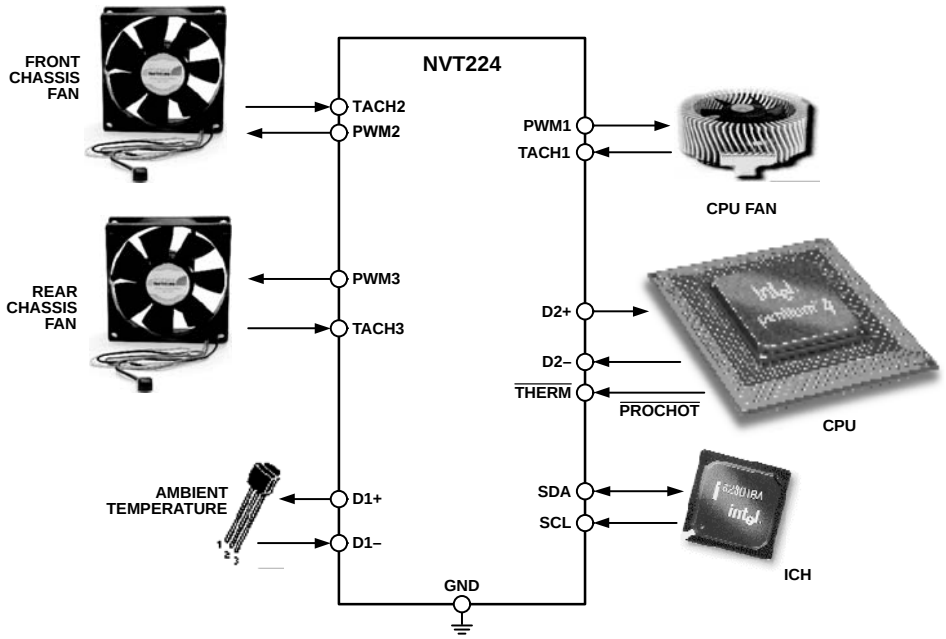


Figure 45. Recommended Implementation 2

Step 2: Configuring the Mux

After the system hardware configuration is determined, the fans can be assigned to particular temperature channels. Not only can fans be assigned to individual channels but the behavior of the fans is also configurable. For example, fans can be run under automatic fan control, manually under software control, or at the fastest speed calculated by multiple temperature channels. The mux is the bridge between temperature measurement channels and the three PWM outputs.

Bits [7:5] (BHVR) of Register 0x5C, Register 0x5D, and Register 0x5E (PWM configuration registers) control the behavior of the fans connected to the PWM1, PWM2, and PWM3 outputs. The values selected for these bits determine how the mux connects a temperature measurement channel to a PWM output.

Automatic Fan Control Mux Options

Bits [7:5] (BHVR), Register 0x5C, Register 0x5D, and Register 0x5E.

000 = Remote 1 temperature controls PWMx
001 = local temperature controls PWMx
010 = Remote 2 temperature controls PWMx
101 = Fastest speed calculated by local and Remote 2 temperature controls PWMx
110 = Fastest speed calculated by all three temperature channel controls PWMx

The fastest speed calculated options pertain to controlling one PWM output based on multiple temperature channels. The thermal characteristics of the three temperature zones can be set to drive a single fan. An example is the fan turning on when Remote 1 temperature exceeds 60°C or when the local temperature exceeds 45°C.

Other Mux Options

Bits [7:5] (BHVR), Register 0x5C, Register 0x5D, and Register 0x5E.

011 = PWMx runs full speed.
100 = PWMx disabled (default).
111 = manual mode. PWMx is running under software control. In this mode, PWM current duty cycle registers (0x30 to 0x32) are writable and control the PWM outputs.

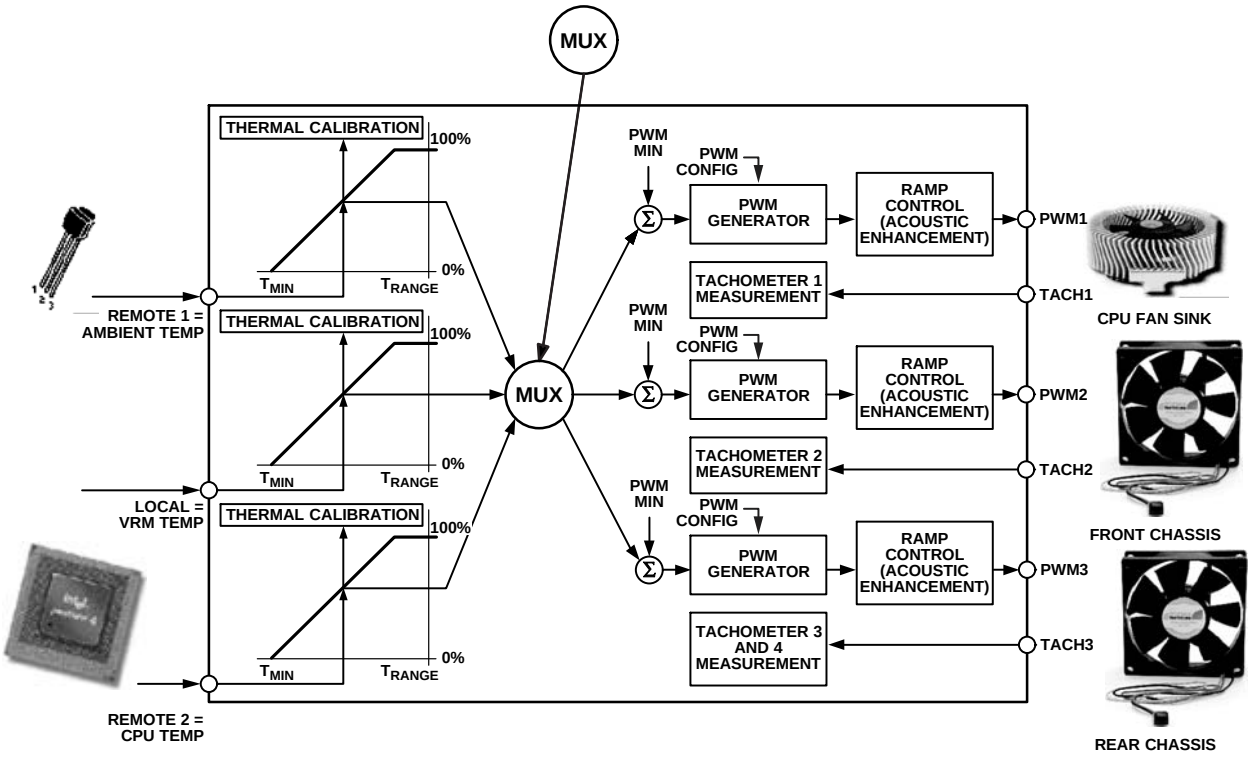


Figure 46. Assigning Temperature Channels to Fan Channels

Mux Configuration Example

This is an example of how to configure the mux in a system using the NVT224 to control three fans. The CPU fan sink is controlled by PWM1, the front chassis fan is controlled by PWM2, and the rear chassis fan is controlled by PWM3. The mux is configured for the following fan control behavior:

- PWM1 (CPU fan sink) is controlled by the fastest speed calculated by the local (VRM temperature) and Remote 2 (processor) Temperatures. In this case, the CPU fan sink is also used to cool the VRM.
- PWM2 (front chassis fan) is controlled by the Remote 1 Temperature (ambient).
- PWM3 (rear chassis fan) is controlled by the Remote 1 Temperature (ambient).

Example Mux Settings

Bits [7:5] (BHVR), PWM1 Configuration Register (0x5C).
101 = Fastest speed calculated by local and Remote 2 temperature controls PWM1

Bits [7:5] (BHVR), PWM2 Configuration Register (0x5D).
000 = Remote 1 temperature controls PWM2

Bits [7:5] (BHVR), PWM3 Configuration Register (0x5E).
000 = Remote 1 temperature controls PWM3

These settings configure the mux, as shown in Figure 47.

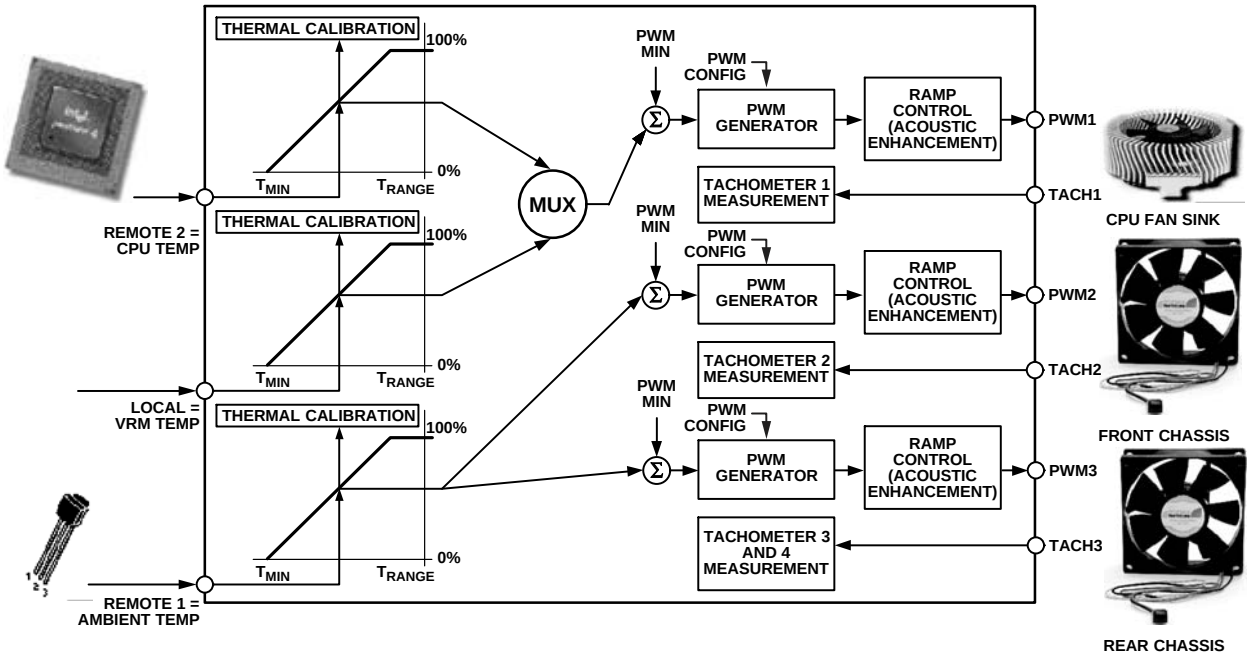


Figure 47. Mux Configuration Example

Step 3: T_{MIN} Settings for Thermal Calibration Channels

T_{MIN} is the temperature at which the fans turn on under automatic fan control. The speed at which the fan runs at T_{MIN} is programmed later in the process. The T_{MIN} values chosen are temperature channel specific, for example, 25°C for ambient channel, 30°C for VRM temperature, and 40°C for processor temperature.

T_{MIN} is an 8−bit value, either twos complement or Offset 64, that can be programmed in 1°C increments. There is a T_{MIN} register associated with each temperature measurement channel: Remote 1, local, and Remote 2 temperatures. Once the T_{MIN} value is exceeded, the fan turns on and runs at the minimum PWM duty cycle. The fan turns off once the temperature has dropped below $T_{MIN} - T_{HYST}$.

To overcome fan inertia, the fan is spun up until two valid TACH rising edges are counted. See the Fan Startup Timeout Section for more details. In some cases, primarily for psycho−acoustic reasons, it is desirable that the fan never switch off below T_{MIN}. Bits [7:5] of Enhanced Acoustics Register 1 (0x62), when set, keep the fans running at the PWM minimum duty cycle, if the temperature should fall below T_{MIN}.

T_{MIN} Registers

Register 0x67, Remote 1 Temperature T_{MIN} = 0x5A (90°C)

Register 0x68, Local Temperature T_{MIN} = 0x5A (90°C)

Register 0x69, Remote 2 Temperature T_{MIN} = 0x5A (90°C)

Enhanced Acoustics Register 1 (0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below $T_{MIN} - T_{HYST}$.

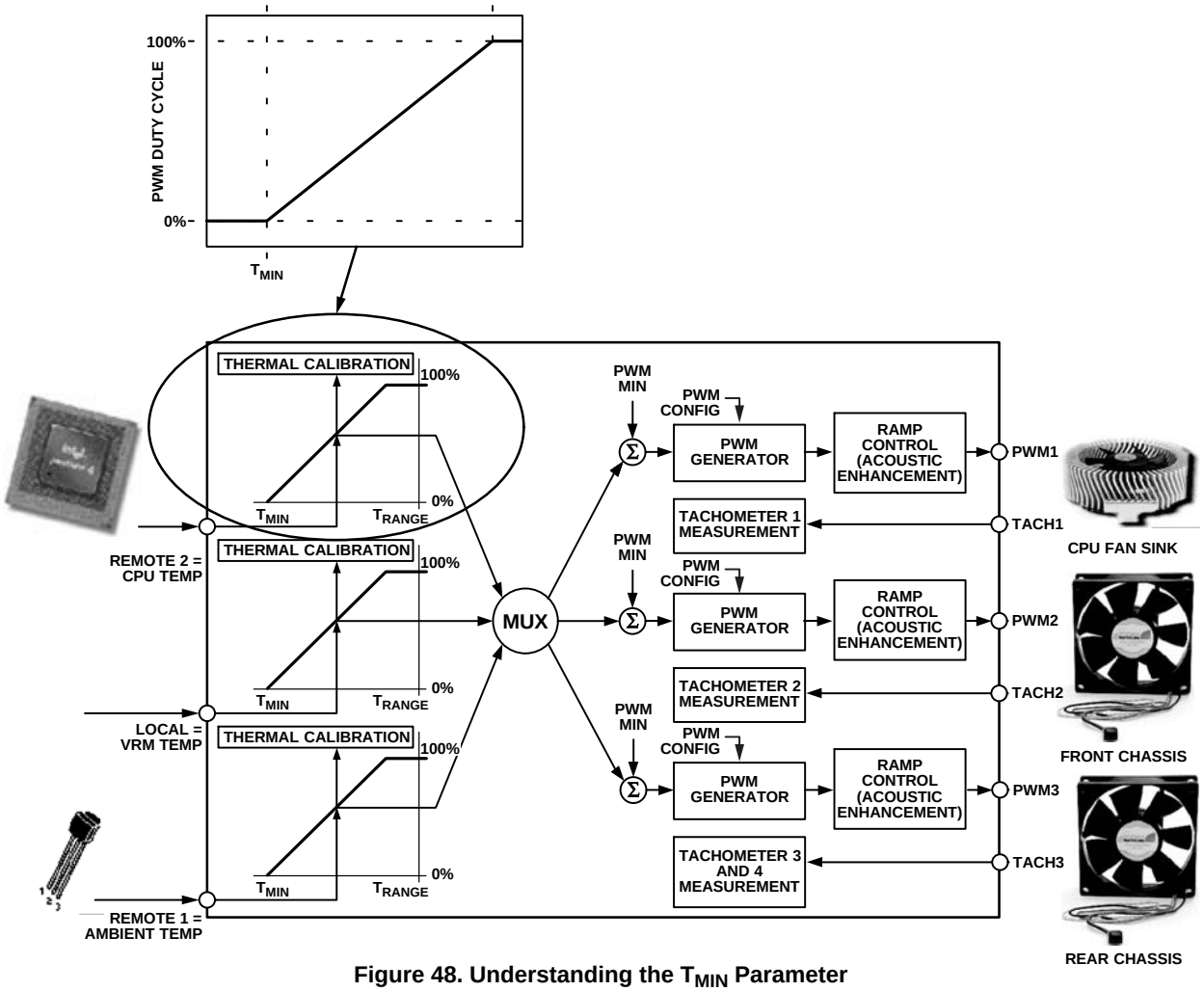


Figure 48. Understanding the T_{MIN} Parameter

Step 4: PWM_{MIN} for Each PWM (Fan) Output

PWM_{MIN} is the minimum PWM duty cycle at which each fan in the system runs. It is also the start speed for each fan under automatic fan control once the temperature rises above TMIN. For maximum system acoustic benefit, PWM_{MIN} should be as low as possible. Depending on the fan used, the PWM_{MIN} setting is usually in the 20% to 33% duty cycle range. This value can be found through fan validation.

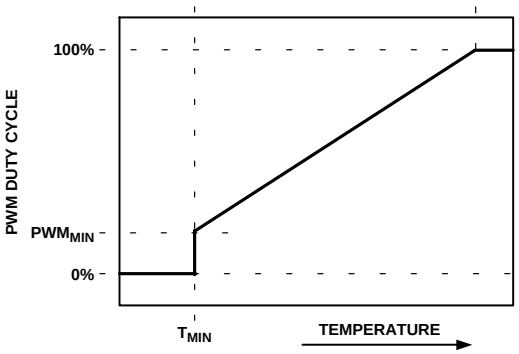


Figure 49. PWM_{MIN} Determines Minimum PWM Duty Cycle

More than one PWM output can be controlled from a single temperature measurement channel. For example, Remote 1 temperature can control PWM1 and PWM2 outputs. If two different fans are used on PWM1 and PWM2, the fan characteristics can be set up differently. As a result, Fan 1 driven by PWM1 can have a different PWM_{MIN} value than Fan 2 connected to PWM2. Figure 50 illustrates this as $PWM1_{MIN}$ (front fan) turns on at a minimum duty cycle of 20%, while $PWM2_{MIN}$ (rear fan) turns on at a minimum of 40% duty cycle. Note that both fans turn on at exactly the same temperature, defined by T_{MIN}.

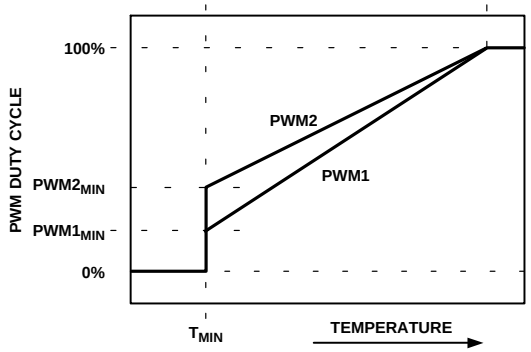


Figure 50. Operating Two Different Fans from a Single Temperature Channel

Programming the PWM_{MIN} Registers

The PWM_{MIN} registers are 8−bit registers that allow the minimum PWM duty cycle for each output to be configured anywhere from 0% to 100%. This allows the minimum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM_{MIN} register is given by:

Value (decimal) = PWM_{MIN} /0.39

Example 1: For a minimum PWM duty cycle of 50%,
Value (decimal) = 50/0.39 = 128 (decimal)
Value = 128 (decimal) or 80 (hex)

Example 2: For a minimum PWM duty cycle of 33%,
Value (decimal) = 33/0.39 = 85 (decimal)
Value = 85 (decimal) or 54 (hex)

PWM_{MIN} Registers

Register 0x64, PWM1 Minimum Duty Cycle = 0x80 (50% default)

Register 0x65, PWM2 Minimum Duty Cycle = 0x80 (50% default)

Register 0x66, PWM3 Minimum Duty Cycle = 0x80 (50% default)

Note on Fan Speed and PWM Duty Cycle

The PWM duty cycle does not directly correlate to fan speed in RPM. Running a fan at 33% PWM duty cycle does not equate to running the fan at 33% speed. Driving a fan at 33% PWM duty cycle actually runs the fan at closer to 50% of its full speed. This is because fan speed in %RPM generally relates to the square root of the PWM duty cycle. Given a PWM square wave as the drive signal, fan speed in RPM approximates to:

$$\%\ \text{fanspeed} = \sqrt{\text{PWM duty cycle} \times 10} \qquad \text{(eq. 4)}$$

Step 5: PWM_{MAX} for PWM (Fan) Outputs

PWM_{MAX} is the maximum duty cycle that each fan in the system runs at under the automatic fan speed control loop. For maximum system acoustic benefit, PWM_{MAX} should be as low as possible but should be capable of maintaining the processor temperature limit at an acceptable level. If the $\overline{\text{THERM}}$ temperature limit is exceeded, the fans are still boosted to 100% for fail−safe cooling.

There is a PWM_{MAX} limit for each fan channel. The default value of all PWM_{MAX} registers is 0xFF.

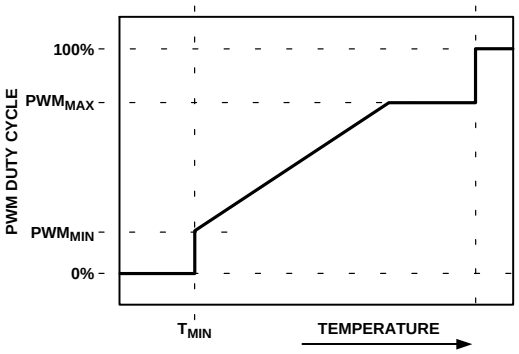


Figure 51. PWM_{MAX} Determines Maximum PWM Duty Cycle Below the $\overline{\text{THERM}}$ Temperature Limit

Programming the PWM_{MAX} Registers

The PWM_{MAX} registers are 8−bit registers that allow the maximum PWM duty cycle for each output to be configured anywhere from 0% to 100%. This allows the maximum PWM duty cycle to be set in steps of 0.39%.

The value to be programmed into the PWM_{MAX} register is given by:

Value (decimal) = PWM_{MAX}/0.39

Example 1: For a maximum PWM duty cycle of 50%,
Value (decimal) − 50/0.39 = 128 (decimal)
Value = 128 (decimal) or 80 (hex)

Example 2: For a minimum PWM duty cycle of 75%,
Value (decimal) = 75/0.39 = 192 (decimal)
Value = 192 (decimal) or C0 (hex)

PWM_{MAX} Registers

Register 0x38, PWM1 Maximum DutyCycle = 0xFF (100% default)

Register 0x39, PWM2 Maximum Duty Cycle = 0xFF (100% default)

Register 0x3A, PWM3 Maximum Duty Cycle = 0xFF (100% default)

Step 6: T_{RANGE} for Temperature Channels

T_{RANGE} is the range of temperature over which automatic fan control occurs once the programmed T_{MIN} temperature has been exceeded. T_{RANGE} is the temperature range between PWM_{MIN} and 100% PWM where the fan speed changes linearly. Otherwise stated, it is the line drawn between the T_{MIN}/PWM_{MIN} and the (T_{MIN} + T_{RANGE}) /PWM 100% intersection points.

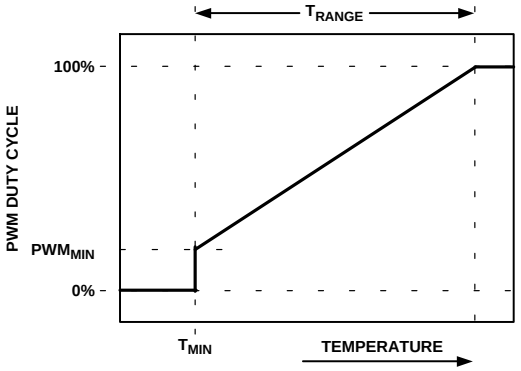


Figure 52. T_{RANGE} Parameter Affects Cooling Slope

The T_{RANGE} is determined by the following procedure:

1. Determine the maximum operating temperature for that channel (for example, 70°C).
2. Determine, experimentally, the fan speed (PWM duty cycle value) that does not exceed the temperature at the worst−case operating points. (For example, 70°C is reached when the fans are running at 50% PWM duty cycle.)
3. Determine the slope of the required control loop to meet these requirements.
4. Using the NVT224 evaluation software, graphically program and visualize this functionality.

As PWM_{MIN} is changed, the automatic fan control slope also changes.

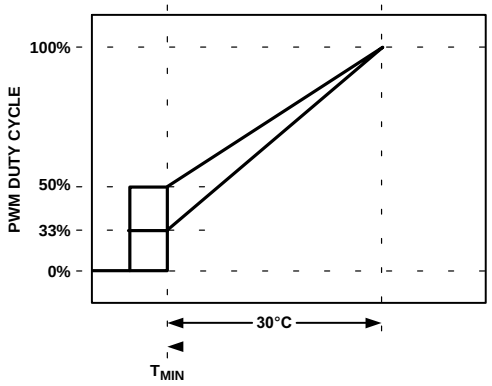


Figure 53. Adjusting PWM_{MIN} Changes the Automatic Fan Control Slope

As T_{RANGE} is changed, the slope also changes. As T_{RANGE} gets smaller, the fans reach 100% speed with a smaller temperature change.

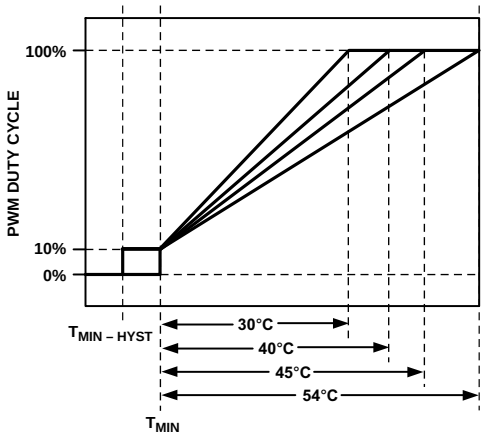


Figure 54. Increasing T_{RANGE} Changes the AFC Slope

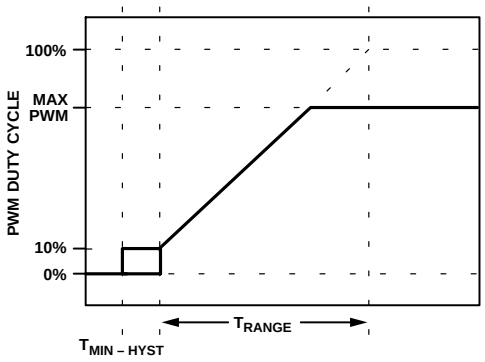


Figure 55. Changing PWM_{MAX} Does Not Change the AFC Slope

Selecting T_{RANGE}

The T_{RANGE} value can be selected for each temperature channel: Remote 1, local, and Remote 2 temperatures. Bits [7:4] (RANGE) of Register 0x5F to Register 0x61 define the T_{RANGE} value for each temperature channel.

Table 10. Selecting a T_{RANGE} Value

Bits [7:4] (Note 1)	**T_{RANGE} (°C)**
0000	2
0001	2.5
0010	3.33
0011	4
0100	5
0101	6.67
0110	8
0111	10
1000	13.33
1001	16
1010	20
1011	26.67
1100	32 (default)
1101	40
1110	53.33
1111	80

1. Register 0x5F configures Remote 1 T_{RANGE}; Register 0x60 configures local T_{RANGE}; Register 0x61 configures Remote 2 T_{RANGE}.

Actual Changes in PWM Output (Advanced Acoustics Settings)

While the automatic fan control algorithm describes the general response of the PWM output, the enhanced acoustics registers (0x62 and 0x63) can be used to set/clamp the maximum rate of change of PWM output for a given temperature zone. This means if T_{RANGE} is programmed with a steep AFC slope, a relatively small change in temperature can cause a large change in PWM output and an audible change in fan speed, which may be noticeable/ annoying to users. Decreasing the PWM output's maximum rate of change, by programming the smoothing on the appropriate temperature channels (Register 0x62 and Register 0x63), clamps the fan speed's maximum rate of change in the event of a temperature spike. The PWM duty cycle increases slowly until the PWM duty cycle reaches the appropriate duty cycle as defined by the AFC curve.

Figure 56 shows PWM duty cycle versus temperature for each T_{RANGE} setting. The lower graph shows how each T_{RANGE} setting affects fan speed vs. temperature. As can be seen from the graph, the effect on fan speed is non−linear.

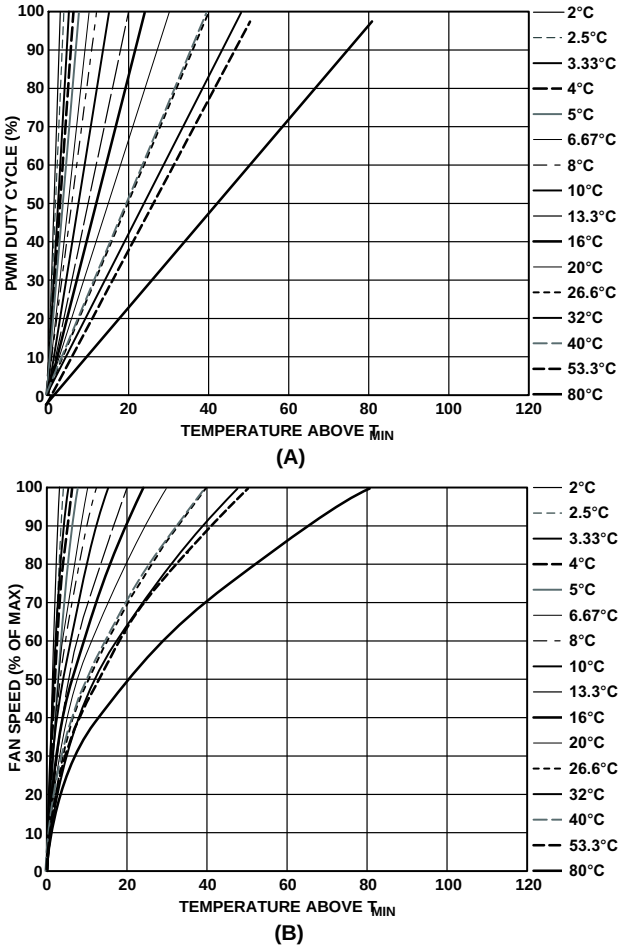


Figure 56. T_{RANGE} vs. Actual Fan Speed (not PWM Drive) Profile

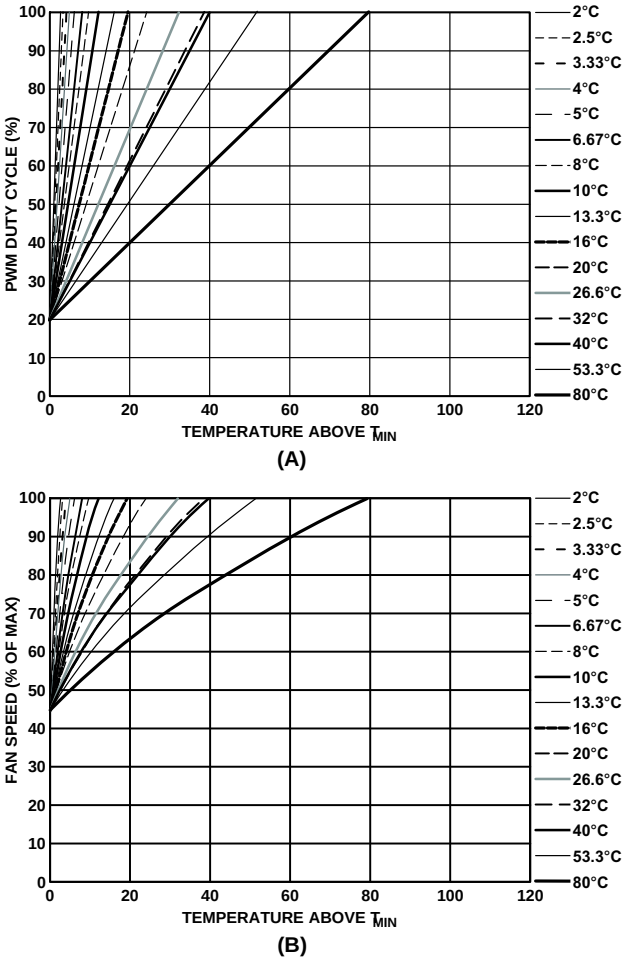


Figure 57. T_{RANGE} and % Fan Speed Slopes with PWM_{MIN} = 20%

The graphs in Figure 56 assume that the fan starts from 0% PWM duty cycle. Clearly, the minimum PWM duty cycle, PWM_{MIN}, needs to be factored in to see how the loop actually performs in the system. Figure 57 shows how T_{RANGE} is affected when the PWM_{MIN} value is set to 20%. It can be seen that the fan actually runs at about 45% fan speed when the temperature exceeds T_{MIN}.

Example: Determining T_{RANGE} for Each Temperature Channel

The following example shows how the different T_{MIN} and T_{RANGE} settings can be applied to three different thermal zones. In this example, the following T_{RANGE} values apply:

T_{RANGE} = 80°C for ambient temperature

T_{RANGE} = 53.33°C for CPU temperature

T_{RANGE} = 40°C for VRM temperature

This example uses the mux configuration described in Step 2: Configuring the Mux, with the NVT224 connected as shown in Figure 47. Both CPU temperature and VRM temperature drive the CPU fan connected to PWM1.

Ambient temperature drives the front chassis fan and rear chassis fan connected to PWM2 and PWM3. The front chassis fan is configured to run at PWM_{MIN} = 20%. The rear chassis fan is configured to run at PWM_{MIN} = 30%. The CPU fan is configured to run at PWM_{MIN} = 10%.

Note that the control range for 4−wire fans is much wider than that for 3−wire fans. In many cases, 4−wire fans can start with a PWM drive of as little as 20% or less. In extreme cases, some 3−wire fans do not run unless a PWM drive of 60% or more is applied.

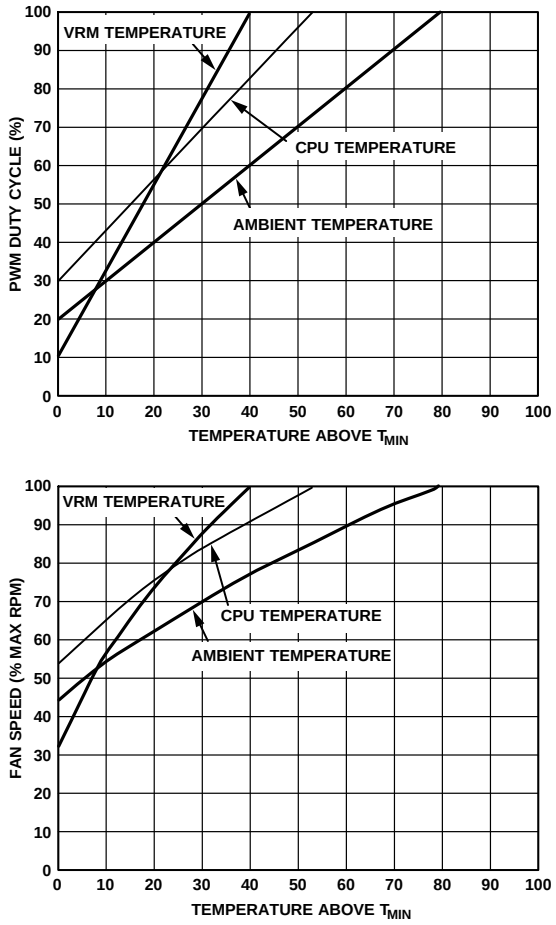


Figure 58. T_{RANGE} and % Fan Speed Slopes for VRM, Ambient, and CPU Temperature Channels

Step 7: $T_{\overline{THERM}}$ for Temperature Channels

$T_{\overline{THERM}}$ is the absolute maximum temperature allowed on a temperature channel. Above this temperature, a component such as the CPU or VRM might be operating beyond its safe operating limit. When the temperature measured exceeds $T_{\overline{THERM}}$, all fans drive at 100% PWM duty cycle (full speed) to provide critical system cooling.

The fans remain running at 100% until the temperature drops below $T_{\overline{THERM}}$ − hysteresis, where hysteresis is the number programmed into the hysteresis registers (0x6D and 0x6E). The default hysteresis value is 4°C.

The $T_{\overline{THERM}}$ limit should be considered the maximum worst−case operating temperature of the system. Because exceeding any $T_{\overline{THERM}}$ limit runs all fans at 100%, it has very negative acoustic effects. Ultimately, this limit should be set up as a fail−safe, and the designer should ensure that it is not exceeded under normal system operating conditions.

Note that $T_{\overline{THERM}}$ limits are non−maskable and affect the fan speed no matter how automatic fan control settings are configured. This allows some flexibility because a T_{RANGE} value can be selected based on its slope, while a hard limit (such as 70°C) can be programmed as T_{MAX} (the temperature at which the fan reaches full speed) by setting $T_{\overline{THERM}}$ to that limit (for example, 70°C).

$\overline{THERM}$ Registers

Register 0x6A, Remote 1 $\overline{THERM}$ Temperature Limit = 0x64 (100°C default)

Register 0x6B, Local $\overline{THERM}$ Temperature Limit = 0x64 (100°C default)

Register 0x6C, Remote 2 $\overline{THERM}$ Temperature Limit = 0x64 (100°C default)

$\overline{THERM}$ Hysteresis

$\overline{THERM}$ hysteresis on a particular channel is configured via the hysteresis settings in Register 0x6D and Register 0x6E. For example, setting hysteresis on the Remote 1 channel also sets the hysteresis on Remote 1 $\overline{THERM}$.

Hysteresis Registers

Register 0x6D, Remote 1 and Local Temperature/T_{MIN} Hysteresis Register

Bits [7:4] (HYSR1), Remote 1 Temperature Hysteresis (4°C default)

Bits [3:0] (HYSL), Local Temperature Hysteresis (4°C default)

Register 0x6E, Remote 2 Temperature T_{MIN} Hysteresis Register

Bits [7:4] (HYSR2), Remote 2 Temperature Hysteresis (4°C default)

Because each hysteresis setting is four bits, hysteresis values are programmable from 1°C to 15°C. It is not recommended that hysteresis values ever be programmed to 0°C because this disables hysteresis. In effect, this causes the fans to cycle (during a $\overline{THERM}$ event) between normal speed and 100% speed or, while operating close to T_{MIN}, between normal speed and off, creating unsettling acoustic noise.

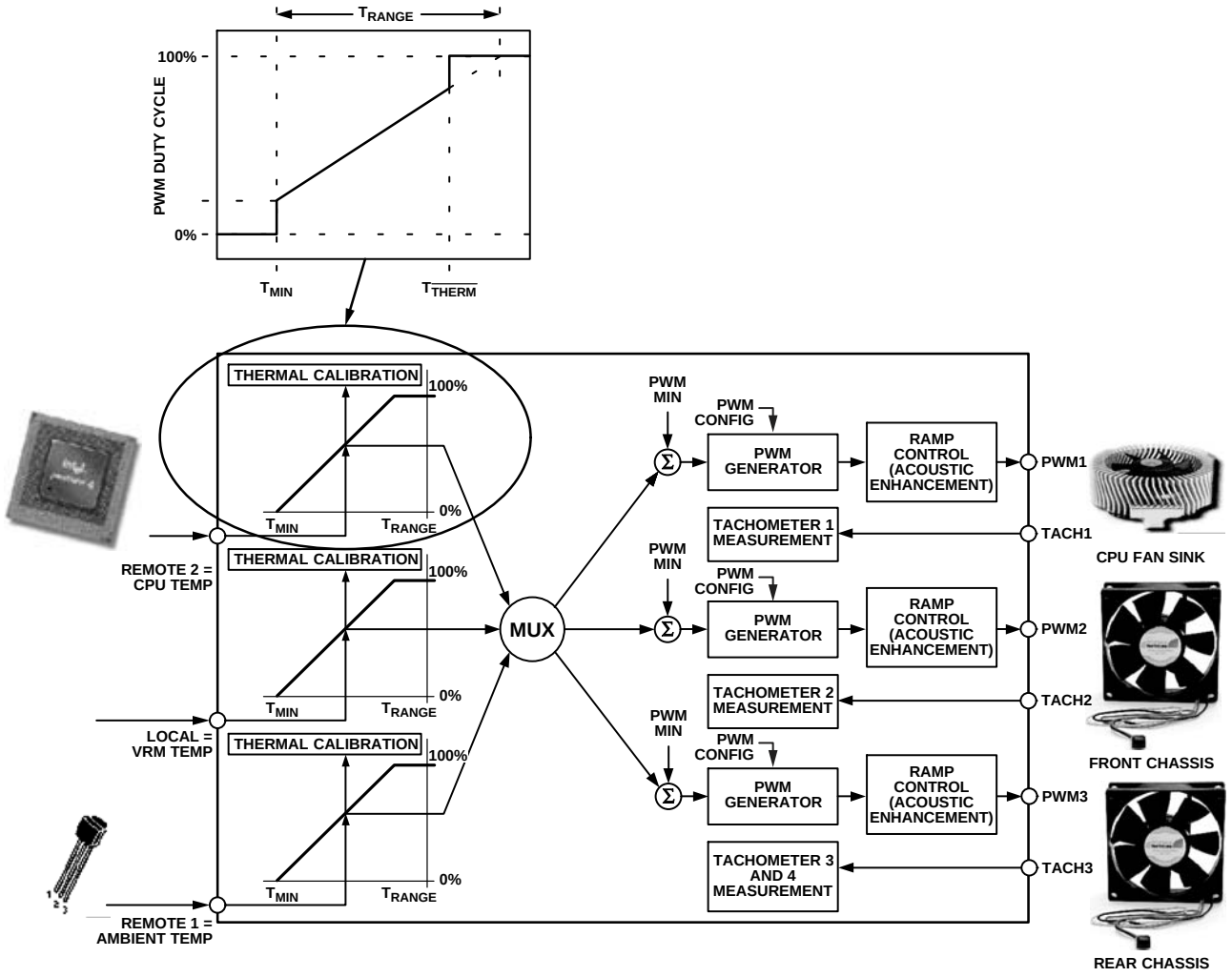


Figure 59. How $T_{\overline{THERM}}$ Relates to Automatic Fan Control

Step 8: T_{HYST} for Temperature Channels

T_{HYST} is the amount of extra cooling a fan provides after the temperature measured has dropped back below T_{MIN} before the fan turns off. The premise for temperature hysteresis (T_{HYST}) is that, without it, the fan would merely chatter, or cycle on and off regularly, whenever the temperature is hovering at about the T_{MIN} setting.

The T_{HYST} value chosen determines the amount of time needed for the system to cool down or heat up as the fan turns on and off. Values of hysteresis are programmable in the range 1°C to 15°C. Larger values of T_{HYST} prevent the fans from chattering on and off. The T_{HYST} default value is set at 4°C.

The T_{HYST} setting applies not only to the temperature hysteresis for fan on/off, but the same setting is used for the $T_{\overline{THERM}}$ hysteresis value, described in Step 6: T_{RANGE} for Temperature Channels. Therefore, programming Register 0x6D and Register 0x6E sets the hysteresis for both fan on/off and the $\overline{THERM}$ function.

In some applications, it is required that fans not turn off below T_{MIN} but remain running at PWM_{MIN}. Bits [7:5] of Enhanced Acoustics Register 1 (0x62) allow the fans to be turned off or to be kept spinning below T_{MIN}. If the fans are always on, the T_{HYST} value has no effect on the fan when the temperature drops below T_{MIN}.

$\overline{THERM}$ Hysteresis

Any hysteresis programmed via Register 0x6D and Register 0x6E also applies to hysteresis on the appropriate $\overline{THERM}$ channel.

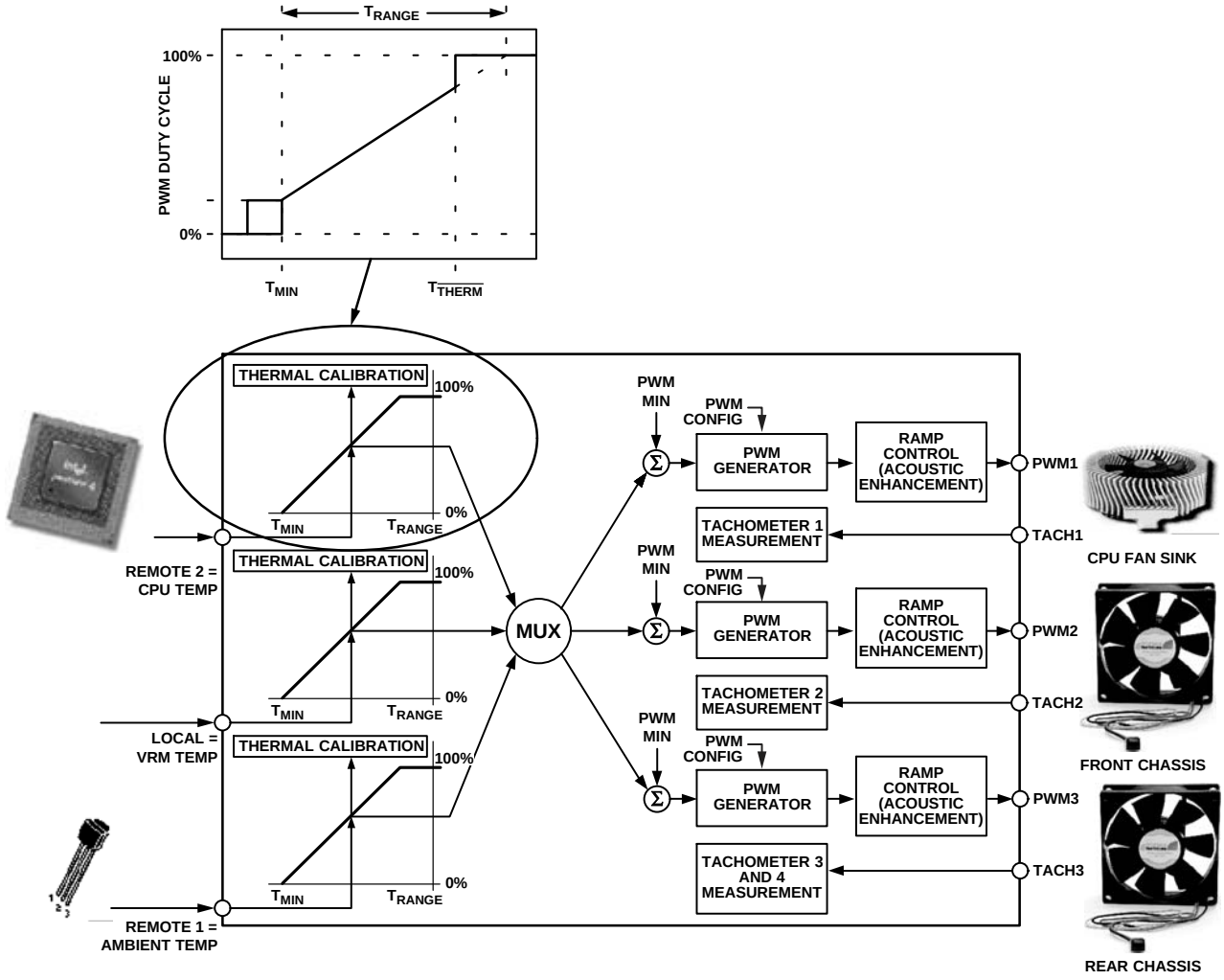


Figure 60. The T_{HYST} Value Applies to Fan On/Off Hysteresis and $\overline{THERM}$ Hysteresis

Enhanced Acoustics Register 1 (0x62)

Bit 7 (MIN3) = 0, PWM3 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 7 (MIN3) = 1, PWM3 runs at PWM3 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 0, PWM2 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 6 (MIN2) = 1, PWM2 runs at PWM2 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 0, PWM1 is off (0% PWM duty cycle) when temperature is below $T_{MIN} - T_{HYST}$.

Bit 5 (MIN1) = 1, PWM1 runs at PWM1 minimum duty cycle below $T_{MIN} - T_{HYST}$.

Configuration Register 6 (0x10)

Bit 0 (SLOW Remote 1), 1 slows the ramp rate for PWM changes associated with the Remote 1 temperature channel by 4.

Bit 1 (SLOW Local), 1 slows the ramp rate for PWM changes associated with the Local temperature channel by 4.

Bit 2 (SLOW Remote 2), 1 slows the ramp rate for PWM changes associated with the Remote 2 temperature channel by 4.

Bit 7 (ExtraSlow), 1 slows the ramp rate for all fans by a factor of 39.2%.

The following sections list the ramp−up times when the SLOW bit is set for each temperature monitoring channel.

Enhanced Acoustics Register 1 (0x62)

Bits [2:0] (ACOU1), select the ramp rate for PWM outputs associated with the Remote 1 temperature input.

000 = 37.5 sec
001 = 18.8 sec
010 = 12.5 sec
011 = 7.5 sec
100 = 4.7 sec
101 = 3.1 sec
110 = 1.6 sec
111 = 0.8 sec

Enhanced Acoustics Register 2 (0x63)

Bits [2:0] (ACOU3), select the ramp rate for PWM outputs associated with the local temperature channel.

000 = 37.5 sec
001 = 18.8 sec
010 = 12.5 sec
011 = 7.5 sec
100 = 4.7 sec
101 = 3.1 sec
110 = 1.6 sec
111 = 0.8 sec

Bits [6:4] (ACOU2), select the ramp rate for PWM outputs associated with the Remote 2 temperature input.

000 = 37.5 sec
001 = 18.8 sec
010 = 12.5 sec
011 = 7.5 sec
100 = 4.7 sec
101 = 3.1 sec
110 = 1.6 sec
111 = 0.8 sec

When Bit 7 of Configuration Register 6 (0x10) = 1, the ramp rates change to the following values:

000 = 52.2 sec
001 = 26.1 sec
010 = 17.4 sec
011 = 10.4 sec
100 = 6.5 sec
101 = 4.4 sec
110 = 2.2 sec
111 = 1.1 sec

Setting the appropriate SLOW bits [2:0] of Configuration Register 6 (0x10) slows the ramp rate further by a factor of 4.

Register Tables

Table 11. NVT224 Registers

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x10	R/W	Configuration Register 6	Extra Slow	V_{CCP} Low	RES	RES	$\overline{\text{THERM}}$ in Manual	SLOW Remote 2	SLOW Local	SLOW Remote 1	0x00	
0x11	R	Configuration Register 7	RES	RES	RES	RES	RES	RES	RES	Dis $\overline{\text{THERM}}$ Hys	0x00	
0x21	R	V_{CCP} Reading	9	8	7	6	5	4	3	2	0x00	
0x22	R	V_{CC} Reading	9	8	7	6	5	4	3	2	0x00	
0x25	R	Remote 1 Temp	9	8	7	6	5	4	3	2	0x80	
0x26	R	Local Temp	9	8	7	6	5	4	3	2	0x80	
0x27	R	Remote 2 Temp	9	8	7	6	5	4	3	2	0x80	
0x28	R	TACH1 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x29	R	TACH1 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2A	R	TACH2 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2B	R	TACH2 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2C	R	TACH3 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2D	R	TACH3 High Byte	15	14	13	12	11	10	9	8	0x00	
0x2E	R	TACH4 Low Byte	7	6	5	4	3	2	1	0	0x00	
0x2F	R	TACH4 High Byte	15	14	13	12	11	10	9	8	0x00	
0x30	R/W	PWM1 Current Duty Cycle	7	6	5	4	3	2	1	0	0x00	
0x31	R/W	PWM2 Current Duty Cycle	7	6	5	4	3	2	1	0	0x00	
0x32	R/W	PWM3 Current Duty Cycle	7	6	5	4	3	2	1	0	0x00	
0x38	R/W	PWM1 Max Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x39	R/W	PWM2 Max Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x3A	R/W	PWM3 Max Duty Cycle	7	6	5	4	3	2	1	0	0xFF	
0x3D	R	Device ID Reg	7	6	5	4	3	2	1	0	0x75	
0x3E	R	Company ID Number	7	6	5	4	3	2	1	0	0x41	
0x40	R/W	Config Reg 1	RES	TODIS	FSPDIS	Vx1	FSPD	RDY	LOCK	STRT	0x05	Yes
0x41	R	Interrupt Status Reg 1	OOL	R2T	LT	R1T	RES	V_{CC}	V_{CCP}	RES	0x00	
0x42	R	Interrupt Status Reg 2	D2	D1	F4P	FAN3	FAN2	FAN1	OVT	RES	0x00	
0x46	R/W	V_{CCP} Low Limit	7	6	5	4	3	2	1	0	0x00	
0x47	R/W	V_{CCP} High Limit	7	6	5	4	3	2	1	0	0xFF	
0x48	R/W	V_{CC} Low Limit	7	6	5	4	3	2	1	0	0x00	

Table 11. NVT224 Registers

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x49	R/W	V_{CC} High Limit	7	6	5	4	3	2	1	0	0xFF	
0x4E	R/W	Remote 1 Temp Low Limit	7	6	5	4	3	2	1	0	0x01	
0x4F	R/W	Remote 1 Temp High Limit	7	6	5	4	3	2	1	0	0xFF	
0x50	R/W	Local Temp Low Limit	7	6	5	4	3	2	1	0	0x01	
0x51	R/W	Local Temp High Limit	7	6	5	4	3	2	1	0	0xFF	
0x52	R/W	Remote 2 Temp Low Limit	7	6	5	4	3	2	1	0	0x01	
0x53	R/W	Remote 2 Temp High Limit	7	6	5	4	3	2	1	0	0xFF	
0x54	R/W	TACH1 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x55	R/W	TACH1 Min High Byte	15	14	13	12	11	10	9	8	0xFF	
0x56	R/W	TACH2 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x57	R/W	TACH2 Min High Byte	15	14	13	12	11	10	9	8	0xFF	
0x58	R/W	TACH3 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x59	R/W	TACH3 Min High Byte	15	14	13	12	11	10	9	8	0xFF	
0x5A	R/W	TACH4 Minimum Low Byte	7	6	5	4	3	2	1	0	0xFF	
0x5B	R/W	TACH4 Min High Byte	15	14	13	12	11	10	9	8	0xFF	
0x5C	R/W	PWM1 Configuration Register	BHVR	BHVR	BHVR	INV	RES	SPIN	SPIN	SPIN	0x82	Yes
0x5D	R/W	PWM2 Configuration Register	BHVR	BHVR	BHVR	INV	RES	SPIN	SPIN	SPIN	0x82	Yes
0x5E	R/W	PWM3 Config Register	BHVR	BHVR	BHVR	INV	RES	SPIN	SPIN	SPIN	0x82	Yes
0x5F	R/W	Remote 1 T_{RANGE}/ PWM1 Freq	RANGE	RANGE	RANGE	RANGE	HF/LF	FREQ	FREQ	FREQ	0xC4	Yes
0x60	R/W	Local T_{RANGE}/ PWM2 Freq	RANGE	RANGE	RANGE	RANGE	HF/LF	FREQ	FREQ	FREQ	0xC4	Yes
0x61	R/W	Remote 2 T_{RANGE}/ PWM3 Freq	RANGE	RANGE	RANGE	RANGE	HF/LF	FREQ	FREQ	FREQ	0xC4	Yes
0x62	R/W	Enhanced Acoustics Reg 1	MIN3	MIN2	MIN1	SYNC	EN1	ACOU1	ACOU1	ACOU1	0x00	Yes
0x63	R/W	Enhanced Acoustics Reg 2	EN2	ACOU2	ACOU2	ACOU2	EN3	ACOU3	ACOU3	ACOU3	0x00	Yes
0x64	R/W	PWM1 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	Yes

Table 11. NVT224 Registers

Addr	R/W	Desc	Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0	De-fault	Lock-able
0x65	R/W	PWM2 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	Yes
0x66	R/W	PWM3 Min Duty Cycle	7	6	5	4	3	2	1	0	0x80	Yes
0x67	R/W	Remote 1 Temp T_{MIN}	7	6	5	4	3	2	1	0	0x5A	Yes
0x68	R/W	Local Temp T_{MIN}	7	6	5	4	3	2	1	0	0x5A	Yes
0x69	R/W	Remote 2 Temp T_{MIN}	7	6	5	4	3	2	1	0	0x5A	Yes
0x6A	R/W	Remote 1 $\overline{\text{THERM}}$ Temp Limit	7	6	5	4	3	2	1	0	0x64	Yes
0x6B	R/W	Local $\overline{\text{THERM}}$ Temp Limit	7	6	5	4	3	2	1	0	0x64	Yes
0x6C	R/W	Remote 2 $\overline{\text{THERM}}$ Temp Limit	7	6	5	4	3	2	1	0	0x64	Yes
0x6D	R/W	Remote 1 and Local Temp/T_{MIN} Hysteresis	HYSR1	HYSR1	HYSR1	HYSR1	HYSL	HYSL	HYSL	HYSL	0x44	Yes
0x6E	R/W	Remote 2 Temp/T_{MIN} Hysteresis	HYSR2	HYSR2	HYSR2	HYSR2	RES	RES	RES	RES	0x40	Yes
0x6F	R/W	XNOR Tree Test Enable	RES	RES	RES	RES	RES	RES	RES	XEN	0x00	Yes
0x70	R/W	Remote 1 Temp Offset	7	6	5	4	3	2	1	0	0x00	Yes
0x71	R/W	Local Temp Offset	7	6	5	4	3	2	1	0	0x00	Yes
0x72	R/W	Remote 2 Temp Offset	7	6	5	4	3	2	1	0	0x00	Yes
0x73	R/W	Config Reg 2	SHDN	CONV	ATTN	AVG	RES	RES	RES	RES	0x00	Yes
0x74	R/W	Interrupt Mask Reg 1	OOL	R2T	LT	R1T	RES	V_{CC}	V_{CCP}	RES	0x00	
0x75	R/W	Interrupt Mask Reg 2	D2	D1	F4P	FAN3	FAN2	FAN1	OVT	RES	0x00	
0x76	R/W	Extended Res 1	RES	RES	V_{CC}	V_{CC}	V_{CCP}	V_{CCP}	RES	RES	0x00	
0x77	R/W	Extended Res 2	TDM2	TDM2	LTMP	LTMP	TDM1	TDM1	RES	RES	0x00	
0x78	R/W	Configuration Reg 3	DC4	DC3	DC2	DC1	FAST	BOOST	$\overline{\text{THERM}}$	$\overline{\text{ALERT}}$ Enable	0x00	Yes
0x79	R	$\overline{\text{THERM}}$ Timer Status Register	TMR	TMR	TMR	TMR	TMR	TMR	TMR	ASRT/ TMRO	0x00	
0x7A	R/W	$\overline{\text{THERM}}$ Timer Limit Register	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	LIMT	0x00	
0x7B	R/W	TACH Pulses per Revolution	FAN4	FAN4	FAN3	FAN3	FAN2	FAN2	FAN1	FAN1	0x55	
0x7C	R/W	Configuration Reg 5	R2 $\overline{\text{THERM}}$ O/P Only	Local $\overline{\text{THERM}}$ O/P Only	R1 $\overline{\text{THERM}}$ O/P Only	RES	GPIOP	GPIOD	Temp Offset	TWOS COMPL	0x01	Yes
0x7D	R/W	Configuration Reg 4	RES	RES	BpAtt V_{CCP}	RES	Max/ Full on $\overline{\text{THERM}}$	$\overline{\text{THERM}}$ Disable	PIN9 FUNC	PIN9 FUNC	0x00	Yes
0x7E	R	Test Reg 1	Do not write to these registers								0x00	Yes
0x7F	R	Test Reg 2	Do not write to these registers								0x00	Yes

Table 12. Register 0x10 — Configuration Register 6 (Power−On Default = 0x00) (Notes 1 and 2)

Bit No.	Mnemonic	R/W	Description
[0]	SLOW Remote 1	R/W	When this bit is set, Fan 1 smoothing times are multiplied x4 for Remote 1 temperature channel (as defined in Register 0x62).
[1]	SLOW Local	R/W	When this bit is set, Fan 2 smoothing times are multiplied x4 for local temperature channel (as defined in Register 0x63).
[2]	SLOW Remote 2	R/W	When this bit is set, Fan 3 smoothing times are multiplied x4 for Remote 2 temperature channel (as defined in Register 0x63).
[3]	$\overline{\text{THERM}}$ in Manual	R/W	When this bit is set, $\overline{\text{THERM}}$ is enabled in manual mode. (Note 1)
[5:4]	Reserved	N/A	Reserved. Do not write to these bits.
[6]	V_{CCP}Low	R/W	V_{CCP}LO = 1. When the power is supplied from 3.3 V STANDBY and the core voltage (V_{CCP}) drops below its V_{CCP} low limit value (Register 0x46), the following occurs: Bit 1 in Interrupt Status Register 1 is set. $\overline{\text{SMBALERT}}$ is generated, if enabled. $\overline{\text{PROCHOT}}$ monitoring is disabled. Everything is re−enabled once V_{CCP} increases above the V_{CCP} low limit. When V_{CCP} increases above the low limit: $\overline{\text{PROCHOT}}$ monitoring is enabled. Fans return to their programmed state after a spin−up cycle.
[7]	ExtraSlow	R/W	When this bit is set, all fan smoothing times are increased by a further 39.2%.

1. A $\overline{\text{THERM}}$ event always overrides any fan setting (even when fans are disabled).
2. This register becomes read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 13. Register 0x11 — Configuration Register 7 (Power−On Default = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[0]	Dis $\overline{\text{THERM}}$ Hys	R/W	Setting this bit to 1 disables $\overline{\text{THERM}}$ hysteresis.
[7:1]	Reserved	N/A	Reserved. Do not write to these bits

1. This register becomes read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 14. Voltage Reading Registers (Power−On Default = 0x00) (Notes 1 and 2)

Register Address	R/W	Description
0x21	Read−only	Reflects the voltage measurement at the V_{CCP} input on Pin 14 (8 MSBs of reading).
0x22	Read−only	Reflects the voltage measurement at the V_{CC} input on Pin 3 (8 MSBs of reading).

1. If the extended resolution bits of these readings are also read, the extended resolution registers (Reg. 0x76, Reg. 0x77) must be read first. Once the extended resolution registers are read, the associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.
2. V_{CC} (Pin 3) is the supply voltage for the NVT224.

Table 15. Temperature Reading Registers (Power−On Default = 0x80) (Notes 1 and 2)

Register Address	R/W	Description
0x25	Read−only	Remote 1 temperature reading (8 MSBs of reading). (Notes 3 and 4)
0x26	Read−only	Local temperature reading (8 MSBs of reading).
0x27	Read−only	Remote 2 temperature reading (8 MSBs of reading).

1. These temperature readings can be in twos complement or Offset 64 format; this interpretation is determined by Bit 0 of Configuration Register 5 (0x7C).
2. If the extended resolution bits of these readings are also read, the extended resolution registers (0x76 and 0x77) must be read first. Once the extended resolution registers are read, all associated MSB reading registers are frozen until read. Both the extended resolution registers and the MSB registers are frozen.
3. In twos complement mode, a temperature reading of −128°C (0x80) indicates a diode fault (open or short) on that channel.
4. In Offset 64 mode, a temperature reading of −64°C (0x00) indicates a diode fault (open or short) on that channel.

Table 16. Fan Tachometer Reading Registers (Power−On Default = 0x00) (Note 1)

Register Address	R/W	Description
0x28	Read−only	TACH1 low byte.
0x29	Read−only	TACH1 high byte.
0x2A	Read−only	TACH2 low byte.
0x2B	Read−only	TACH2 high byte.
0x2C	Read−only	TACH3 low byte.
0x2D	Read−only	TACH3 high byte.
0x2E	Read−only	TACH4 low byte.
0x2F	Read−only	TACH4 high byte.

1. These registers count the number of 11.11 μs periods (based on an internal 90 kHz clock) that occur between a number of consecutive fan TACH pulses (default = 2). The number of TACH pulses used to count can be changed using the TACH pulses per revolution register (0x7B). This allows the fan speed to be accurately measured. Because a valid fan tachometer reading requires that two bytes be read, the low byte must be read first. Both the low and high bytes are then frozen until read. At power−on, these registers contain 0x0000 until the first valid fan TACH measurement is read into these registers. This prevents false interrupts from occurring while the fans are spinning up.
   A count of 0xFFFF indicates that a fan is one of the following:
   - Stalled or blocked (object jamming the fan).
   - Failed (internal circuitry destroyed).
   - Not populated. (The NVT224 expects to see a fan connected to each TACH. If a fan is not connected to that TACH, its TACH minimum high and low bytes should be set to 0xFFFF.)
   - Alternate function, for example, TACH4 reconfigured as a $\overline{\text{THERM}}$ pin.).

Table 17. Current PWM Duty Cycle Registers (Power−On Default = 0x00) (Note 1)

Register Address	R/W	Description
0x30	R/W	PWM1 current duty cycle (0% to 100% duty cycle = 0x00 to 0xFF).
0x31	R/W	PWM2 current duty cycle (0% to 100% duty cycle = 0x00 to 0xFF).
0x32	R/W	PWM3 current duty cycle (0% to 100% duty cycle = 0x00 to 0xFF).

1. These registers reflect the PWM duty cycle driving each fan at any given time. When in automatic fan speed control mode, the NVT224 reports the PWM duty cycles back through these registers. The PWM duty cycle values vary according to temperature in automatic fan speed control mode. During fan startup, these registers report back 0x00. In software mode, the PWM duty cycle outputs can be set to any duty cycle value by writing to these registers.

Table 18. Maximum PWM Duty Cycle Registers (Power−On Default = 0xFF) (Notes 1 and 2)

Register Address	R/W	Description
0x38	R/W	Maximum duty cycle for PWM1 output, default = 100% (0xFF).
0x39	R/W	Maximum duty cycle for PWM2 output, default = 100% (0xFF).
0x3A	R/W	Maximum duty cycle for PWM3 output, default = 100% (0xFF).

1. This register becomes read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to this register fail.
2. These registers set the maximum PWM duty cycle of the PWM output.

Table 19. Register 0x40 — Configuration Register 1 (Power−On Default = 0x04)

Bit No.	Mnemonic	R/W	Description
[0]	STRT (Notes 1, 2)	R/W	Logic 1 enables monitoring and PWM control outputs based on the limit settings programmed. Logic 0 disables monitoring and PWM control based on the default powerup limit settings. Note that the limit values programmed are preserved even if a Logic 0 is written to this bit and the default settings are enabled. This bit does not become locked once Bit 1 (LOCK) has been set.
[1]	LOCK	Write Once	Logic 1 locks all limit values to their current settings. Once this bit is set, all lockable registers become read−only and cannot be modified until the NVT224 is powered down and powered up again. This prevents rogue programs such as viruses from modifying critical system limit settings. This bit is lockable.
[2]	RDY	Read−only	This bit is set to 1 by the NVT224 to indicate only that the device is fully powered up and ready to begin system monitoring.
[3]	FSPD	R/W	When set to 1, this bit runs all fans at max speed as programmed in the PWM current duty cycle registers (0x30 to 0x32). Power−on default = 0. This bit is not locked at any time.
[4]	Vx1	R/W	BIOS should set this bit to a 1 when the NVT224 is configured to measure current from the controller and to measure the CPU's core voltage. This bit allows monitoring software to display CPU watts usage. This bit is lockable.
[5]	FSPDIS	R/W	Logic 1 disables fan spin−up for two TACH pulses. Instead, the PWM outputs go high for the entire fan spin−up timeout selected.
[6]	TODIS	R/W	When this bit is set to 1, the SMBus timeout feature is disabled. This allows the NVT224 to be used with SMBus controllers that cannot handle SMBus timeouts. This bit is lockable.
[7]	RES		Reserved.

1. Bit 0 (STRT) of Configuration Register 1 (0x40) remains writable after the lock bit is set.
2. When monitoring is disabled, PWM outputs always go to 100% for thermal protection.

Table 20. Register 0x41 — Interrupt Status Register 1 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W	Description
[1]	V_{CCP}	Read−only	V_{CCP} = 1 indicates that the V_{CCP} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[2]	V_{CC}	Read−only	V_{CC} = 1 indicates that the V_{CC} high or low limit has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[4]	R1T	Read−only	R1T = 1 indicates that the Remote 1 low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[5]	LT	Read−only	LT = 1 indicates that the local low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[6]	R2T	Read−only	R2T = 1 indicates that the Remote 2 low or high temperature has been exceeded. This bit is cleared on a read of the status register only if the error condition has subsided.
[7]	OOL	Read−only	OOL = 1 indicates that an out−of−limit event has been latched in Interrupt Status Register 2. This bit is a logical OR of all status bits in Interrupt Status Register 2. Software can test this bit in isolation to determine whether any of the voltage, temperature, or fan speed readings represented by Interrupt Status Register 2 are out−of−limit, which saves the need to read Interrupt Status Register 2 every interrupt or polling cycle.

Table 21. Register 0x42 — Interrupt Status Register 2 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W	Description
[1]	OVT	Read−only	OVT = 1 indicates that one of the $\overline{\text{THERM}}$ overtemperature limits has been exceeded. This bit is cleared on a read of the status register when the temperature drops below $\overline{\text{THERM}}$ – T_{HYST}.
[2]	FAN1	Read−only	FAN1 = 1 indicates that Fan 1 has dropped below minimum speed or has stalled. This bit is not set when the PWM1 output is off.
[3]	FAN2	Read−only	FAN2 = 1 indicates that Fan 2 has dropped below minimum speed or has stalled. This bit is not set when the PWM2 output is off.
[4]	FAN3	Read−only	FAN3 = 1 indicates that Fan 3 has dropped below minimum speed or has stalled. This bit is not set when the PWM3 output is off.
[5]	F4P	Read−only	F4P = 1 indicates that Fan 4 has dropped below minimum speed or has stalled. This bit is not set when the PWM3 output is off.
		R/W	When Pin 9 is programmed as a GPIO output, writing to this bit determines the logic output of the GPIO.
		Read−only	If Pin 9 is configured as the $\overline{\text{THERM}}$ timer input for $\overline{\text{THERM}}$ monitoring, this bit is set when the $\overline{\text{THERM}}$ assertion time exceeds the limit programmed in the $\overline{\text{THERM}}$ timer limit register (0x7A).
[6]	D1	Read−only	D1 = 1 indicates either an open or short circuit on the Thermal Diode 1 inputs.
[7]	D2	Read−only	D2 = 1 indicates either an open or short circuit on the Thermal Diode 2 inputs.

Table 22. Voltage Limit Registers (Note 1)

Register Address	R/W	Description (Note 2)	Power−On Default
0x46	R/W	V_{CCP} low limit.	0x00
0x47	R/W	V_{CCP} high limit.	0xFF
0x48	R/W	V_{CC} low limit.	0x00
0x49	R/W	V_{CC} high limit.	0xFF

1. Setting the Configuration Register 1 lock bit has no effect on these registers.
2. High limits: an interrupt is generated when a value exceeds its high limit (> comparison); low limits: an interrupt is generated when a value is equal to or below its low limit (≤ comparison).

Table 23. Temperature Limit Registers (Note 1)

Register Address	R/W	Description (Note 2)	Power−On Default
0x4E	R/W	Remote 1 temperature low limit.	0x81
0x4F	R/W	Remote 1 temperature high limit.	0x7F
0x50	R/W	Local temperature low limit.	0x81
0x51	R/W	Local temperature high limit.	0x7F
0x52	R/W	Remote 2 temperature low limit.	0x81
0x53	R/W	Remote 2 temperature high limit.	0x7F

1. Exceeding any of these temperature limits by 1°C causes the appropriate status bit to be set in the interrupt status register. Setting the Configuration Register 1 lock bit has no effect on these registers.
2. High limits: an interrupt is generated when a value exceeds its high limit (> comparison); low limits: an interrupt is generated when a value is equal to or below its low limit (≤ comparison).

Table 24. Fan Tachometer Limit Registers (Note 1)

Register Address	R/W	Description	Power−On Default
0x54	R/W	TACH1 minimum low byte.	0xFF
0x55	R/W	TACH1 minimum high byte/single−channel ADC channel select.	0xFF
0x56	R/W	TACH2 minimum low byte.	0xFF
0x57	R/W	TACH2 minimum high byte.	0xFF
0x58	R/W	TACH3 minimum low byte.	0xFF
0x59	R/W	TACH3 minimum high byte.	0xFF
0x5A	R/W	TACH4 minimum low byte.	0xFF
0x5B	R/W	TACH4 minimum high byte.	0xFF

1. Exceeding any of the TACH limit registers by 1 indicates that the fan is running too slowly or has stalled. The appropriate status bit is set in Interrupt Status Register 2 to indicate the fan failure. Setting the Configuration Register 1 lock bit has no effect on these registers.

Table 25. Register 0x55 — TACH1 Minimum High Byte (Power−On Default = 0xFF)

Bit No.	Mnemonic	R/W	Description
[4:0]	Reserved	Read−only	These bits are reserved when Bit 6 of Configuration Register 2 (0x73) is set (single−channel ADC mode). Otherwise, these bits represent Bits [4:0] of the TACH1 minimum high byte register.
[7:5]	SCADC	R/W	When Bit 6 of Configuration Register 2 (0x73) is set (single−channel ADC mode), these bits are used to select the only channel from which the ADC makes measurements. Otherwise, these bits represent Bits [7:5] of the TACH1 minimum high byte register.

Table 26. PWM Configuration Registers (Note 1)

Register Address	R/W	Description	Power−On Default
0x5C	R/W	PWM1 configuration.	0x62
0x5D	R/W	PWM2 configuration.	0x62
0x5E	R/W	PWM3 configuration.	0x62

1. These registers become read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 27. Register 0x05C, Register 0x5D, and Register 0x5E — PWM Configuration Registers (Power−On Default = 0x62)

Bit No.	Mnemonic	R/W	Description
[2:0]	SPIN	R/W	These bits control the startup timeout for PWMx. The PWM output stays high until two valid TACH rising edges are seen from the fan. If there is not a valid TACH signal during the fan TACH measurement directly after the fan startup timeout period, the TACH measurement reads 0xFFFF and Interrupt Status Register 2 reflects the fan fault. If the TACH minimum high and low bytes contain 0xFFFF or 0x0000, the Interrupt Status Register 2 bit is not set, even if the fan has not started. 000 = No startup timeout 001 = 100 ms 010 = 250 ms (default) 011 = 400 ms 100 = 667 ms 101 = 1 sec 110 = 2 sec 111 = 4 sec
[4]	INV	R/W	This bit inverts the PWM output. The default is 0, which corresponds to a logic high output for 100% duty cycle. Setting this bit to 1 inverts the PWM output so that 100% duty cycle corresponds to a logic low output.
[7:5]	BHVR	R/W	These bits assign each fan to a particular temperature sensor for localized cooling. 000 = Remote 1 temperature controls PWMx (automatic fan control mode). 001 = Local temperature controls PWMx (automatic fan control mode). 010 = Remote 2 temperature controls PWMx (automatic fan control mode). 011 = PWMx runs full speed. 100 = PWMx disabled (default). 101 = Fastest speed calculated by local and Remote 2 temperature controls PWMx. 110 = Fastest speed calculated by all three temperature channel controls PWMx. 111 = Manual Mode. PWM duty cycle registers (0x30 to 0x32) become writable.

Table 28. Temp T_{RANGE}/PWM Frequency Registers (Note 1)

Register Address	R/W	Description	Power−On Default
0x5F	R/W	Remote 1 T_{RANGE}/PWM1 frequency.	0xC4
0x60	R/W	Local T_{RANGE}/PWM2 frequency.	0xC4
0x61	R/W	Remote 2 T_{RANGE}/PWM3 frequency.	0xC4

1. These registers become read−only when the Configuration Register 1 lock bit is set. Any subsequent attempts to write to these registers fail.

Table 29. Register 0x05F, Register 0x60, and Register 0x61 — Temp T_{RANGE}/PWM Frequency Registers (Power−On Default = 0xC4)

Bit No.	Mnemonic	R/W	Description
[2:0]	FREQ	R/W	These bits control the PWMx frequency. 000 = 11.0 Hz 001 = 14.7 Hz 010 = 22.1 Hz 011 = 29.4 Hz 100 = 35.3 Hz (default) 101 = 44.1 Hz 110 = 58.8 Hz 111 = 88.2 Hz
[3]	HF/LF	R/W	HF/LF =1, enables high frequency PWM output for 4−wire fans. Once enabled, 3−wire fan specific settings have no effect (this means, pulse stretching).
[7:4]	RANGE	R/W	These bits determine the PWM duty cycle vs. the temperature slope for automatic fan control. 0000 = 2°C 0001 = 2.5°C 0010 = 3.33°C 0011 = 4°C 0100 = 5°C 0101 = 6.67°C 0110 = 8°C 0111 = 10°C 1000 = 13.33°C 1001 = 16°C 1010 = 20°C 1011 = 26.67°C 1100 = 32°C (default) 1101 = 40°C 1110 = 53.33°C 1111 = 80°C

Table 30. Register 0x62 — Enhanced Acoustics Register 1 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
[2:0]	ACOU1	R/W	Assuming that PWMx is associated with the Remote 1 temperature channel, these bits define the maximum rate of change of the PWMx output for Remote 1 temperature related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan.
			When Bit 7 of Configuration Register 6 (0x10) is 0
			Time Slot Increase / **Time for 0% to 100%** 000 = 1 — 37.5 sec 001 = 2 — 18.8 sec 010 = 3 — 12.5 sec 011 = 4 — 7.5 sec 100 = 8 — 4.7 sec 101 = 12 — 3.1 sec 110 = 24 — 1.6 sec 111 = 48 — 0.8 sec
			When Bit 7 of Configuration Register 6 (0x10) is 1
			Time Slot Increase / **Time for 0% to 100%** 000 = 1 — 52.2 sec 001 = 2 — 26.1 sec 010 = 3 — 17.4 sec 011 = 4 — 10.4 sec 100 = 8 — 6.5 sec 101 = 12 — 4.4 sec 110 = 24 — 2.2 sec 111 = 48 — 1.1 sec
[3]	EN1	R/W	When this bit is 1, smoothing is enabled on the Remote 1 temperature channel.
[4]	SYNC	R/W	SYNC = 1 synchronizes fan speed measurements on TACH2, TACH3, and TACH4 to PWM3. This allows up to three fans to be driven from PWM3 output and their speeds to be measured. SYNC = 0 synchronizes only TACH3 and TACH4 to PWM3 output.
[5]	MIN1	R/W	When the NVT224 is in automatic fan control mode, this bit defines whether PWM1 is off (0% duty cycle) or at PWM1 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value. 0 = 0% duty cycle below T_{MIN} – hysteresis. 1 = PWM1 minimum duty cycle below T_{MIN} – hysteresis.
[6]	MIN2	R/W	When the NVT224 is in automatic fan speed control mode, this bit defines whether PWM2 is off (0% duty cycle) or at PWM2 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value. 0 = 0% duty cycle below T_{MIN} – hysteresis. 1 = PWM 2 minimum duty cycle below T_{MIN} – hysteresis.
[7]	MIN3	R/W	When the NVT224 is in automatic fan speed control mode, this bit defines whether PWM3 is off (0% duty cycle) or at PWM3 minimum duty cycle when the controlling temperature is below its T_{MIN} – hysteresis value. 0 = 0% duty cycle below T_{MIN} – hysteresis. 1 = PWM3 minimum duty cycle below T_{MIN} – hysteresis.

1. This register becomes read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 31. Register 0x63 — Enhanced Acoustics Register 2 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description	
[2:0]	ACOU3	R/W	Assuming that PWMx is associated with the local temperature channel, these bits define the maximum rate of change of the PWMx output for local temperature related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan.	
			When Bit 7 of Configuration Register 6 (0x10) is 0	
			Time Slot Increase	**Time for 0% to 100%**
			000 = 1 001 = 2 010 = 3 011 = 4 100 = 8 101 = 12 110 = 24 111 = 48	37.5 sec 18.8 sec 12.5 sec 7.5 sec 4.7 sec 3.1 sec 1.6 sec 0.8 sec
			When Bit 7 of Configuration Register 6 (0x10) is 1	
			Time Slot Increase	**Time for 0% to 100%**
			000 = 1 001 = 2 010 = 3 011 = 4 100 = 8 101 = 12 110 = 24 111 = 48	52.2 sec 26.1 sec 17.4 sec 10.4 sec 6.5 sec 4.4 sec 2.2 sec 1.1 sec
[3]	EN3	R/W	When this bit is 1, smoothing is enabled on the Local temperature channel.	
[6:4]	ACOU2	R/W	Assuming that PWMx is associated with the Remote 2 temperature channel, these bits define the maximum rate of change of the PWMx output for Remote 2 temperature related changes. Instead of the fan speed jumping instantaneously to its newly determined speed, it ramps gracefully at the rate determined by these bits. This feature ultimately enhances the acoustics of the fan.	
			When Bit 7 of Configuration Register 6 (0x10) is 0	
			Time Slot Increase	**Time for 0% to 100%**
			000 = 1 001 = 2 010 = 3 011 = 4 100 = 8 101 = 12 110 = 24 111 = 48	37.5 sec 18.8 sec 12.5 sec 7.5 sec 4.7 sec 3.1 sec 1.6 sec 0.8 sec
			When Bit 7 of Configuration Register 6 (0x10) is 1	
			Time Slot Increase	**Time for 0% to 100%**
			000 = 1 001 = 2 010 = 3 011 = 4 100 = 8 101 = 12 110 = 24 111 = 48	52.2 sec 26.1 sec 17.4 sec 10.4 sec 6.5 sec 4.4 sec 2.2 sec 1.1 sec
[7]	EN2	R/W	When this bit is 1, smoothing is enabled on the Remote 2 temperature channel.	

1. This register becomes read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to this register fail.

Table 32. PWM Minimum Duty Cycle Registers (Note 1)

Register Address	R/W	Description	Power−On Default
0x64	R/W	PWM1 minimum duty cycle.	0x80 (50% duty cycle)
0x65	R/W	PWM2 minimum duty cycle.	0x80 (50% duty cycle)
0x66	R/W	PWM3 minimum duty cycle.	0x80 (50% duty cycle)

1. These registers become read−only when the NVT224 is in automatic fan control mode.

Table 33. Register 0x64, Register 0x65, Register 0x66 — PWM Minimum Duty Cycle Registers (Power−On Default = 0x80; 50% Duty Cycle)

Bit No.	Mnemonic	R/W	Description
[7:0]	PWM Duty Cycle	R/W	These bits define the PWM_{MIN} duty cycle for PWMx. 0x00 = 0% duty cycle (fan off). 0x40 = 25% duty cycle. 0x80 = 50% duty cycle. 0xFF = 100% duty cycle (fan full speed).

Table 34. T_{MIN} Registers (Note 1 and 2)

Register Address	R/W	Description	Power−On Default
0x67	R/W	Remote 1 temperature T_{MIN}	0x5A (90°C)
0x68	R/W	Local temperature T_{MIN}	0x5A (90°C)
0x69	R/W	Remote 2 temperature T_{MIN}	0x5A (90°C)

1. These are the T_{MIN} registers for each temperature channel. When the temperature measured exceeds T_{MIN}, the appropriate fan runs at minimum speed and increases with temperature according to T_{RANGE}.
2. These registers become read−only when the Configuration Register 1 lock bit is set. Any subsequent attempts to write to these registers fail.

Table 35. $\overline{\text{THERM}}$ Temperature Limit Registers (Note 1)

Register Address	R/W (Note 2)	Description	Power−On Default
0x6A	R/W	Remote 1 $\overline{\text{THERM}}$ temperature limit.	0x64 (100°C)
0x6B	R/W	Local $\overline{\text{THERM}}$ temperature limit.	0x64 (100°C)
0x6C	R/W	Remote 2 $\overline{\text{THERM}}$ temperature limit.	0x64 (100°C)

1. If any temperature measured exceeds its $\overline{\text{THERM}}$ limit, all PWM outputs drive their fans at 100% duty cycle. This is a fail−safe mechanism incorporated to cool the system in the event of a critical overtemperature. It also ensures some level of cooling in the event that software or hardware locks up. If set to 0x80, this feature is disabled. The PWM output remains at 100% until the temperature drops below a $\overline{\text{THERM}}$ Limit − Hysteresis. If the $\overline{\text{THERM}}$ pin is programmed as an output, then exceeding these limits by 0.25°C can cause the $\overline{\text{THERM}}$ pin to assert low as an output.
2. These registers become read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 36. Temperature/T_{MIN} Hysteresis Registers (Note 1)

Register Address	R/W (Note 2)	Bit Name	Description	Power−On Default
0x6D	R/W	HYSL [3:0]	Remote 1 and local temperature hysteresis. Local temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the local temperature and AFC loops.	0x44
		HYSR1 [7:4]	Remote 1 temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the Remote 1 temperature and AFC loops.	
0x6E	R/W	HYSR2 [7:4]	Remote 2 temperature hysteresis. Local temperature hysteresis. 0°C to 15°C of hysteresis can be applied to the local temperature and AFC loops.	0x40

1. Each 4−bit value controls the amount of temperature hysteresis applied to a particular temperature channel. Once the temperature for that channel falls below its T_{MIN} value, the fan remains running at PWM_{MIN} duty cycle until the temperature = T_{MIN} − hysteresis. Up to 15°C of hysteresis can be assigned to any temperature channel. The hysteresis value chosen also applies to that temperature channel, if its $\overline{\text{THERM}}$ limit is exceeded. The PWM output being controlled goes to 100%, if the $\overline{\text{THERM}}$ limit is exceeded and remains at 100% until the temperature drops below $\overline{\text{THERM}}$ − hysteresis. For acoustic reasons, it is recommended that the hysteresis value not be programmed to less than 4°C. Setting the hysteresis value lower than 4°C causes the fan to switch on and off regularly when the temperature is close to T_{MIN}.
2. These registers become read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 37. XNOR Tree Test Enable Register

Register Address	R/W (Note 1)	Bit Name	Description	Power−On Default
0x6F	R/W	XEN [0]	XNOR tree test enable register. If the XEN bit is set to 1, the device enters the XNOR tree test mode. Clearing the bit removes the device from the XNOR tree test mode.	0x00
		RES [7:1]	Unused. Do not write to these bits.	

1. These registers become read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 38. Remote 1 Temperature Offset Register

Register Address	R/W (Note 1)	Bit Name	Description	Power−On Default
0x70	R/W	[7:0]	Remote 1 temperature offset. Allows a twos complement offset value to be automatically added to or subtracted from the Remote 1 temperature reading. This is to compensate for any inherent system offsets such as PCB trace resistance. LSB value = 0.5°C.	0x00

1. These registers become read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 39. Local Temperature Offset Register

Register Address	R/W (Note 1)	Bit Name	Description	Power−On Default
0x71	R/W	[7:0]	Local temperature offset. Allows a twos complement offset value to be automatically added to or subtracted from the local temperature reading. LSB value = 0.5°C.	0x00

1. These registers become read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 40. Remote 2 Temperature Offset Register (Note 1)

Register Address	R/W	Bit Name	Description	Power−On Default
0x72	R/W	[7:0]	Remote 2 temperature offset. Allows a twos complement offset value to be automatically added to or subtracted from the Remote 2 temperature reading. This is to compensate for any inherent system offsets such as PCB trace resistance. LSB value = 0.5°C.	0x00

1. These registers become read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 41. Register 0x73 — Configuration Register 2 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
[0:3]	RES		Reserved.
[4]	AVG	R/W	AVG = 1, averaging on the temperature and voltage measurements is turned off. This allows measurements on each channel to be made much faster.
[5]	ATTN	R/W	ATTN = 1, the NVT224 removes the attenuators from the V_{CCP} input. The V_{CCP} input can be used for other functions such as connecting up external sensors.
[6]	CONV	R/W	CONV = 1, the NVT224 is put into a single−channel ADC conversion mode. In this mode, the NVT224 can be made to read continuously from one input only, for example, Remote 1 temperature. The appropriate ADC channel is selected by writing to Bits [7:5] of TACH1 minimum high byte register (0x55).
			Register 0x55, Bits [7:5]
			000 Reserved 001 V_{CCP} 010 V_{CC} (3.3 V) 011 Reserved 100 Reserved 101 Remote 1 temperature 110 Local temperature 111 Remote 2 temperature
[7]	SHDN	R/W	SHDN = 1, NVT224 goes into shutdown mode. All PWM outputs assert low (or high depending on state of the INV bit) to switch off all fans. The PWM current duty cycle registers read 0x00 to indicate that the fans are not being driven.

1. These registers become read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 42. Register 0x74 — Interrupt Mask Register 1 (Power−On Default <7:0> = 0x00)

Bit No.	Mnemonic	R/W	Description
[1]	V_{CCP}	R/W	V_{CCP} = 1, masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the V_{CCP} channel.
[2]	V_{CC}	R/W	V_{CC} = 1, masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the V_{CC} channel.
[4]	R1T	R/W	R1T = 1, masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the Remote 1 temperature channel.
[5]	LT	R/W	LT = 1, masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the local temperature channel.
[6]	R2T	R/W	R2T = 1, masks $\overline{\text{SMBALERT}}$ for out−of−limit conditions on the Remote 2 temperature channel.
[7]	OOL	R/W	OOL = 0, when one or more alerts are generated in Interrupt Status Register 2, assuming that all the mask bits in the Interrupt Mask Register 2 (0x75) = 1, $\overline{\text{SMBALERT}}$ is still asserted. OOL = 1, when one or more alerts are generated in Interrupt Status Register 2, assuming that all the mask bits in the Interrupt Mask Register 2 (0x75) = 1, $\overline{\text{SMBALERT}}$ is not asserted.

Table 43. Register 0x75 — Interrupt Mask Register 2 (Power−On Default <7:0> = 0x00)

Bit No.	Mnemonic	R/W	Description
[1]	OVT	Read−only	OVT = 1, masks $\overline{\text{SMBALERT}}$ for overtemperature $\overline{\text{THERM}}$ conditions.
[2]	FAN1	R/W	FAN1 = 1, masks $\overline{\text{SMBALERT}}$ for a Fan 1 fault.
[3]	FAN2	R/W	FAN2 = 1, masks $\overline{\text{SMBALERT}}$ for a Fan 2 fault.
[4]	FAN3	R/W	FAN3 = 1, masks $\overline{\text{SMBALERT}}$ for a Fan 3 fault.
[5]	F4P	R/W	F4P = 1, masks $\overline{\text{SMBALERT}}$ for a Fan 4 fault. If the TACH4 pin is being used as the $\overline{\text{THERM}}$ input, this bit masks $\overline{\text{SMBALERT}}$ for a $\overline{\text{THERM}}$ timer event.
[6]	D1	R/W	D1 = 1, masks $\overline{\text{SMBALERT}}$ for a diode open or short on a Remote 1 channel.
[7]	D2	R/W	D2 = 1, masks $\overline{\text{SMBALERT}}$ for a diode open or short on a Remote 2 channel.

Table 44. Register 0x76 — Extended Resolution Register 1 (Note 1)

Bit No.	Mnemonic	R/W	Description
[3:2]	V_{CCP}	R/W	V_{CCP} LSBs. Holds the 2 LSBs of the 10−bit V_{CCP} measurement.
[5:4]	V_{CC}	R/W	V_{CC} LSBs. Holds the 2 LSBs of the 10−bit V_{CC} measurement.

1. If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 45. Register 0x77 — Extended Resolution Register 2 (Note 1)

Bit No.	Mnemonic	R/W	Description
[3:2]	TDM1	R/W	Remote 1 temperature LSBs. Holds the 2 LSBs of the 10−bit Remote 1 temperature measurement.
[5:4]	LTMP	R/W	Local temperature LSBs. Holds the 2 LSBs of the 10−bit local temperature measurement.
[7:6]	TDM2	R/W	Remote 2 temperature LSBs. Holds the 2 LSBs of the 10−bit Remote 2 temperature measurement.

1. If this register is read, this register and the registers holding the MSB of each reading are frozen until read.

Table 46. Register 0x78 — Configuration Register 3 (Power−On Default = 0x00) (Note 1)

Bit No.	Mnemonic	R/W	Description
[0]	$\overline{\text{ALERT}}$ Enable	R/W	$\overline{\text{ALERT}}$ = 1, Pin 5 (PWM2/$\overline{\text{SMBALERT}}$) is configured as an $\overline{\text{SMBALERT}}$ interrupt output to indicate out−of−limit error conditions.
[1]	$\overline{\text{THERM}}$	R/W	$\overline{\text{THERM}}$ Enable = 1 enables $\overline{\text{THERM}}$ timer monitoring functionality on Pin 9. Also determined by Bit 0 and Bit 1 (PIN9FUNC) of Configuration Register 4. When $\overline{\text{THERM}}$ is asserted, if the fans are running and the boost bit is set, the fans run at full speed. Alternatively, $\overline{\text{THERM}}$ can be programmed so that a timer is triggered to time how long $\overline{\text{THERM}}$ has been asserted.
[2]	BOOST	R/W	When $\overline{\text{THERM}}$ is an input and BOOST = 1, assertion of $\overline{\text{THERM}}$ causes all fans to run at the maximum programmed duty cycle for fail−safe cooling.
[3]	FAST	R/W	FAST = 1, enables fast TACH measurements on all channels. This increases the TACH measurement rate from once per second to once every 250 ms (4x).
[4]	DC1	R/W	DC1 = 1, enables TACH measurements to be continuously made on TACH1. Fans must be driven by dc. Setting this bit prevents pulse stretching because it is not required for dc−driven motors.
[5]	DC2	R/W	DC2 = 1, enables TACH measurements to be continuously made on TACH2. Fans must be driven by dc. Setting this bit prevents pulse stretching because it is not required for dc−driven motors.
[6]	DC3	R/W	DC3 = 1, enables TACH measurements to be continuously made on TACH3. Fans must be driven by dc. Setting this bit prevents pulse stretching because it is not required for dc−driven motors.
[7]	DC4	R/W	DC4 = 1, enables TACH measurements to be continuously made on TACH4. Fans must be driven by dc. Setting this bit prevents pulse stretching because it is not required for dc−driven motors.

1. These registers become read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 47. Register 0x79 — $\overline{\text{THERM}}$ Timer Status Register (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W	Description
[0]	ASRT/ TMR0	Read−only	This bit is set high on the assertion of the $\overline{\text{THERM}}$ input and is cleared on read. If the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms, this bit is set and becomes the LSB of the 8−bit TMR reading. This allows $\overline{\text{THERM}}$ assertion times from 45.52 ms to 5.82 sec to be reported back with a resolution of 22.76 ms.
[7:1]	TMR	Read−only	Times how long $\overline{\text{THERM}}$ input is asserted. These seven bits read zero until the $\overline{\text{THERM}}$ assertion time exceeds 45.52 ms.

Table 48. $\overline{\text{THERM}}$ Timer Limit Register (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W	Description
[7:0]	LIMT	R/W	Sets the maximum $\overline{\text{THERM}}$ assertion length allowed before an interrupt is generated. This is an 8−bit limit with a resolution of 22.76 ms allowing $\overline{\text{THERM}}$ assertion limits of 45.52 ms to 5.82 sec to be programmed. If the $\overline{\text{THERM}}$ assertion time exceeds this limit, Bit 5 (F4P) of Interrupt Status Register 2 (0x42) is set. If the limit value is 0x00, an interrupt is generated immediately on the assertion of the $\overline{\text{THERM}}$ input.

Table 49. Register 0x7B — TACH Pulses per Revolution Register (Power−On Default = 0x55)

Bit No.	Mnemonic	R/W	Description
[1:0]	FAN1	R/W	Sets the number of pulses to be counted when measuring Fan 1 speed. Can be used to determine fan pulses per revolution for an unknown fan type. Pulses Counted 00 = 1 01 = 2 (default) 10 = 3 11 = 4
[3:2]	FAN2	R/W	Sets the number of pulses to be counted when measuring Fan 2 speed. Can be used to determine fan pulses per revolution for an unknown fan type. Pulses Counted 00 = 1 01 = 2 (default) 10 = 3 11 = 4
[5:4]	FAN3	R/W	Sets the number of pulses to be counted when measuring Fan 3 speed. Can be used to determine fan pulses per revolution for an unknown fan type. Pulses Counted 00 = 1 01 = 2 (default) 10 = 3 11 = 4
[7:6]	FAN4	R/W	Sets the number of pulses to be counted when measuring Fan 4 speed. Can be used to determine fan pulses per revolution for an unknown fan type. Pulses Counted 00 = 1 01 = 2 (default) 10 = 3 11 = 4

Table 50. Register 0x7C — Configuration Register 5 (Power−On Default = 0x01)

Bit No.	Mnemonic	R/W (Note 1)	Description
[0]	TWOS COMPL	R/W	Twos complement = 1, sets the temperature range to twos complement temperature range. Twos complement = 0, changes the temperature range to Offset 64. When this bit is changed, the NVT224 interprets all relevant temperature register values as defined by this bit.
[1]	TempOffset	R/W	TempOffset = 0, sets offset range to −63°C to +64°C with 0.5°C resolution. TempOffset = 1, sets offset range to −63°C to +127°C with 1°C resolution. These settings apply to the 0x70, 0x71, and 0x72 registers (Remote 1, local, and Remote 2 temperature offset registers).
[2]	GPIOD	R/W	GPIO direction. When the GPIO function is enabled, this determines whether the GPIO is an input (0) or an output (1).
[3]	GPIOP	R/W	GPIO polarity. When the GPIO function is enabled and is programmed as an output, this bit determines whether the GPIO is active low (0) or high (1).
[4]	RES		Reserved.
[5]	R1 $\overline{\text{THERM}}$	R/W	R1 $\overline{\text{THERM}}$ = 0, $\overline{\text{THERM}}$ temperature limit functionality is enabled for the Remote 1 temperature channel. $\overline{\text{THERM}}$ can also be disabled on any channel by the following: In offset 64 mode, writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit. In twos complement mode, writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit.
[6]	Local $\overline{\text{THERM}}$	R/W	Local $\overline{\text{THERM}}$ = 0, $\overline{\text{THERM}}$ temperature limit functionality enabled for local temperature channel. $\overline{\text{THERM}}$ can also be disabled on any channel by the following: In Offset 64 mode, writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit. In twos complement mode, writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit.
[7]	R2 $\overline{\text{THERM}}$	R/W	R2 $\overline{\text{THERM}}$ = 0, $\overline{\text{THERM}}$ temperature limit functionality enabled for Remote 2 temperature channel. $\overline{\text{THERM}}$ can also be disabled on any channel by the following: In offset 64 mode, writing 64°C to the appropriate $\overline{\text{THERM}}$ temperature limit. In twos complement mode, writing 128°C to the appropriate $\overline{\text{THERM}}$ temperature limit.

1. These registers become read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 51. Register 0x7D — Configuration Register 4 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W (Note 1)	Description
[1:0]	PIN9FUNC	R/W	These bits set the functionality of Pin 9: 00 = TACH4 (default) 01 = Bidirectional $\overline{\text{THERM}}$ 10 = $\overline{\text{SMBALERT}}$ 11 = GPIO
[2]	$\overline{\text{THERM}}$ Disable	R/W	$\overline{\text{THERM}}$ Disable = 0, $\overline{\text{THERM}}$ overtemperature output is enabled assuming $\overline{\text{THERM}}$ is correctly configured (Register 0x78, Register 0x7C, and Register 0x7D). $\overline{\text{THERM}}$ Disable = 1, $\overline{\text{THERM}}$ overtemperature output is disabled on all channels. $\overline{\text{THERM}}$ can also be disabled on any channel by the following: In Offset 64 mode, writing −64°C to the appropriate $\overline{\text{THERM}}$ temperature limit. In twos complement mode, writing −128°C to the appropriate $\overline{\text{THERM}}$ temperature limit.
[3]	Max/Full on $\overline{\text{THERM}}$	R/W	Max/Full on $\overline{\text{THERM}}$ = 0. When $\overline{\text{THERM}}$ limit is exceeded, fans go to full speed. Max/Full on $\overline{\text{THERM}}$ = 1. When $\overline{\text{THERM}}$ limit is exceeded, fans go to maximum speed as defined in Register 0x38, Register 0x39, and Register 0x3A.
[4:7]	RES		Unused.
[5]	BpAttV_{CCP}	R/W	Bypass V_{CCP} attenuator. When set, the measurement scale for this channel changes from 0 V (0x00) to 2.2965 V (0xFF).
[6:7]	RES		Unused.

1. These registers become read−only when the Configuration Register 1 lock bit is set to 1. Any subsequent attempts to write to these registers fail.

Table 52. Register 0x7E — Manufacturer's Test Register 1 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W	Description
[7:0]	Reserved	Read−only	Manufacturer's test register. These bits are reserved for manufacturer's test purposes and should not be written to under normal operation.

Table 53. Register 0x7F — Manufacturer's Test Register 2 (Power−On Default = 0x00)

Bit No.	Mnemonic	R/W	Description
[7:0]	Reserved	Read−only	Manufacturer's test register. These bits are reserved for manufacturer's test purposes and should not be written to under normal operation.

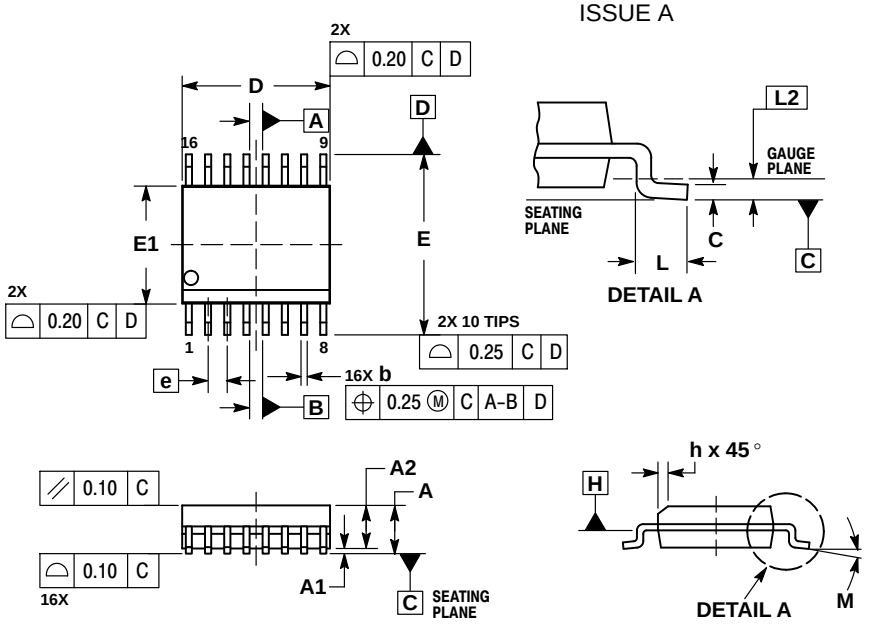
ORDERING INFORMATION

Device Number	Temperature Range	Package Option	Package	Shipping†
NVT224ARQZ	−40°C to +125°C	RQ−16	16−Lead QSOP (Pb−Free)	98 Units / Rail
NVT224ARQZ−REEL	−40°C to +125°C	RQ−16	16−Lead QSOP (Pb−Free)	2500 / Tape & Reel
NVT224ARQZ−RL7	−40°C to +125°C	RQ−16	16−Lead QSOP (Pb−Free)	1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.
*The "Z" suffix indicates Pb−Free part.

PACKAGE DIMENSIONS

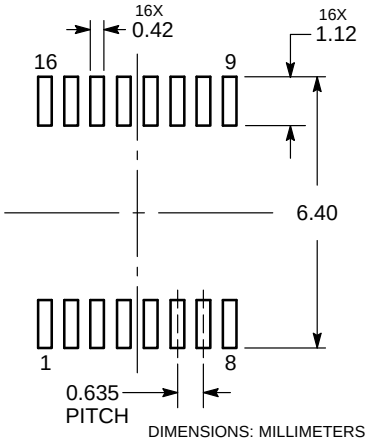
QSOP16
CASE 492
ISSUE A



NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b DOES NOT INCLUDE DAMBAR PROTRUSION.
4. DIMENSION D DOES NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.005 PER SIDE. DIMENSION E1 DOES NOT INCLUDE INTERLEAD FLASH OR PROTRUSION. INTERLEAD FLASH OR PROTRUSION SHALL NOT EXCEED 0.005 PER SIDE. D AND E1 ARE DETERMINED AT DATUM H.
5. DATUMS A AND B ARE DETERMINED AT DATUM H.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.053	0.069	1.35	1.75
A1	0.004	0.010	0.10	0.25
A2	0.049	----	1.24	----
b	0.008	0.012	0.20	0.30
c	0.007	0.010	0.19	0.25
D	0.193 BSC		4.89 BSC	
E	0.237 BSC		6.00 BSC	
E1	0.154 BSC		3.90 BSC	
e	0.025 BSC		0.635 BSC	
h	0.009	0.020	0.22	0.50
L	0.016	0.050	0.40	1.27
L2	0.010 BSC		0.25 BSC	
M	0 °	8 °	0 °	8 °

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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