

## FEATURES

- RS-485 transceiver with electrical data isolation**
- Complies with ANSI TIA/EIA-485-A and ISO 8482: 1987(E)**
- 500 kbps data rate**
- Slew rate-limited driver outputs**
- Low power operation: 2.5 mA maximum**
- Suitable for 5 V or 3.3 V operations ( $V_{DD1}$ )**
- High common-mode transient immunity: >25 kV/ $\mu$ s**
- True fail-safe receiver inputs**
- Chatter-free power-up/power-down protection**
- 256 nodes on bus**
- Thermal shutdown protection**
- Safety and regulatory approvals**
  - UL recognition: 2500 V rms for 1 minute per UL 1577
  - VDE certificates of conformity
  - DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12
  - $V_{IORM} = 560$  V peak
- Operating temperature range:  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$**

## APPLICATIONS

- Low power RS-485/RS-422 networks
- Isolated interfaces
- Building control networks
- Multipoint data transmission systems

## GENERAL DESCRIPTION

The ADM2481 differential bus transceiver is an integrated, galvanically isolated component designed for bidirectional data communication on balanced, multipoint bus transmission lines. It complies with ANSI EIA/TIA-485-A and ISO 8482: 1987(E). Using *i*Coupler® technology from Analog Devices, Inc., the ADM2481 combines a 3-channel isolator, a three-state differential line driver, and a differential input receiver into a single package. The logic side of the device is powered with either a 5 V or 3 V supply, and the bus side uses a 5 V supply only.

The ADM2481 is slew-limited to reduce reflections with improperly terminated transmission lines. The controlled slew rate limits the data rate to 500 kbps. The input impedance of the device is 96 k $\Omega$ , allowing up to 256 transceivers on the bus. Its driver has an active-high enable feature. The driver differential outputs and receiver differential inputs are connected internally

## FUNCTIONAL BLOCK DIAGRAM

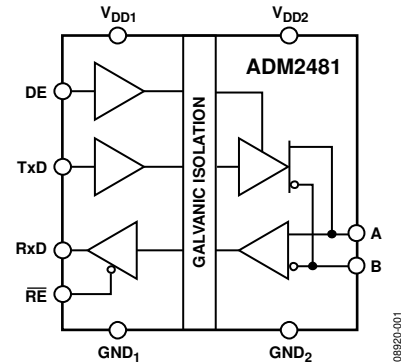


Figure 1.

08920-001

to form a differential input/output (I/O) port. When the driver is disabled or when  $V_{DD1}$  or  $V_{DD2} = 0$  V, this imposes minimal loading on the bus. An active-high receiver disable feature, which causes the receiver output to enter a high impedance state, is provided as well.

The receiver inputs have a true fail-safe feature that ensures a logic-high receiver output level when the inputs are open or shorted. This guarantees that the receiver outputs are in a known state before communication begins and at the point when communication ends.

Current limiting and thermal shutdown features protect against output short circuits and bus contention situations that might cause excessive power dissipation. The part is fully specified over the industrial temperature range of  $-40^{\circ}\text{C}$  to  $+85^{\circ}\text{C}$  and is available in a 16-lead, wide body SOIC package.

Rev. B

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## REVISION HISTORY

### 4/2018—Rev. A to Rev. B

Change to Minimum External Air Gap (Clearance) Parameter, Value Column, Table 5 .....	4
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### 6/2012—Rev. 0 to Rev. A

Updated Safety and Regulatory Approvals (Throughout) .....	1
Updated Outline Dimensions .....	17
Changes to Ordering Guide .....	17

### 7/2010—Revision 0: Initial Version

## SPECIFICATIONS

$3.0\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ ,  $4.75\text{ V} \leq V_{DD2} \leq 5.25\text{ V}$ ,  $T_A = T_{MIN}$  to  $T_{MAX}$ , unless otherwise noted.

Table 1.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
<b>DRIVER</b>						
Differential Outputs						
Differential Output Voltage				5	V	$R_L = \infty$ , see Figure 16
	$V_{OD}$	2.0		5	V	$R_L = 50\ \Omega$ (RS-422), see Figure 16
	$V_{OD}$	1.5		5	V	$R_L = 27\ \Omega$ (RS-485), see Figure 16
	$V_{OD3}$	1.5		5	V	$V_{TEST} = -7\text{ V to } +12\text{ V}$ , $V_{DD1} \geq 4.75$ , see Figure 17
$\Delta  V_{OD} $ for Complementary Output States				0.2	V	$R_L = 27\ \Omega$ or $50\ \Omega$ , see Figure 16
Common-Mode Output Voltage	$V_{OC}$			3	V	$R_L = 27\ \Omega$ or $50\ \Omega$ , see Figure 16
$\Delta  V_{OC} $ for Complementary Output States				0.2	V	$R_L = 27\ \Omega$ or $50\ \Omega$ , see Figure 16
Output Short-Circuit Current,	$I_{SC}$					
$V_{OUT} = \text{High}$		-250		+250	mA	$-7\text{ V} \leq V_{OUT} \leq +12\text{ V}$
$V_{OUT} = \text{Low}$		-250		+250	mA	$-7\text{ V} \leq V_{OUT} \leq +12\text{ V}$
<b>Logic Inputs</b>						
Input High Voltage	$V_{IH}$	$0.7 V_{DD1}$			V	TxD, DE, $\overline{RE}$
Input Low Voltage	$V_{IL}$			$0.25 V_{DD1}$	V	TxD, DE, $\overline{RE}$
CMOS Logic Input Current (TxD, DE, $\overline{RE}$ )	$I_I$	-10	+0.01	+10	$\mu\text{A}$	TxD, DE, $\overline{RE} = V_{DD1}$ or 0 V
<b>RECEIVER</b>						
<b>Differential Inputs</b>						
Differential Input Threshold Voltage	$V_{TH}$	-200	-125	-30	mV	$-7\text{ V} \leq V_{CM} \leq +12\text{ V}$
Input Hysteresis	$V_{HYS}$		20		mV	$-7\text{ V} \leq V_{CM} \leq +12\text{ V}$
Input Resistance (A, B)		96	150		k $\Omega$	$-7\text{ V} \leq V_{CM} \leq +12\text{ V}$
Input Current (A, B)				0.125	mA	$V_{IN} = 12\text{ V}$
				-0.1	mA	$V_{IN} = -7\text{ V}$
<b>RxD Logic Output</b>						
Output High Voltage	$V_{OH}$	$V_{DD1} - 0.1$			V	$I_{OUT} = 20\ \mu\text{A}$ , $V_A - V_B = 0.2\text{ V}$
		$V_{DD1} - 0.4$	$V_{DD1} - 0.2$		V	$I_{OUT} = 4\text{ mA}$ , $V_A - V_B = 0.2\text{ V}$
Output Low Voltage	$V_{OL}$			0.1	V	$I_{OUT} = -20\ \mu\text{A}$ , $V_A - V_B = -0.2\text{ V}$
				0.4	V	$I_{OUT} = -4\text{ mA}$ , $V_A - V_B = -0.2\text{ V}$
Output Short-Circuit Current	$I_{SC}$	7		85	mA	$V_{OUT} = \text{GND or } V_{CC}$
Three-State Output Leakage Current				$\pm 1$	$\mu\text{A}$	$0.4\text{ V} \leq V_{OUT} \leq 2.4\text{ V}$
<b>POWER SUPPLY CURRENT</b>						
Logic Side	$I_{DD1}$			2.5	mA	$4.5\text{ V} \leq V_{DD1} \leq 5.5\text{ V}$ , outputs unloaded, $\overline{RE} = 0\text{ V}$
				1.3	mA	$3.0\text{ V} \leq V_{DD1} \leq 3.6\text{ V}$ , outputs unloaded, $\overline{RE} = 0\text{ V}$
Bus Side	$I_{DD2}$			2.0	mA	Outputs unloaded, DE = 5 V
				1.7	mA	Outputs unloaded, DE = 0 V
COMMON-MODE TRANSIENT IMMUNITY <sup>1</sup>	$V_{CM}$	25			kV/ $\mu\text{s}$	TxD = $V_{DD1}$ or 0 V, $V_{CM} = 1\text{ kV}$ , transient magnitude = 800 V

<sup>1</sup> Common-mode transient immunity is the maximum common-mode voltage slew rate that can be sustained while maintaining specification-compliant operation.  $V_{CM}$  is the common-mode potential difference between the logic and bus sides. The transient magnitude is the range over which the common mode is slewed. The common-mode voltage slew rates apply to both rising and falling common-mode voltage edges.

**TIMING SPECIFICATIONS**

3.0 V ≤ V<sub>DD1</sub> ≤ 5.5 V, 4.75 V ≤ V<sub>DD2</sub> ≤ 5.25 V, T<sub>A</sub> = T<sub>MIN</sub> to T<sub>MAX</sub>, unless otherwise noted.

Table 2.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions/Comments
<b>DRIVER</b>						
Maximum Data Rate		500			kbps	
Propagation Delay	t <sub>PLH</sub> , t <sub>PHL</sub>	250		620	ns	R <sub>L</sub> = 54 Ω, C <sub>L1</sub> = C <sub>L2</sub> = 100 pF, see Figure 18 and Figure 22
Skew	t <sub>SKEW</sub>			40	ns	R <sub>L</sub> = 54 Ω, C <sub>L1</sub> = C <sub>L2</sub> = 100 pF, see Figure 18 and Figure 22
Rise/Fall Time	t <sub>r</sub> , t <sub>f</sub>	200		600	ns	R <sub>L</sub> = 54 Ω, C <sub>L1</sub> = C <sub>L2</sub> = 100 pF, see Figure 18 and Figure 22
Enable Time				1050	ns	R <sub>L</sub> = 500 Ω, C <sub>L</sub> = 100 pF, see Figure 19 and Figure 24
Disable Time				1050	ns	R <sub>L</sub> = 500 Ω, C <sub>L</sub> = 15 pF, see Figure 19 and Figure 24
<b>RECEIVER</b>						
Propagation Delay	t <sub>PLH</sub> , t <sub>PHL</sub>	400		1050	ns	C <sub>L</sub> = 15 pF, see Figure 20 and Figure 23
Differential Skew	t <sub>SKEW</sub>			250	ns	C <sub>L</sub> = 15 pF, see Figure 20 and Figure 23
Enable Time			25	70	ns	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 15 pF, see Figure 21 and Figure 25
Disable Time			40	70	ns	R <sub>L</sub> = 1 kΩ, C <sub>L</sub> = 15 pF, see Figure 21 and Figure 25

**PACKAGE CHARACTERISTICS**

Table 3.

Parameter	Symbol	Min	Typ	Max	Unit	Test Conditions
Resistance (Input-Output) <sup>1</sup>	R <sub>I-O</sub>		10 <sup>12</sup>		Ω	
Capacitance (Input-Output) <sup>1</sup>	C <sub>I-O</sub>		3		pF	f = 1 MHz
Input Capacitance <sup>2</sup>	C <sub>I</sub>		4		pF	

<sup>1</sup> Device is considered a 2-terminal device: Pin 1 to Pin 8 are shorted together, and Pin 9 to Pin 16 are shorted together.

<sup>2</sup> Input capacitance is from any input data pin to ground.

**REGULATORY INFORMATION**

Table 4. ADM2481 Approvals

Organization	Approval Type	Notes
UL	Recognized under the Component Recognition Program of Underwriters Laboratories, Inc.	In accordance with UL 1577, each ADM2481 is proof tested by applying an insulation test voltage of ≥ 3000 V rms for 1 second (current leakage detection limit = 5 μA).
VDE	Certified according to DIN V VDE V 0884-10 (VDE V 0884-10): 2006-12	In accordance with DIN V VDE V 0884-10, each ADM2481 is proof tested by applying an insulation test voltage of ≥ 1050 V peak for 1 second (partial discharge detection limit = 5 pC).

**INSULATION AND SAFETY-RELATED SPECIFICATIONS**

Table 5.

Parameter	Symbol	Value	Unit	Conditions
Rated Dielectric Insulation Voltage		2500	V rms	1-minute duration
Minimum External Air Gap (Clearance)	L(I01)	7.6	mm	Measured from input terminals to output terminals, shortest distance through air
Minimum External Tracking (Creepage)	L(I02)	7.6	mm	Measured from input terminals to output terminals, shortest distance along body
Minimum Internal Gap (Internal Clearance)		0.017 min	mm	Insulation distance through insulation
Tracking Resistance (Comparative Tracking Index)	CTI	>175	V	DIN IEC 112/VDE 0303 Part 1
Isolation Group		IIIa		Material Group (Table 1 in DIN VDE 0110,1/89)

**VDE 0884 INSULATION CHARACTERISTICS**

This isolator is suitable for basic electrical isolation only within this safety limit data. Maintenance of this safety data shall be ensured by means of protective circuits.

**Table 6.**

<b>Description</b>	<b>Symbol</b>	<b>Characteristic</b>	<b>Unit</b>
Installation Classification per DIN VDE 0110 for Rated Mains Voltage		I to IV	
≤150 V rms		I to III	
≤300 V rms		I to II	
≤400 V rms		40/85/21	
Climatic Classification		2	
Pollution Degree (Table 1 in DIN VDE 0110)			
Maximum Working Insulation Voltage	$V_{IORM}$	560	$V_{PEAK}$
Input to Output Test Voltage, Method b1	$V_{PR}$	1050	$V_{PEAK}$
$V_{IORM} \times 1.875 = V_{PR}$ , 100% Production Tested			
$t_m = 1$ sec, Partial Discharge of < 5 pC			
Input-to-Output Test Voltage, Method a			
(After Environmental Tests, Subgroup 1)			
$V_{IORM} \times 1.6 = V_{PR}$ , $t_m = 60$ sec, Partial Discharge of < 5 pC		896	$V_{PEAK}$
(After Input and/or Safety Test, Subgroup 2/3)			
$V_{IORM} \times 1.2 = V_{PR}$ , $t_m = 60$ sec, Partial Discharge of < 5 pC	$V_{PR}$	672	$V_{PEAK}$
Highest Allowable Overvoltage			
(Transient Overvoltage, $t_{TR} = 10$ sec)	$V_{TR}$	4000	$V_{PEAK}$
Safety-Limiting Values (Maximum Value Allowed in the Event of a Failure; see Figure 13)			
Case Temperature	$T_S$	150	°C
Input Current	$I_{S, INPUT}$	265	mA
Output Current	$I_{S, OUTPUT}$	335	mA
Insulation Resistance at $T_S$ , $V_{IO} = 500$ V	$R_S$	>10 <sup>9</sup>	Ω

## ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ , unless otherwise noted. All voltages are relative to their respective ground.

Table 7.

Parameter	Rating
$V_{DD1}$	-0.5 V to +7 V
$V_{DD2}$	-0.5 V to +6 V
Digital Input Voltage (DE, $\overline{\text{RE}}$ , TxD)	-0.5 V to $V_{DD1} + 0.5$ V
Digital Output Voltage (RxD)	-0.5 V to $V_{DD1} + 0.5$ V
Driver Output/Receiver Input Voltage	-9 V to +14 V
ESD Rating: Contact	
Human Body Model (A, B Pins)	$\pm 2$ kV
Operating Temperature Range	-40°C to +85°C
Storage Temperature Range	-55°C to +150°C
Average Output Current per Pin	-35 mA to +35 mA
$\theta_{JA}$ Thermal Impedance	65°C/W
Lead Temperature	
Soldering (10 sec)	260°C
Vapor Phase (60 sec)	215°C
Infrared (15 sec)	220°C

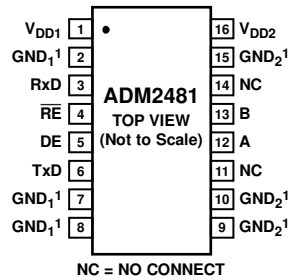
Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NC = NO CONNECT

<sup>1</sup> PIN 2, PIN 7, AND PIN 8 MUST BE CONNECTED TO GND<sub>1</sub>.  
 PIN 9, PIN 10, AND PIN 15 MUST BE CONNECTED TO GND<sub>2</sub>.

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Figure 2. Pin Configuration

Table 8. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	V <sub>DD1</sub>	Power Supply (Logic Side).
2, 7, 8	GND <sub>1</sub>	Ground (Logic Side).
3	RxD	Receiver Output Data. When enabled, if $(A - B) \geq -30$ mV, then RxD = high; if $(A - B) \leq -200$ mV, then RxD = low. This is a tristate output when the receiver is disabled, that is, when RE is driven high.
4	$\overline{RE}$	Receiver Enable Input. This is an active-low input. Driving this input low enables the receiver, and driving it high disables the receiver.
5	DE	Driver Enable Input. Driving the input high enables the driver, and driving it low disables the driver.
6	TxD	Transmit Data Input. Data to be transmitted by the driver is applied to this input.
9, 10, 15	GND <sub>2</sub>	Ground (Bus Side).
11, 14	NC	No Connect.
12	A	Noninverting Driver Output/Receiver Input. When the driver is disabled, or when V <sub>DD1</sub> or V <sub>DD2</sub> is powered down, Pin A is put into a high impedance state to avoid overloading the bus.
13	B	Inverting Driver Output/Receiver Input. When the driver is disabled, or when V <sub>DD1</sub> or V <sub>DD2</sub> is powered down, Pin B is put into a high impedance state to avoid overloading the bus.
16	V <sub>DD2</sub>	Power Supply (Bus Side).

TYPICAL PERFORMANCE CHARACTERISTICS

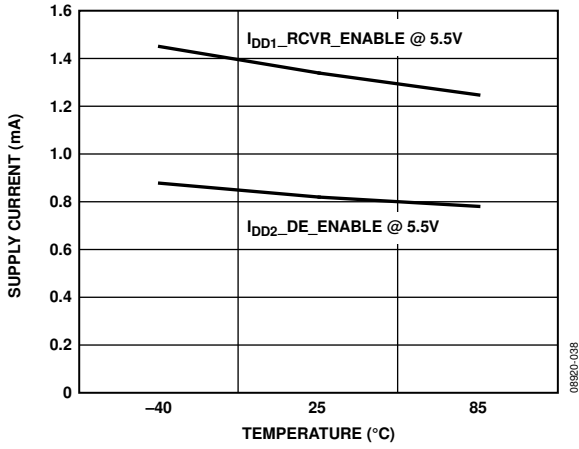


Figure 3. Unloaded Supply Current vs. Temperature

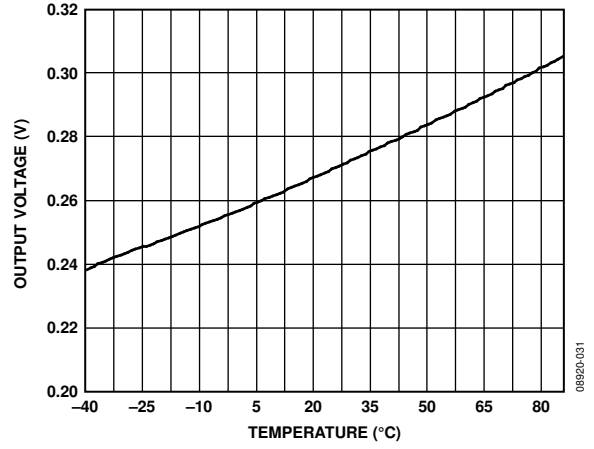


Figure 6. Receiver Output Low Voltage vs. Temperature,  $I_{OUT} = -4$  mA

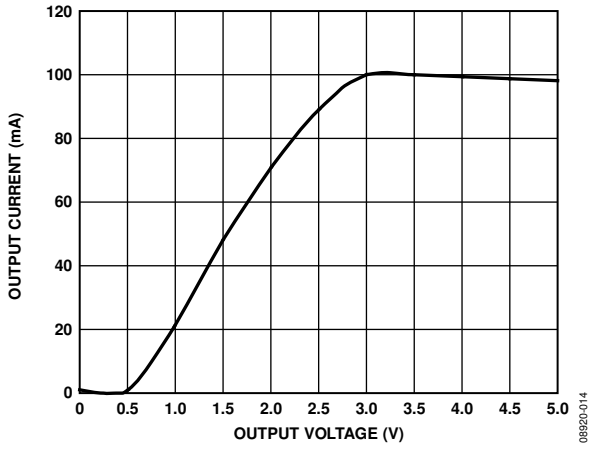


Figure 4. Output Current vs. Driver Output Low Voltage

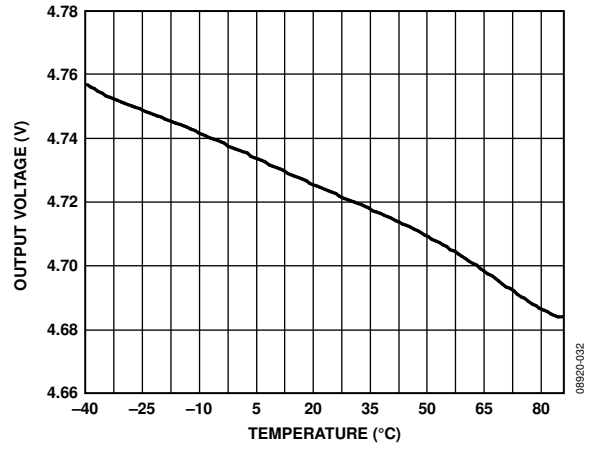


Figure 7. Receiver Output High Voltage vs. Temperature,  $I_{OUT} = 4$  mA

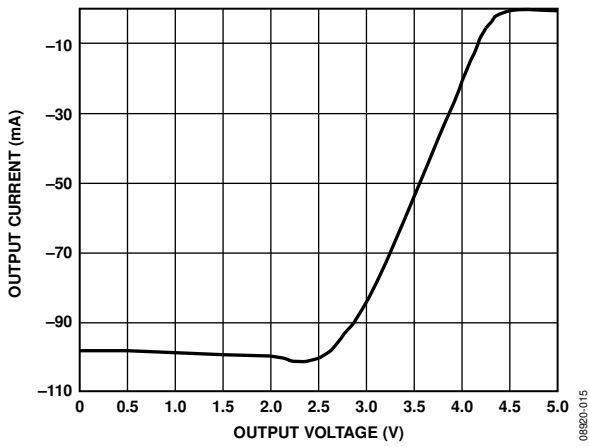


Figure 5. Output Current vs. Driver Output High Voltage

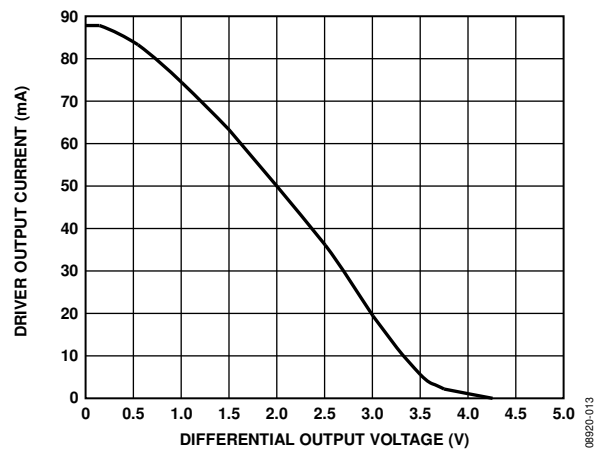


Figure 8. Driver Output Current vs. Differential Output Voltage



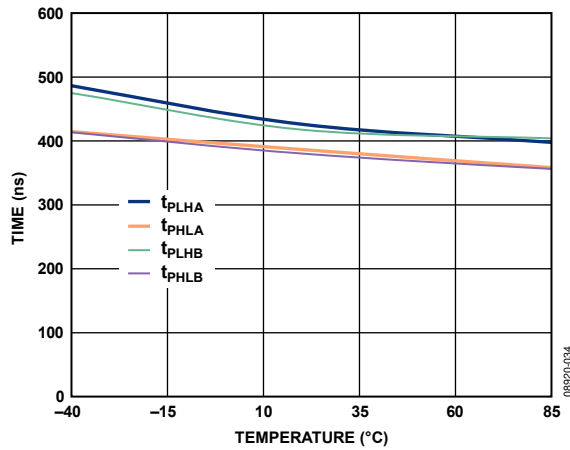


Figure 9. Driver Propagation Delay vs. Temperature

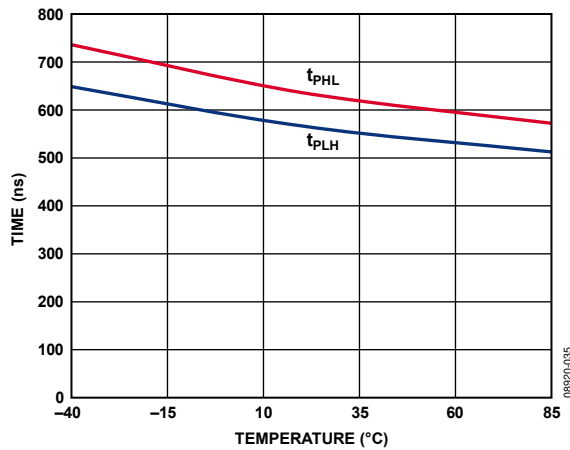


Figure 10. Receiver Propagation Delay vs. Temperature

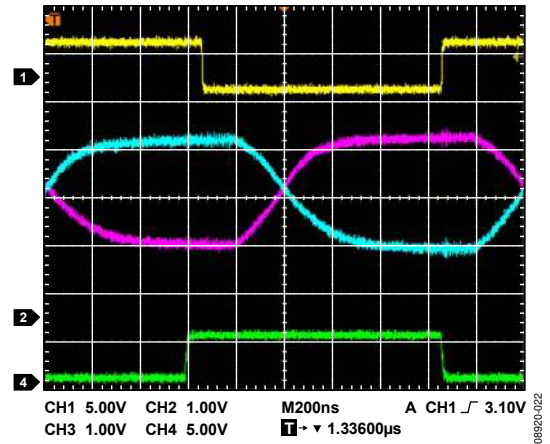


Figure 11. Driver/Receiver Propagation Delay, High to Low

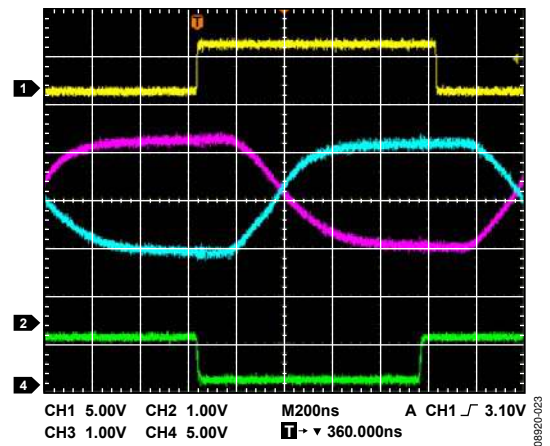


Figure 12. Driver/Receiver Propagation Delay, Low to High

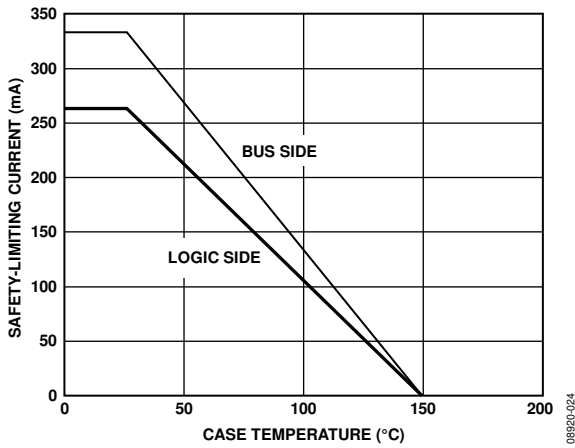


Figure 13. Thermal Derating Curve, Dependence of Safety-Limiting Values with Case Temperature per VDE 0884

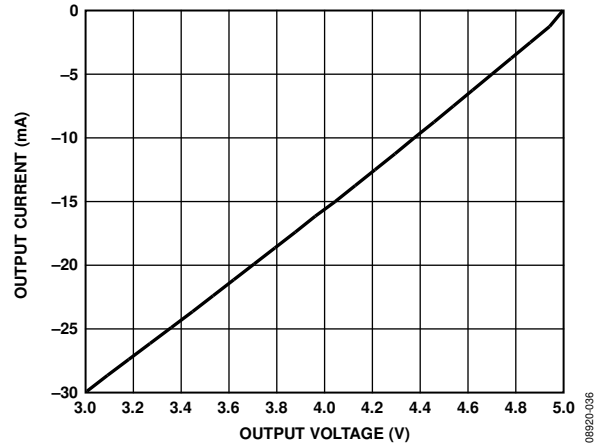


Figure 15. Output Current vs. Receiver Output High Voltage

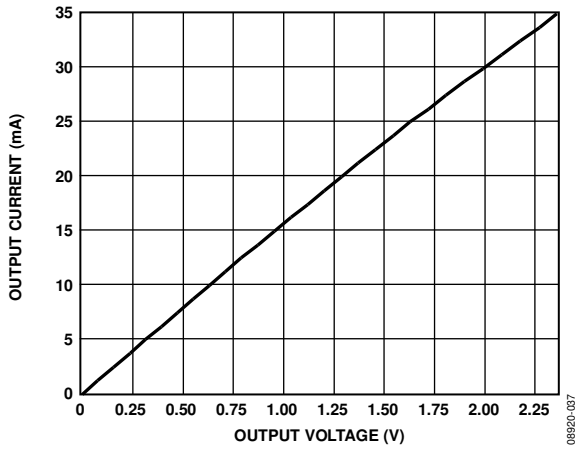


Figure 14. Output Current vs. Receiver Output Low Voltage

TEST CIRCUITS

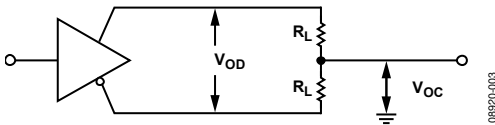


Figure 16. Driver Voltage Measurement

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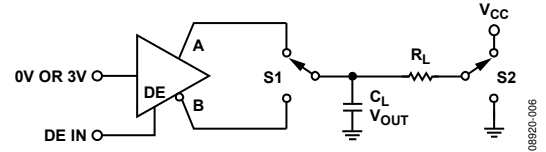


Figure 19. Driver Enable/Disable

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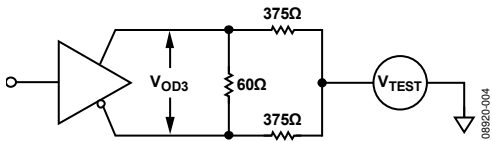


Figure 17. Driver Voltage Measurement over Common-Mode Range

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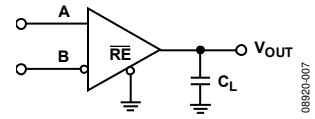


Figure 20. Receiver Propagation Delay

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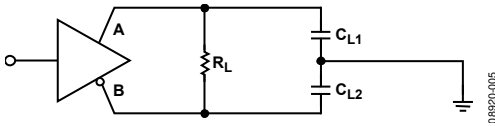


Figure 18. Driver Propagation Delay

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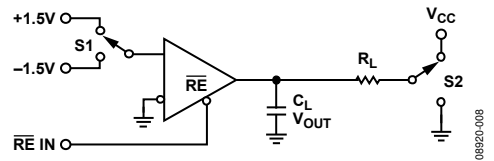


Figure 21. Receiver Enable/Disable

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### SWITCHING CHARACTERISTICS

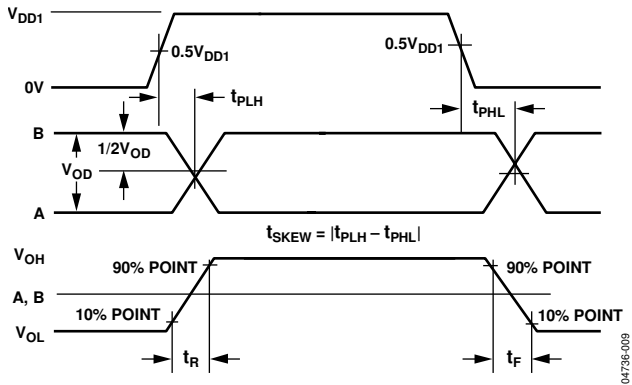


Figure 22. Driver Propagation Delay, Rise/Fall Timing

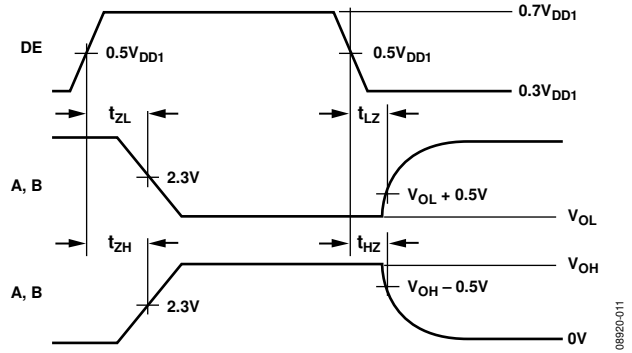


Figure 24. Driver Enable/Disable Timing

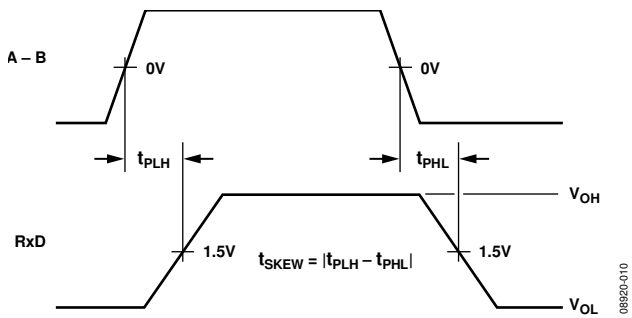


Figure 23. Receiver Propagation Delay

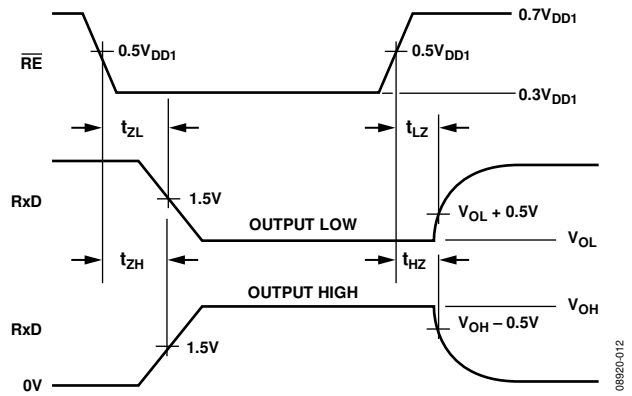


Figure 25. Receiver Enable/Disable Timing

# CIRCUIT DESCRIPTION

## ELECTRICAL ISOLATION

In the ADM2481, electrical isolation is implemented on the logic side of the interface. Therefore, the part has two main sections: a digital isolation section and a transceiver section (see Figure 26). Driver input and data enable signals, applied to the TxD and DE pins, respectively, and referenced to logic ground ( $GND_1$ ), are coupled across an isolation barrier to appear at the transceiver section referenced to isolated ground ( $GND_2$ ).

Similarly, the receiver output, referenced to isolated ground in the transceiver section, is coupled across the isolation barrier to appear at the RxD pin referenced to logic ground ( $GND_1$ ).

## *iCoupler Technology*

The digital signals are transmitted across the isolation barrier using *iCoupler* technology. This technique uses chip scale transformer windings to couple the digital signals magnetically from one side of the barrier to the other. Digital inputs are encoded into waveforms that are capable of exciting the primary transformer winding. At the secondary winding, the induced waveforms are then decoded into the binary value that was originally transmitted.

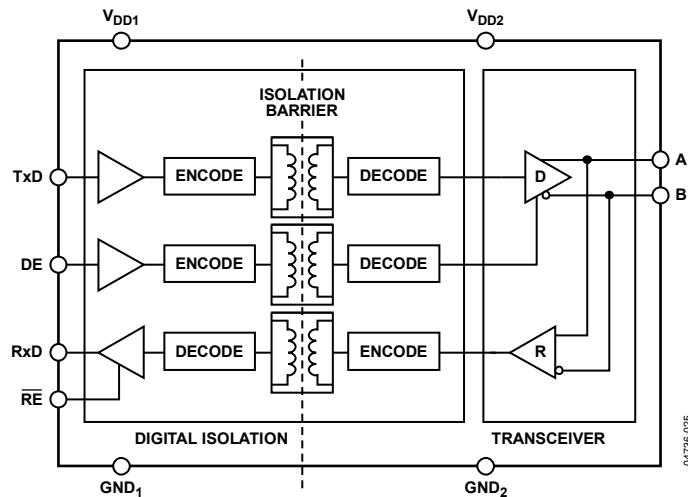


Figure 26. Digital Isolation and Transceiver Sections

**TRUTH TABLES**

The following truth tables use the abbreviations shown in Table 9.

**Table 9.**

Letter	Description
H	High level
L	Low level
X	Don't care
Z	High impedance (off)
NC	Disconnected

**Table 10. Transmitting**

Supply Status		Inputs		Outputs	
V <sub>DD1</sub>	V <sub>DD2</sub>	DE	TxD	A	B
On	On	H	H	H	L
On	On	H	L	L	H
On	On	L	X	Z	Z
On	Off	X	X	Z	Z
Off	On	L	L	Z	Z
Off	Off	X	X	Z	Z

**Table 11. Receiving**

Supply Status		Inputs		Outputs
V <sub>DD1</sub>	V <sub>DD2</sub>	A – B (V)	RE	RxD
On	On	>–0.03	L or NC	H
On	On	<–0.2	L or NC	L
On	On	–0.2 < A – B < –0.03	L or NC	Indeterminate
On	On	Inputs open	L or NC	H
On	On	X	H	Z
On	Off	X	L or NC	H
Off	Off	X	L or NC	L

**THERMAL SHUTDOWN**

The ADM2481 contains thermal shutdown circuitry that protects the part from excessive power dissipation during fault conditions. Shorting the driver outputs to a low impedance source can result in high driver currents. The thermal sensing circuitry detects the increase in die temperature under this condition and disables the driver outputs. This circuitry is designed to disable the driver outputs when a die temperature of 150°C is reached. As the device cools, the drivers are re-enabled at a temperature of 140°C.

**TRUE FAIL-SAFE RECEIVER INPUTS**

The receiver inputs have a true fail-safe feature that ensures that the receiver output is high when the inputs are open or shorted. During line-idle conditions, when no driver on the bus is enabled, the voltage across a terminating resistance at the receiver input decays to 0 V. With traditional transceivers, receiver input thresholds specified between –200 mV and +200 mV mean that external bias resistors are required on the A and B pins to ensure that the receiver outputs are in a known state. The true fail-safe receiver input feature eliminates the need for bias resistors by specifying the receiver input threshold between –30 mV and –200 mV. The guaranteed negative threshold means that when the voltage between A and B decays to 0 V, the receiver output is guaranteed to be high.

**MAGNETIC FIELD IMMUNITY**

Because *i*Couplers use a coreless technology, no magnetic components are present, and the problem of magnetic saturation of the core material does not exist. Therefore, *i*Couplers have essentially infinite dc field immunity. The analysis that follows defines the conditions under which this might occur. The 3 V operating condition of the ADM2481 is examined because it represents the most susceptible mode of operation.

The limitation on the ac magnetic field immunity of the *i*Coupler is set by the condition in which the induced error voltage in the receiving coil (the bottom coil in this case) is made sufficiently large, either to falsely set or reset the decoder. The voltage induced across the bottom coil is given by

$$V = \left( \frac{-d\beta}{dt} \right) \sum \pi r_n^2; \quad n = 1, 2, \dots, N$$

where, if the pulses at the transformer output are greater than 1.0 V in amplitude:

$\beta$  is the magnetic flux density (gauss).

$N$  is the number of turns in receiving coil.

$r_n$  is the radius of  $n$ th turn in receiving coil (cm).

The decoder has a sensing threshold of about 0.5 V; therefore, there is a 0.5 V margin in which induced voltages can be tolerated.

Given the geometry of the receiving coil and an imposed requirement that the induced voltage is, at most, 50% of the 0.5 V margin at the decoder, a maximum allowable magnetic field is calculated, as shown in Figure 27.

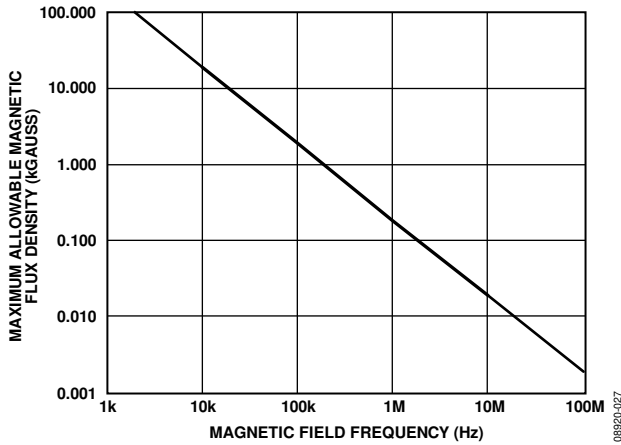


Figure 27. Maximum Allowable External Magnetic Flux Density

For example, at a magnetic field frequency of 1 MHz, the maximum allowable magnetic field of 0.2 kgauss induces a voltage of 0.25 V at the receiving coil. This is about 50% of the sensing threshold and does not cause a faulty output transition. Similarly, if such an event occurs during a transmitted pulse and is the worst-case polarity, it reduces the received pulse from >1.0 V to 0.75 V. This is well above the 0.5 V sensing threshold of the decoder.

These magnetic flux density values are shown in Figure 28, using more familiar quantities such as maximum allowable current flow, at given distances away from the ADM2481 transformers.

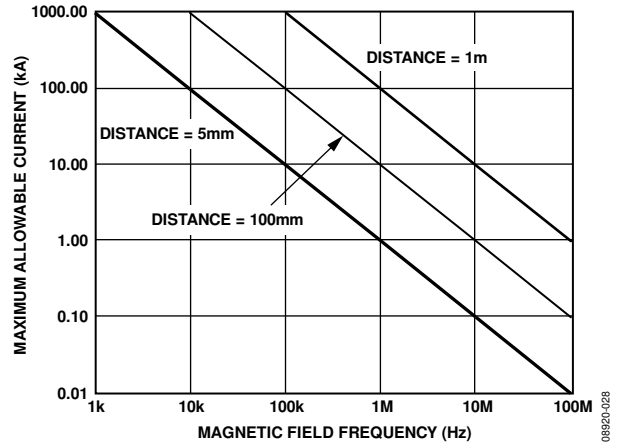


Figure 28. Maximum Allowable Current for Various Current-to-ADM2481 Spacings

At combinations of strong magnetic field and high frequency, any loops formed by printed circuit board traces could induce large enough error voltages to trigger the thresholds of succeeding circuitry. To avoid this possibility, take care in the layout of such traces.

## APPLICATIONS INFORMATION

### PRINTED CIRCUIT BOARD (PCB) LAYOUT

The ADM2481 signal isolated RS-485 transceiver requires no external interface circuitry for the logic interfaces. Power supply bypassing is required at the input and output supply pins (see Figure 29).

Bypass capacitors are most conveniently connected between Pin 1 and Pin 2 for  $V_{DD1}$  and between Pin 15 and Pin 16 for  $V_{DD2}$ . The capacitor value must be between 0.01  $\mu\text{F}$  and 0.1  $\mu\text{F}$ . The total lead length between both ends of the capacitor and the input power supply pin must not exceed 20 mm.

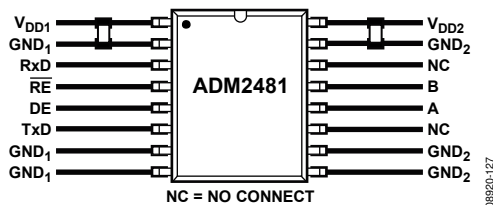


Figure 29. Recommended Printed Circuit Board Layout

In applications involving high common-mode transients, take care to ensure that board coupling across the isolation barrier is minimized. Furthermore, the board layout must be designed such that any coupling that does occur equally affects all pins on a given component side.

Failure to ensure this can cause voltage differentials between pins that exceed the absolute maximum ratings of the device, thereby leading to latch-up or permanent damage.

### ISOLATED POWER SUPPLY CIRCUIT

The ADM2481 requires isolated power capable of 5 V at 100 mA to be supplied between the  $V_{DD2}$  and  $\text{GND}_2$  pins. If no suitable integrated power supply is available, a discrete circuit, such as the one in Figure 30, can be used. A center-tapped transformer provides electrical isolation. The primary winding is excited with a pair of square waveforms that are 180° out of phase with each other. A pair of Schottky diodes and a smoothing capacitor are used to create a rectified signal from the secondary winding. The ADP3330 linear voltage regulator provides a regulated power supply to the bus-side circuitry of the ADM2481.

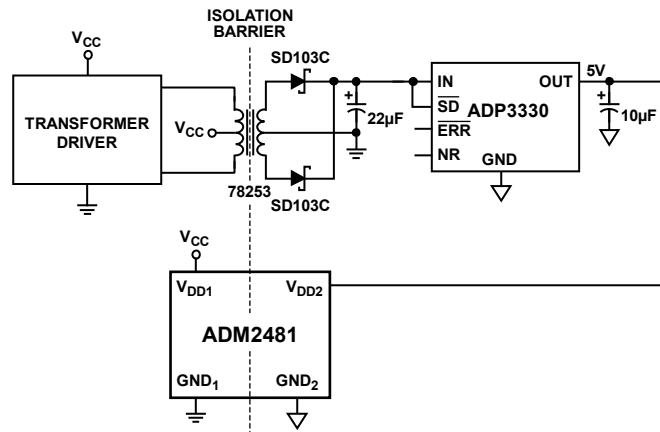
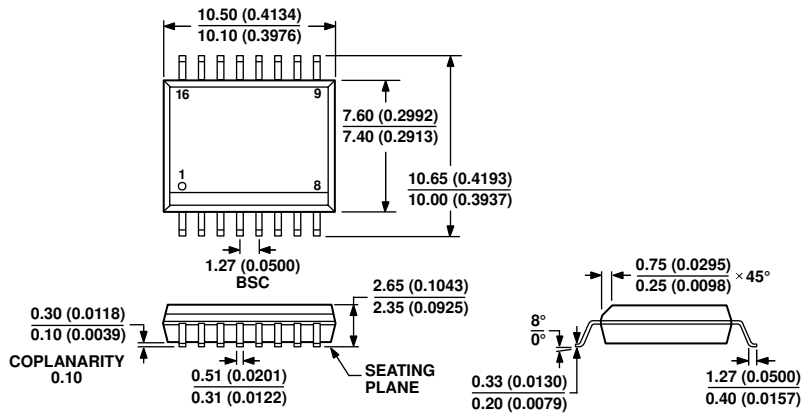


Figure 30. Isolated Power Supply Circuit



# OUTLINE DIMENSIONS



COMPLIANT TO JEDEC STANDARDS MS-013-AA  
 CONTROLLING DIMENSIONS ARE IN MILLIMETERS; INCH DIMENSIONS  
 (IN PARENTHESES) ARE ROUNDED-OFF MILLIMETER EQUIVALENTS FOR  
 REFERENCE ONLY AND ARE NOT APPROPRIATE FOR USE IN DESIGN.

03-27-2007-B

Figure 31. 16-Lead Standard Small Outline Package [SOIC\_W]  
 Wide Body  
 (RW-16)

Dimensions shown in millimeters and (inches)

## ORDERING GUIDE

Model <sup>1</sup>	Data Rate (kbps)	Temperature Range	Package Description	Package Option
ADM2481BRWZ	500	-40°C to +85°C	16-Lead, Wide Body SOIC_W	RW-16
ADM2481BRWZ-RL7	500	-40°C to +85°C	16-Lead, Wide Body SOIC_W	RW-16
EVAL-ADM2481EBZ			ADM2481 Evaluation Board	

<sup>1</sup> Z = RoHS Compliant Part.