Digital Power Management IC 2MHz, 600mA DC/DC with Triple 300mA LDOs

General Description

The MIC2811/21 are high performance power management ICs, supporting four output voltage rails with maximum efficiency. The four rails are generated by a single 600mA DC/DC converter and three 300mA LDOs. LDO1 and LDO2 are capable of operating at a low input voltage down to 1.65V useful for post regulating the output voltage of the DC-DC converter. The MIC2811 supports the use of a bypass cap for improved noise performance on LDO1 & LDO2 while the MIC2821 offers a separate enable pin for LDO3.

Featuring an operating frequency of 2MHz, the DC to DC converter uses small values of L and C to reduce board space but still retains operating efficiencies up to 86% at load currents up to 600mA.

The MIC2811/21 feature a μCap design, operating with very small ceramic output capacitors and inductors for stability, reducing required board space and component cost and it is available in fixed output voltages in the 16-pin 3mm × 3mm MLF® leadless package.

Data sheets and support documentation can be found on Micrel's web site at: www.micrel.com.

Applications

- Mobile phones / PDAs
- Portable media players
- Mobile Television Receivers

Features

- 2MHz DC/DC converter and 3 LDOs
- Tiny 16-pin 3mm x 3mm MLF® package
- Thermal Shutdown Protection
- ±2% Output Voltage Accuracy on all outputs
- Current Limit Protection

DC/DC Converter

- 2.7V to 5.5V input voltage range
- Output current to 600mA
- 2MHz PWM operation
- Up to 86% efficiency (1.2V output)

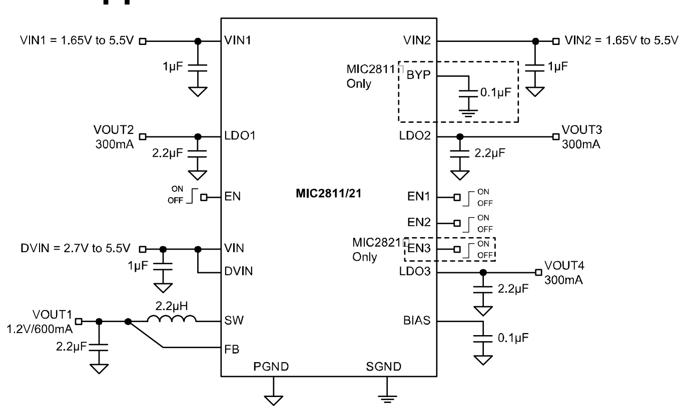
LDO 1 & 2

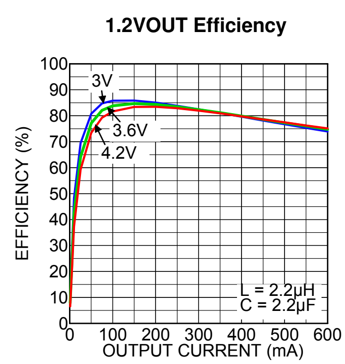
- 1.65V to 5.5V input voltage range
- 300mA output current
- Fixed Output voltage as low as 0.8V
- Low 142mV dropout
- 70dB PSRR at 1kHz

LDO 3

- 2.7V to 5.5V input voltage range
- 300mA output current
- Fixed Output voltage as low as 1.0V

Typical Application





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Ordering Information

Part Number	Marking Code	Voltage(1)	Junction Temperature Range	Package(2)
MIC2811-4GJLYML	YHA4	1.2V/1.8V/2.5V/2.7V	–40°C to +125°C	16-Pin 3x3 MLF®
MIC2811-4GMSYML	YHA3	1.2V/1.8V/2.8V/3.3V	–40°C to +125°C	16-Pin 3x3 MLF®
MIC2821-4GJLYML	YJA2	1.2V/1.8V/2.5V/2.7V	–40°C to +125°C	16-Pin 3x3 MLF®
MIC2821-4GMSYML	YJA3	1.2V/1.8V/2.8V/3.3V	–40°C to +125°C	16-Pin 3x3 MLF®

Note:

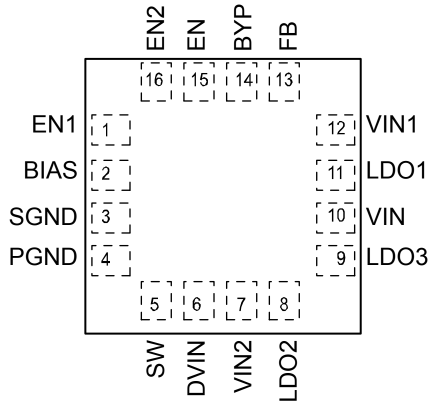
1. Output Voltage of DC/DC, LDO1, LDO2, LDO3 respectively

For additional voltage options, contact Micrel Marketing. Available fixed output voltage range for each output is as follows:

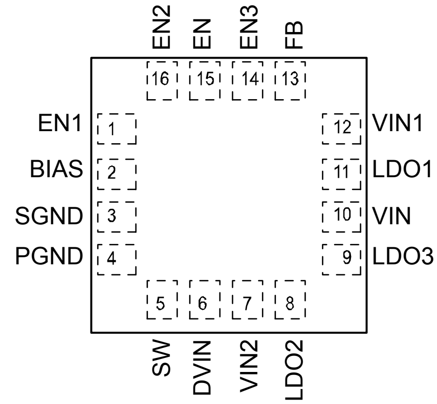
	min	max	
DC/DC	1.0	2.0	(Adjustable output also available)
LDO1	0.8	3.6	
LDO2	0.8	3.6	
LDO3	1.0	3.9	

2. MLF is a GREEN RoHS compliant package. Lead finish is NiPdAu. Mold compound is Halogen Free.

Pin Configuration



MIC2811
16-Pin 3mm x 3mm MLF® (ML)
(Top View)



MIC2821
16-Pin 3mm x 3mm MLF® (ML)
(Top View)

Pin Description

Pin Number MIC2811	Pin Number MIC2821	Pin Name	Pin Name
1	1	EN1	Enable Input (LDO 1). Active High Input. Logic High = On; Logic Low = Off; Do not leave floating.
2	2	BIAS	Internal circuit bias supply. It must be de-coupled to signal ground with a 0.1µF capacitor and should not be loaded.
3	3	SGND	Signal ground.
4	4	PGND	Power ground.
5	5	SW	Switch (Output): Internal power MOSFET output switches.
6	6	DVIN	Power Supply for DC/DC converter. Must be tied to VIN.
7	7	VIN2	Power Supply to LDO2.
8	8	LDO2	Output of LDO2.
9	9	LDO3	Output of LDO3.
10	10	VIN	Supply to bias circuitry and power to LDO3, must be tied to DVIN.
11	11	LDO1	Output of LDO1.
12	12	VIN1	Power Supply to LDO1.
13	13	FB	Feedback input to the error amplifier of the DC/DC converter. Adjust version: Use external resistor divider from DC/DC output to set VOUT. Fixed voltage version: Connect directly to VOUT of the DC/DC converter.
14	N/A	BYP	Reference Bypass. Connect external 0.1µF to GND to reduce output noise. May be left open. Do not connect directly to GND.
N/A	14	EN3	Enable Input (LDO3). Active High Input. Logic High = On; Logic Low = Off; Do not leave floating.
15	N/A	EN	Enable Input (DC/DC and LDO3). Active High Input. Logic High = On; Logic Low = Off; Do not leave floating.
N/A	15	EN	Enable Input (DC/DC). Active High Input. Logic High = On; Logic Low = Off; Do not leave floating.
16	16	EN2	Enable Input (LDO2). Active High Input. Logic High = On; Logic Low = Off; Do not leave floating.

Absolute Maximum Ratings(1)

Supply Voltage (DV_{IN}, V_{IN}, V_{IN1}, V_{IN2}) .... 0V to +6V
Enable Voltage (V_{EN}, V_{EN1}, V_{EN2}, V_{EN3}) .... 0V to +6V
Power Dissipation .... Internally Limited(3)
Lead Temperature (Soldering, 10 sec.) .... 260°C
Storage Temperature (T_S)..................–65°C ≤ T_J ≤ +150°C
ESD Rating(4) 2kV

Operating Ratings(2)

Supply voltage (DV_{IN}, V_{IN}) .... +2.7V to +5.5V
Supply voltage (V_{IN1}, V_{IN2}) .... +1.65V to V_{IN}
Enable Input Voltage (V_{EN}, V_{EN1}, V_{EN2}, V_{EN3}) ...... 0V to V_{IN}
Junction Temperature Range (T_J) ....–40°C to +125°C
Package Thermal Resistance
3mm x 3mm MLF-16 (θ_{JA}) ....56°C/W

Electrical Characteristics(5)

$DV_{IN} = V_{IN} = V_{IN1} = V_{IN2} = V_{OUTMAX}$ + 1V, L = 2.2µH; $C_{OUTDC/DC}$ = 2.2µF, $C_{OUT1} = C_{OUT2} = C_{OUT3}$ = 2.2µF; $I_{OUTDC/DC}$ = 20mA;
$I_{OUTLDO1} = I_{OUTLDO2} = I_{OUTLDO2}$ = 100µA; T_J = 25°C, **bold** values indicate –40°C ≤ T_J ≤ +125°C; unless noted.

Parameter	Conditions	Min	Typ	Max	Units
UVLO Threshold	Rising input voltage during turn-on (DVIN & VIN Only)	**2.45**	2.55	**2.65**	V
UVLO Hysteresis			100		mV
Ground Pin Current	V_{FB} = 1.1*V_{FBNOM} (not switching);		800	1100	µA
	LDO2 or LDO1 Only ($V_{EN} = V_{EN3}$ = GND)		55	85 95	µA µA
	LDO3 only ($V_{EN} = V_{EN1} = V_{EN2}$ = GND / MIC2821 only)		40		µA
	All 3 LDOs		120		µA
Ground Pin Current in Shutdown	All EN = 0V		0.2	5	µA
Over-temperature Shutdown			160		°C
Over-temperature Shutdown Hysteresis			23		°C
Enable Input Voltage	Logic Low			**0.2**	V
	Logic High	**1.1**			V
Enable Input Current			0.1	**1**	µA

Electrical Characteristics - DC/DC Converter

$DV_{IN} = V_{IN} = V_{EN} = V_{OUTDC/DC}$ + 1V, L = 2.2µH; $C_{OUTDC/DC}$ = 2.2µF, $C_{OUT1} = C_{OUT2} = C_{OUT3}$ = 2.2µF; $I_{OUTDC/DC}$ = 20mA; T_J = 25°C, **bold** values indicate –40°C to + 125°C; unless noted.

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage Accuracy	Fixed Output Voltages	-2 **-3**		+2 **+3**	% %
Current Limit in PWM Mode	V_{FB} = 0.9*V_{FBNOM}	0.75	1.2	1.8	A
FB pin input current (ADJ only)			1		nA
Output Voltage Line Regulation	V_{OUT} > 2.4V; $V_{IN} = V_{OUT}$ + 300mV to 5.5V, I_{LOAD}= 20mA V_{OUT} < 2.4V; V_{IN} = 2.7V to 5.5V, I_{LOAD}= 20mA		0.2		%/V %/V
Output Voltage Load Regulation	20mA < I_{LOAD} < 300mA		0.2	1.5	%
Maximum Duty Cycle	V_{FB} ≤ 0.4V	100			%
Switch ON-Resistance	PMOS (0.7*V_{FBNOM}) NMOS (1.1*V_{FBNOM})		0.5 0.55		Ω Ω
Oscillator Frequency		**1.8**	2	**2.2**	MHz
Turn-on Time					
Turn-on Time (DC/DC)	I_{LOAD} = 300mA; C_{BYP} = 0.1µF		83	**350**	µs

Electrical Characteristics - LDO1 and LDO2

$V_{IN} = DV_{IN} = V_{OUTMAX} + 1V$, $V_{IN1} = V_{EN1} = V_{LDO1} + 1V$; $V_{IN2} = V_{EN2} = V_{LDO2} + 1V$; $C_{OUTLDO1} = C_{OUTLDO2} = 2.2\mu F$, $I_{LDO1} = I_{LDO2} = 100\mu A$; $T_J = 25°C$, $V_{EN} = V_{EN3}$ = GND, **bold** values indicate $-40°C \leq T_J \leq +125°C$; unless noted.

Parameter	Conditions	Min	Typ	Max	Units
Output Voltage Accuracy		-2.0 **-3.0**		+2.0 **+3.0**	% %
Output Current Capability	$V_{IN} \geq 1.8V$	300			mA
Load Regulation	I_{OUT} = 100µA to 300mA		0.3	**1.5**	%
Line Regulation	$V_{IN1(2)} = V_{LDO1(2)}$ +1V to 5.5V		0.02	0.3	%/V
Dropout Voltage	I_{OUT} = 300mA @ Vout > 1.5V		142	**300**	mV
Current Limit	V_{OUT} = 0V	**350**	650	900	mA
Ripple Rejection	f = up to 1kHz; C_{OUT} = 2.2µF; C_{BYP} = 0.1µF f = 20kHz; C_{OUT} = 2.2µF; C_{BYP} = 0.1µF		70 44		dB dB
Output Voltage Noise	C_{OUT} = 2.2µF; C_{BYP} = 0.1µF; 10Hz to 100KHz		30		μV_{RMS}

Electrical Characteristics – LDO3

$V_{IN} = DV_{IN} = V_{EN3} = V_{LDO3}$ +1 V; C_{OUT3} = 2.2µF; $I_{OUTLDO3}$ = 100µA; T_J = 25°C, $V_{EN1} = V_{EN2}$ = GND

bold values indicate $-40°C \leq T_J \leq +125°C$; unless noted.

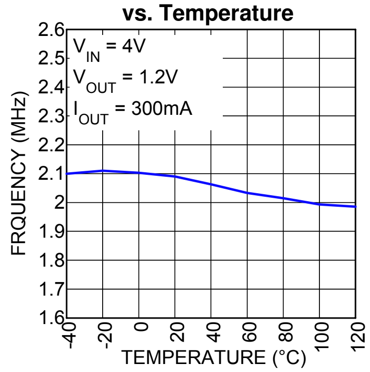
Parameter	Conditions	Min	Typ	Max	Units
Output Voltage Accuracy		-2.0 **-3.0**		+2.0 **+3.0**	% %
Line Regulation	$V_{IN} = V_{OUT}$ +1V to 5.5V; I_{OUT} = 100µA		0.03	0.5	%/V
Load Regulation	I_{OUT} = 100µA to 300mA @ 3.3V		0.50	**1.5**	%
Dropout Voltage	I_{OUT} = 300mA @ Vin = 2.7V		210	**350**	mV
Ripple Rejection	f = up to 1kHz; C_{OUT} = 2.2µF f = 20kHz; C_{OUT} = 2.2µF		45 20		dB dB
Current Limit	V_{OUT} = 0V	**350**	600	980	mA
Output Voltage Noise	C_{OUT} = 2.2µF, 10Hz to 100kHz		470		μV_{RMS}

Notes:

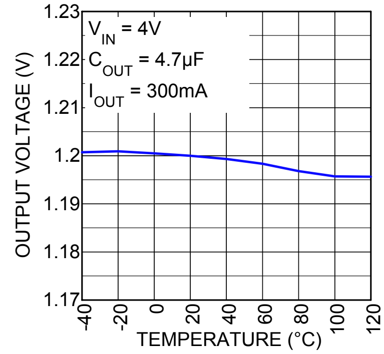
1. Exceeding the absolute maximum rating may damage the device.
2. The device is not guaranteed to function outside its operating rating.
3. The maximum allowable power dissipation of any T_A (ambient temperature) is $P_{D(max)} = (T_{J(max)} - T_A) / \theta_{JA}$. Exceeding the maximum allowable power dissipation will result in excessive die temperature, and the regulator will go into thermal shutdown.
4. Devices are ESD sensitive. Handling precautions recommended. Human body model, 1.5k in series with 100pF.
5. Specification for packaged product only.

Typical Characteristics (DC/DC Converter)

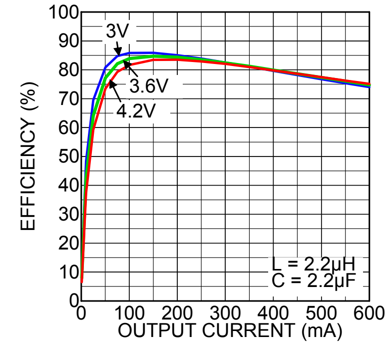
SW Frequency vs. Temperature



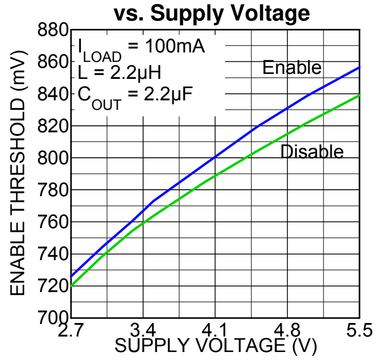
Output Voltage vs. Temperature



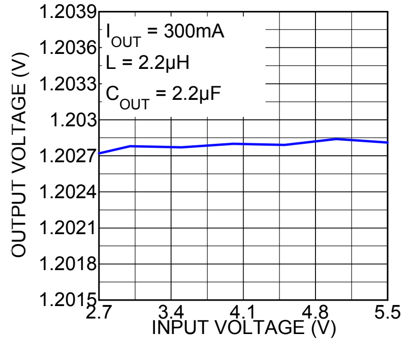
1.2VOUT Efficiency



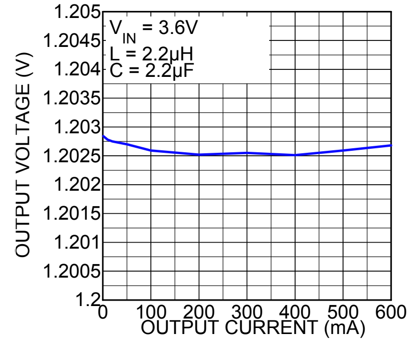
DC/DC Enable Threshold vs. Supply Voltage



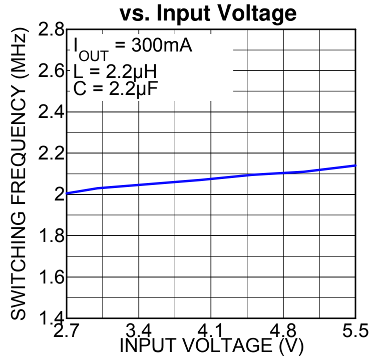
Line Regulation



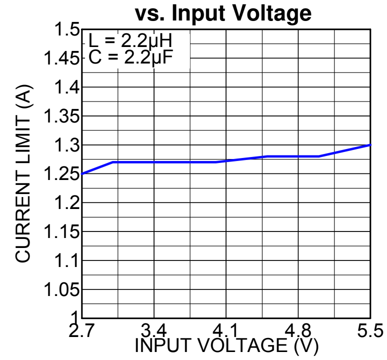
Load Regulation



Switching Frequency vs. Input Voltage

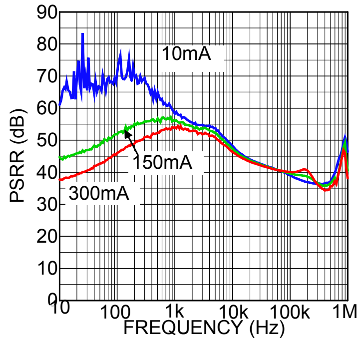


Current Limit vs. Input Voltage

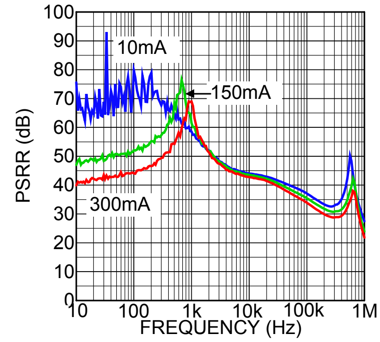


Typical Characteristics (LDO)

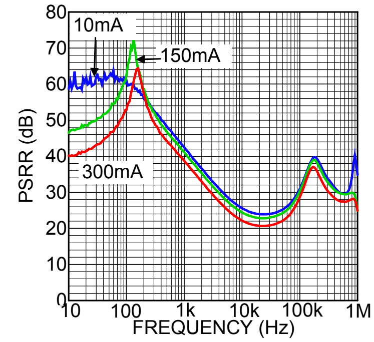
MIC2811 LDO1 PSRR



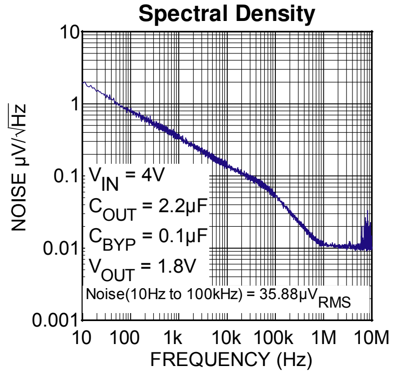
MIC2811 LDO2 PSRR



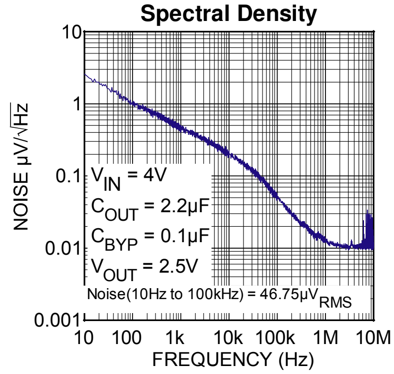
MIC2811 LDO3 PSRR



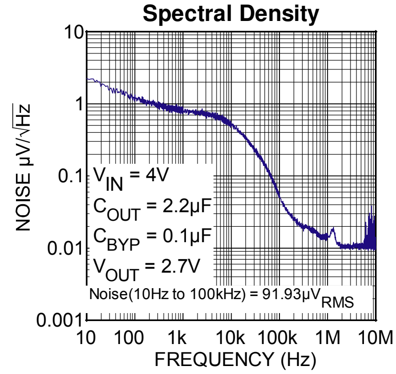
MIC2811 LDO1 Output Noise Spectral Density



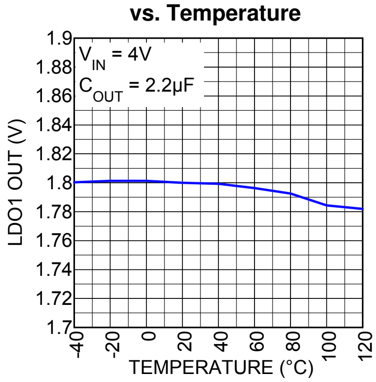
MIC2811 LDO2 Output Noise Spectral Density



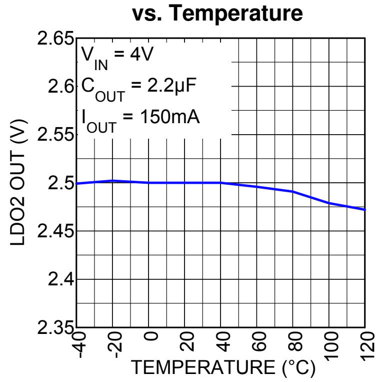
MIC2811 LDO3 Output Noise Spectral Density



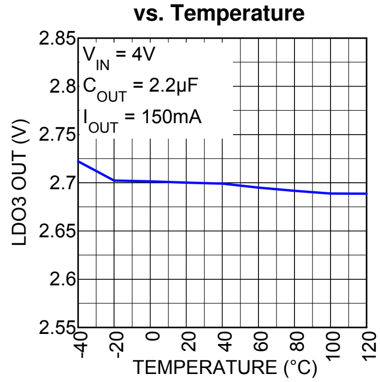
LDO1 vs. Temperature



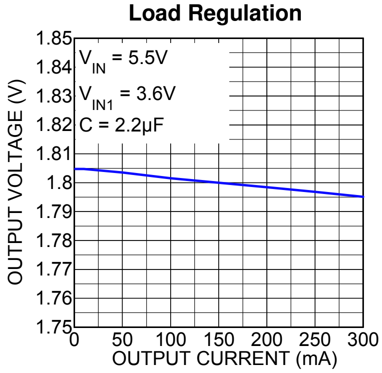
LDO2 vs. Temperature



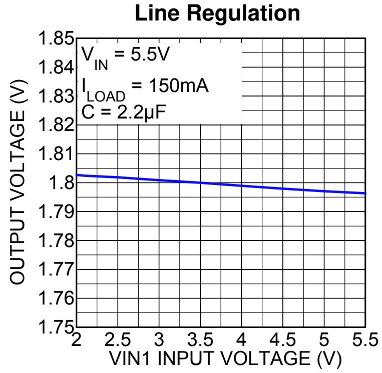
LDO3 vs. Temperature



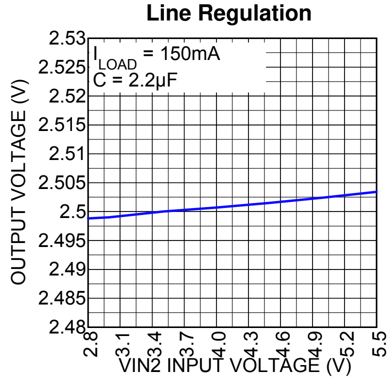
LDO1 Load Regulation



LDO1 Line Regulation

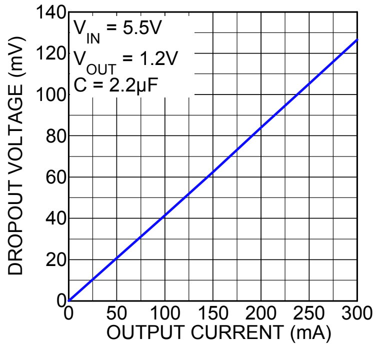


LDO2 Line Regulation

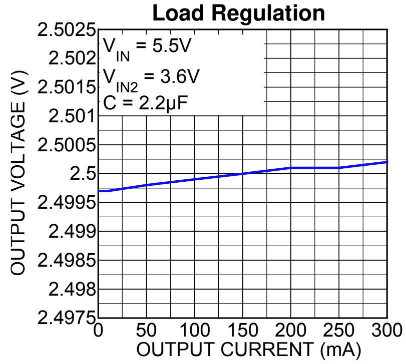


Typical Characteristics (LDO cont.)

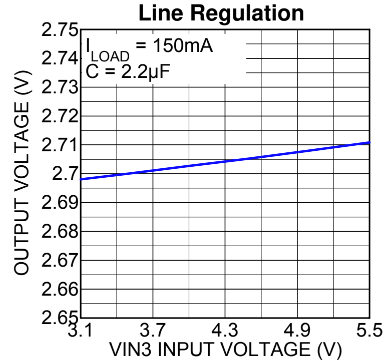
LDO2 Dropout Voltage vs. Load Current



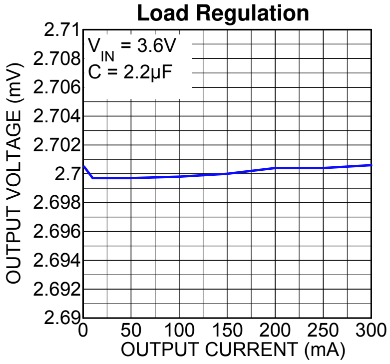
LDO2 Load Regulation



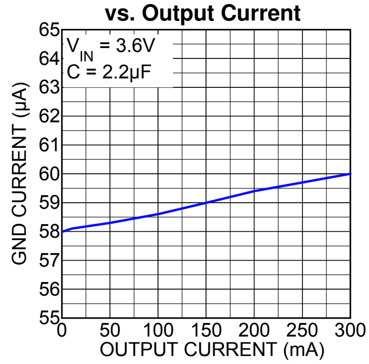
LDO3 Line Regulation



LDO3 Load Regulation

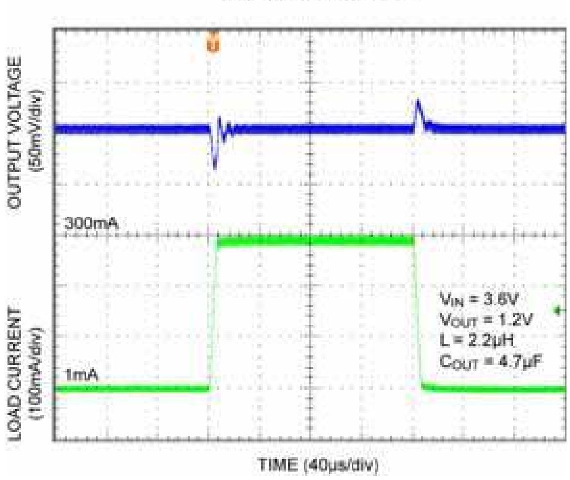


LDO2 GND Current vs. Output Current

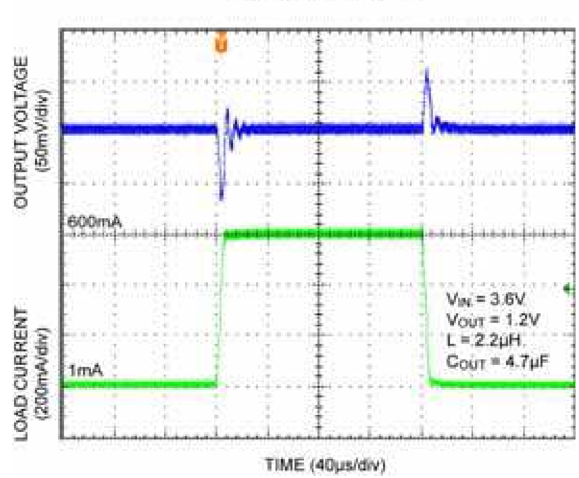


Functional Characteristics (DC/DC Converter)

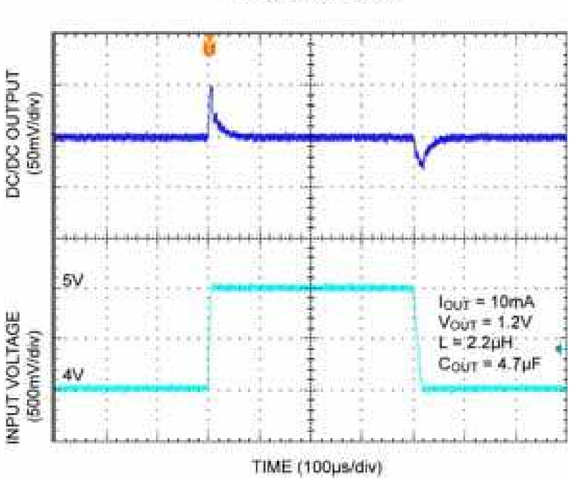
Load Transient



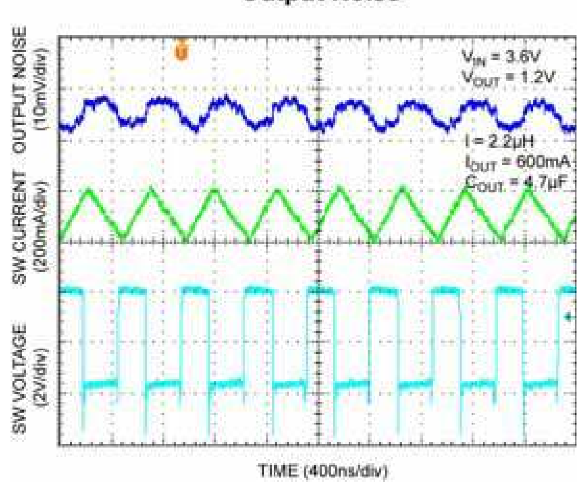
Load Transient



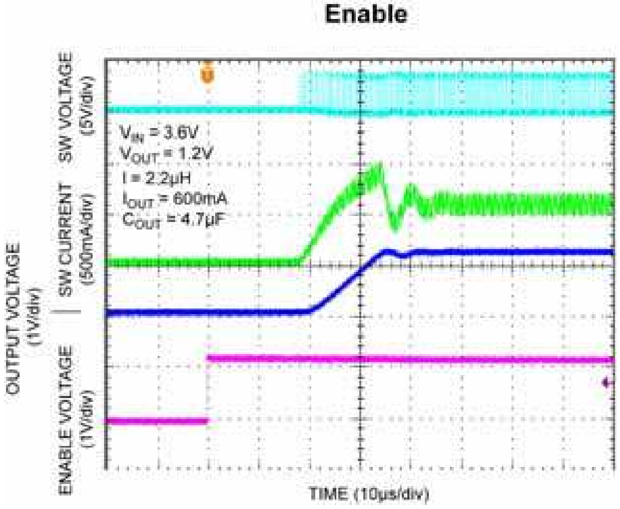
Line Transient



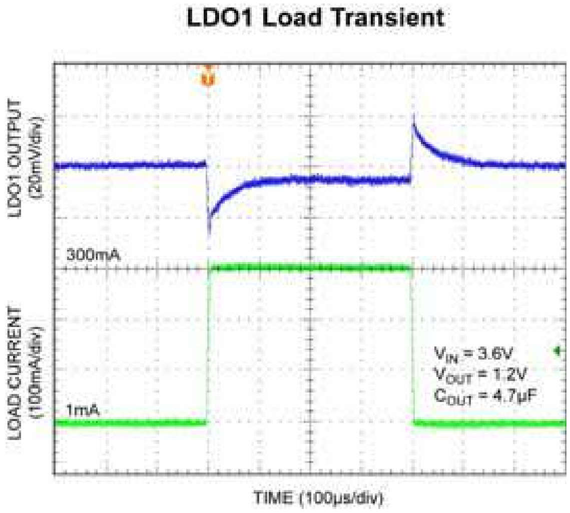
Output Noise

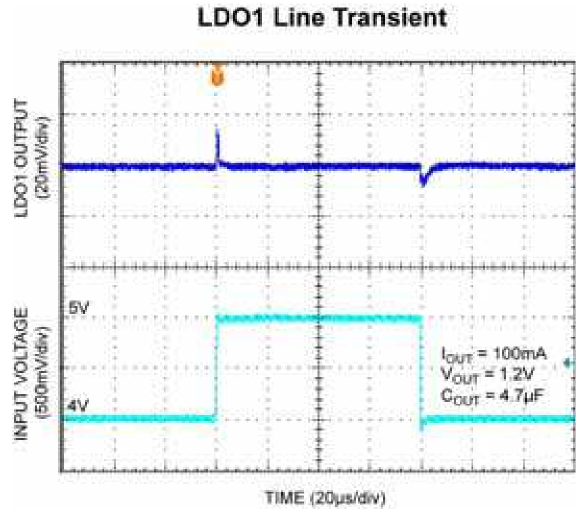


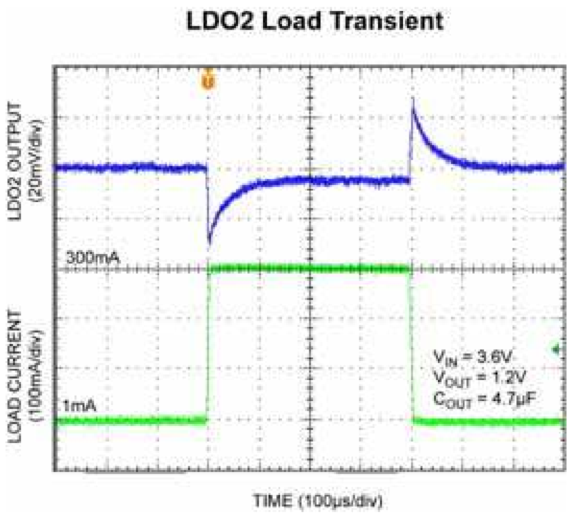
Enable

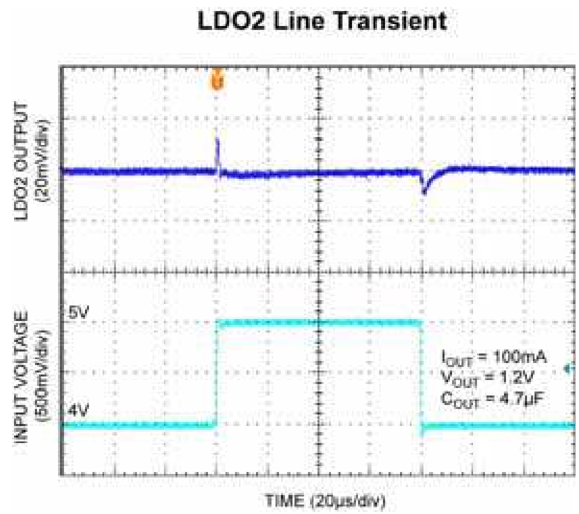


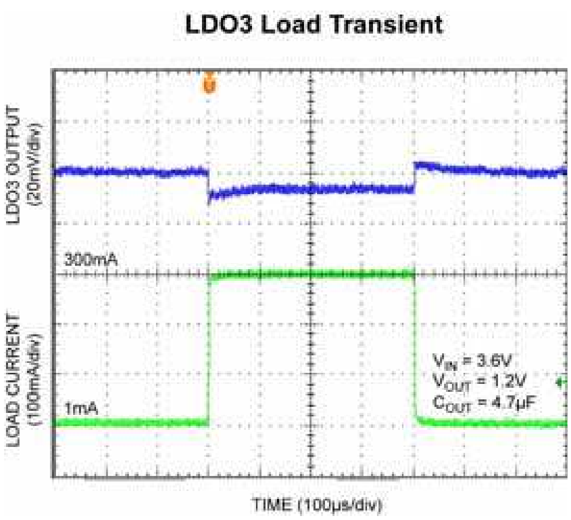
Functional Characteristics (LDO)

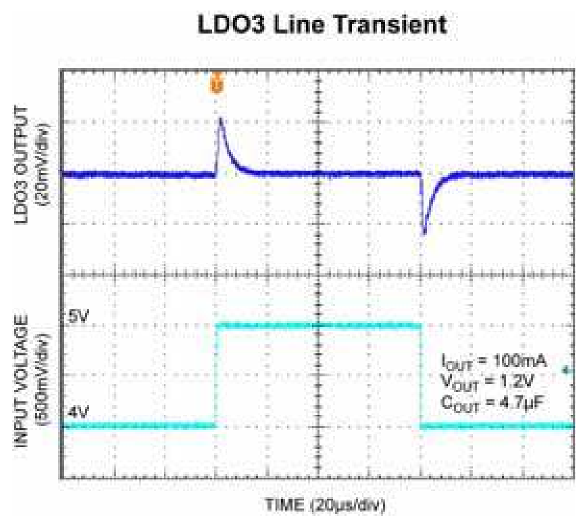




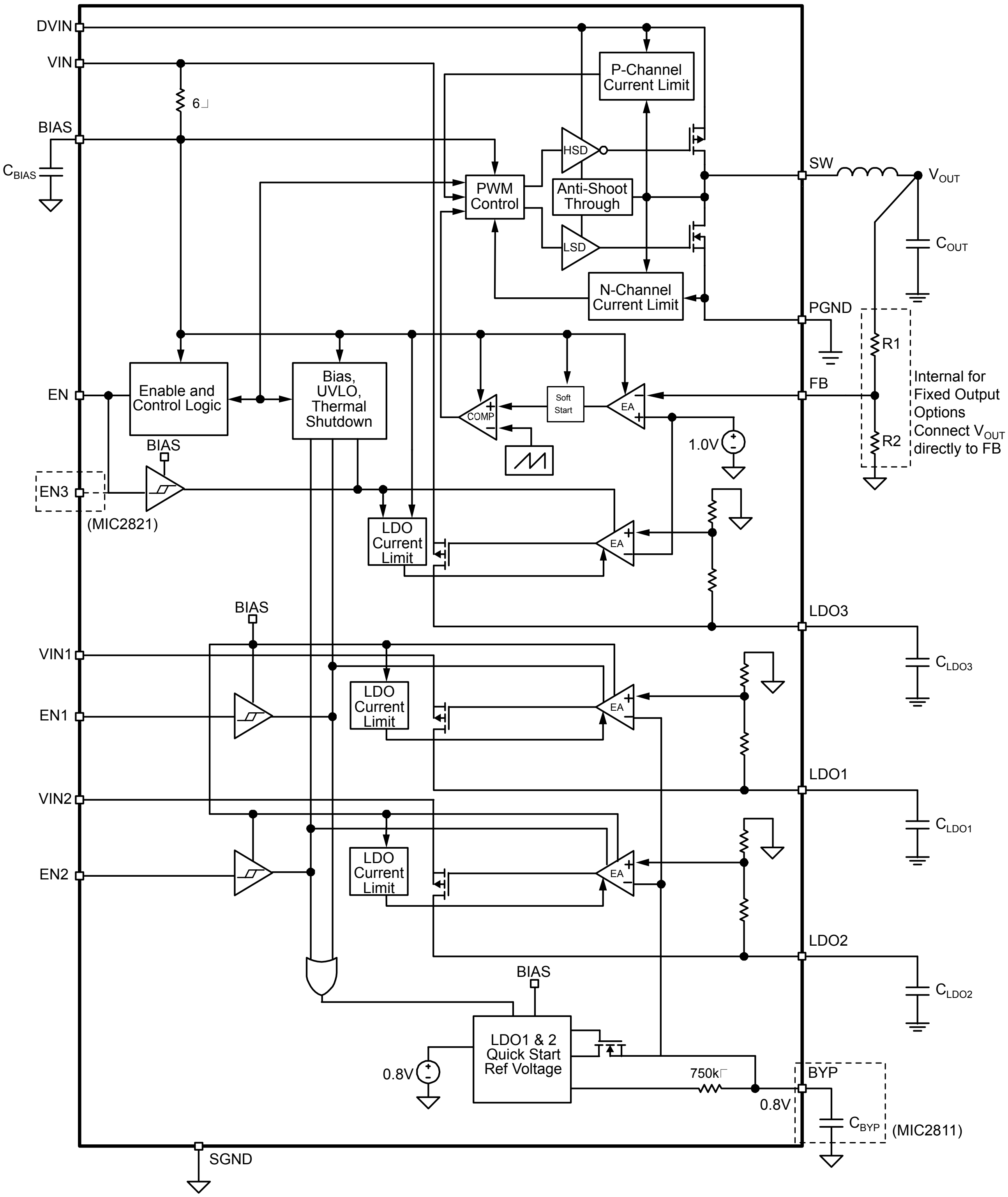








Functional Diagram



Block Diagram

Applications Information

The MIC2811 and MIC2821 are power management ICs with a single integrated step-down regulator and three low dropout regulators. LDO1, LDO2, and LDO3 are 300mA low dropout regulators supplied by their own independent input voltage pins. The supply to LDO3 (V_{IN}) also powers the bias circuitry and must be available for any output to be operational. This supply requires an external connection to DVIN. The step-down regulator is a 2MHz 600mA PWM power supply, using small values of L and C operating at over 90% efficiency.

DVIN/VIN/VIN1/VIN2

All four regulators, the switch mode regulator, LDO1, LDO2, and LDO3 have their own unique input voltage supply pin. VIN provides power to LDO3 and internal circuitry shared by all the regulators and therefore must be available for any of the regulators to operate properly. DVIN and VIN must be tied together and have a minimum input voltage of 2.7V. Inputs to LDO1 (VIN1) and LDO2 (VIN2) can go as low as 1.65V, but should never exceed the VIN and DVIN input voltage. Due to the high switching speeds, a 1µF input capacitor is recommended close to the DVIN, decoupled to the PGND pin.

LDO1

Regulated output voltage of LDO1. Power is provided by VIN1 and enabled through EN1. Recommended output capacitance is 2.2µF, decoupled to the SGND pin.

LDO2

Regulated output voltage of LDO2. Power is provided by VIN2 and enabled through EN2. Recommended output capacitance is 2.2µF, decoupled to the SGND pin.

LDO3

Regulated output voltage of LDO3. Power is provided by VIN and enabled through EN (MIC2811) or EN3 (MIC2821). Recommended output capacitance is 2.2µF, decoupled to the SGND pin.

SW

The switch (SW) pin connects directly to the inductor and provides the switching current necessary to operate in PWM mode. Due to the high speed switching on this pin, the switch node should be routed away from sensitive nodes.

DC/DC Output Capacitor

The DC/DC regulator requires an output capacitor for proper operation. Values of greater than 2.2µF improve transient response and noise reduction at high frequency. X7R/X5R dielectric-type ceramic capacitors are recommended because of their superior temperature performance. X7R-type capacitors change capacitance by 15% over their operating temperature range and are the most stable type of ceramic capacitors. Z5U and Y5V dielectric capacitors change value by as much as 50% to 60% respectively over their operating temperature ranges and for that reason are not recommended. Larger output capacitances can be achieved by placing tantalum or aluminum electrolytics in parallel with the ceramic capacitor. For example, a 100µF electrolytic in parallel with a 10µF ceramic can provide the transient and high frequency noise performance of a 100µF ceramic at a significantly lower cost. Specific undershoot/overshoot performance will depend on both the values and ESR/ESL of the capacitors.

Inductor Selection

Inductor selection will be determined by the following (not necessarily in the order of importance);

- Inductance
- Rated current value
- Size requirements
- DC resistance (DCR)

The MIC2811 and MIC2821 are designed for use with a 2.2µH inductor. Maximum current ratings of the inductor are generally given in two methods; permissible DC current and saturation current. Permissible DC current can be rated either for a 40°C temperature rise or a 10% to 20% loss in inductance. Ensure the inductor selected can handle the maximum operating current. When saturation current is specified, make sure that there is enough margin that the peak current will not saturate the inductor. Peak inductor current can be calculated as follows:

$$I_{PK} = I_{OUT} + \frac{V_{OUT}\left(1 - \frac{V_{OUT}}{V_{IN}}\right)}{2 \times f \times L}$$

The size requirements refer to the area and height requirements that are necessary to fit a particular design. Please refer to the inductor dimensions on their datasheet.

DC resistance is also important. While DCR is inversely proportional to size, DCR can represent a significant efficiency loss.

Efficiency Considerations

Efficiency is defined as the amount of useful output power, divided by the amount of power supplied.

$$Efficiency\_\% = \left(\frac{Vout \times Iout}{Vin \times Iin}\right) \times 100$$

Maintaining high efficiency serves two purposes. It reduces power dissipation in the power supply, reducing the need for heat sinks and thermal design considerations and it reduces consumption of current for battery powered applications. Reduced current draw from a battery increases the devices operating time and is critical in hand held devices.

There are two types of losses in switching converters; DC losses and switching losses. DC losses are simply the power dissipation of I^2R. Power is dissipated in the high side switch during the on cycle. Power loss is equal to the high side MOSFET R_{DSON} multiplied by the Switch Current^2. During the off cycle, the low side N-channel MOSFET conducts, also dissipating power. Device operating current also reduces efficiency. The product of the quiescent (operating) current and the supply voltage is another DC loss.

Over 100mA, efficiency loss is dominated by MOSFET R_{DSON} and inductor losses. Higher input supply voltages will increase the Gate to Source threshold on the internal MOSFETs, reducing the internal R_{DSON}. This improves efficiency by reducing DC losses in the device. All but the inductor losses are inherent to the device. In which case, inductor selection becomes increasingly critical in efficiency calculations. As the inductors are reduced in size, the DC resistance (DCR) can become quite significant. The DCR losses can be calculated as follows:

$$L\_Pd = Iout^2 \times DCR$$

From that, the loss in efficiency due to inductor resistance can be calculated as follows;

$$Efficiency\_Loss = \left[1 - \left(\frac{Vout \times Iout}{Vout \times Iout + L\_Pd}\right)\right] \times 100$$

Efficiency loss due to DCR is minimal at light loads and gains significance as the load is increased. Inductor selection becomes a trade-off between efficiency and size in this case.

PGND

Power ground (PGND) is the ground path for the high current PWM mode. The current loop area for the power ground should be as small as possible.

SGND

Signal ground (SGND) is the ground path for the biasing and control circuitry. The current loop for the signal ground should be as small as possible.

BYP (MIC2811 only)

For enhanced noise and PSRR performance on LDO1 & LDO2, the internal reference of the MIC2811 can be bypassed with a capacitor to ground. A quick-start feature allows for quick turn-on of the output voltage. The recommended nominal bypass capacitor is 0.1µF, but it can be increased, which will also result in an increase to the start-up time.

MIC2811 Layout Recommendations

A poor layout of the MIC2811 may cause unwanted voltage and current spikes. This can lead to noise on DC voltages and EMI radiating to nearby devices. The following are recommendations for the MIC2811/21 layout. The evaluation board layout is included as an example.

1. Place the MIC2811/21 with the pad size designated in the “Recommended Land Patterns” page of the Micrel website.

2. When laying out the components, keep the MIC2811, inductor, and filter capacitors physically close to keep traces as short as possible. The traces between these components carry relatively high switching currents and can affect adjacent signals.

3. The input capacitor between DVIN and PGND should be placed right next to the MIC2811/21. This will eliminate trace inductance effects and reduce internal noise for the MIC2811/21 control circuitry. The trace from the DVIN filter capacitor to the MIC2811/21 device should not be routed through any vias. This lessens the chance of noise coupling by the effective antenna of the via.

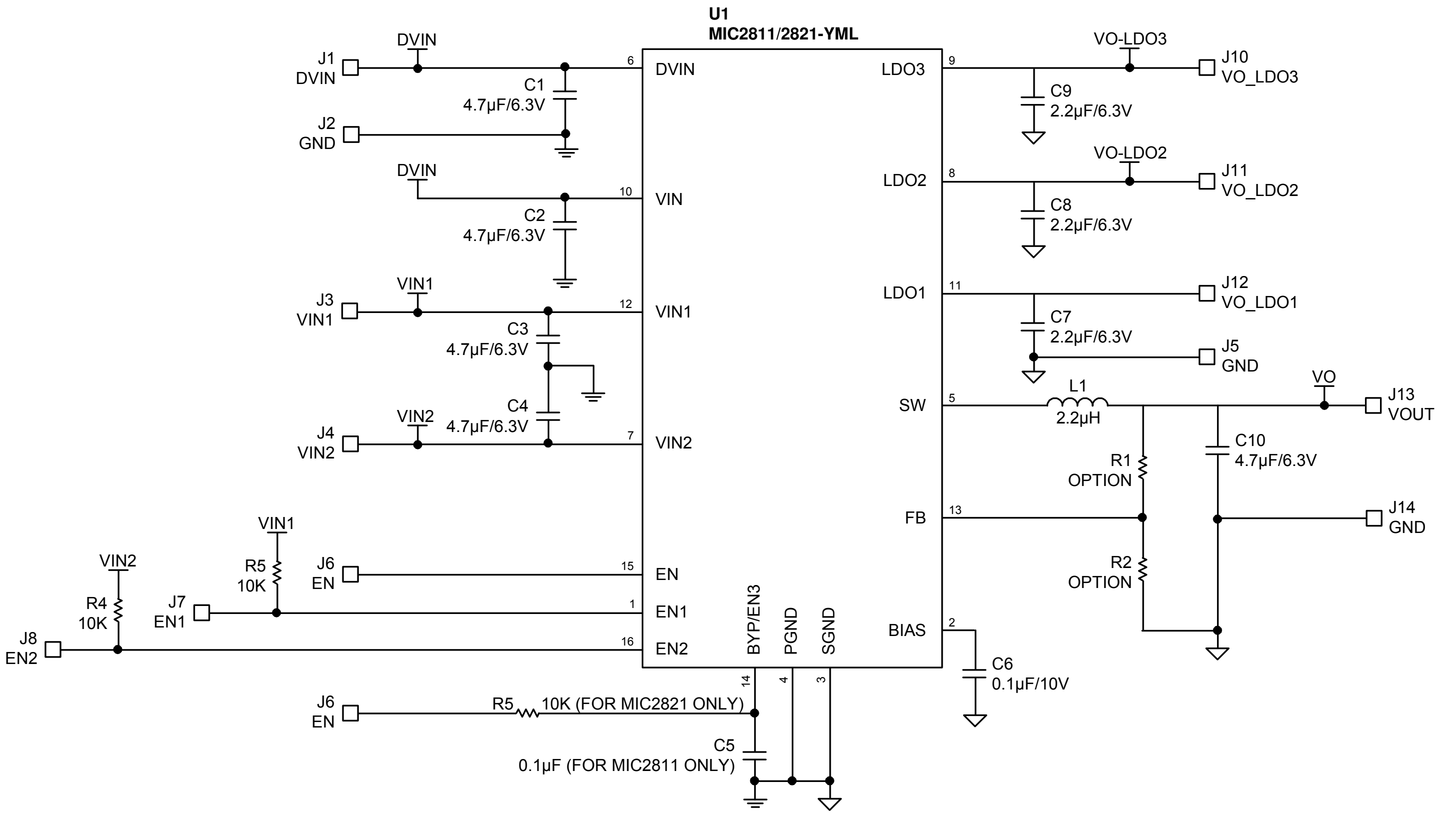
4. Monitoring the path of the switching currents will help minimize the radiated noise. In the first half of the switching cycle, current flows from the input filter capacitor through the high side switch within the MIC2811, then through the inductor to the output filter capacitor and lastly through ground. In the second half of the switching cycle, current is pulled up from ground through the low side synchronous switch within the MIC2807 by the inductor, to the output filter capacitor and then back through ground, forming a second current loop. Route these loops to ensure the current curls in the same direction, preventing magnetic field reversal between the switching cycles.

5. Connect the Bypass capacitor (MIC2811 Only) to the BYP pin and the AGND pin. AGND and PGND should be connected close to the chip at a single point in order to minimize undesirable behavior due to ground bounce. Input and output filter capacitors should be connected to PGND.

6. Connections between power components and the MIC2811 should have wide traces. It is good practice to use a minimum of 30mils (0.762mm) per Ampere for 1oz copper weight.

7. Route noise sensitive traces such as Feedback (FB), BIAS, and BYP away from the switching traces and the inductor. Noise coupled into these pins can affect the accuracy of the output. The Feedback pin should be connected at point of load for an accurate load regulation.

MIC2811/2821-YML Schematic



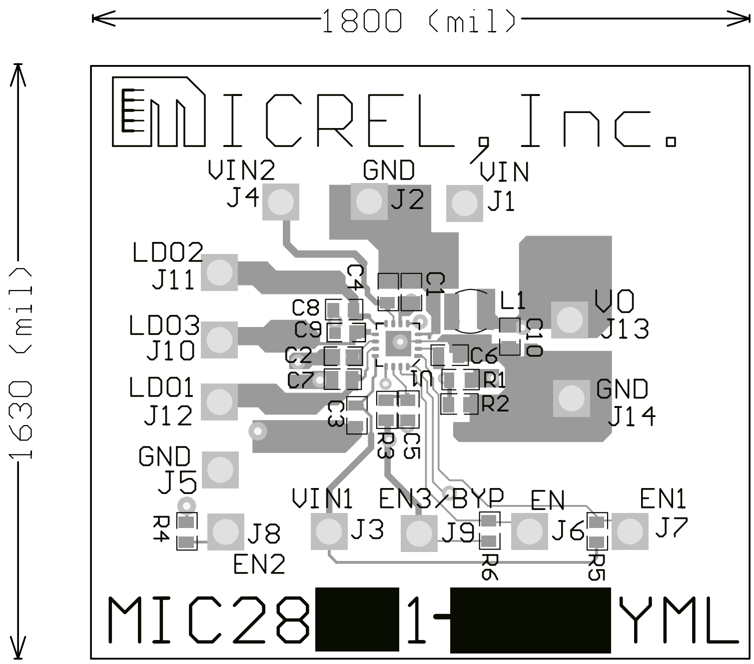
Bill of Materials

Item	Part Number	Manufacturer	Description	Qty.
C1, C2, C3, C4, C10	06036D475KAT2A	AVX[1]	4.7µF, 6.3V, 0603, X5R Ceramic Capacitor	5
	JMK107BJ475MA-T	Taiyo Yuden[5]		
	C1608X5R0J475K	TDK[3]		
	GRM188R60J475KE19D	muRATA[2]		
C7, C8, C9	C1608X5R0J225K	TDK[3]	2.2µF, 6.3V, 0603, X5R Ceramic Capacitor	3
	06036D225KAT2A	AVX[1]		
	GRM188R60J225KE19D	muRata[2]		
	VJ0603G225KXYAT	Vishay[4]		
C5, C6	C1005X7R1A104K	TDK[3]	0.1µF, 10V, X5R Ceramic Capacitor (C5 for MIC2811 EV Board only)	2
	VJ0603Y104KXQCW1BC	Vishay[4]		
L1	CDRH2D11HPNP	Sumida [6]	2.2µH, 1.1A, 3.2x3.2x1.2mm Inductor	1
	ME3220-222-ML	Coilcraft[7]	2.2µH, 1.1A, 2.5x3.2x2mm Inductor	
R1	CRCW06030R00FRT1	Vishay[4]	0Ω, 0603, 1% resistor	1
R2			Open	0
R3, R4, R5	CRCW06031002FRT1	Vishay[4]	10kΩ, 0603, 1% resistor	3
U1	**MIC2811/21**	**Micrel, Inc.[8]**	**16-Pin 3mm x 3mm MLF®**	**1**

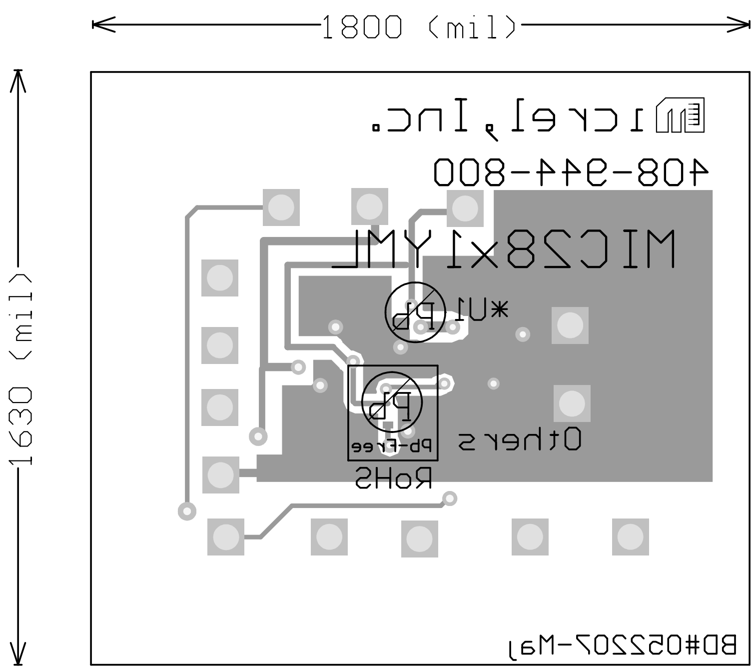
Notes:

1. AVX: www.avx.com
2. Murata: www.murata.com
3. TDK: www.tdk.com
4. Vishay: www.vishay.com
5. Taiyo Yuden: www.t-yuden.com
6. Sumida: www.sumida.com
7. Coilcraft: www.coilcraft.com
8. **Micrel, Inc.: www.micrel.com**

PCB Layout Recommendations

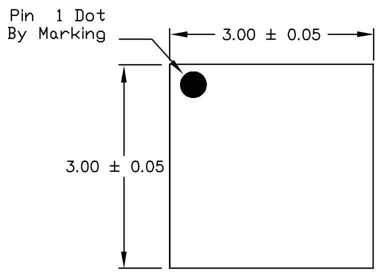


Top Layer

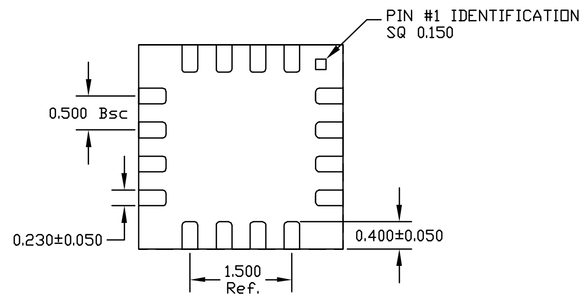


Bottom Layer

Package Information

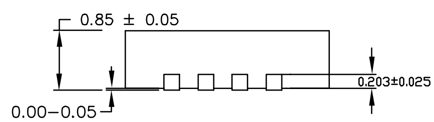


TOP VIEW



BOTTOM VIEW

NOTES:
1. ALL DIMENSIONS ARE IN MILLIMETERS, ANGLES ARE IN DEGREES.
   N IS THE TOTAL NUMBER OF TERMINALS.
2. MAX PACKAGE WARPAGE IS 0.05mm, MAX ALLOWABLE BURRS IS 0.076 mm IN ALL DIRECTIONS.
3. PIN #1 ID ON TOP WILL BE LASER/INK MARKED.



SIDE VIEW

16-Pin 3mm x 3mm MLF® (ML)

MICREL, INC. 2180 FORTUNE DRIVE SAN JOSE, CA 95131 USA
TEL +1 (408) 944-0800 FAX +1 (408) 474-1000 WEB http://www.micrel.com

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