agere systems

Data Sheet
March 2001

Dual Differential Transceiver BTF1A With Idle Bus Indicator

Features

Driver Features

- Produces a logic zero in third state
- 400 mV difference voltage in third state
- Two line drivers per package
- Logic to convert TTL input logic levels to differential, pseudo-emmiter coupled logic (ECL) output logic levels
- No line loading when V_{CC} = 0 V
- High output driver for 50 Ω loads
- 200 mA short-circuit current (typical)
- 2.0 ns maximum propagation delay
- <0.2 ns output skew (typical)

Receiver Features

- Two line receivers per package
- High input impedance ≅ 8 kΩ
- Logic that converts differential input logic levels to TTL output logic levels
- 4.0 ns maximum propagation delay
- <0.20 V input sensitivity (typical)
- –1.2 V to +7.2 V common-mode range

Common Device Features

- Common enable for each driver/receiver pair
- Operating temperature range: –40 °C to +125 °C (wider than the 41 Series)
- Single 5.0 V ± 5% supply
- 400 Mbits/s maximum data rate
- Meets enhanced small device interface (ESDI) standards
- Electrostatic discharge (ESD) performance better than the 41 Series
- Lower power requirement than the 41 Series

Description

The BTF1A device is a dual differential transceiver circuit that transmits and receives digital data over balanced transmission lines and is compatible with Lucent Technologies Microelectronics Group differential drivers and receivers. It is designed to provide a strong logic zero when in the third state. The minimum difference voltage in the third state is 400 mV. It is designed specifically for bus applications where a well-defined logic state is needed when the bus is idle. The driver puts out a logic **zero** when in the third state mode, which is easily overriden by an active buffer on the bus. When all the buffers on the bus are inactive (third state), the signal on the bus is a **zero** indicating that the bus is idle.

The dual drivers translate input TTL logic levels to differential pseudo-ECL output levels. The dual receiver converts differential input logic levels to TTL output levels. Each driver/receiver pair has its own common enable control allowing serial data and a control clock to be transmitted and received on a single integrated circuit. The BTF1A transceiver requires the customer to supply termination resistors on the circuit board.

The powerdown loading characteristics of the receiver input circuit are approximately 8 kΩ relative to the power supplies; hence, it will not load the transmission line when the circuit is powered down. For those circuits with termination resistors, the line will remain impedance matched when the circuit is powered down. The driver does not load the line when it is powered down.

Pin Information

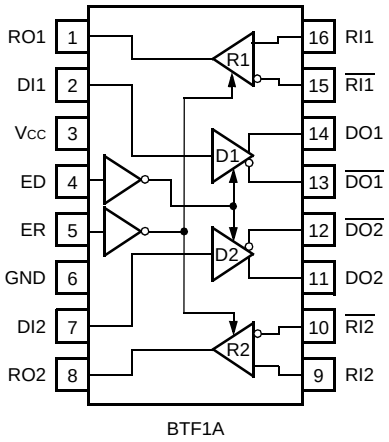

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Figure 1. Differential Transceiver Logic Diagram

Table 1. Enable Truth Table

ED	ER	D1	D2	R1	R2
0	0	Active	Active	Active	Active
1	0	Disabled	Disabled	Active	Active
0	1	Active	Active	Disabled	Disabled
1	1	Disabled	Disabled	Disabled	Disabled

Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings can cause permanent damage to the device. These are absolute stress ratings only. Functional operation of the device is not implied at these or any other conditions in excess of those given in the operational sections of the data sheet. Exposure to absolute maximum ratings for extended periods can adversely affect device reliability.

Table 2. Absolute Maximum Ratings

Parameter	Symbol	Min	Max	Unit
Power Supply Voltage	V_{CC}	—	6.5	V
Ambient Operating Temperature	T_A	–40	125	°C
Storage Temperature	T_{stg}	–55	150	°C

Electrical Characteristics

For variations in electrical characteristics over the temperature range, see Figure 10 through Figure 12.

Table 3. Power Supply Current Characteristics

T_A = –40 °C to +125 °C, V_{CC} = 5 V ± 0.25 V.

Parameter	Symbol	Min	Typ	Max	Unit
Power Supply Current (V_{CC} = 5.5 V)					
All Outputs Disabled	I_{CC}	—	40	65	mA
All Outputs Enabled	I_{CC}	—	20	35	mA

Third State

The BTF1A driver produces pseudo-ECL levels, and has a third-state mode, which is different than a conventional TTL device. When a driver is placed in the third state, the base of the output transistors are pulled low, bringing the outputs below the active-low level. The BTF1A is unique because it provides a logic zero at its output when in the third state. If all the buffers on the bus are in the third state, the BTF1A is designed to deliver a logic zero to the bus to act as an indicator that the bus is idle. The guaranteed zero level, Vdo – Vdo, is 0.4 V.

Electrical Characteristics (continued)

Table 4. Driver Voltage and Current Characteristics

For variations in output voltage over the temperature range, see Figure 10 and Figure 11. T_A = –40 °C to +125 °C.

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltages:					
Low[1]	V_{OL}	V_{OH} – 1.4	V_{OH} – 1.1	V_{OH} – 0.65	V
High[1]:	V_{OH}	V_{CC} – 1.8	V_{CC} – 1	V_{CC} – 0.8	V
Differential Voltage (V_{OH} – V_{OL})	V_{DIFF}	0.65	1.1	1.4	V
Output Voltage Third State:					
Difference Voltage $V\overline{do}$ - Vdo	V_{DIFZ}	0.4	0.6	—	V
Third State, I_{OH} = –1.0 mA, V_{CC} = 4.75 V	V_{OZ}	—	—	V_{OL} – 0.2	V
Output Voltages (T_A = 0 °C to 85 °C):					
Low[1]	V_{OL}	V_{OH} – 1.4	V_{OH} – 1.1	V_{OH} – 0.8	V
High[1]:	V_{OH}	V_{CC} – 1.5	V_{CC} – 1	V_{CC} – 0.8	V
Differential Voltage (V_{OH} – V_{OL})	V_{DIFF}	0.8	1.1	1.4	V
Input Voltages:					
Low, V_{CC} = 5.25 V:	V_{IL}[2]	—	—	0.8	V
Data Input	V_{IL}[3]	—	—	0.8	V
Enable Input	V_{IL}[3]	—	—	0.7	V
High, V_{CC} = 4.75 V	V_{IH}[2]	2.0	—	—	V
Clamp, V_{CC} = 4.75 V, I_I = –5.0 mA	V_{IK}	—	—	–1.0	V
Short-circuit Output Current, V_{CC} = 5.25 V	I_{OS}	–100	—	—	mA
Input Currents, V_{CC} = 5.25 V:					
Low, V_I = 0.4 V	I_{IL}	—	—	–400	µA
High, V_I = 2.7 V	I_{IH}	—	—	20	µA
Reverse, V_I = 5.25 V	I_{IH}	—	—	100	µA

1. Values are with terminations as per Figure 7.
2. The input levels and difference voltage provide zero noise immunity and should be tested only in a static, noise-free environment.
3. Test must be performed one lead at a time to prevent damage to the device.

Electrical Characteristics (continued)

Table 5. Receiver Voltage and Current Characteristics

For variation in minimum V_{OH} and maximum V_{OL} over the temperature range, see Figure 10. T_A = –40 °C to +125 °C.

Parameter	Symbol	Min	Typ	Max	Unit
Output Voltages V_{CC} = 4.75 V:					
Low, I_{OL} = 8.0 mA[1]	V_{OL}	—	—	0.5	V
High, I_{OH} = –400 µA	V_{OH}	2.4	—	—	V
Enable Input Voltages:					
Low, V_{CC} = 5.25 V	V_{IL}[1]	—	—	0.7	V
High, V_{CC} = 4.75 V	V_{IH}[1]	2.0	—	—	V
Clamp, V_{CC} = 4.75 V, I_I = –5.0 mA	V_{IK}	—	—	–1.0	V
Minimum Differential Input Voltages, $V_{IH} - V_{IL}$:[2]					
–0.80 V < V_{IH} < 7.2 V, –1.2 V < V_{IL} < 6.8 V	V_{TH}[1]	—	0.1	0.20	V
Input Offset Voltage	V_{OFF}	—	0.03	0.05	V
Output Currents, V_{CC} = 5.25 V:					
Off-state (high Z), V_O = 0.4 V	I_{OZL}	—	—	–20	µA
Off-state (high Z), V_O = 2.4 V	I_{OZH}	—	—	20	µA
Short Circuit	I_{OS}[3]	–25	—	–100	mA
Enable Input Currents, V_{CC} = 5.25 V:					
Low, V_{IN} = 0.4 V	I_{IL}	—	—	–400	µA
High, V_{IN} = 2.7 V	I_{IH}	—	—	20	µA
Reverse, V_{IN} = 5.5 V	I_{IH}	—	—	100	µA
Differential Input Currents:					
Low, V_{IN} = –1.2 V	I_{IL}	—	—	–1.0	mA
High, V_{IN} = 7.2 V	I_{IH}	—	—	1.0	mA

1. The input levels and difference voltage provide zero noise immunity and should be tested only in a static, noise-free environment.
2. Outputs of unused receivers assume a logic 1 level when the inputs are left open. (It is recommended that all unused positive inputs be tied to the positive power supply. No external series resistor is required.)
3. Test must be performed one lead at a time to prevent damage to the device.

Timing Characteristics

Table 6. Driver Timing Characteristics (See Figure 3 and Figure 4.)

For t_{P1} and t_{P2} propagation delays over the temperature range, see Figure 13. Propagation delay test circuit connected to output is shown in Figure 7. T_A = –40 °C to +125 °C, V_{CC} = 5 V ± 0.25 V.

Parameter	Symbol	Min	Typ	Max	Unit
Propagation Delay:					
Input High to Output[1]	t_{P1}[2]	0.8	1.2	2.0	ns
Input Low to Output[1]	t_{P2}[2]	0.8	1.2	2.0	ns
Capacitive Delay	Δtp	—	0.02	0.03	ns/pF
Disable Time (either E1 or E2):					
High-to-High Impedance	t_{PHZ}	4	8	12	ns
Low-to-High Impedance	t_{PLZ}	4	8	12	ns
Enable Time (either E1 or E2):					
High Impedance to High	t_{PZH}	4	8	12	ns
High Impedance to Low	t_{PZL}	4	8	12	ns
Output Skew:					
$\lvert t_{P1} - t_{P2} \rvert$	t_{skew1}	—	0.1	0.3	ns
$\lvert t_{PHH} - t_{PHL} \rvert$, $\lvert t_{PLH} - t_{PLL} \rvert$	t_{skew2}	—	0.2	0.5	ns
Difference Between Drivers	Δt_{skew}	—	—	0.3	ns
Rise Time (20%—80%)	t_{tLH}	—	0.7	2	ns
Fall Time (80%—20%)	t_{tHL}	—	0.7	2	ns

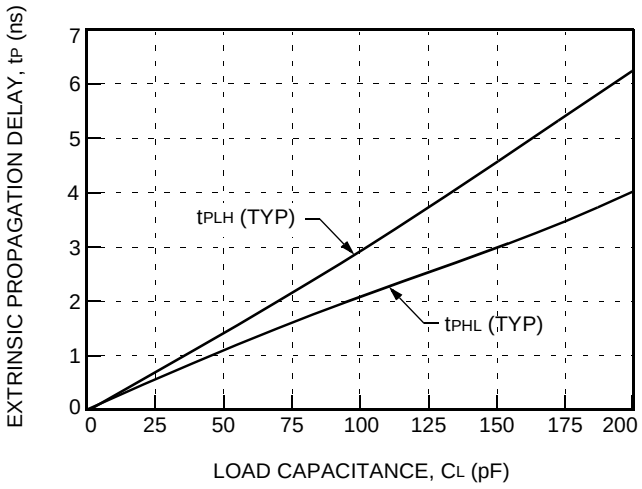
1. CL = 5 pF. Capacitor is connected from each output to ground.
2. tP1 and tP2 are measured from the 1.5 V point of the input to the crossover point of the outputs (see Figure 3).

Table 7. Receiver Timing Characteristics (See Figure 5 and Figure 6.)

For propagation delays (t_{PLH} and t_{PHL}) over the temperature range, see Figure 14 and Figure 15. Propagation delay test circuit connected to output is shown in Figure 8. T_A = –40 °C to +125 °C, V_{CC} = 5 V ± 0.25 V.

Parameter	Symbol	Min	Typ	Max	Unit
Propagation Delay:					
Input to Output High	t_{PLH}	1.5	2.5	4.0	ns
Input to Output Low	t_{PHL}	1.5	2.5	4.0	ns
Pulse Width Distortion, ltpHL-tpLHI:					
Load Capacitance (C_L) = 15 pF	tskew1	—	—	0.7	ns
Load Capacitance (C_L) = 150 pF	tskew1	—	—	4.0	ns
Output Waveform Skews:					
Part-to-Part Skew, T_A = 75 °C	Δtskew1p-p	—	0.8	1.4	ns
Part-to-Part Skew, T_A = –40 °C to +125 °C	Δtskew1p-p	—	—	1.5	ns
Same Part Skew	Δtskew	—	—	0.3	ns
Disable Time, C_L = 5 pF:					
High-to-high Impedance	t_{PHZ}	—	5	12	ns
Low-to-high Impedance	t_{PLZ}	—	5	12	ns
Enable Time:					
High Impedance to High	t_{PZH}	—	8	12	ns
High Impedance to Low	t_{PZL}	—	8	12	ns
Rise Time (20%—80%)	t_{tLH}	—	—	3.0	ns
Fall Time (80%—20%)	t_{tHL}	—	—	3.0	ns

Timing Characteristics (continued)



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Note: This graph is included as an aid to the system designers. Total circuit delay varies with load capacitance. The total delay is the sum of the delay due to the external capacitance and the intrinsic delay of the device.

Figure 2. Typical Extrinsic Propagation Delay Versus Load Capacitance at 25 °C

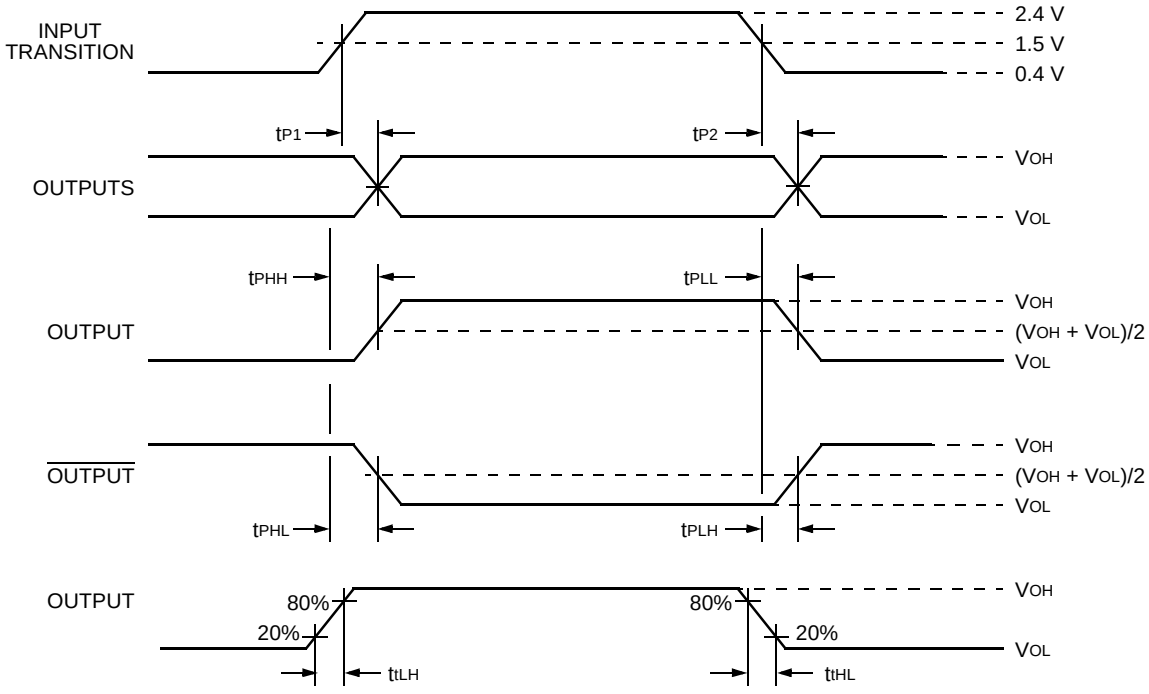

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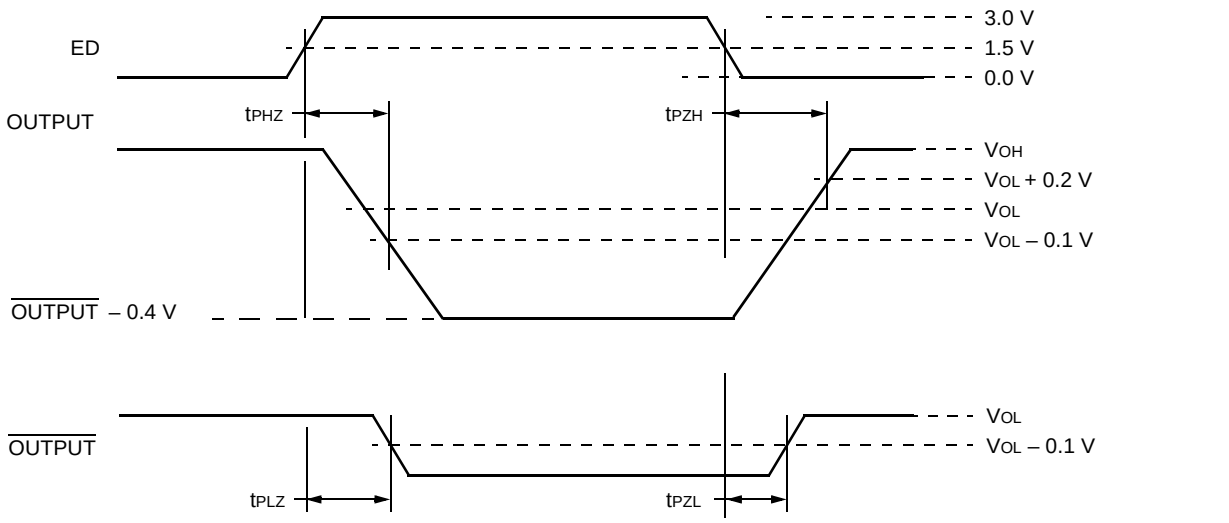
Figure 3. Driver Propagation Delay Timing

Timing Characteristics (continued)



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Note: In the third state, OUTPUT is 0.4 V more negative than $\overline{\text{OUTPUT}}$.

Figure 4. Driver Enable and Disable Timing

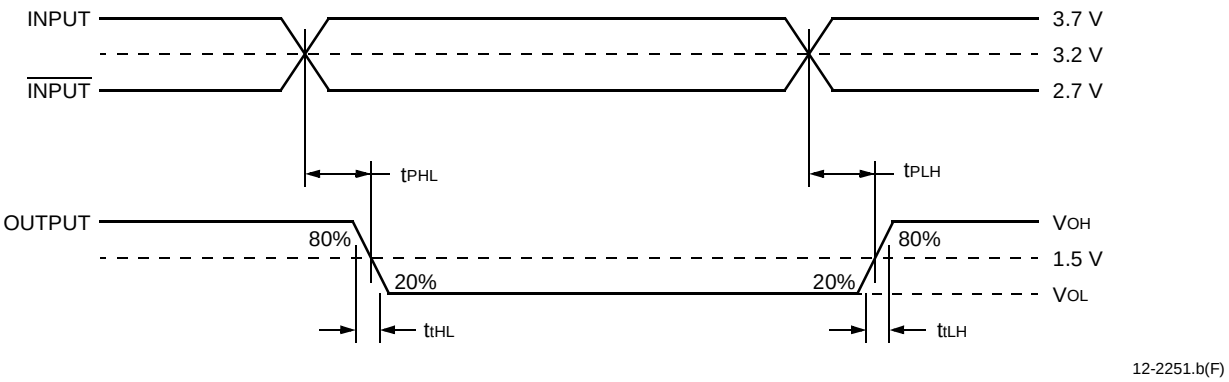

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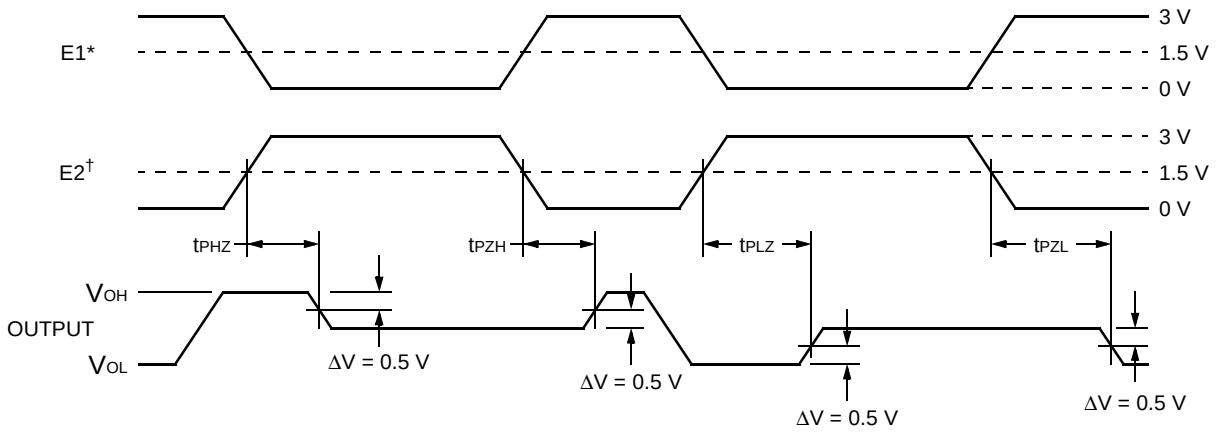
Figure 5. Receiver Propagation Delay Timing

Timing Characteristics (continued)



* E2 = 1 while E1 changes state.
† E1 = 0 while E2 changes state.

Figure 6. Receiver Enable and Disable Timing

Test Conditions

Parametric values specified under the Electrical Characteristics and Timing Characteristics sections for the data transmission driver devices are measured with the following output load circuits.

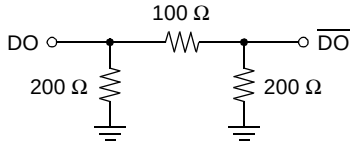
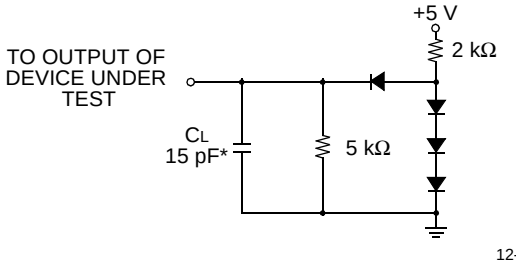


Figure 7. Driver Propagation Delay Test Circuit



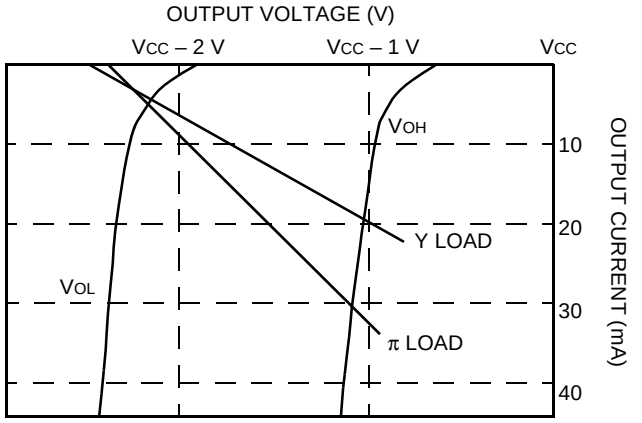
* Includes probe and jig capacitances.

Note: All 458E, IN4148, or equivalent diodes.

Figure 8. Receiver Propagation Delay Test Circuit

Output Characteristics

Figure 9 illustrates typical driver output characteristics. Included are load lines for two typical termination configurations.



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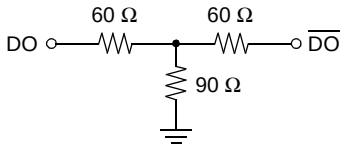
A. Output Current vs. Output Voltage for Loads Shown in B and C



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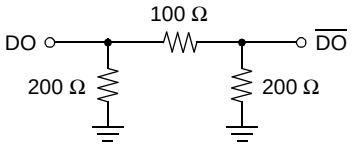
B. Y Load



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C. π Load

Figure 9. Driver Output Current vs. Voltage Characteristics

Temperature Characteristics

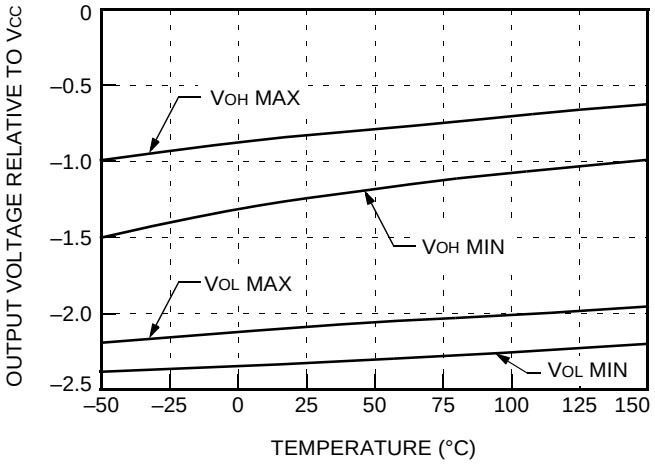

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Figure 10. VOL and VOH Extremes for Drivers vs. Temperature for 100 Ω Load

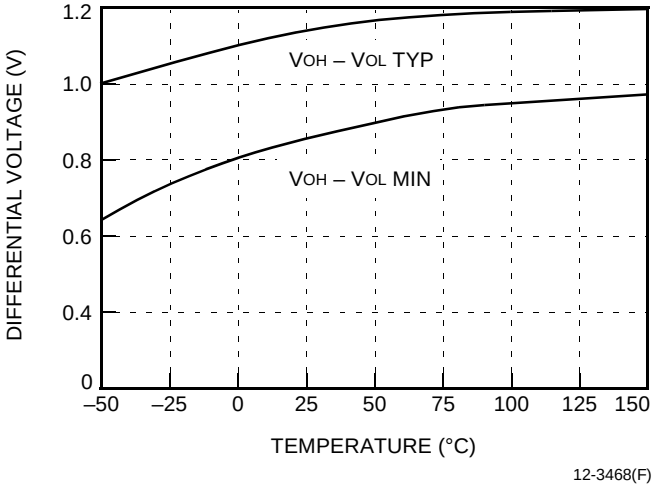

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Figure 11. Differential Voltage (VOH – VOL) for Drivers vs. Temperature

Temperature Characteristics (continued)

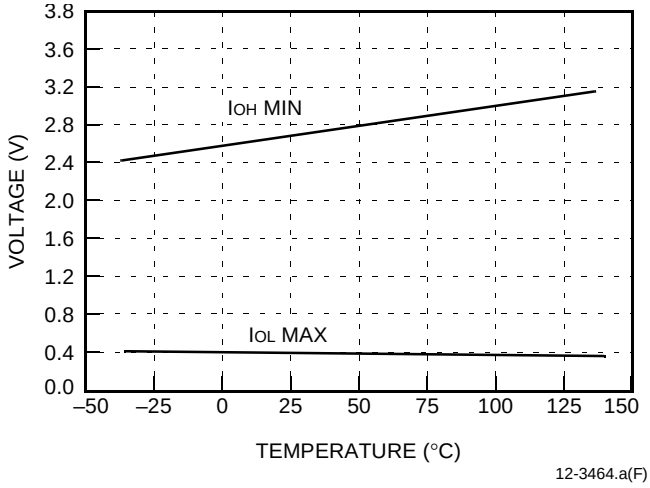


Figure 12. Minimum V_{OH} and Maximum V_{OL} vs. Temperature at V_{CC} = 4.5 V for the Receiver

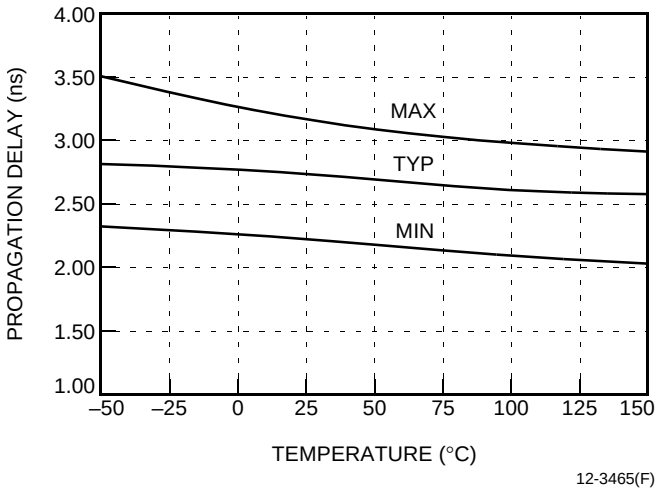


Figure 14. Propagation Delay for a High Output (t_{PLH}) vs. Temperature at V_{CC} = 5.0 V for the Receivers

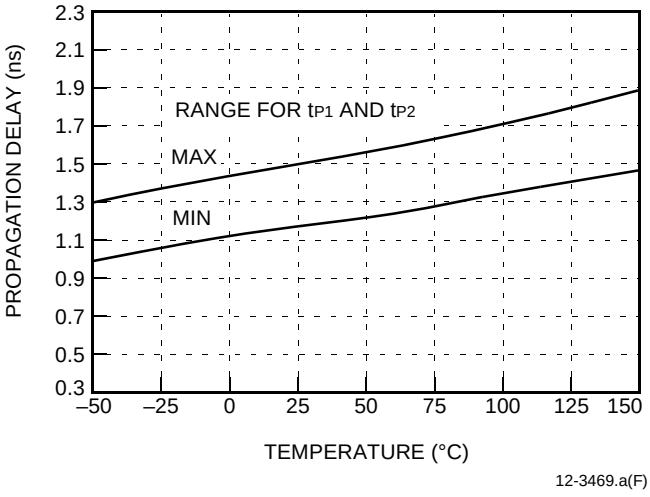


Figure 13. Min and Max for t_{P1} and t_{P2} Propagation Delays vs. Temperature for the Driver

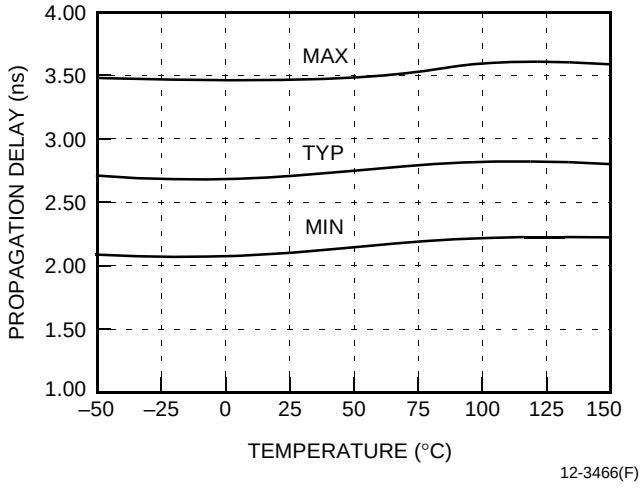


Figure 15. Propagation Delay for a Low Output (t_{PHL}) vs. Temperature at V_{CC} = 5.0 V for the Receivers

Handling Precautions

CAUTION: This device is susceptible to damage as a result of ESD. Take proper precautions during both handling and testing. Follow guidelines such as JEDEC Publication No. 108-A (Dec. 1988).

When handling and mounting line driver products, proper precautions should be taken to avoid exposure to ESD. The user should adhere to the following basic rules for ESD control:

1. Assume that all electronic components are sensitive to ESD damage.
2. Never touch a sensitive component unless properly grounded.
3. Never transport, store, or handle sensitive components except in a static-safe environment.

ESD Failure Models

Lucent employs two models for ESD events that can cause device damage or failure:

1. A human body model (HBM) that is used by most of the industry for ESD-susceptibility testing and protection-design evaluation. ESD voltage thresholds are dependent on the critical parameters used to define the model. A standard HBM (resistance = 1500 Ω, capacitance = 100 pF) is widely used and, therefore, can be used for comparison purposes.
2. A charged-device model (CDM), which many believe is the better simulator of electronics manufacturing exposure.

Table 8 and Table 9 illustrate the role these two models play in the overall prevention of ESD damage. HBM ESD testing is intended to simulate an ESD event from a charged person. The CDM ESD testing simulates charging and discharging events that occur in production equipment and processes, e.g., an integrated circuit sliding down a shipping tube.

The HBM ESD threshold voltage presented here was obtained by using these circuit parameters.

Table 8. Typical ESD Thresholds for Data Transmission Transceivers

Device	HBM Threshold	CDM Threshold
Differential Inputs	>800	>1000
All Other Pins	>2000	>1000

Table 9. ESD Damage Protection

	ESD Threat Controls	
	Personnel	**Processes**
Control	Wrist straps ESD shoes Antistatic flooring	Static-dissipative materials Air ionization
Model	Human body model (HBM)	Charged-device model (CDM)

Latch Up

Latch up evaluation has been performed on the data transmission receivers. Latch up testing determines if the power-supply current exceeds the specified maximum due to the application of a stress to the device under test. A device is considered susceptible to latch up if the power supply current exceeds the maximum level and remains at that level after the stress is removed.

Lucent performs latch up testing per an internal test method which is consistent with JEDEC Standard No. 17 (previously JC-40.2) *CMOS Latch Up Standardized Test Procedure*.

Latch up evaluation involves three separate stresses to evaluate latch up susceptibility levels:

1. dc current stressing of input and output pins.
2. Power supply slew rate.
3. Power supply overvoltage.

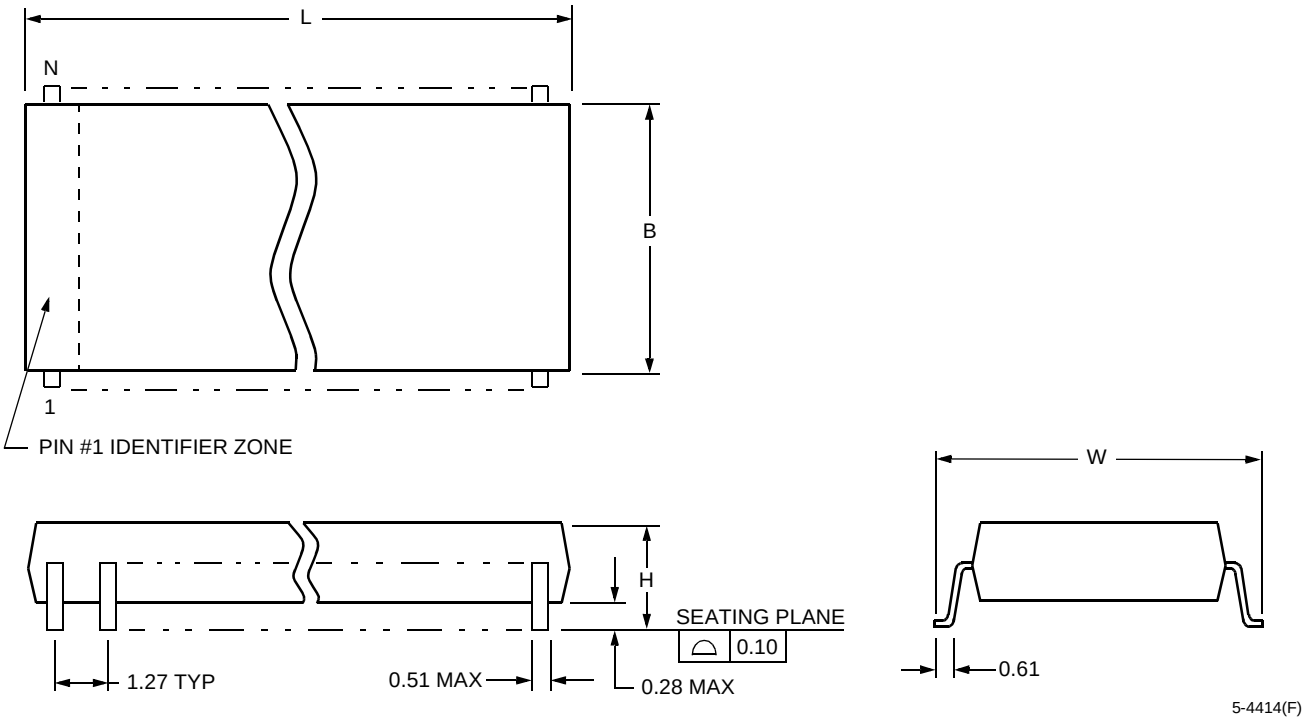
Table 10. Latch Up Test Criteria and Test Results

		dc Current Stress of I/O Pins	Power Supply Slew Rate	Power Supply Overvoltage
Data Transmission Receiver ICs	**Minimum Criteria**	≥150 mA	≤1 µs	≥1.75 x Vmax
	Test Results	≥250 mA	≤100 ns	≥2.25 x Vmax

Outline Diagrams

16-Pin SOIC (SONB/SOG)

Dimensions are in millimeters.



Package Description	Number of Pins (N)	Package Dimensions			
		Maximum Length (L)	Maximum Width Without Leads (B)	Maximum Width Including Leads (W)	Maximum Height Above Board (H)
Small-Outline, Gull-Wing (SOG)	16	10.49	7.62	10.64	2.67

Note: The dimensions in this oultine diagram are intended for informational purposes only. For detailed schematics to assist your design efforts, please contact your Lucent Technologies sales representative.

Power Dissipation

System designers incorporating Lucent data transmission drivers in their applications should be aware of package and thermal information associated with these components.

Proper thermal management is essential to the long-term reliability of any plastic encapsulated integrated circuit. Thermal management is especially important for surface-mount devices, given the increasing circuit pack density and resulting higher thermal density. A key aspect of thermal management involves the junction temperature (silicon temperature) of the integrated circuit.

Several factors contribute to the resulting junction temperature of an integrated circuit:

- Ambient use temperature
- Device power dissipation
- Component placement on the board
- Thermal properties of the board
- Thermal impedance of the package

Thermal impedance of the package is referred to as Θ_{ja} and is measured in °C rise in junction temperature per watt of power dissipation. Thermal impedance is also a function of airflow present in system application.

The following equation can be used to estimate the junction temperature of any device:

$T_j = T_A + P_D \Theta_{ja}$

where:

T_j is device junction temperature (°C).

T_A is ambient temperature (°C).

P_D is power dissipation (W).

Θ_{ja} is package thermal impedance (junction to ambient—°C/W).

The power dissipation estimate is derived from two factors:

- Internal device power
- Power associated with output terminations

Multiplying I_{CC} times V_{CC} provides an estimate of internal power dissipation.

The power dissipated in the output is a function of the:

- Termination scheme on the outputs
- Termination resistors
- Duty cycle of the output

Package thermal impedance depends on:

- Airflow
- Package type (e.g., DIP, SOIC, SOIC/NB)

The junction temperature can be calculated using the previous equation, after power dissipation levels and package thermal impedances are known.

Figure 16 illustrates the thermal impedance estimates for the various package types as a function of airflow. This figure shows that package thermal impedance is higher for the narrow-body SOIC package. Particular attention should, therefore, be paid to the thermal management issues when using this package type.

In general, system designers should attempt to maintain junction temperature below 125 °C. The following factors should be used to determine if specific data transmission drivers in particular package types meet the system reliability objectives:

- System ambient temperature
- Power dissipation
- Package type
- Airflow

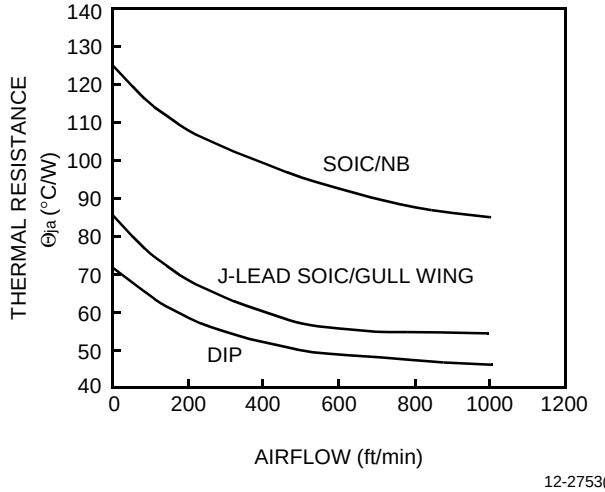


Figure 16. Power Dissipation

Ordering Information

Part Number	Driver Terminating[1]	Receiver Terminating[2]	Package Type	Comcode
BTF1A16G	None	None	16-pin, Plastic SOIC	108648861
BTF1A16G-TR	None	None	Tape and Reel SOIC	108698887

1. Indicates on-chip output terminating resistors from each driver output to ground.
2. Indicates on-chip input terminations across receiver inputs.

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