February 2006

FAN6520B
Single Synchronous Buck PWM Controller

Features

- Accepts 1.5V to 5V for V_{IN}
- Output Range 0.8V to V_{IN}
  - 0.8V Internal Reference
  - ±1.5% Over Line Voltage and Temperature
- Drives N-Channel MOSFETs
- Simple Single-Loop Control Design
  - Voltage-Mode PWM Control
- Fast Transient Response
  - High-Bandwidth Error Amplifier
  - Full 0% to 100% Duty Cycle
- Small Converter Size
  - 300kHz Fixed Frequency Oscillator
  - Internal Soft-Start
  - 8-Lead SOIC

Applications

- Power Supplies for PC Subsystems and Peripherals
- MCH, GTL, and AGP Supplies
- Cable Modems, Set Top Boxes, and DSL Modems
- DSP, Memory
- Low-Voltage Distributed Power Supplies
- ACPI Power Control
- 5V Input DC-DC Regulators

Description

The FAN6520B makes simple work out of implementing a complete control and protection scheme in a DC-DC stepdown converter.

Designed to drive N-channel MOSFETs in a synchronous buck topology, the FAN6520B integrates the control, output adjustment, and monitoring functions into a single 8-lead package.

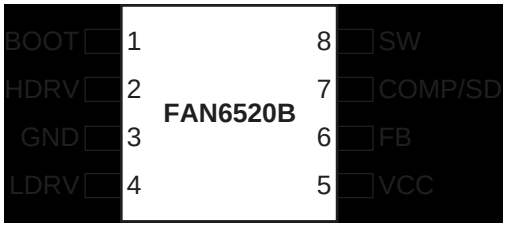
The FAN6520B is easy to use, employs a single feedback loop, and voltage-mode control with fast transient response. The output voltage can be precisely regulated to as low as 0.8V, with a maximum tolerance of 1.5% over temperature and line voltage variations. A fixed frequency oscillator reduces design complexity while balancing cost and typical application cost. The error amplifier features a 15MHz gain-bandwidth product and an 8V/µs slew rate which enables high converter bandwidth for fast transient performance. The resulting PWM duty cycles range from 0% to 100%.

The FAN6520B is rated for operation from 0° to +70°C with the FAN6520BI rated from –40° to +85°C.

Ordering Information

Part Number	Temperature Range	Package	Packing
FAN6520B	0°C to 70°C	SOIC-8	Rails
FAN6520BMX	0°C to 70°C	SOIC-8	Tape and Reel
FAN6520BIM	–40°C to 85°C	SOIC-8	Rails
FAN6520BIMX	–40°C to 85°C	SOIC-8	Tape and Reel

Pin Configuration



FAN6520BM 8-pin SOIC Package

Pin Definitions

Pin #	Pin Name	Pin Function Description
1	BOOT	**Bootstrap Supply Input.** Provides a boosted voltage to the high-side MOSFET driver. Connect to bootstrap capacitor and diode as shown in Figure 1.
2	HDRV	**High Side Gate Drive Output.** Connect to the gate of the high-side power MOSFET(s). This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the upper MOSFET has turned off.
3	GND	**Ground.** The signal and power ground for the IC. Tie this pin to the ground island/plane through the lowest impedance connection available. Connect directly to source of low-side MOSFET(s).
4	LDRV	**Low Side Gate Drive Output.** Connect to the gate of the low-side power MOSFET(s). This pin is also monitored by the adaptive shoot-through protection circuitry to determine when the lower MOSFET has turned off.
5	VCC	**VCC.** Provides bias power to the IC and the drive voltage for LDRV. Bypass with a good quality ceramic capacitor (X7R or X5R) as close to this pin as possible.
6	FB	**Feedback.** This pin is the inverting input of the internal error amplifier. Use this pin, in combination with the COMP pin, to compensate the voltage-control feedback loop of the converter.
7	COMP/SD	**COMP/SD.** This is a multiplexed pin. During operation, the output of the error amplifier drives this pin. Pulling COMP to a level below 0.8V disables the controller. Disabling the controller causes the oscillator to stop, the HDRV and LDRV outputs to be held low, and the soft-start circuitry to re-arm. Connect a 75kΩ resistor between VCC and COMP/SD pin to pull up.
8	SW	**Switch Node Input.** Connect as shown in Figure 1. The SW pin provides return for the high-side bootstrapped driver, is a sense point for the adaptive shoot-thru protection.

Typical Application

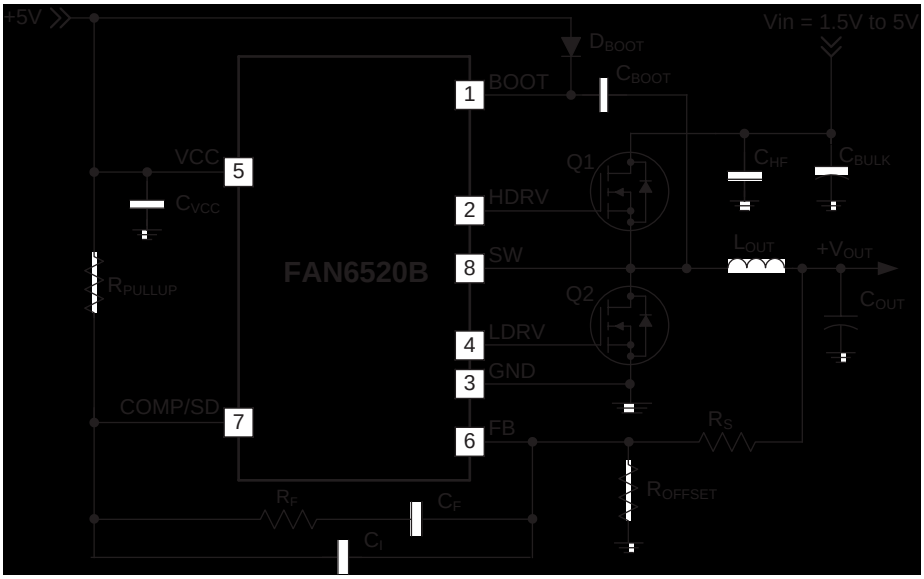


Figure 1. Typical Application

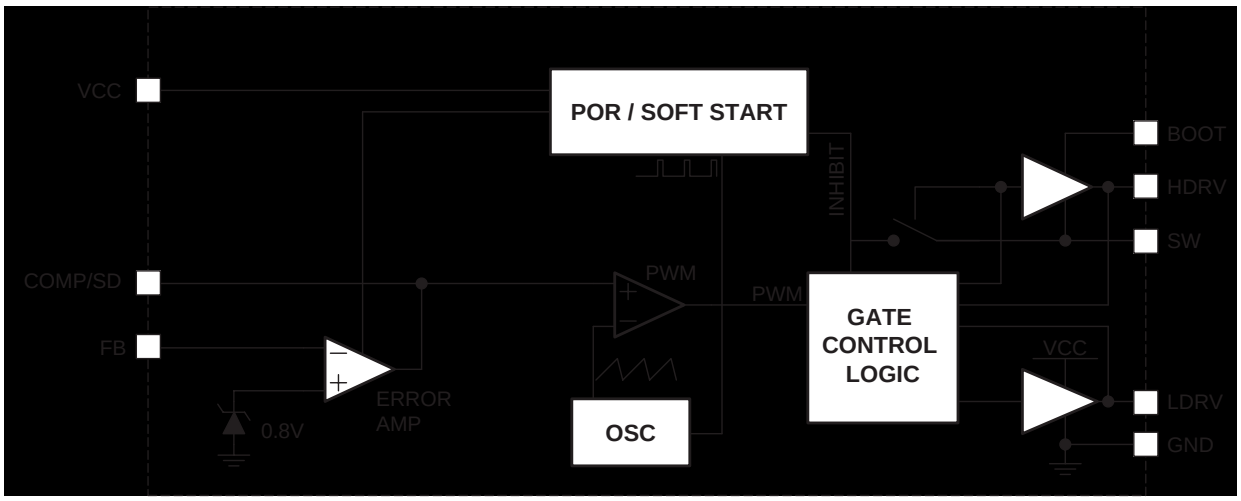


Figure 2. Functional Block Diagram

Absolute Maximum Ratings

Absolute maximum ratings are the values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.

Parameter		Min.	Max.	Units
VCC to GND			6	V
VBOOT to GND			15	V
HDRV ($V_{BOOT} - V_{SW}$)			6	V
LDRV		–0.5	6	V
SW to PGND	Continuous	–0.5	6	V
	Transient (t < 50nsec)	–3	7	V
All other pins			5.5	V

Thermal Information

Parameter	Min.	Typ.	Max.	Units
Storage Temperature	–65		150	°C
Lead Soldering Temperature, 10 seconds			300	°C
Vapor Phase, 60 seconds			215	°C
Infrared, 15 seconds			220	°C
Power Dissipation (P_D), T_A = 25°C			715	mW
Thermal Resistance – Junction to Case θ_{JC}		40		°C/W
Thermal Resistance – Junction to Ambient θ_{JA}		140		°C/W

Recommended Operating Conditions

Parameter	Conditions	Min.	Typ.	Max.	Units
Supply Voltage VCC	VCC to PGND	4.5	5	5.5	V
Ambient Temperature (T_A)	FAN6520B	0		70	°C
	FAN6520BI	–40		85	°C
Junction Temperature (T_J)		–40		125	°C

Electrical Specifications

VCC = 5V, and TA = 25°C using circuit in Figure 1 unless otherwise noted. The • denotes specifications which apply over the full operating temperature range.

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Units
Supply Current							
VCC Current	I_{VCC}	HDRV, LDRV open	•	1.5	2.4	3.8	mA
Power-On Reset							
Rising VCC POR Threshold	POR		•	4.00	4.22	4.45	V
VCC POR Threshold Hysteresis					170		mV
Oscillator							
Frequency	F_{OSC}	FAN6520B	•	250	300	340	kHz
		FAN6520BI	•	230	300	340	kHz
Ramp Amplitude	ΔV_{OSC}		•		1.5		Vp-p
Reference							
Reference Voltage	V_{REF}	T_A = 0 to 70°C	•	788	800	812	mV
		FAN6520BI	•	780	800	820	mV
Error Amplifier							
DC Gain		Note 2			88		dB
Gain – Bandwidth Product	GBW	Note 2			15		MHz
Slew Rate	S/R	Note 2			8		V/µs
Gate Drivers							
HDRV pull-up resistance	R_{HUP}				2.5		Ω
HDRV pull-down resistance	R_{HDN}				2.0		Ω
LDRV pull-up resistance	R_{LUP}				2.5		Ω
LDRV pull-down resistance	R_{LDN}				1.0		Ω
Disable							
Disable Threshold	$V_{DISABLE}$	Note 3		400	800		mV

Notes:

1. All limits at operating temperature extremes are guaranteed by design, characterization and statistical quality control.
2. Specifications guaranteed by design/characterization (not production tested).
3. To ensure shutdown, COMP/SD pin should be held below 400mV while sinking 6mA of current.

Circuit Description

Initialization

The FAN6520B automatically initializes upon receipt of power. The Power-On Reset (POR) function continually monitors the bias voltage at the VCC pin. When the supply voltage exceeds its POR threshold, the IC initiates the soft-start operation.

Soft-Start

The POR function initiates the soft-start sequence. Soft-start clamps the error amplifier output (COMP pin) and reference input (noninverting terminal of the error amp) to the internally generated soft-start voltage. Figure 3 shows a typical start up interval where the COMP pin has been released from a grounded (system shutdown) state. The clamp on the error amplifier (COMP pin) initially controls the converter's output voltage during soft-start. The oscillator's triangular waveform is compared to the ramping error amplifier voltage. This generates SW pulses of increasing width that charge the output capacitor(s). When the internally generated soft-start voltage exceeds the feedback (FB pin) voltage, the output voltage is in regulation. This method provides a rapid and controlled output voltage rise. The entire startup sequence typically takes about 11ms.

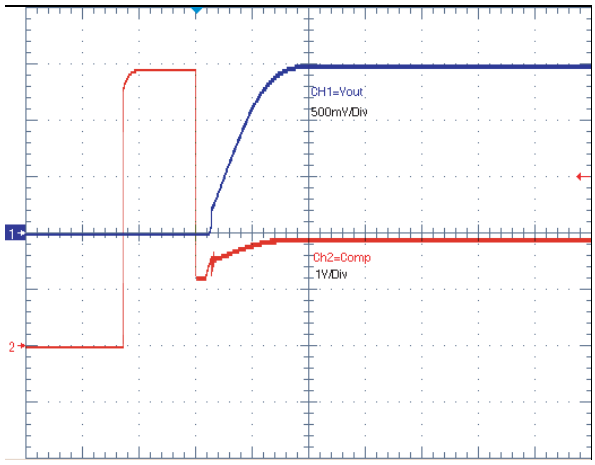


Figure 3. Soft-Start Interval

Adaptive Gate Drive

The FAN6520B incorporates a MOSFET shoot-through protection method which allows a converter to both sink and source current. Care should be exercised when designing a converter with the FAN6520B when it is known that the converter may sink current.

When the converter is sinking current, it is behaving as a boost converter that is regulating its input voltage. This means that the converter is boosting current into the VCC rail, which supplies the bias voltage to the FAN6520B. If this current has nowhere to go—such as to other distributed loads on the VCC rail, through a voltage limiting protection device, or other methods—the capacitance on the VCC bus will absorb the current. This situation will allow the voltage level of the VCC rail to increase. If the voltage level of the rail is boosted to a level that exceeds the maximum voltage rating of the FAN6520B, then the IC will experience an irreversible failure and the converter will no longer be operational. Ensure that there is a path for the current to follow other than the capacitance on the rail to prevent this failure mode.

Application Guidelines

Layout Considerations

As in any high frequency switching converter, layout is very important. Switching current from one power device to another can generate voltage transients across the impedances of the interconnecting bond wires and circuit traces. Use wide, short-printed circuit traces to minimize these interconnecting impedances. The critical components should be located as close together as possible, using ground plane construction or single point grounding.

Figure 4 shows the critical power components of the converter. To minimize the voltage overshoot, the interconnecting wires indicated by heavy lines should be part of a ground or power plane in a printed circuit board. The components shown in Figure 4 should be located as close together as possible. Please note that the capacitors C_{IN} and C_{OUT} may each represent numerous physical capacitors. Locate the FAN6520B as close as possible to Q1 and Q2 MOSFETs. The circuit traces for the MOSFETs' gate and source connections from the FAN6520B must be sized to handle up to 1A peak current.

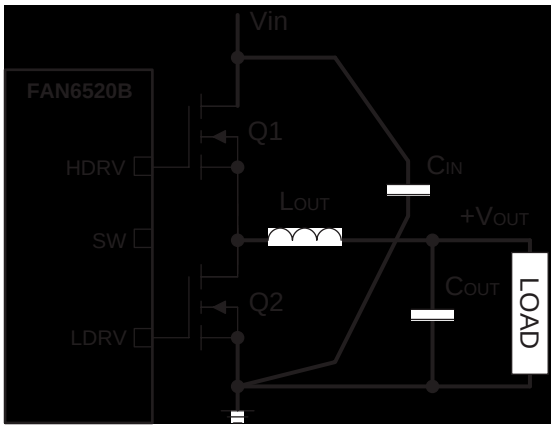


Figure 4. Printed Circuit Board Power and Ground Planes or Islands

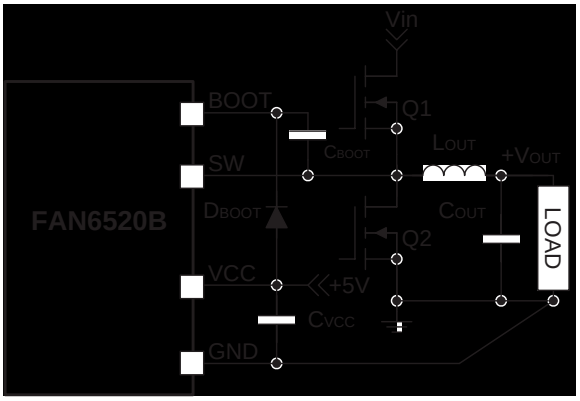


Figure 5. PC Board Small Signal Layout Guidelines

Figure 5 shows the circuit traces that require additional layout consideration. Use single point and ground plane construction for the circuits shown. Minimize any leakage current paths on the COMP pin and locate the resistor, R_{PULLUP} close to the COMP pin. Provide local VCC decoupling between VCC and GND pins. Locate the capacitor, CBOOT as close as practical to the BOOT and PHASE pins. All components used for feedback compensation should be located as close to the IC as practical.

Feedback Compensation

Figure 6 highlights the voltage-mode control loop for a synchronous-rectified buck converter. The output voltage (V_{OUT}) is regulated to the reference voltage level. The error amplifier (Error Amp) output ($V_{E/A}$) is compared with the oscillator (OSC) triangular wave to provide a pulse-width modulated (PWM) wave with an amplitude of V_{IN} at the SW node. The PWM wave is smoothed by the output LC filter (L_{OUT} and C_{OUT}).

The modulator transfer function is the small-signal transfer function of V_{OUT}/V_{COMP}. This function is dominated by a DC Gain and the output filter (L_{OUT} and C_{OUT}), with a double pole break frequency at F_{LC} and a zero at F_{ESR}. The DC Gain of the modulator is simply the input voltage (V_{IN}) divided by the peak-to-peak oscillator voltage ΔV_{OSC}.

The following equations define the modulator break frequencies as a function of the output LC filter:

$$F_{LC} = \frac{1}{2\pi\sqrt{L \cdot C}} \quad (15)$$

$$F_{ESR} = \frac{1}{2\pi \cdot ESR \cdot C} \quad (16)$$

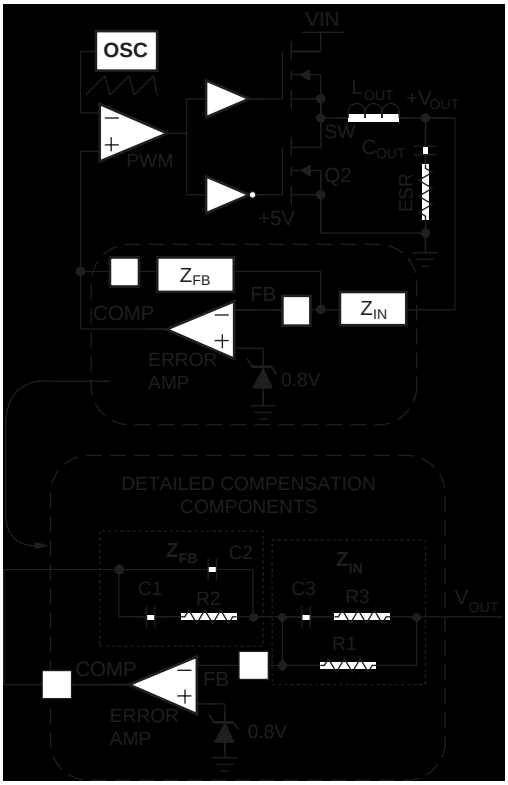


Figure 6. Voltage Mode Buck Converter Compensation Design

1. The compensation network consists of the error amplifier (internal to the FAN6520B) and the impedance networks Z_{IN} and Z_{FB}. The goal of the compensation network is to provide a closed loop transfer function with the highest 0dB crossing frequency (F_{0dB}) and adequate phase margin. Phase margin is the difference between the closed loop phase at F_{0dB} and 180 degrees. The equations below relate the compensation network's poles, zeros and gain to the components (R1, R2, R3, C1, C2, and C3) in Figure 6.

$$F_{Z1} = \frac{1}{2\pi R_2 C_1} \quad (17)$$

$$F_{P1} = \frac{1}{2\pi R_2\left(\frac{C_1 C_2}{C_1 + C_2}\right)} \quad (18)$$

$$F_{Z2} = \frac{1}{2\pi C_3(R_1 + R_3)} \quad (19)$$

$$F_{P2} = \frac{1}{2\pi R_3 C_3} \quad (20)$$

Use the following steps to locate the poles and zeros of the compensation network:

2. Pick gain (R2/R1) for the desired converter bandwidth.
3. Place 1st zero below the filter's double pole (~75% F_{LC}).
4. Place 2nd zero at filter's double pole.
5. Place 1st pole at the ESR zero.
6. Place 2nd pole at half the switching frequency.
7. Check gain against the error amplifier's open-loop gain.
8. Estimate phase margin. Repeat if necessary.

Figure 7 shows an asymptotic plot of the DC-DC converter's gain vs. frequency. The actual Modulator Gain has a high gain peak due to the high Q factor of the output filter and is not shown in Figure 7. Using the above guidelines should give a Compensation Gain similar to the curve plotted. The open loop error amplifier gain bounds the compensation gain. Check the compensation gain at FP2 with the capabilities of the error amplifier. The Closed Loop Gain is constructed on the graph of Figure 7 by adding the Modulator Gain (in dB) to the Compensation Gain (in dB). This is equivalent to multiplying the modulator transfer function by the compensation transfer function and plotting the gain.

The compensation gain uses external impedance networks Z_{FB} and Z_{IN} to provide a stable, high bandwidth (BW) overall loop. A stable control loop has a gain crossing with a –20dB/decade slope and a phase margin greater than 45°. Include worst case component variations when determining phase margin.

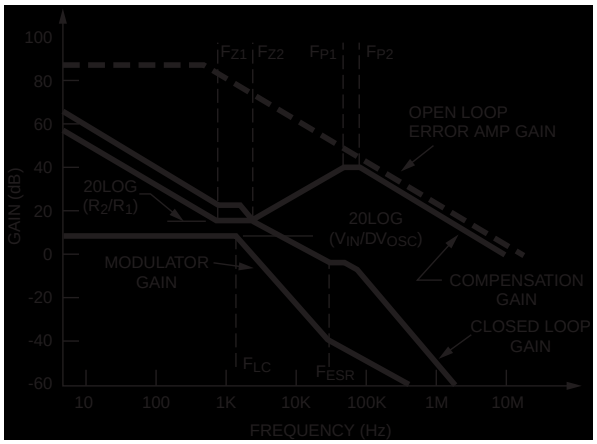


Figure 7. Asymptotic Bode Plot of Converter Gain

An output capacitor is required to filter the output and supply the load transient current. The filtering requirements are a function of the switching frequency and the ripple current. The load transient requirements are a function of the slew rate (di/dt) and the magnitude of the transient load current. These requirements are generally met with a mix of capacitors and careful layout.

Component Selection

Output Capacitors (C_{OUT})

Modern components and loads are capable of producing transient load rates above 1A/ns. High frequency capacitors initially supply the transient and slow the current load rate seen by the bulk capacitors. Effective Series Resistance (ESR) and voltage rating are typically the prime considerations for the bulk filter capacitors, rather than actual capacitance requirements. High-frequency decoupling capacitors should be placed as close to the power pins of the load as physically possible. Be careful not to add inductance in the circuit board wiring that could cancel the performance of these low inductance components. Consult with the load manufacturer on specific decoupling requirements. Use only specialized low-ESR capacitors intended for switching-regulator applications for the bulk capacitors. The bulk capacitor's ESR will determine the output ripple voltage and the initial voltage drop after a high slew-rate transient. An aluminum electrolytic capacitor's ESR value is related to the case size with lower ESR available in larger case sizes. However, the Equivalent Series Inductance (ESL) of these capacitors increases with case size and can reduce the usefulness of the capacitor to high slew-rate transient loading. Unfortunately, ESL is not a specified parameter. Work with your capacitor supplier and measure the capacitor's impedance with frequency to select a suitable component. In most cases, multiple electrolytic capacitors of small case size perform better than a single large case capacitor.

Output Inductor (L_{OUT})

The output inductor is selected to meet the output voltage ripple requirements and minimize the converter's response time to the load transient. The inductor value determines the converter's ripple current and the ripple voltage is a function of the ripple current. The ripple voltage (ΔV) and current (ΔI) are approximated by the following equations:

$$\Delta I = \frac{V_{IN} - V_{OUT}}{F_{SW} \cdot L} \qquad \Delta V \approx ESR \cdot \Delta I \qquad (1)$$

Increasing the inductance value reduces the ripple current and voltage. However, a large inductance value reduces the converter's ability to quickly respond to a load transient. One of the parameters limiting the converter's response to a load transient is the time required to change the inductor current. Given a sufficiently fast control loop design, the FAN6520B will provide either 0% or 100% duty cycle in response to a load transient. The response time is the time required to slew the inductor current from an initial current value to the transient current level. During this interval the difference between the inductor current and the transient current level must be supplied by the output capacitor. Minimizing the response time can minimize the output capacitance required.

Depending upon the whether there is a load application or a load removal, the response time to a load transient (I_{STEP}) is different. The following equations give the approximate response time interval for application and removal of a transient load:

$$T_{RISE} = \frac{L \cdot I_{STEP}}{V_{IN} - V_{OUT}}$$

$$T_{FALL} = \frac{L \cdot I_{STEP}}{V_{OUT}}$$

where T_{RISE} is the response time to the application of a positive I_{STEP}, and T_{FALL} is the response time to a load removal (negative I_{STEP}). The worst case response time can be either at the application or removal of load. Be sure to check both of these equations at the minimum and maximum output levels for the worst case response time.

Input Capacitor Selection

Use a mix of input bypass capacitors to control the voltage overshoot across the MOSFETs. Use small ceramic capacitors for high-frequency decoupling and bulk capacitors to supply the current needed each time Q1 turns on. Place the small ceramic capacitors physically close to the MOSFETs and between the drain of Q1 and the source of Q2. The important parameters for the bulk input capacitor are the voltage rating and the RMS current rating. For reliable operation, select the bulk capacitor with voltage and current ratings above the maximum input voltage and the largest RMS current required by the circuit. The capacitor voltage rating should be at least 1.25 times greater than the maximum input voltage and a voltage rating of 1.5 times is a conservative guideline.

The RMS current rating requirement (I_{RMS}) for the input capacitor of a buck regulator is:

$$I_{RMS} = I_L \sqrt{(D - D^2)} \quad (2)$$

where the converter duty cycle; $D = \frac{V_{OUT}}{V_{IN}}$. For a through-hole design, several electrolytic capacitors may be needed. For surface-mount designs, solid tantalum capacitors can be used, but caution must be exercised with regard to the capacitor's surge current rating. The capacitors must be capable of handling the surge current at power-up. Some capacitor series available from reputable manufacturers are surge current tested.

Bootstrap Circuit

The bootstrap circuit uses a charge storage capacitor (C_{BOOT}) and the internal diode, as shown in Figure 1. Selection of these components should be done after the high-side MOSFET has been chosen. The required capacitance is determined using the following equation:

$$C_{BOOT} = \frac{Q_G}{\Delta V_{BOOT}} \quad (3)$$

where Q_G is the total gate charge of the high-side MOSFET, and ΔV_{BOOT} is the voltage droop allowed on the high-side MOSFET drive. To prevent loss of gate drive, the bootstrap capacitance should be at least 50 times greater than the C_{ISS} of Q1. If FB is < 800mV for 32 consecutive cycles, then LDRV is turned on for ~1.6µs to charge the bootstrap capacitor.

Thermal Considerations

Total device dissipation:

$$P_D = P_Q + P_{HDRV} + P_{LDRV} \quad (4)$$

where P_Q represents quiescent power dissipation:

$$P_Q = V_{CC} \cdot 2.7mA \quad (5)$$

P_{HDRV} represents internal power dissipation of the upper FET driver.

$$P_{HDRV} = P_{H(R)} \cdot P_{H(F)} \quad (6)$$

Where $P_{H(R)}$ and $P_{H(F)}$ are internal dissipations for the rising and falling edges respectively:

$$P_{H(R)} = P_{Q1} \cdot \frac{R_{HUP}}{R_{HUP} + R_E + R_G} \quad (7)$$

$$P_{H(F)} = P_{Q1} \cdot \frac{R_{HDN}}{R_{HDN} + R_E + R_G} \quad (8)$$

where:

$$P_{Q1} = Q_{G1} \cdot V_{GS(Q1)} \cdot F_{SW} \quad (9)$$

Where Q_{G1} is total gate charge of Q1 for its applied V_{GS}.

As described in the equations above, the total power consumed in driving the gate is divided in proportion to the resistances in series with the MOSFET's internal gate node as shown in Figure 8.

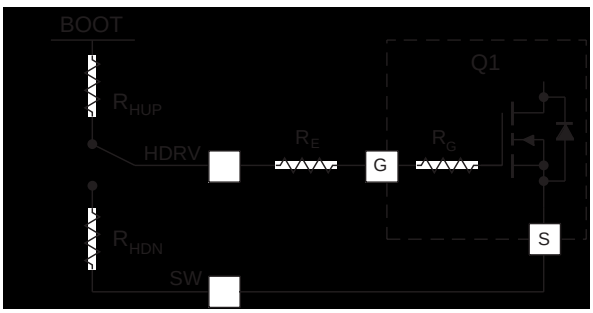


Figure 8. Driver Dissipation Model

R_G is the polysilicon gate resistance, internal to the FET. R_E is the external gate drive resistor implemented in many designs. Note that the introduction of R_E can reduce driver power dissipation, but excess R_E may cause errors in the "adaptive gate drive" circuitry. For more information please refer to Fairchild app note *AN-6003, "Shoot-through" in Synchronous Buck Converters.* (http://www.fairchildsemi.com/an/AN/AN-6003.pdf)

P_{LDRV} is dissipation of the lower FET driver.

$$P_{LDRV} = P_{L(R)} \cdot P_{L(F)} \quad (10)$$

Where $P_{H(R)}$ and $P_{H(F)}$ are internal dissipations for the rising and falling edges, respectively:

$$P_{L(R)} = P_{Q2} \cdot \frac{R_{LUP}}{R_{LUP} + R_E + R_G} \quad (11)$$

$$P_{L(F)} = P_{Q2} \cdot \frac{R_{LDN}}{R_{HDN} + R_E + R_G} \quad (12)$$

where:

$$P_{Q2} = Q_{G2} \cdot V_{GS(Q2)} \cdot F_{SW} \quad (13)$$

Power MOSFET Selection

For more information on MOSFET selection for synchronous buck regulators, refer to: *AN-6005: Synchronous Buck MOSFET Loss Calculations.*

This Fairchild app note is located at:
http://www.fairchildsemi.com/an/AN/AN-6005.pdf

Losses in a MOSFET are the sum of its switching (P_{SW}) and conduction (P_{COND}) losses.

In typical applications, the FAN6520B converter's output voltage is low with respect to its input voltage, therefore the lower MOSFET (Q2) is conducting the full load current for most of the cycle. Therefore choose a MOSFET for Q2 which has low $R_{DS(ON)}$ to minimize conduction losses.

In contrast, the high-side MOSFET (Q1) has a much shorter duty cycle, and its conduction loss will therefore have less of an impact. Q1, however, sees most of the switching losses, so Q1's primary selection criteria should be gate charge.

High-Side Losses

Figure 9 shows a MOSFET's switching interval, with the upper graph being the voltage and current on the Drain to Source and the lower graph detailing V_{GS} vs. time with a constant current charging the gate. The x-axis, therefore, is also representative of gate charge (Q_G) . C_{ISS} = C_{GD} + C_{GS}, and it controls t1, t2, and t4 timing. C_{GD} receives the current from the gate driver during t3 (as V_{DS} is falling). The gate charge (Q_G) parameters on the lower graph are either specified or can be derived from the MOSFET's datasheet.

Assuming switching losses are about the same for both the rising edge and falling edge, Q1's switching losses, occur during the shaded time when the MOSFET has voltage across it and current through it.

These losses are given by:

$$P_{UPPER} = P_{SW} + P_{COND}$$

$$P_{SW} = \left(\frac{V_{DS} \cdot I_L}{2} \cdot 2 \cdot t_s\right) F_{SW} \quad (14)$$

$$P_{COND} = \left(\frac{V_{OUT}}{V_{IN}}\right) \cdot I_{OUT}^2 \cdot R_{DS(ON)} \quad (15)$$

where:

P_{UPPER} is the upper MOSFET's total losses, and P_{SW} and P_{COND} are the switching and conduction losses for a given MOSFET. $R_{DS(ON)}$ is at the maximum junction temperature (T_J). t_S is the switching period (rise or fall time) and is t2+t3 (Figure 9).

The driver's impedance and C_{ISS} determine t2 while t3's period is controlled by the driver's impedance and Q_{GD}. Since most of t_S occurs when V_{GS} = V_{SP} we can use a constant current assumption for the driver to simplify the calculation of t_S:

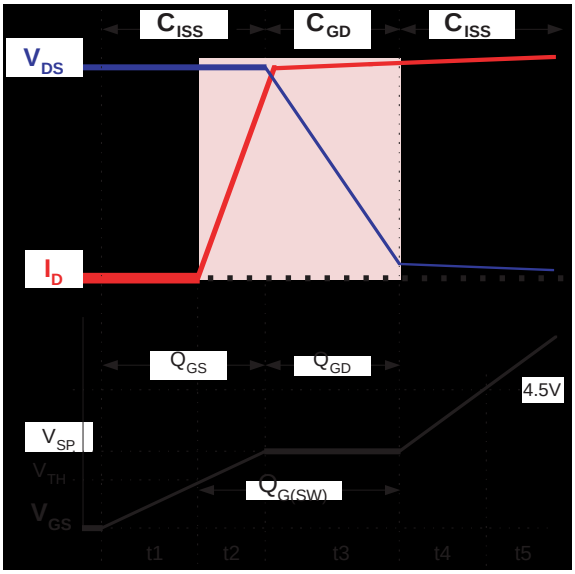


Figure 9. Switching Losses and Q_G

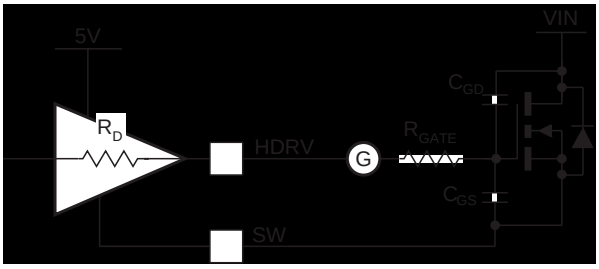


Figure 10. Drive Equivalent Circuit

$$t_s \approx \frac{Q_{G(SW)}}{I_{DRIVER}} \approx \frac{Q_{G(SW)}}{\left(\frac{VCC - V_{SP}}{R_{DRIVER} + R_{GATE}}\right)} \quad (16)$$

Most MOSFET vendors specify Q_{GD} and Q_{GS}. $Q_{G(SW)}$ can be determined as: $Q_{G(SW)} = Q_{GD} + Q_{GS} - Q_{TH}$ where Q_{TH} is the gate charge required to get the MOSFET to its threshold (V_{TH}). For the high-side MOSFET, $V_{DS} = V_{IN}$, which can be as high as 20V in a typical portable application. Care should also be taken to include the delivery of the MOSFET's gate power (P_{GATE}) in calculating the power dissipation required for the FAN6520B:

$$P_{GATE} = Q_G \cdot VCC \cdot F_{SW} \quad (17)$$

where Q_G is the total gate charge to reach VCC.

Low-Side Losses

Q2, however, switches on or off with its parallel shottky diode conducting, therefore $V_{DS} \approx 0.5V$. Since P_{SW} is proportional to V_{DS}, Q2's switching losses are negligible and we can select Q2 based on $R_{DS(ON)}$ only.

Conduction losses for Q2 are given by:

$$P_{COND} = (1\text{-}D) \cdot I_{OUT}^2 \cdot R_{DS(ON)} \quad (18)$$

where $R_{DS(ON)}$ is the $R_{DS(ON)}$ of the MOSFET at the highest operating junction temperature and

$D = \frac{V_{OUT}}{V_{IN}}$ is the minimum duty cycle for the converter.

Since $D_{MIN} < 20\%$ for portable computers, $(1\text{-}D) \approx 1$ produces a conservative result, further simplifying the calculation.

The maximum power dissipation ($P_{D(MAX)}$) is a function of the maximum allowable die temperature of the low-side MOSFET, the $\theta_{J\text{-}A}$, and the maximum allowable ambient temperature rise:

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_{A(MAX)}}{\theta_{J-A}} \quad (19)$$

$\theta_{J\text{-}A}$, depends primarily on the amount of PCB area that can be devoted to heat sinking (see Fairchild app note AN-1029 for SO-8 MOSFET thermal information).

Typical Application Circuit

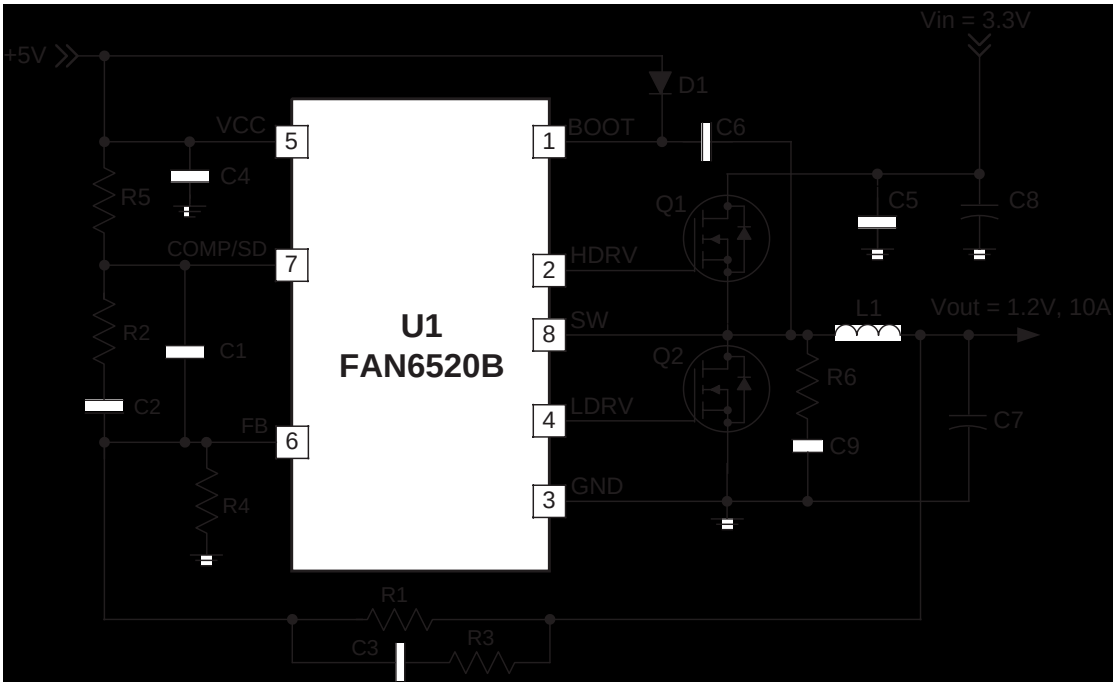


Figure 11. 3.3V to 1.2V, 10A DC-DC Converter

Typical Application Bill of Materials (1.2V, 10 Amps)

Ref Des	Description	Manufacturer	P/N	Qty
C1	Capacitor, 220pF, 10%, X7R, 0603	Any	–	1
C2, C3	Capacitor, 22nF, 10%, X7R, 0603	Any	–	2
C4	Capacitor, 1µF, 10%, X7R, 0805	Any	–	1
C5, C9	Capacitor, 3900pF, 10%, X7R, 0603	Any	–	2
C6	Capacitor, 0.1µF, 10%, X7R, 0603	Any	–	1
C7	Capacitor, 560µF, 4V, 7mΩ, 8X11, 5.58A	United Chemi-con	PSA4VB560MH11	1
C8	Capacitor, 390µF, 6.3V, 8mΩ, 8X11, 5.08A	United Chemi-con	PSA6.3VB390MH11	2
D1	Diode, 200mA, 100V	Fairchild	MMSD4148	1
L1	Inductor, 1.8µ, 16A, 3.2mΩ	Inter-Technical	SC5018-1R8M	1
Q1	Mosfet, N, 30V, 50A, 11.3mΩ, DPAK	Fairchild	FDD6296	1
Q2	Mosfet, N, 30V, 94A, 6.8mΩ, DPAK	Fairchild	FDD8896	1
R1	Resistor, 1.00KΩ, 1%, 0603	Any	–	1
R2	Resistor, 3.74KΩ, 1%, 0603	Any	–	1
R3	Resistor, 120Ω, 5%, 0603	Any	–	1
R4	Resistor, 2.00KΩ, 1%, 0603	Any	–	1
R5	Resistor, 10KΩ, 5%, 0603	Any	–	1
R6	Resistor, 1.5Ω, 5%, 0805	Any	–	1
U1	IC, Single Synchronous Buck PWM, SOIC 8	Fairchild	FAN6520B	1

Contact factory for the latest bill of materials.

Dimensional Outline Drawing