

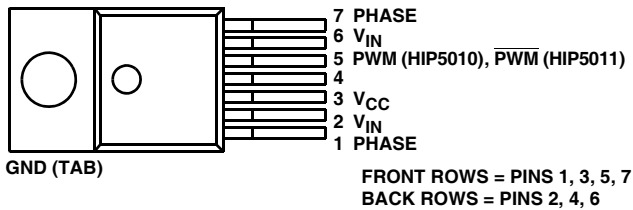
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**7V, 17A SynchroFET™ Complementary Drive Synchronous Half-Bridge**

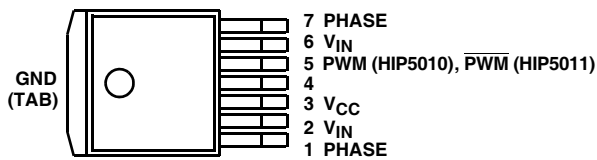
Designed with the P6 and Pentium® in mind, the Intersil SynchroFET™ family provides a new approach for implementing a synchronous rectified buck switching regulator. The SynchroFET replaces two power DMOSs, a Schottky diode, two gate drivers and synchronous control circuitry. The complementary drive circuit turns the upper FET on and the lower FET off when the input from the PWM is high. When the input from the PWM goes low the upper FET turns off and the lower FET turns on. The HIP5011 has a PWM pin that inverts the relationship from the input to PHASE. This architecture allows the designer to utilize a low cost single-ended PWM controller in either a current or voltage mode configuration. The SynchroFET operates in continuous conduction mode reducing EMI constraints and enabling high bandwidth operation. Several features ensure easy start-up. First, the supply currents stay below specification as the supply voltages ramp up; no unexpected surges occur that might perturb a soft-start or deplete a charge-pump. Second, any power-up sequence of the V<sub>CC</sub>, V<sub>IN</sub>, or PWM pins can be used without causing large currents. Third, the chip operates when V<sub>CC</sub> is greater than 2V so V<sub>CC</sub> can be created from a charge pump powered from V<sub>IN</sub>.

**Pinouts**

**HIP5010IS1, HIP5011IS1 (SIP - VERTICAL)  
TOP VIEW**



**HIP5010IS, HIP5011IS (SIP - GULLWING)  
TOP VIEW**



**Features**

- Complementary Drive, Half-Bridge Power NMOS
- Use With Low-Cost Single-Output PWM Controllers
- Improve Efficiency Over Conventional Buck Converter with Schottky Clamp
- Minimum Deadtime Provided by Adaptive Shoot-Through Protection Eliminates External Schottky
- Grounded Case for Low EMI and Simple Heatsinking
- Low Operating Current
- Frequency Exceeding 1MHz
- Dual Polarity Input Options
- All Pins Surge Protected

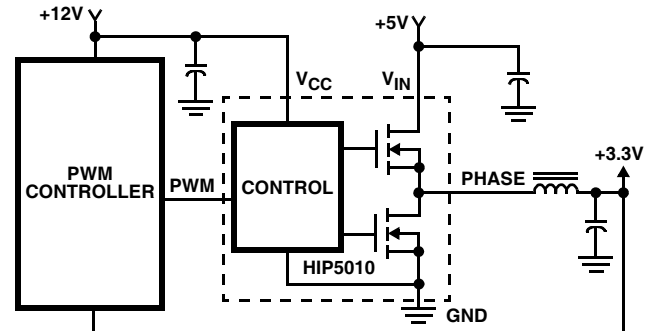
**Applications**

- 5V to ≤3.3V Synchronous Buck Converters
- Pentium and P6 Power Supplies
- PowerPC™ Power Supplies
- Bus Terminations (BTL and GTL)
- Drive 5V Motors Directly from Microprocessor

**Ordering Information**

PART NUMBER	TEMP. RANGE (°C)	PACKAGE	PKG. NO.
HIP5010IS	-40 to 85	7 Ld Gullwing SIP	Z7.05B
HIP5010IS1	-40 to 85	7 Ld Staggered Vertical SIP	Z7.05C
HIP5011IS	-40 to 85	7 Ld Gullwing SIP	Z7.05B
HIP5011IS1	-40 to 85	7 Ld Staggered Vertical SIP	Z7.05C

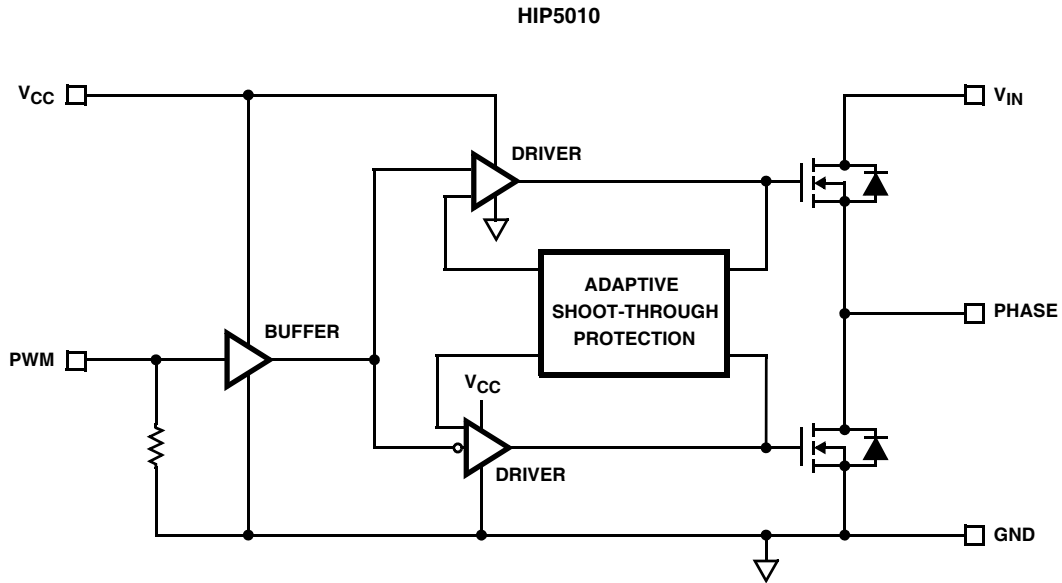
**Typical Application Block Diagram**



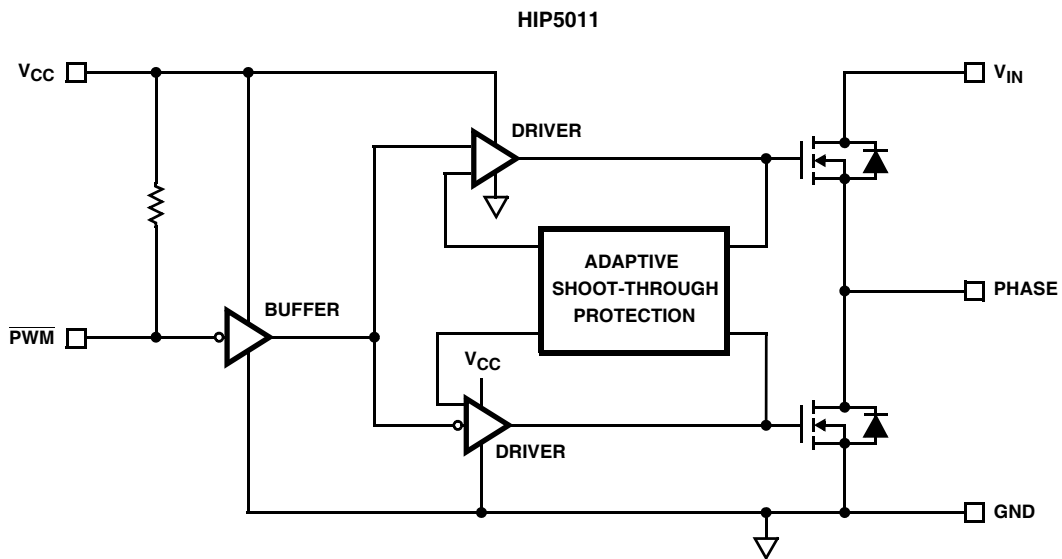
**SYNCHRONOUS RECTIFIED BUCK CONVERTER**

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PowerPC™ is a trademark of International Business Machines.  
SynchroFET™ is a trademark of Intersil Corporation.

**Non-Inverting SynchroFET Block Diagram**



**Inverting SynchroFET Block Diagram**



# HIP5010, HIP5011

## Absolute Maximum Ratings

Supply Voltage, $V_{CC}$ . . . . .	+16V
Input Voltage $V_{IN}$ . . . . .	+7V
$I_{PHASE}$ , $I_{VIN}$ , $I_{GND}$ ( $T_J = 25^\circ\text{C}$ ) . . . . .	17A (Repetitive Peak)
$I_{PHASE}$ , $I_{VIN}$ , $I_{GND}$ ( $T_J = 150^\circ\text{C}$ ) . . . . .	15A (Repetitive Peak)
PWM Input . . . . .	-4V to +16V
ESD Classification . . . . .	Class 3 (4kV)
Lead Temperature (Soldering 10s) (Lead Tips Only) . . . . .	300°C
Storage Temperature Range . . . . .	-65°C to 150°C
Junction Temperature Range . . . . .	-40°C to 150°C

## Operating Conditions

Supply Voltage, $V_{CC}$ . . . . .	+12V, $\pm 20\%$
Input Voltage $V_{IN}$ . . . . .	0V to 5.5V
Supply Voltage, $V_{CC}$ , minimum for charge-pumped start-up . . . . .	+4.0V

## Thermal Information (Typical)

Package	$\theta_{JC}^{\dagger\dagger}$ (°C/W)	$\theta_{JA}$ (°C/W) <sup>†</sup>				3 <sup>†††</sup>
		0	1	2	3	
SOIC (IB) . . . . .	26	63	45	42	41	35
SIP (IS) . . . . .	2	55	30	25	24	18
SIP (IS1) . . . . .	2	-	-	-	-	-

† Versus additional square inches of 1 ounce copper on the printed circuit board.

††  $\theta_{JC}$  is measured to pin 12 for the SOIC. Printed circuit board had 1 square inch of copper. For SIP Packages value shown is typical with an infinite heat sink.

††† 200 linear feet per minute of air flow.

$I_{PHASE}$  - SIPs: 11.5A(RMS), 11.2A(DC); SOIC: 7.4A(RMS), 7.4A(DC)  
 $I_{VIN}$  . . . SIPs: 10.0A(RMS), 8.5A(DC); SOIC: 6.4A(RMS), 6.4A(DC)  
 $I_{GND}$  . . . SIPs: 8.5A(RMS), 6.0A(DC); SOIC: 5.4A(RMS), 5.4A(DC)

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the recommended operating conditions of this specification is not implied.

## Electrical Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = 25^\circ\text{C}$			$T_J = -40^\circ\text{C}$ $T_J = 150^\circ\text{C}$		UNITS
			MIN	TYP	MAX	MIN	MAX	
$r_{DS(ON)}$ Upper MOSFET	$R_{DSU}$	$V_{CC} = 12\text{V}$ , $V_{IN} = 5\text{V}$	-	34	39	-	65	mΩ
$r_{DS(ON)}$ Lower MOSFET	$R_{DSL}$	$V_{CC} = 12\text{V}$ , $V_{IN} = 5\text{V}$	-	36	42	-	68	mΩ
$V_{IN}$ Operating Current	$I_{VINO}$	$V_{IN} = 5\text{V}$ , No Load, 500kHz	-	5	8	-	10	mA
$V_{IN}$ Quiescent Current	$I_{VIN}$	PWM or $\overline{\text{PWM}} = V_{CC}$ or GND	-	0.1	10	-	100	μA
$V_{CC}$ Operating Current	$I_{CCO}$	$V_{CC} = 12\text{V}$ , 500kHz	-	8	12	-	15	mA
$V_{CC}$ Quiescent Current (HIP5010)	$I_{CCIH}$	PWM = $V_{CC}$	-	80	-	-	400	μA
$V_{CC}$ Quiescent Current (HIP5010)	$I_{CCIL}$	PWM = GND	-	0.1	10	-	100	μA
$V_{CC}$ Quiescent Current (HIP5011)	$I_{CCNIH}$	$\overline{\text{PWM}} = V_{CC}$	-	0.1	10	-	100	μA
$V_{CC}$ Quiescent Current (HIP5011)	$I_{CCNIL}$	$\overline{\text{PWM}} = \text{GND}$	-	140	-	-	400	μA
Low Level PWM Input Voltage	$V_{IL}$		-	1.8	-	1	-	V
High Level PWM Input Voltage	$V_{IH}$		-	2.1	-	-	3	V
PWM Input Voltage Hysteresis	$V_{IHYS}$		-	0.3	-	-	-	V
Input Pulldown Resistance (HIP5010)	$R_{PWM}$		-	220	-	100	400	kΩ
Input Pullup Resistance (HIP5011)	$R_{PWM}$		-	220	-	100	400	kΩ

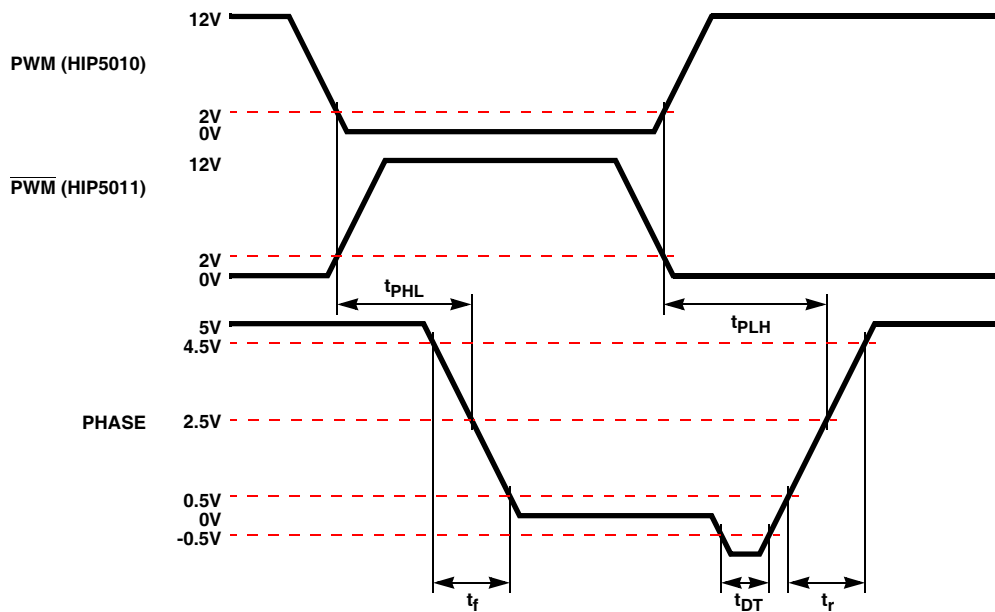
## Switching Specifications

PARAMETERS	SYMBOL	TEST CONDITIONS	$T_J = 25^\circ\text{C}$			$T_J = -40^\circ\text{C}$ $T_J = 150^\circ\text{C}$		UNITS
			MIN	TYP	MAX	MIN	MAX	
Upper Device Turn-Off Delay	$t_{PHL}$	$V_{CC} = 12\text{V}$ , $I_{PHASE} = -1\text{A}$	-	30	50	-	80	ns
Lower Device Turn-Off Delay	$t_{PLH}$	$V_{CC} = 12\text{V}$ , $I_{PHASE} = +1\text{A}$	-	30	50	-	80	ns
Dead Time	$t_{DT}$	$V_{CC} = +12\text{V}$ , $I_{PHASE} = -1\text{A}$	-	10	-	-	-	ns
Phase Rise-Time	$t_r$	$V_{CC} = 12\text{V}$ , $I_{PHASE} = -1\text{A}$	-	20	-	-	-	ns
Phase Fall-Time	$t_f$	$V_{CC} = 12\text{V}$ , $I_{PHASE} = +1\text{A}$	-	20	-	-	-	ns

**Pin Descriptions**

SYMBOL	DESCRIPTION
V <sub>CC</sub>	Positive supply to control logic and gate drivers. De-couple this pin to GND.
V <sub>IN</sub>	FET Switch Input Voltage. De-couple this pin to GND. Tie all V <sub>IN</sub> terminals together.
PHASE	Output. Tie all phase terminals together.
PWM (HIP5010) PWM (HIP5011)	Single Ended Control Input. This input connects to the PWM controller output.
GND	System Ground.

**Timing Diagram**



NOTE: I<sub>PHASE</sub> = +1A for t<sub>PLH</sub> and t<sub>f</sub>, I<sub>PHASE</sub> = -1A for t<sub>PHL</sub>, t<sub>DT</sub>, and t<sub>r</sub>.

FIGURE 1.

Typical Performance Curves

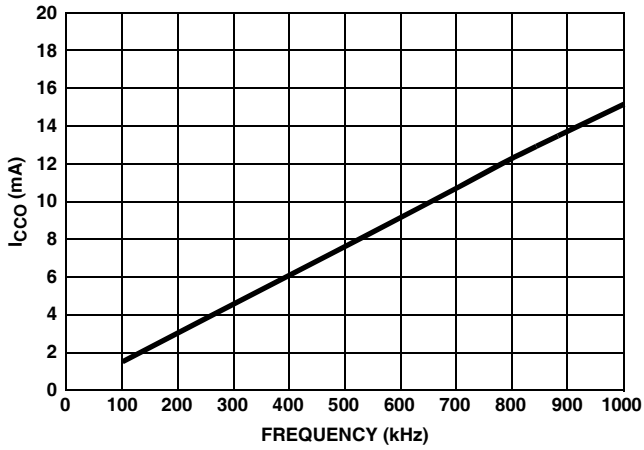


FIGURE 2. I<sub>CCO</sub> vs FREQUENCY

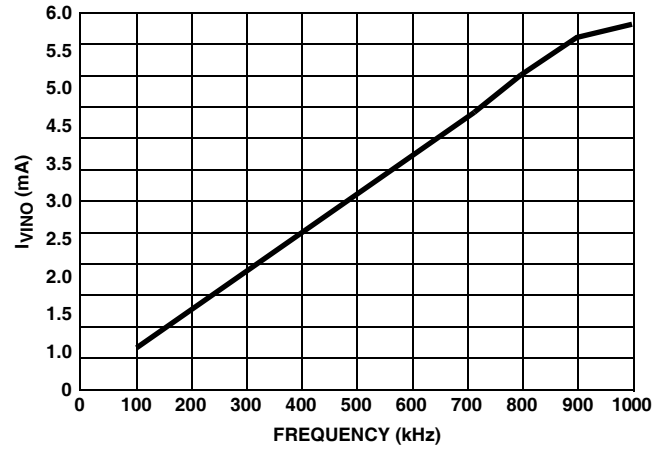


FIGURE 3. I<sub>VINO</sub> vs FREQUENCY

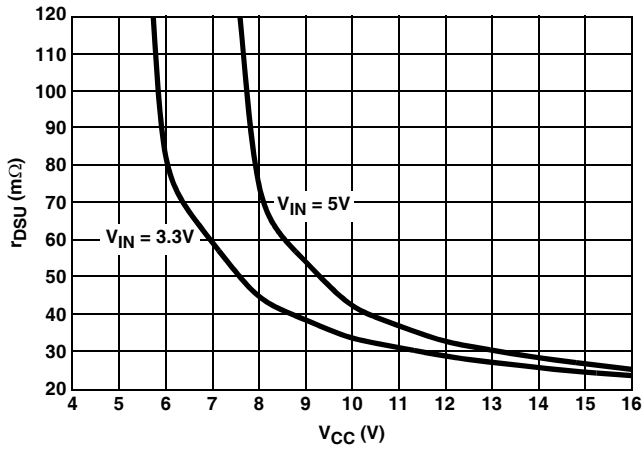


FIGURE 4. R<sub>DSU</sub> vs V<sub>Cc</sub>

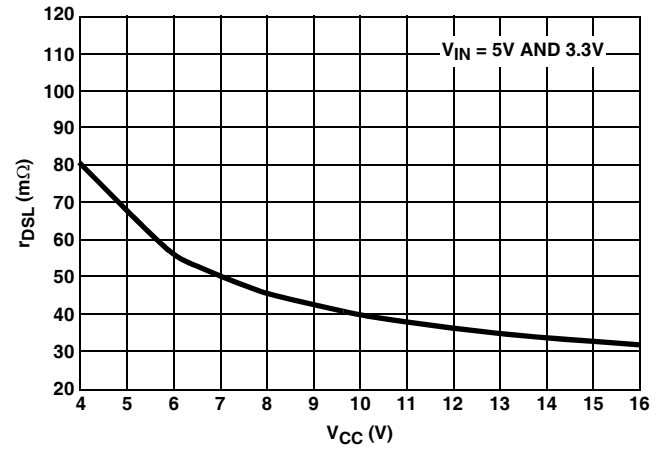


FIGURE 5. R<sub>DSL</sub> vs V<sub>Cc</sub>

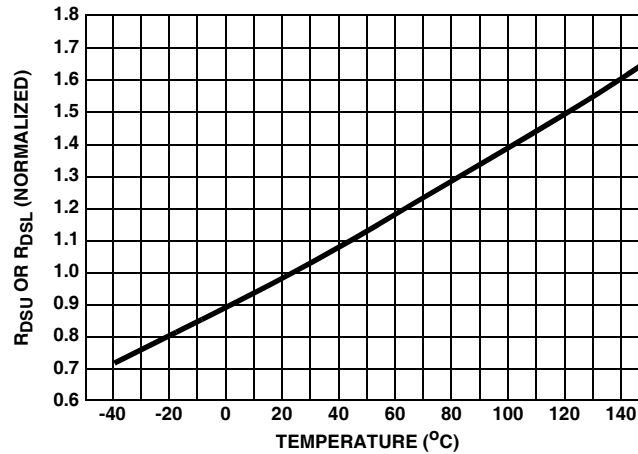
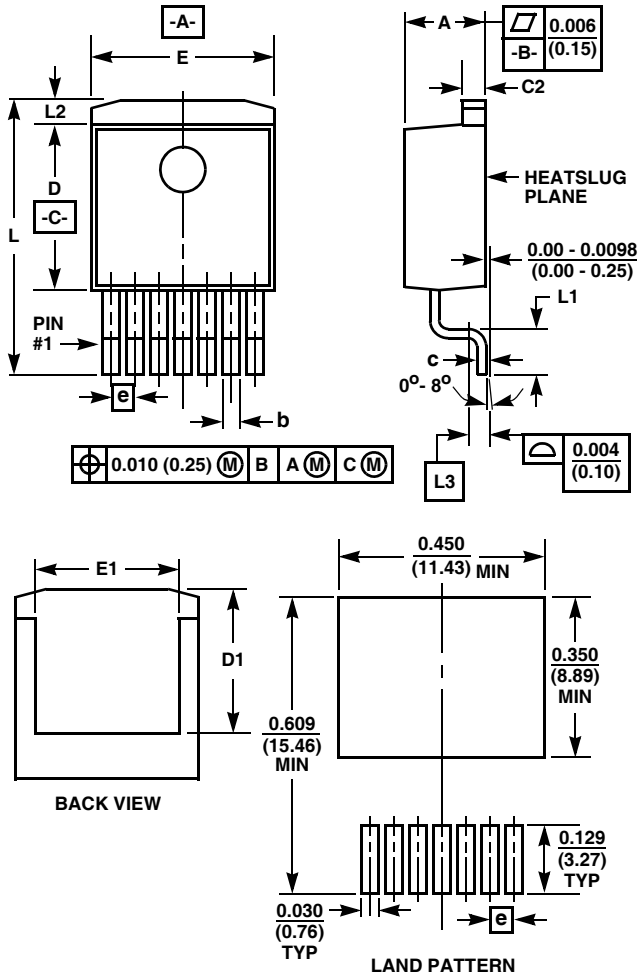


FIGURE 6. R<sub>DSU</sub> OR R<sub>DSL</sub> vs TEMPERATURE

Single-In-Line Plastic Packages (SIP)



Z7.05B

7 LEAD PLASTIC SINGLE-IN-LINE PACKAGE SURFACE MOUNT "GULLWING" LEAD FORM

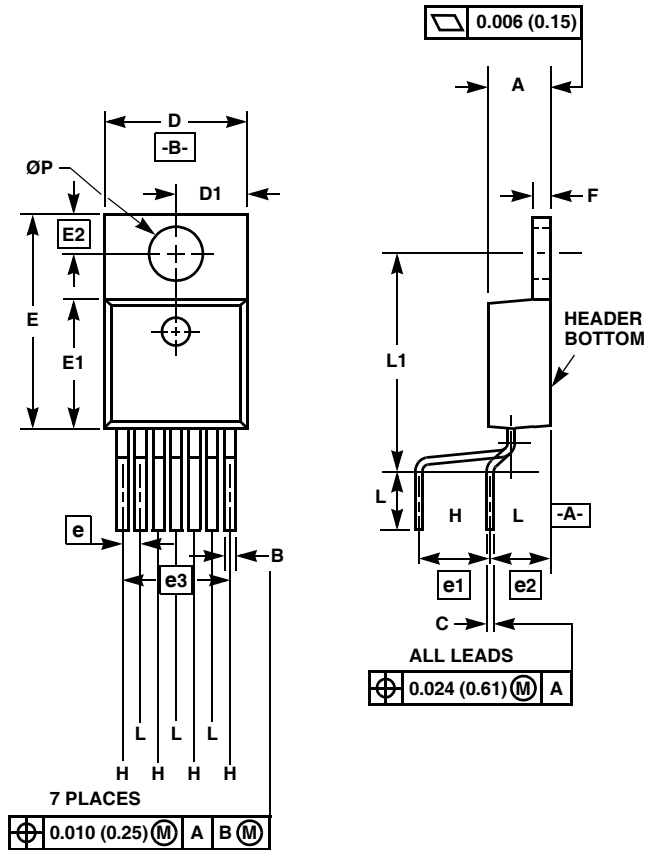
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
C2	0.048	0.055	1.22	1.39	5
D	0.350	0.370	8.89	9.39	-
E	0.395	0.405	10.04	10.28	-
D1	0.310	-	7.88	-	-
E1	0.310	-	7.88	-	-
L	0.549	0.569	13.95	14.45	-
L1	0.068	0.088	1.72	2.24	-
L2	0.045	0.055	1.15	1.40	-
L3	0.030 BSC		0.76 BSC		4
b	0.028	0.034	0.71	0.86	5, 6, 7
c	0.018	0.024	0.46	0.60	5
e	0.050 BSC		1.27 BSC		-

Rev. 2 12/95

NOTES:

1. These package dimensions are within allowable dimensions of JEDEC MO-169AC, Issue A.
2. Controlling dimension: Inch.
3. Dimensioning and tolerance per ANSI Y14.5M-1982.
4. Gauge plane L3 is parallel to heatslug plane.
5. Dimensions include lead finish.
6. Leads are not allowed above the datum -B-.
7. Dimension "b" does not include dambar protrusion. Allowable dambar protrusion shall not cause the lead width to exceed the maximum "b" by more than 0.003" (0.08mm).

Single-In-Line Plastic Packages (SIP)



Z7.05C

7 LEAD PLASTIC SINGLE-IN-LINE PACKAGE STAGGERED VERTICAL LEAD FORM

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.170	0.180	4.32	4.57	-
B	0.028	0.034	0.71	0.86	3, 4
C	0.018	0.024	0.46	0.60	3
D	0.395	0.405	10.04	10.28	-
D1	0.198	0.202	5.03	5.13	-
E	0.595	0.605	15.11	15.37	-
E1	0.350	0.370	8.89	9.39	-
E2	0.110 BSC		2.79 BSC		
e	0.050 BSC		1.27 BSC		-
e1	0.200 BSC		5.08 BSC		-
e2	0.169 BSC		4.29 BSC		-
e3	0.300 BSC		7.62 BSC		-
F	0.048	0.055	1.22	1.39	3
L	0.150	0.176	3.81	4.47	-
L1	0.600	0.620	15.24	15.74	-
ØP	0.147	0.152	3.73	3.86	3

Rev. 1 4/98

NOTES:

1. Controlling dimension: INCH.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimensions include lead finish.
4. Dimension "B" does not include dambar protrusion. Allowable dambar protrusion shall not cause lead width to exceed maximum "B" by more than 0.003 inches (0.08mm).

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