Quad Digitally-Controlled (XDCP™) Potentiometer

The X9251 integrates four digitally controlled potentiometers (XDCP) on a monolithic CMOS integrated circuit.

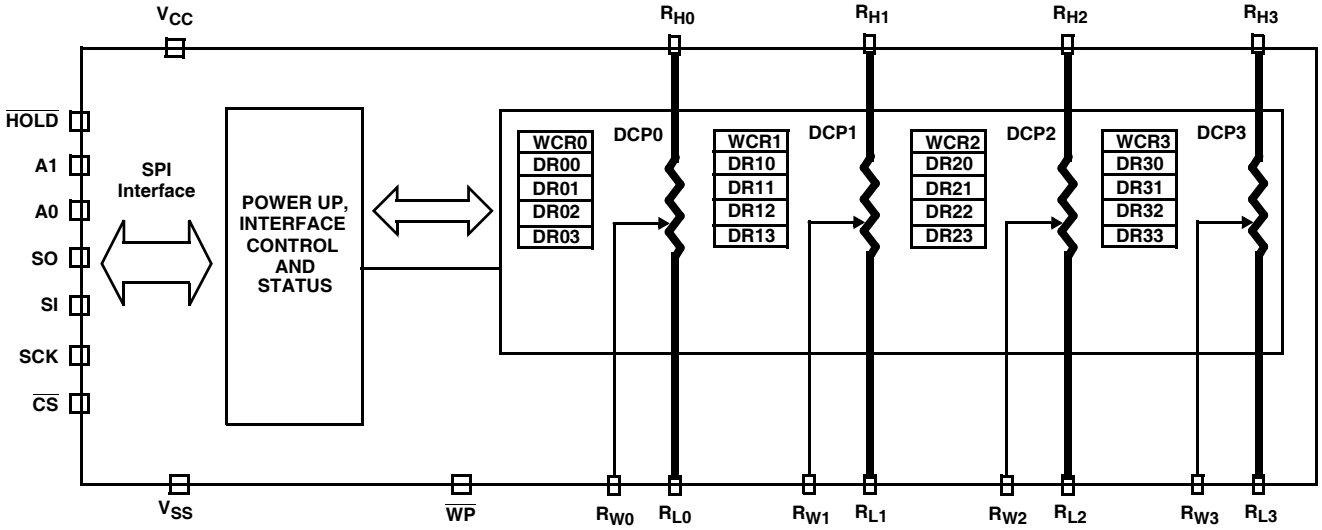
The digitally controlled potentiometers are imple-mented with a combination of resistor elements and CMOS switches. The position of the wipers are controlled by the user through the SPI bus interface. Each potentiometer has associated with it a volatile Wiper Counter Register (WCR) and four non-volatile Data Registers that can be directly written to and read by the user. The content of the WCR controls the position of the wiper. At power-up, the device recalls the content of the default Data Registers of each DCP (DR00, DR10, DR20, and DR30) to the corresponding WCR.

The XDCP can be used as a three-terminal potentiometer or as a two terminal variable resistor in a wide variety of applications including control, parameter adjustments, and signal processing.

Features

- Four potentiometers in one package
- 256 resistor taps–0.4% resolution
- SPI Serial Interface for write, read, and transfer operations of the potentiometer
- Wiper resistance: 100Ω typical @ V_{CC} = 5V
- 4 Non-volatile data registers for each potentiometer
- Non-volatile storage of multiple wiper positions
- Standby current <5µA max
- V_{CC}: 2.7V to 5.5V Operation
- 50kΩ, 100kΩ versions of total resistance
- 100 year data retention
- Single supply version of X9250
- Endurance: 100,000 data changes per bit per register
- 24 Ld SOIC, 24 Ld TSSOP
- Low power CMOS
- Pb-free plus anneal available (RoHS compliant)

Functional Diagram



Ordering Information

PART NUMBER	PART MARKING	V_{CC} LIMITS (V)	POTENTIOMENTER ORGANIZATION (kΩ)	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
X9251US24	X9251US	5 ±10%	50	0 to +70	24 Ld SOIC (300 mil)	M24.3
X9251US24Z (Note)	X9251US Z			0 to +70	24 Ld SOIC (300 mil) (Pb-free)	M24.3
X9251UV24	X9251UV			0 to +70	24 Ld TSSOP (4.4mm)	MDP0044
X9251UV24Z (Note)	X9251UV Z			0 to +70	24 Ld TSSOP (4.4mm) (Pb-free)	MDP0044
X9251TS24	X9251TS		100	0 to +70	24 Ld SOIC (300 mil)	M24.3
X9251TS24Z (Note)	X9251TS Z			0 to +70	24 Ld SOIC (300 mil) (Pb-free)	M24.3
X9251TS24I	X9251TS I			-40 to +85	24 Ld SOIC (300 mil)	M24.3
X9251TS24IZ (Note)	X9251TS ZI			-40 to +85	24 Ld SOIC (300 mil) (Pb-free)	M24.3
X9251TV24I	X9251TV I			-40 to +85	24 Ld TSSOP (4.4mm)	MDP0044
X9251TV24IZ (Note)	X9251TV ZI			-40 to +85	24 Ld TSSOP (4.4mm) (Pb-free)	MDP0044
X9251US24I-2.7	X9251US G	2.7 to 5.5	50	-40 to +85	24 Ld SOIC (300 mil)	M24.3
X9251US24IZ-2.7 (Note)	X9251US ZG			-40 to +85	24 Ld SOIC (300 mil) (Pb-free)	M24.3
X9251UV24-2.7	X9251UV F			0 to +70	24 Ld TSSOP (4.4mm)	MDP0044
X9251UV24Z-2.7 (Note)	X9251UV ZF			0 to +70	24 Ld TSSOP (4.4mm) (Pb-free)	MDP0044
X9251UV24I-2.7	X9251UV G			-40 to +85	24 Ld TSSOP (4.4mm)	MDP0044
X9251UV24IZ-2.7 (Note)	X9251UV ZG			-40 to +85	24 Ld TSSOP (4.4mm) (Pb-free)	MDP0044
X9251TS24-2.7	X9251TS F		100	0 to +70	24 Ld SOIC (300 mil)	M24.3
X9251TS24Z-2.7 (Note)	X9251TS ZF			0 to +70	24 Ld SOIC (300 mil) (Pb-free)	M24.3
X9251TV24-2.7	X9251TV F			0 to +70	24 Ld TSSOP (4.4mm)	MDP0044
X9251TV24Z-2.7 (Note)	X9251TV ZF			0 to +70	24 Ld TSSOP (4.4mm) (Pb-free)	MDP0044
X9251TV24I-2.7	X9251TV G			-40 to +85	24 Ld TSSOP (4.4mm)	MDP0044
X9251TV24IZ-2.7 (Note)	X9251TV ZG			-40 to +85	24 Ld TSSOP (4.4mm) (Pb-free)	MDP0044

*Add "T1" suffix for tape and reel.

NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

Circuit Level Applications

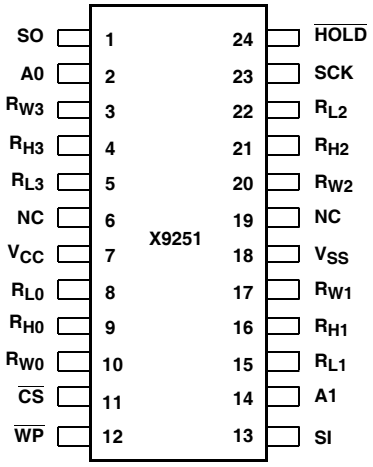
- Vary the gain of a voltage amplifier
- Provide programmable dc reference voltages for comparators and detectors
- Control the volume in audio circuits
- Trim out the offset voltage error in a voltage amplifier circuit
- Set the output voltage of a voltage regulator
- Trim the resistance in Wheatstone bridge circuits
- Control the gain, characteristic frequency and Q-factor in filter circuits
- Set the scale factor and zero point in sensor signal conditioning circuits
- Vary the frequency and duty cycle of timer ICs
- Vary the dc biasing of a pin diode attenuator in RF circuits
- Provide a control variable (I, V, or R) in feedback circuits

System Level Applications

- Adjust the contrast in LCD displays
- Control the power level of LED transmitters in communication systems
- Set and regulate the DC biasing point in an RF power amplifier in wireless systems
- Control the gain in audio and home entertainment systems
- Provide the variable DC bias for tuners in RF wireless systems
- Set the operating points in temperature control systems
- Control the operating point for sensors in industrial systems
- Trim offset and gain errors in artificial intelligent systems

Pinout

X9251
(24 LD SOIC/TSSOP)
TOP VIEW



Pin Assignments

PIN (SOIC)	SYMBOL	FUNCTION
1	SO	Serial Data Output for SPI bus
2	A0	Device Address for SPI bus. (See Note 1)
3	R_{W3}	Wiper Terminal of DCP3
4	R_{H3}	High Terminal of DCP3
5	R_{L3}	Low Terminal of DCP3
7	V_{CC}	System Supply Voltage
8	R_{L0}	Low Terminal of DCP0
9	R_{H0}	High Terminal of DCP0
10	R_{W0}	Wiper Terminal of DCP0
11	$\overline{CS}$	SPI bus. Chip Select active low input
12	$\overline{WP}$	Hardware Write Protect - active low
13	SI	Serial Data Input for SPI bus
14	A1	Device Address for SPI bus. (See Note 1)
15	R_{L1}	Low Terminal of DCP1
16	R_{H1}	High Terminal of DCP1
17	R_{W1}	Wiper Terminal of DCP1
18	V_{SS}	System Ground
20	R_{W2}	Wiper Terminal of DCP2
21	R_{H2}	High Terminal of DCP2
22	R_{L2}	Low Terminal of DCP2
23	SCK	Serial Clock for SPI bus
24	$\overline{HOLD}$	Device select. Pauses the SPI serial bus.
6, 19	NC	No Connect

NOTE:

1. A0 and A1 device address pins must be tied to a logic level.

Pin Descriptions

Bus Interface Pins

SERIAL OUTPUT (SO)

SO is a serial data output pin. During a read cycle, data is shifted out on this pin. Data is clocked out by the falling edge of the serial clock.

SERIAL INPUT (SI)

SI is the serial data input pin. All opcodes, byte addresses and data to be written to the device registers are input on this pin. Data is latched by the rising edge of the serial clock.

SERIAL CLOCK (SCK)

The SCK input is used to clock data into and out of the X9251.

HOLD ($\overline{HOLD}$)

$\overline{HOLD}$ is used in conjunction with the $\overline{CS}$ pin to select the device. Once the part is selected and a serial sequence is underway, $\overline{HOLD}$ may be used to pause the serial communication with the controller without resetting the serial sequence. To pause, $\overline{HOLD}$ must be brought LOW while SCK is LOW. To resume communication, $\overline{HOLD}$ is brought HIGH, again while SCK is LOW. If the pause feature is not used, $\overline{HOLD}$ should be held HIGH at all times.

DEVICE ADDRESS (A1 AND A0)

The address inputs are used to set the two least significant bits of the slave address. A match in the slave address serial data stream must be made with the address input in order to initiate communication with the X9251. Device pins A1 and A0 must be tied to a logic level which specifies the internal address of the device, see Figures 2, 3, 4, 5 and 6.

CHIP SELECT ($\overline{CS}$)

When $\overline{CS}$ is HIGH, the X9251 is deselected and the SO pin is at high impedance, and (unless an internal write cycle is underway) the device is in the standby state. $\overline{CS}$ LOW enables the X9251, placing it in the active power mode. It should be noted that after a power-up, a HIGH to LOW transition on $\overline{CS}$ is required prior to the start of any operation.

Potentiometer Pins

R_H, R_L

The R_H and R_L pins are equivalent to the terminal connections on a mechanical potentiometer. Since there are 4 potentiometers, there are 4 sets of R_H and R_L such that R_{H0} and R_{L0} are the terminals of DCP0 and so on.

R_W

The wiper pin are equivalent to the wiper terminal of a mechanical potentiometer. Since there are 4 potentiometers, there are 4 sets of R_W such that R_{W0} is the terminals of DCP0 and so on.

Supply Pins

SYSTEM SUPPLY VOLTAGE (V_{CC}) AND SUPPLY GROUND (V_{SS})

The V_{CC} pin is the system supply voltage. The V_{SS} pin is the system ground.

Other Pins

NO CONNECT

No connect pins should be left floating. This pins are used for Intersil manufacturing and testing purposes.

HARDWARE WRITE PROTECT INPUT ($\overline{WP}$)

The $\overline{WP}$ pin when LOW prevents non-volatile writes to the Data Registers.

Principles of Operation

The X9251 is an integrated circuit incorporating four DCPs and their associated registers and counters, and a serial interface providing direct communication between a host and the potentiometers.

DCP Description

Each DCP is implemented with a combination of resistor elements and CMOS switches. The physical ends of each DCP are equivalent to the fixed terminals of a mechanical potentiometer (R_H and R_L pins). The RW pin is an intermediate node, equivalent to the wiper terminal of a mechanical potentiometer.

The position of the wiper terminal within the DCP is controlled by an 8-bit volatile Wiper Counter Register (WCR).

One of Four Potentiometers

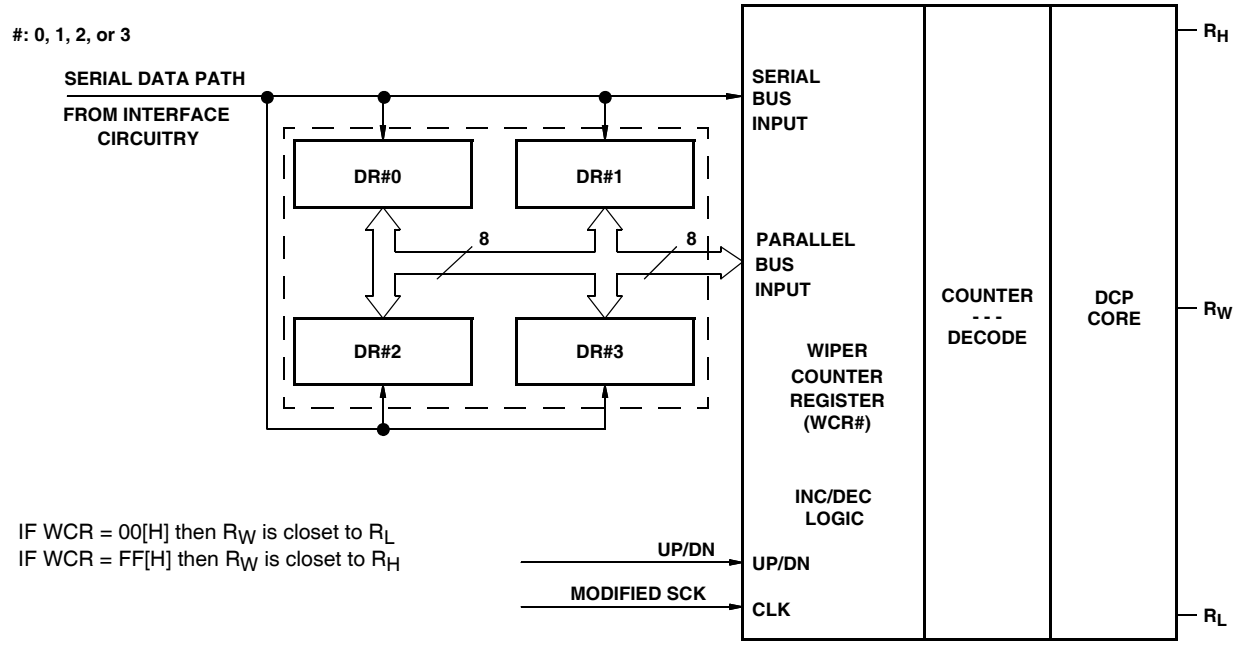


FIGURE 1. DETAILED POTENTIOMETER BLOCK DIAGRAM

Power Up and Down Recommendations

There are no restrictions on the power-up or power-down conditions of V_{CC} and the voltages applied to the potentiometer pins provided that V_{CC} is always more positive than or equal to V_H, V_L, and V_W (i.e., $V_{CC} \geq V_H$, V_L, V_W). The V_{CC} ramp rate specification is always in effect.

Wiper Counter Register (WCR)

The X9251 contains four Wiper Counter Registers, one for each potentiometer. The Wiper Counter Register can be envisioned as a 8-bit parallel and serial load counter with its outputs decoded to select one of 256 wiper positions along its resistor array. The contents of the WCR can be altered in four ways: it may be written directly by the host via the Write Wiper Counter Register instruction (serial load); it may be written indirectly by transferring the contents of one of four associated data registers via the XFR Data Register instruction (parallel load); it can be modified one step at a time by the Increment/Decrement instruction (See Instruction section for more details). Finally, it is loaded with the contents of its Data Register zero (DR#0) upon power-up. (See Figure 1)

The wiper counter register is a volatile register; that is, its contents are lost when the X9251 is powered-down. Although the register is automatically loaded with the value in DR#0 upon power-up, this may be different from the value present at power-down. Power-up guidelines are recommended to ensure proper loadings of the DR#0 value into the WCR#.

Data Registers (DR)

Each of the four DCPs has four 8-bit non-volatile Data Registers. These can be read or written directly by the host. Data can also be transferred between any of the four Data Registers and the associated Wiper Counter Register. All operations changing data in one of the Data Registers is a non-volatile operation and takes a maximum of 10ms.

If the application does not require storage of multiple settings for the potentiometer, the Data Registers can be used as regular memory locations for system parameters or user preference data.

Bits [7:0] are used to store one of the 256 wiper positions or data (0 ~ 255).

Status Register (SR)

This 1-bit Status Register is used to store the system status.

WIP: Write In Progress status bit, read only.

- When WIP = 1, indicates that high-voltage write cycle is in progress.
- When WIP = 0, indicates that no high-voltage write cycle is in progress.

TABLE 1. WIPER COUNTER REGISTER, WCR (8-bit), WCR[7:0]: USED TO STORE THE CURRENT WIPER POSITION (VOLATILE)

WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0
(MSB)							(LSB)

TABLE 2. DATA REGISTER, DR (8-bit), DR[7:0]: USED TO STORE WIPER POSITIONS OR DATA (NON-VOLATILE)

Bit 7	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0
(MSB)							(LSB)

Serial Interface

The X9251 supports the SPI interface hardware conventions. The device is accessed via the SI input with data clocked in, on the rising SCK. $\overline{CS}$ must be LOW and the $\overline{HOLD}$ and $\overline{WP}$ pins must be HIGH during the entire operation.

The SO and SI pins can be connected together, since they have three state outputs. This can help to reduce system pin count.

Identification Byte

The first byte sent to the X9251 from the host, following a $\overline{CS}$ going HIGH to LOW, is called the Identification Byte. The most significant four bits of the Identification Byte are a Device Type Identifier, ID[3:0]. For the X9251, this is fixed as 0101 (refer to Table 3).

The least significant four bits of the Identification Byte are the Slave Address bits, AD[3:0]. For the X9251, A3 is 0, A2 is 0, A1 is the logic value at the input pin A1, and A0 is the logic value at the input pin A0. Only the device which Slave Address matches the incoming bits sent by the master executes the instruction. The A1 and A0 inputs can be actively driven by CMOS input signals or tied to V_{CC} or V_{SS}.

Instruction Byte

The next byte sent to the X9251 contains the instruction and register pointer information. The four most significant bits are used provide the instruction opcode (I[3:0]). The RB and RA bits point to one of the four Data Registers of each associated XDCP. The least two significant bits point to one of four Wiper Counter Registers or DCPs.The format is shown below in Table 4.

TABLE 3. IDENTIFICATION BYTE FORMAT

	Device Type Identifier				Slave Address			
	ID3	ID2	ID1	ID0	A3	A2	A1	A0
	0	1	0	1	0	0	Pin A1 Logic Value	Pin A0 Logic Value
	(MSB)							(LSB)

TABLE 4. INSTRUCTION BYTE FORMAT

	Instruction Opcode				Register Selection		DCP Selection (WCR Selection)	
	I3	I2	I1	I0	RB	RA	P1	P0
	(MSB)							(LSB)

Data Register Selection

REGISTER	RB	RA
DR#0	0	0
DR#1	0	1
DR#2	1	0
DR#3	1	1

#: 0, 1, 2, or 3

TABLE 5. INSTRUCTION SET

INSTRUCTION	INSTRUCTION SET								OPERATION
	I3	I2	I1	I0	RB	RA	P1	P0	
Read Wiper Counter Register	1	0	0	1	0	0	1/0	1/0	Read the contents of the Wiper Counter Register pointed to by P1 - P0
Write Wiper Counter Register	1	0	1	0	0	0	1/0	1/0	Write new value to the Wiper Counter Register pointed to by P1 - P0
Read Data Register	1	0	1	1	1/0	1/0	1/0	1/0	Read the contents of the Data Register pointed to by P1 - P0 and RB - RA
Write Data Register	1	1	0	0	1/0	1/0	1/0	1/0	Write new value to the Data Register pointed to by P1 - P0 and RB - RA
XFR Data Register to Wiper Counter Register	1	1	0	1	1/0	1/0	1/0	1/0	Transfer the contents of the Data Register pointed to by P1 - P0 and RB - RA to its associated Wiper Counter Register
XFR Wiper Counter Register to Data Register	1	1	1	0	1/0	1/0	1/0	1/0	Transfer the contents of the Wiper Counter Register pointed to by P1 - P0 to the Data Register pointed to by RB - RA
Global XFR Data Registers to Wiper Counter Registers	0	0	0	1	1/0	1/0	0	0	Transfer the contents of the Data Registers pointed to by RB - RA of all four pots to their respective Wiper Counter Registers
Global XFR Wiper Counter Registers to Data Register	1	0	0	0	1/0	1/0	0	0	Transfer the contents of both Wiper Counter Registers to their respective data Registers pointed to by RB - RA of all four pots
Increment/Decrement Wiper Counter Register	0	0	1	0	0	0	1/0	1/0	Enable Increment/decrement of the Control Latch pointed to by P1 - P0

NOTE: 1/0 = data is one or zero

Instructions

Four of the nine instructions are three bytes in length. These instructions are:

- **Read Wiper Counter Register** – read the current wiper position of the selected potentiometer,
- **Write Wiper Counter Register** – change current wiper position of the selected potentiometer,
- **Read Data Register** – read the contents of the selected Data Register,
- **Write Data Register** – write a new value to the selected Data Register,
- **Read Status** – this command returns the contents of the WIP bit which indicates if the internal write cycle is in progress.

The basic sequence of the three byte instructions is illustrated in Figure 3. These three-byte instructions exchange data between the WCR and one of the Data Registers. A transfer from a Data Register to a WCR is essentially a write to a static RAM, with the static RAM controlling the wiper position. The response of the wiper to this action is delayed by t_{WRL}. A transfer from the WCR (current wiper position), to a Data Register is a write to non-volatile memory and takes a minimum of t_{WR} to complete. The transfer can occur between one of the four potentiometer's WCR, and one of its associated registers, DRs; or it may occur globally, where the transfer occurs between all potentiometers and one associated register. The Read Status Register instruction is the only unique format (See Figure 5).

Four instructions require a two-byte sequence to complete. These instructions transfer data between the host and the X9251; either between the host and one of the data registers or directly between the host and the Wiper Counter Register. These instructions are:

- **XFR Data Register to Wiper Counter Register** – This transfers the contents of one specified Data Register to the associated Wiper Counter Register.
- **XFR Wiper Counter Register to Data Register** – This transfers the contents of the specified Wiper Counter Register to the specified associated Data Register.
- **Global XFR Data Register to Wiper Counter Register** – This transfers the contents of all specified Data Registers to the associated Wiper Counter Registers.
- **Global XFR Wiper Counter Register to Data Register** – This transfers the contents of all Wiper Counter Registers to the specified associated Data Registers.

Increment/Decrement Command

The final command is Increment/Decrement (See Figures 6 and 7). The Increment/Decrement command is different from the other commands. Once the command is issued and the X9251 has responded with an Acknowledge, the master can clock the selected wiper up and/or down in one segment steps; thereby, providing a fine tuning capability to the host.

For each SCK clock pulse (t_{HIGH}) while SI is HIGH, the selected wiper moves one wiper position towards the R_H terminal. Similarly, for each SCK clock pulse while SI is LOW, the selected wiper moves one wiper position towards the R_L terminal. A detailed illustration of the sequence and timing for this operation are shown. See Instruction format for more details.

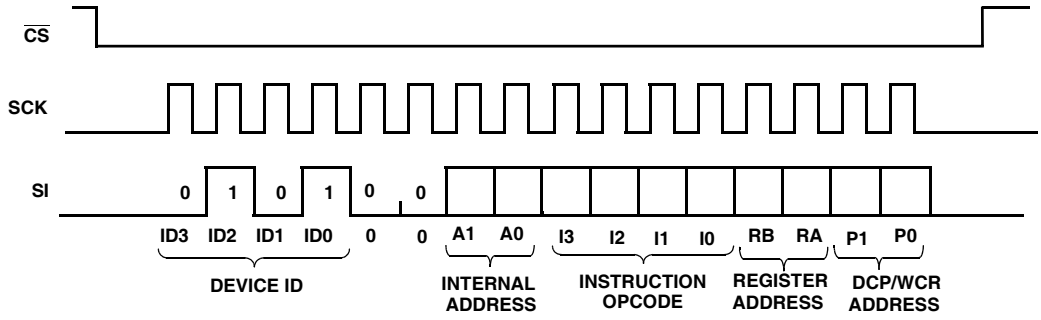


FIGURE 2. TWO-BYTE INSTRUCTION SEQUENCE

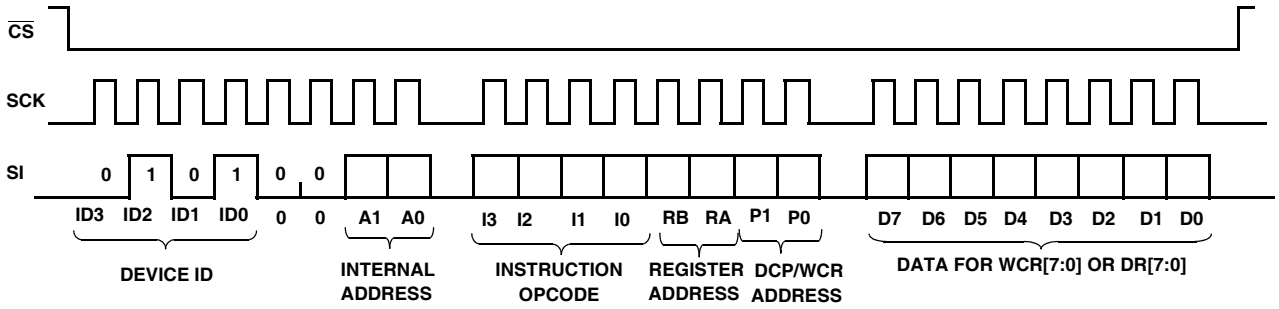


FIGURE 3. THREE-BYTE INSTRUCTION SEQUENCE SPI INTERFACE; WRITE CASE

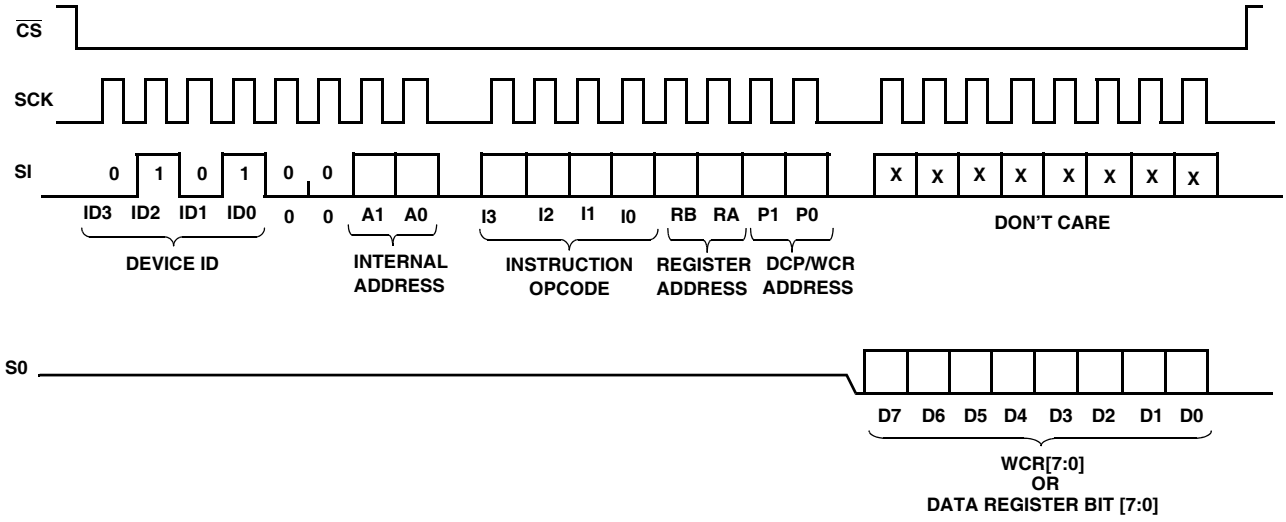


FIGURE 4. THREE-BYTE INSTRUCTION SEQUENCE SPI INTERFACE, READ CASE

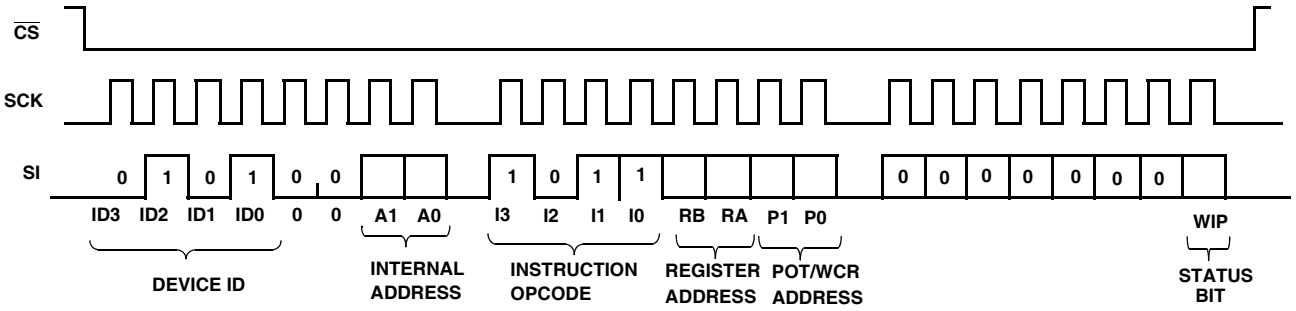


FIGURE 5. THREE-BYTE INSTRUCTION SEQUENCE (READ STATUS REGISTER)

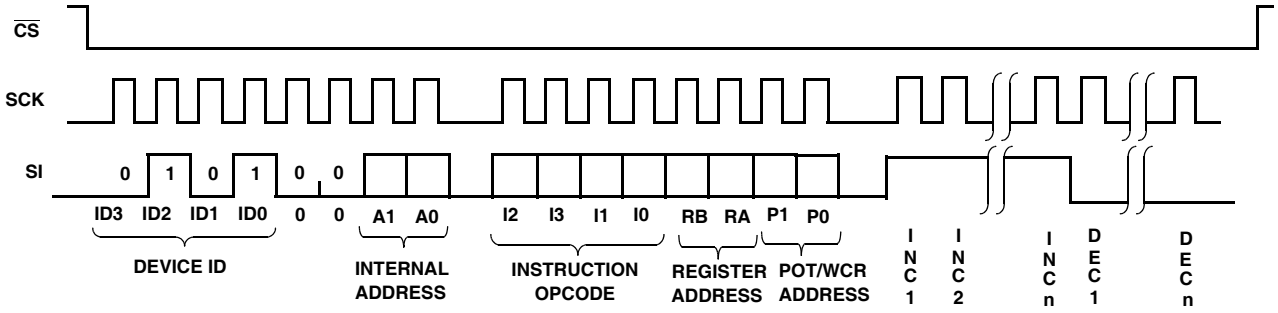


FIGURE 6. INCREMENT/DECREMENT INSTRUCTION SEQUENCE

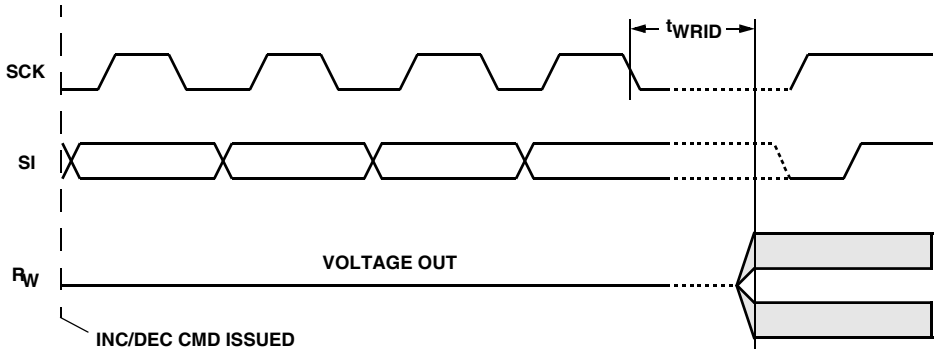


FIGURE 7. INCREMENT/DECREMENT TIMING SPEC

Instruction Format

Read Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				WCR Addresses				Wiper Position (Sent by X9251 on SO)								$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	1	0	0	1	0	0	0	0	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0	

Write Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				WCR Addresses				Data Byte (Sent by Host on SI)								$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	1	0	1	0	0	0	0	0	WCR7	WCR6	WCR5	WCR4	WCR3	WCR2	WCR1	WCR0	

Read Data Register (DR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR and WCR Addresses				Data Byte (Sent by X9271 on SO)								$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	1	0	1	1	RB	RA	P1	P0	D7	D6	D5	D4	D3	D2	D1	D0	

Write Data Register (DR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR and WCR Addresses				Data Byte (Sent by Host on SI)								$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	1	0	0	RB	RA	P1	P0	D7	D6	D5	D4	D3	D2	D1	D0		

Global Transfer Data Register (DR) to Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR Addresses				$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	0	0	0	1	RB	RA	0	0	

NOTES:

1. “A1 ~ A0”: stands for the device addresses sent by the master.
2. WPx refers to wiper position data in the Counter Register
3. “I”: stands for the increment operation, SI held HIGH during active SCK phase (high).
4. “D”: stands for the decrement operation, SI held LOW during active SCK phase (high).

Global Transfer Wiper Counter Register (WCR) to Data Register (DR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR Addresses				$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	0	0	0	RB	RA	0	0		

Transfer Wiper Counter Register (WCR) to Data Register (DR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR and WCR Addresses				$\overline{CS}$ Rising Edge	HIGH-VOLTAGE WRITE CYCLE
	0	1	0	1	0	0	A1	A0	1	1	1	0	RB	RA	0	0		

Transfer Data Register (DR) to Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				DR and WCR Addresses				$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	1	1	0	1	RB	RA	0	0	

Increment/Decrement Wiper Counter Register (WCR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				WCR Addresses				Increment/Decrement (Sent by Master on SI)						$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	0	0	1	0	X	X	0	0	I/D	I/D	.	.	.	I/D	I/D	

Read Status Register (SR)

$\overline{CS}$ Falling Edge	Device Type Identifier				Device Addresses				Instruction Opcode				WCR Addresses				Data Byte (Sent by X9251 on SO)								$\overline{CS}$ Rising Edge
	0	1	0	1	0	0	A1	A0	0	1	0	1	0	0	0	1	0	0	0	0	0	0	0	WIP	

NOTES:

1. “A1 ~ A0”: stands for the device addresses sent by the master.
2. WPx refers to wiper position data in the Counter Register
3. “I”: stands for the increment operation, SI held HIGH during active SCK phase (high).
4. “D”: stands for the decrement operation, SI held LOW during active SCK phase (high).

Absolute Maximum Ratings

Temperature Under Bias . . . . . .-65°C to +135°C
Storage Temperature . . . . . .-65°C to +150°C
Voltage on SCK, $\overline{CS}$, SI, SO, $\overline{WP}$, $\overline{HOLD}$, V_{CC}
with respect to V_{SS} . . . . . -1V to +7V
$\Delta V = | (V_H - VL) |$ 5.5V
Lead Temperature (soldering, 10s) . . . . . .+300°C
I_W (10s) . . . . . ±6mA
Wiper Current. . . . . ±3mA
Power Rating (each pot) 50mW

Operating Conditions

Commercial Temperature Range. . . . . 0°C to +70°C
Industrial Temperature Range . . . . . .-40°C to +85°C
Supply Voltage (V_{CC}) Limits (Note 4)
X9251. . . . . .5V ±10%
X9251-2.7. . . . . 2.7V to 5.5V

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

Analog Characteristics (Over the recommended operating conditions unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			
			MIN	TYP	MAX	UNITS
R_{TOTAL}	End to End Resistance	T version		100		kΩ
R_{TOTAL}	End to End Resistance	U version		50		kΩ
	End to End Resistance Tolerance				±20	%
R_W	Wiper Resistance	$I_W = \frac{V(V_{CC})}{R_{TOTAL}}$ @ V_{CC} = 3V			300	Ω
		$I_W = \frac{V(V_{CC})}{R_{TOTAL}}$ @ V_{CC} = 5V			220	Ω
V_{TERM}	Voltage on any R_H or R_L Pin	V_{SS} = 0V	V_{SS}		V_{CC}	V
	Noise (Note 6)	Ref: 1V		-120		dBV/$\sqrt{Hz}$
	Resolution			0.4		%
	Absolute Linearity (Note 1)	$R_{w(n)(actual)} - R_{w(n)(expected)}$ (Note 5)	-1		+1	MI (Note 3)
	Relative Linearity (Note 2)	$R_{w(n+1)} - [R_{w(n)+MI}]$ (Note 5)	-0.6		+0.6	MI (Note 3)
	Temperature Coefficient of R_{TOTAL}	(Note 6)		±300		ppm/°C
	Ratiometric Temp. Coefficient	(Note 6)		±20		ppm/°C
$C_H/C_L/C_W$	Potentiometer Capacitances	See Macro model, (Note 6)		10/10/25		pF

NOTES:

1. Absolute linearity is utilized to determine actual wiper voltage versus expected voltage as determined by wiper position when used as a potentiometer.
2. Relative linearity is utilized to determine the actual change in voltage between two successive tap positions when used as a potentiometer. It is a measure of the error in step size.
3. MI = RTOT/255 or ($R_H - R_L$)/255, single pot
4. During power up $V_{CC} > V_H$, V_L, and V_W.
5. n = 0, 1, 2, …,255; m = 0, 1, 2, …, 254.

DC Operating Characteristics (Over the recommended operating conditions unless otherwise specified.)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			
			MIN.	TYP	MAX	UNITS
I_{CC1}	V_{CC} supply current (active)	f_{SCK} = 2.5 MHz, SO = Open, V_{CC} = 6V Other Inputs = V_{SS}			400	µA
I_{CC2}	V_{CC} supply current (non-volatile write)	f_{SCK} = 2.5MHz, SO = Open, V_{CC} = 6V Other Inputs = V_{SS}		1	5	mA
I_{SB}	V_{CC} current (standby)	$\overline{SCK}$ = SI = V_{SS}, Addr. = V_{SS}, $\overline{CS}$ = V_{CC} = 6V			3	µA
I_{LI}	Input leakage current	V_{IN} = V_{SS} to V_{CC}			10	µA
I_{LO}	Output leakage current	V_{OUT} = V_{SS} to V_{CC}			10	µA
V_{IH}	Input HIGH voltage		V_{CC} x 0.7			V
V_{IL}	Input LOW voltage				V_{CC} x 0.3	V
V_{OL}	Output LOW voltage	I_{OL} = 3mA			0.4	V
V_{OH}	Output HIGH voltage	I_{OH} = -1mA, $V_{CC} \geq$ +3V	V_{CC} - 0.8			V
V_{OH}	Output HIGH voltage	I_{OH} = -0.4mA, $V_{CC} \leq$ +3V	V_{CC} - 0.4			V

Endurance and Data Retention

PARAMETER	MIN	UNITS
Minimum endurance	100,000	Data changes per bit per register
Data retention	100	years

Capacitance

SYMBOL	TEST	TEST CONDITIONS	TYP	UNITS
$C_{IN/OUT}$ (Note 6)	Input/Output capacitance (SI)	V_{OUT} = 0V	8	pF
C_{OUT} (Note 6)	Output capacitance (SO)	V_{OUT} = 0V	8	pF
C_{IN} (Note 6)	Input capacitance (A0, A1, $\overline{CS}$, $\overline{WP}$, $\overline{HOLD}$, and SCK)	V_{IN} = 0V	6	pF

Power-Up Timing

SYMBOL	PARAMETER	MIN	MAX	UNITS
t_r V_{CC} (Note 6)	V_{CC} Power-up rate	0.2		V/ms
t_{PUR} (Note 7)	Power-up to initiation of read operation		1	ms
t_{PUW} (Note 7)	Power-up to initiation of write operation		50	ms

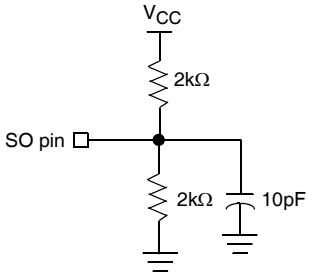
A.C. Test Conditions

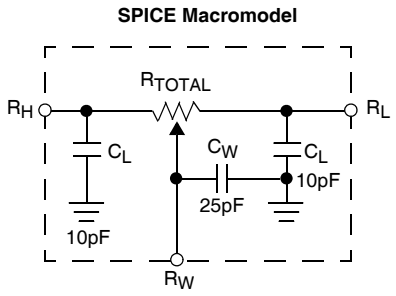
Input Pulse Levels	V_{CC} x 0.1 to V_{CC} x 0.9
Input rise and fall times	10ns
Input and output timing level	V_{CC} x 0.5

NOTES:

6. This parameter is not 100% tested
7. t_{PUR} and t_{PUW} are the delays required from the time the (last) power supply (V_{CC}-) is stable until the specific instruction can be issued. These parameters are periodically sampled and not 100% tested.

Equivalent A.C. Load Circuit





AC TIMING

SYMBOL	PARAMETER	MIN	MAX	UNITS
f_{SCK}	SPI clock frequency		2	MHz
t_{CYC}	SPI clock cycle rime	500		ns
t_{WH}	SPI clock high rime	200		ns
t_{WL}	SPI clock low time	200		ns
t_{LEAD}	Lead time	250		ns
t_{LAG}	Lag time	250		ns
t_{SU}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input setup time	50		ns
t_H	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input hold time	50		ns
t_{RI}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input rise time		2	µs
t_{FI}	SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ input fall time		2	µs
t_{DIS}	SO output disable time	0	250	ns
t_V	SO output valid time		200	ns
t_{HO}	SO output hold time	0		ns
t_{RO} (Note 6)	SO output rise time		100	ns
t_{FO} (Note 6)	SO output fall time		100	ns
t_{HOLD}	$\overline{HOLD}$ time	400		ns
t_{HSU}	$\overline{HOLD}$ setup time	100		ns
t_{HH}	$\overline{HOLD}$ hold time	100		ns
t_{HZ}	$\overline{HOLD}$ low to output in high Z		100	ns
t_{LZ}	$\overline{HOLD}$ high to output in low Z		100	ns
T_I	Noise suppression time constant at SI, SCK, $\overline{HOLD}$ and $\overline{CS}$ inputs		10	ns
t_{CS}	$\overline{CS}$ deselect time	2		µs
t_{WPASU}	$\overline{WP}$, A0 setup time	0		ns
t_{WPAH}	$\overline{WP}$, A0 hold time	0		ns

High-Voltage Write Cycle Timing

SYMBOL	PARAMETER	TYP	MAX	UNITS
t_{WR}	High-voltage write cycle time (store instructions)	5	10	ms

XDCP Timing

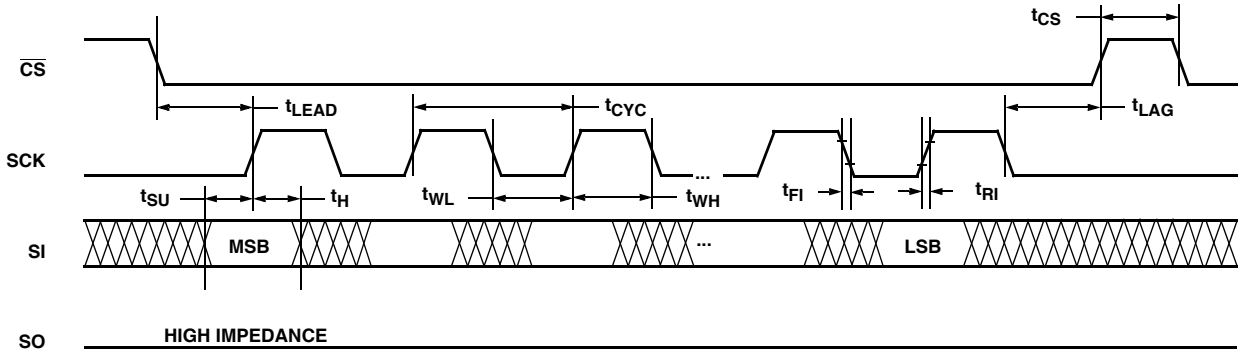
SYMBOL	PARAMETER	MIN	MAX	UNITS
t_{WRPO} (Note 6)	Wiper response time after the third (last) power supply is stable	5	10	µs
t_{WRL} (Note 6)	Wiper response time after instruction issued (all load instructions)	5	10	µs

Symbol Table

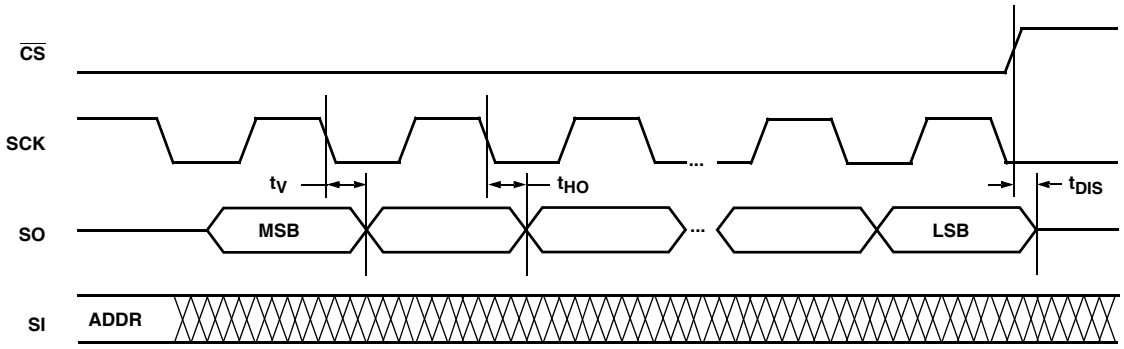
WAVEFORM	INPUTS	OUTPUTS
	Must be steady	Will be steady
	May change from Low to High	Will change from Low to High
	May change from High to Low	Will change from High to Low
	Don't Care: Changes Allowed	Changing: State Not Known
	N/A	Center Line is High Impedance

Timing Diagrams

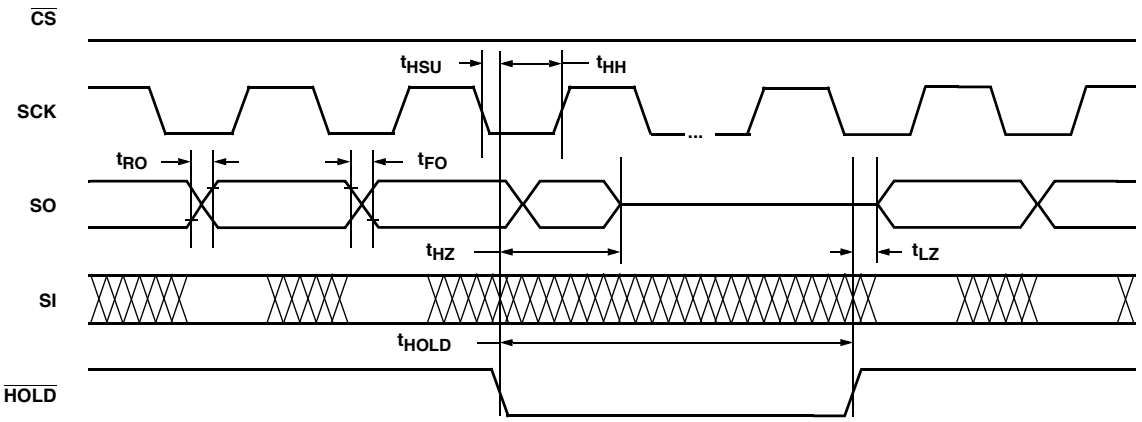
Input Timing



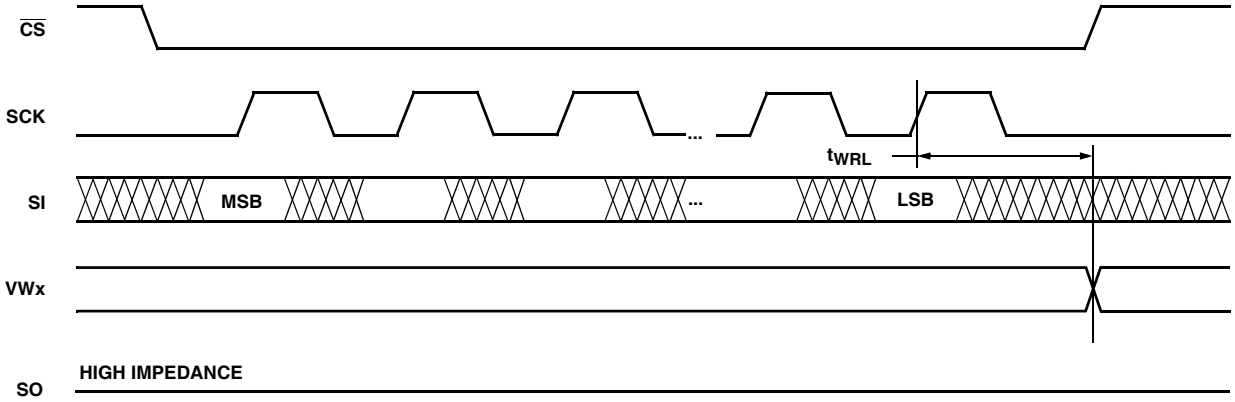
Output Timing



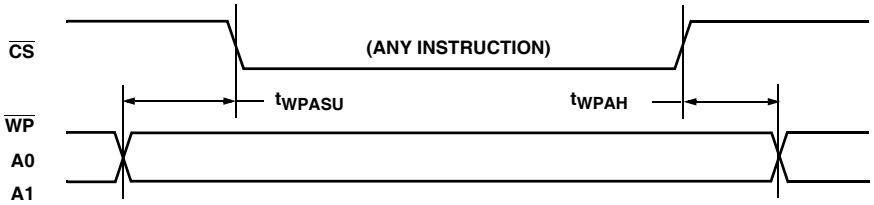
Hold Timing



XDCP Timing (for All Load Instructions)

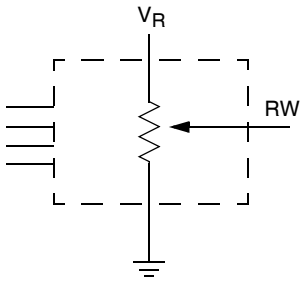


Write Protect and Device Address Pins Timing

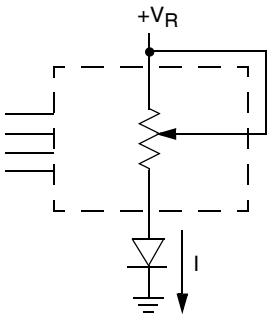


Applications information

Basic Configurations of Electronic Potentiometers



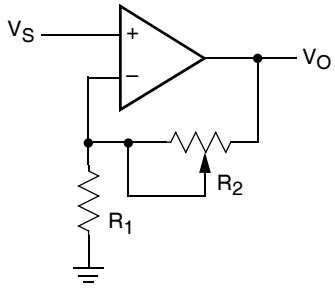
Three terminal Potentiometer; Variable voltage divider



Two terminal Variable Resistor; Variable current

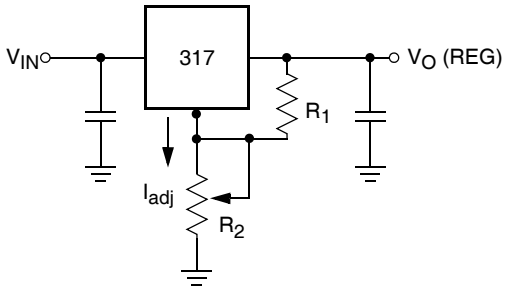
Application Circuits

NON INVERTING AMPLIFIER



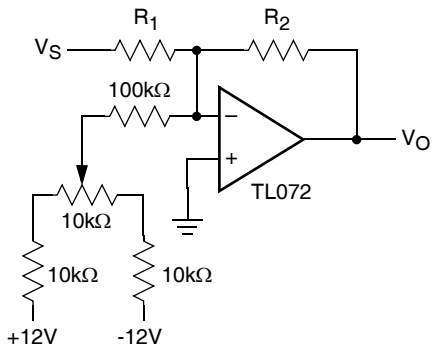
$V_O = (1+R_2/R_1)V_S$

VOLTAGE REGULATOR

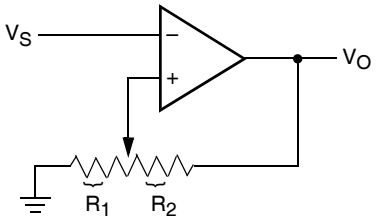


V_O (REG) = 1.25V $(1+R_2/R_1)+I_{adj} R_2$

OFFSET VOLTAGE ADJUSTMENT



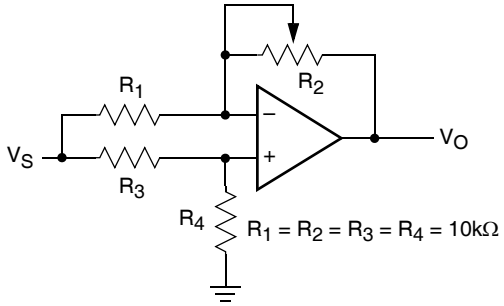
COMPARATOR WITH HYSTERESIS



$V_{UL} = \{R_1/(R_1+R_2)\}\ V_O(max)$
$RL_L = \{R_1/(R_1+R_2)\}\ V_O(min)$

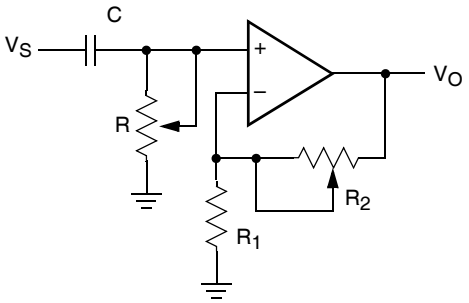
Application Circuits (continued)

ATTENUATOR



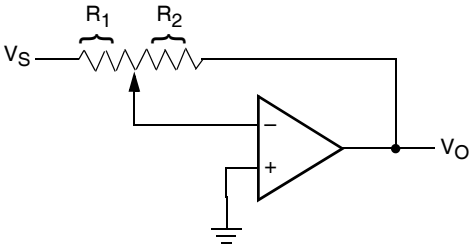
$V_O = G\ V_S$
$-1/2 \leq G \leq +1/2$

FILTER



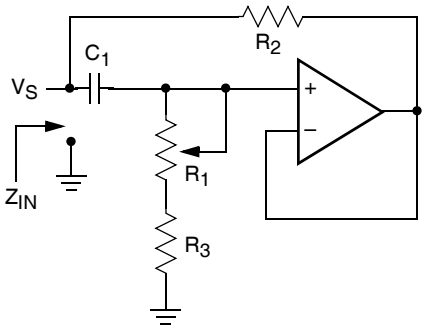
$G_O = 1 + R_2/R_1$
$fc = 1/(2\pi RC)$

INVERTING AMPLIFIER



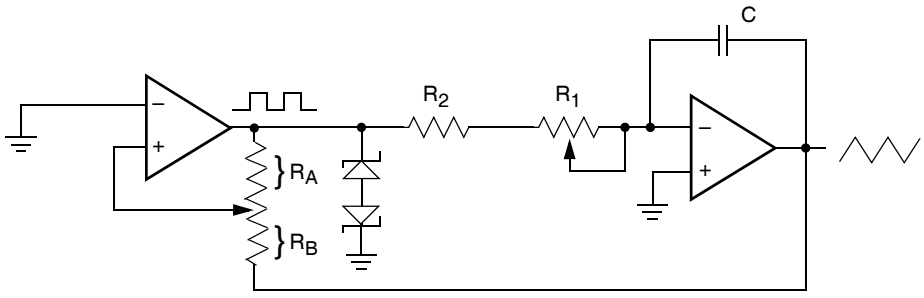
$V_O = G\ V_S$
$G = -R_2/R_1$

EQUIVALENT L-R CIRCUIT



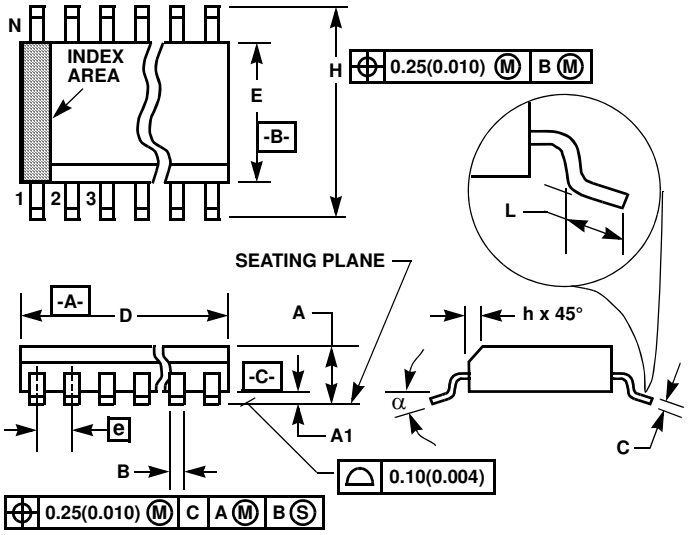
$Z_{IN} = R_2 + s\ R_2\ (R_1 + R_3)\ C_1 = R_2 + s\ Leq$
$(R_1 + R_3) >> R_2$

FUNCTION GENERATOR



frequency $\propto R_1, R_2, C$
amplitude $\propto R_A, R_B$

Small Outline Plastic Packages (SOIC)



NOTES:

1. Symbols are defined in the “MO Series Symbol List” in Section 2.2 of Publication Number 95.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
4. Dimension “E” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
5. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
6. “L” is the length of terminal for soldering to a substrate.
7. “N” is the number of terminal positions.
8. Terminal numbers are shown for reference only.
9. The lead width “B”, as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch)
10. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.

M24.3 (JEDEC MS-013-AD ISSUE C)
24 LEAD WIDE BODY SMALL OUTLINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.0926	0.1043	2.35	2.65	-
A1	0.0040	0.0118	0.10	0.30	-
B	0.013	0.020	0.33	0.51	9
C	0.0091	0.0125	0.23	0.32	-
D	0.5985	0.6141	15.20	15.60	3
E	0.2914	0.2992	7.40	7.60	4
e	0.05 BSC		1.27 BSC		-
H	0.394	0.419	10.00	10.65	-
h	0.010	0.029	0.25	0.75	5
L	0.016	0.050	0.40	1.27	6
N	24		24		7
α	0°	8°	0°	8°	-

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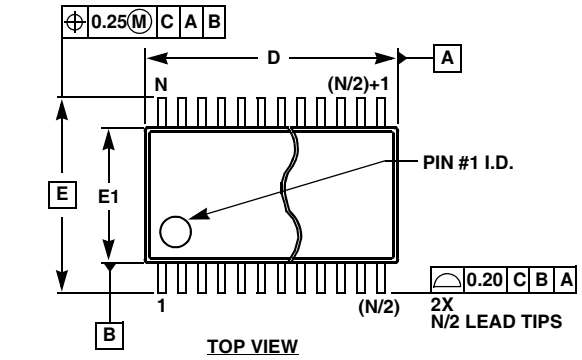
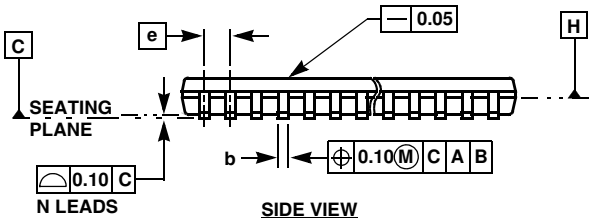
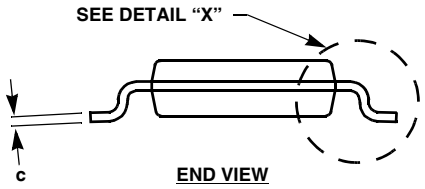
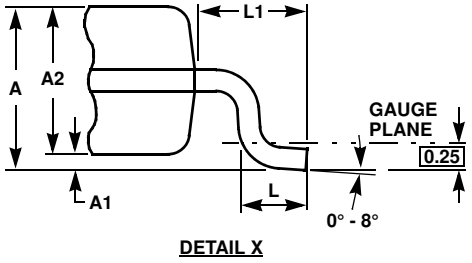
Thin Shrink Small Outline Package Family (TSSOP)









MDP0044

THIN SHRINK SMALL OUTLINE PACKAGE FAMILY

SYMBOL	MILLIMETERS					TOLERANCE
	14 LD	16 LD	20 LD	24 LD	28 LD	
A	1.20	1.20	1.20	1.20	1.20	Max
A1	0.10	0.10	0.10	0.10	0.10	±0.05
A2	0.90	0.90	0.90	0.90	0.90	±0.05
b	0.25	0.25	0.25	0.25	0.25	+0.05/-0.06
c	0.15	0.15	0.15	0.15	0.15	+0.05/-0.06
D	5.00	5.00	6.50	7.80	9.70	±0.10
E	6.40	6.40	6.40	6.40	6.40	Basic
E1	4.40	4.40	4.40	4.40	4.40	±0.10
e	0.65	0.65	0.65	0.65	0.65	Basic
L	0.60	0.60	0.60	0.60	0.60	±0.15
L1	1.00	1.00	1.00	1.00	1.00	Reference

Rev. F 2/07

NOTES:

1. Dimension “D” does not include mold flash, protrusions or gate burrs. Mold flash, protrusions or gate burrs shall not exceed 0.15mm per side.
2. Dimension “E1” does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm per side.
3. Dimensions “D” and “E1” are measured at dAtum Plane H.
4. Dimensioning and tolerancing per ASME Y14.5M-1994.