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Ultra-Low-Power, Single-Channel Integrated Bioimpedance (BioZ) AFE

MAX30002

General Description

The MAX30002 is a complete bioimpedance (BioZ), analog front-end (AFE) solution for wearable applications. It offers high performance for clinical and fitness applications, with ultra-low-power for long battery life. The MAX30002 is a single bioimpedance channel capable of measuring respiration.

The bioimpedance channel has ESD protection, EMI filtering, internal lead biasing, DC leads-off detection, ultra-low-power leads-on detection during standby mode, and a programmable resistive load for built-in self-test. Soft power-up sequencing ensures no large transients are injected into the electrodes. The channel also has high input impedance, low noise, high CMRR, programmable gain, various low-pass and high-pass filter options, and a high resolution analog-to-digital converter. The bioimpedance channel includes integrated programmable current drive, works with common electrodes, and has the flexibility for 2 or 4 electrode measurements. The bioimpedance channel also has AC lead off detection.

The MAX30002 is available in a 30-bump wafer-level package (WLP), operating over the 0°C to +70°C commercial temperature range.

Applications

- Single-Lead Wireless Patches for In-Patient/Out-Patient Monitoring
- Respiration and Hydration Monitors
- Impedance Based Heart Rate Detection

Benefits and Features

- BioZ AFE with High Resolution Data Converter
  - 17 Bits ENOB with 1.1μV_{P-P} Noise for BioZ
- High AC Dynamic Range of 90mV_{P-P} Will Help Prevent Saturation in the Presence of Motion/Direct Electrode Hits
- Longer Battery Life Compared to Competing Solutions
  - 158µW at 1.1V Supply Voltage
- Leads-On Interrupt Feature Allows to Keep the µC in Deep Sleep Mode Until Valid Lead Condition is Detected
  - Lead-On Detect Current: 0.63µA (typ)
- High Accuracy Allows for More Physiological Data Extractions
- 8-Word FIFO Allows the MCU to Stay Powered Down for 256ms with Full Data Acquisition
- High-Speed SPI Interface
- Shutdown Current of 0.58µA (typ)

***Ordering Information* appears at end of data sheet.**

19-100289; Rev 1, 1/23

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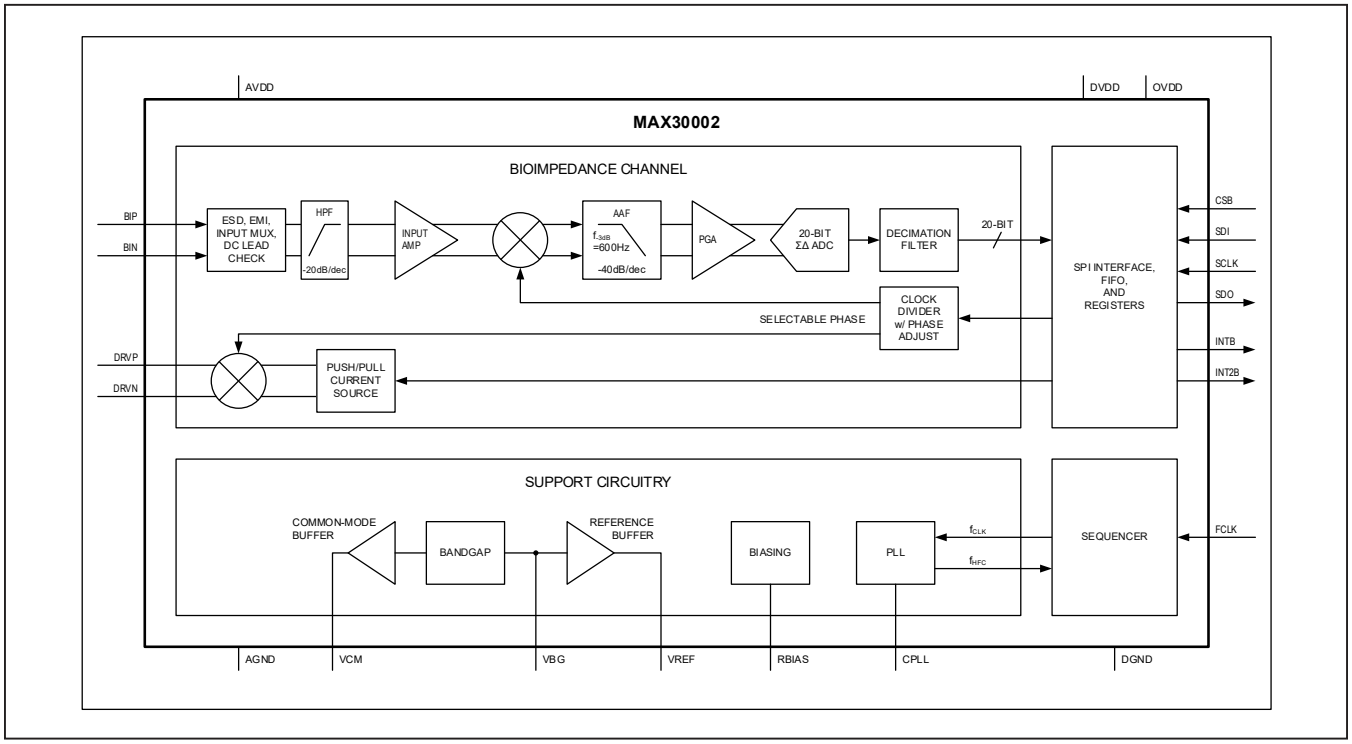
Functional Diagram



Absolute Maximum Ratings

AVDD to AGND .....-0.3V to +2.0V
DVDD to DGND.....-0.3V to +2.0V
AVDD to DVDD .....-0.3V to +0.3V
OVDD to DGND .....-0.3V to +3.6V
AGND to DGND .....-0.3V to +0.3V
CSB, SCLK, SDI, FCLK to DGND .....-0.3V to +3.6V
SDO, INTB, INT2B
to DGND..... -0.3V to the lower of (3.6V and OVDD + 0.3V)
All Other Pins
to AGND ..... -0.3V to the lower of (2.0V and AVDD + 0.3V)
Maximum Current into Any Pin.....±50mA

Continuous Power Dissipation (T_A = +70ºC)
30-Bump WLP
(derate 24.3mW/ºC above +70ºC).....1945.5mW
Operating Temperature Range.....0ºC to +70°C
Junction Temperature.....+150°C
Storage Temperature Range..... -65°C to +150°C
Lead Temperature (Soldering, 10sec).....+300°C
Soldering Temperature (reflow).....+260°C

Package Thermal Characteristics (Note 1)

WLP
Junction-to-Ambient Thermal Resistance (θ_{JA}) .....44°C/W

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Note 1: Package thermal resistances were obtained using the method described in JEDEC specification JESD51-7, using a four-layer board. For detailed information on package thermal considerations, refer to **www.maximintegrated.com/thermal-tutorial**.

Electrical Characteristics

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
BIOIMPEDANCE (BIOZ) CHANNEL						
Signal Generator Resolution		Square wave generator		1		Bits
DRVP/N Injected Full-Scale Current		Programmable, see BIOZ_CGMAG[2:0]		8 to 96		μA_{PK}
DRVP/N Injected Current Accuracy		Internal bias resistor, see EXT_RBIAS	-30		+30	%
		External bias resistor (0.1%, 10ppm, 324kΩ)	-10		+10	
DRVP/N Injected Current Power Supply Rejection				<±1		%/V
DRVP/N Injected Current Temperatue Coefficient		External bias resistor, 32μA_{P-P}, 0 to 70ºC (0.1%, 10ppm, 324kΩ)		50		ppm/°C
DRVP/N Compliance Voltage		V_{DRVP} - V_{DRVN}		±(V_{AVDD}-0.5)		V_{P-P}
Current Injection Frequency		Programmable, see BIOZ_FCGEN[3:0]		0.125 to 131.072		kHz
AC Differential Input Range		Shift from nominal gain < 1% (V_{AVDD} = 1.1V)		25		mV
		Shift from nominal gain < 1% (V_{AVDD} = 1.8V)		90		
BioZ Channel Gain		Programmable, see BIOZ_GAIN[1:0]		10 to 80		V/V
ADC Sample Rate		Programmable, see BIOZ_RATE		24.98 to 64		sps

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
ADC Resolution				20		Bits
Input Referred Noise (BIP, BIN)		BW = 0.05 to 4Hz, Gain = 20x		0.16		μV_{RMS}
		BW = 0.05 to 4Hz, Gain = 20x		1.1		μV_{P-P}
Impedance Resolution		DC to 4Hz, 32μA_{P-P}, 40kHz, Gain = 20x, R_{BODY} = 680Ω		40		$m\Omega_{P-P}$
Input Analog High Pass Filter		Programmable, see BIOZ_AHPF[2:0]		125 to 7200		Hz
Demodulation Phase Range		Programmable, see BIOZ_PHOFF[3:0]		0-168.75		°
Demodulation Phase Resolution				11.25		°
Output Digital Low Pass Filter		DLPF[1:0] = 01		4		Hz
		DLPF[1:0] = 10		8		
		DLPF[1:0] = 11		16		
Output Digital High Pass Filter		DHPF[1:0] = 01		0.05		Hz
		DHPF[1:0] = 1x		0.5		
BIOIMPEDANCE (BIOZ) INPUT MUX						
DC Lead Off Check		IMAG[2:0] = 001		5		nA
		IMAG[2:0] = 010		10		
		IMAG[2:0] = 011		20		
		IMAG[2:0] = 100		50		
		IMAG[2:0] = 101		100		
DC Lead Off Comparator Low Threshold		VTH[1:0] = 11 (Note 4)		V_{MID} - 0.50		V
		VTH[1:0] = 10 (Note 5)		V_{MID} - 0.45		
		VTH[1:0] = 01 (Note 6)		V_{MID} - 0.40		
		VTH[1:0] = 00		V_{MID} - 0.30		
DC Lead Off Comparator High Threshold		VTH[1:0] = 11 (Note 4)		V_{MID} + 0.50		V
		VTH[1:0] = 10 (Note 5)		V_{MID} + 0.45		
		VTH[1:0] = 01 (Note 6)		V_{MID} + 0.40		
		VTH[1:0] = 00		V_{MID} + 0.30		
Lead Bias Impedance		Lead bias enabled, RBIASV[1:0] = 00		50		MΩ
		Lead bias enabled, RBIASV[1:0] = 01		100		
		Lead bias enabled, RBIASV[1:0] = 10		200		
Lead Bias Voltage	V_{MID}	Lead bias enabled		V_{AVDD} / 2.15		V

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Resistive Load Nominal Value	R_{VAL}	Programmable, see BMUX_RNOM[2:0]		0.625 to 5.0		kΩ
Resistive Load Modulation Value	R_{MOD}	Programmable, see BMUX_RMOD[2:0]		15 to 2960		mΩ
Resistive Load Modulation Frequency	F_{MOD}	Programmable, see BMUX_FBIST[1:0]		0.625 to 4.0		Hz
INTERNAL REFERENCE/COMMON-MODE						
V_{BG} Output Voltage	V_{BG}			0.650		V
V_{BG} Output Impedance				100		kΩ
External V_{BG} Compensation Capacitor	C_{BG}		1			µF
V_{REF} Output Voltage	V_{REF}	T_A = +25ºC	0.995	1.000	1.005	V
V_{REF} Temperature Coefficient	TC_{REF}	T_A = 0ºC to +70ºC		10		ppm/ºC
V_{REF} Buffer Line Regulation				330		µV/V
V_{REF} Buffer Load Regulation		I_{LOAD} = 0 to 100µA		25		µV/µA
External V_{REF} Compensation Capacitor	C_{REF}		1	10		µF
VCM Output Voltage	V_{CM}			0.650		V
External V_{CM} Compensation Capacitor	C_{CM}		1	10		µF
DIGITAL INPUTS (SDI, SCLK, CSB, FCLK)						
Input-Voltage High	V_{IH}		0.7 x V_{OVDD}			V
Input-Voltage Low	V_{IL}				0.3 x V_{OVDD}	V
Input Hysteresis	V_{HYS}			0.05 x V_{OVDD}		V
Input Capacitance	C_{IN}			10		pF
Input Current	I_{IN}		-1		+1	µA
DIGITAL OUTPUTS (SDO, INTB, INT2B)						
Output Voltage High	V_{OH}	I_{SOURCE} = 1mA	V_{OVDD} - 0.4			V
Output Voltage Low	V_{OL}	I_{SINK} = 1mA			0.4	V
Three-State Leakage Current			-1		+1	µA
Three-State Output Capacitance				15		pF

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
POWER SUPPLY							
Analog Supply Voltage	V_{AVDD}	Connect AVDD to DVDD		1.1		2.0	V
Digital Supply Voltage	V_{DVDD}	Connect DVDD to AVDD		1.1		2.0	V
Interface Supply Voltage	V_{OVDD}	Power for I/O drivers only		1.65		3.6	V
Supply Current	I_{AVDD} + I_{DVDD}	BioZ channel , LN_BIOZ = 0 CGMAG[2:0] = 011	V_{AVDD} = V_{DVDD} = +1.1V		144		µA
			V_{AVDD} = V_{DVDD} = +1.8V		163		
			V_{AVDD} = V_{DVDD} = +2.0V		170	190	
		BioZ channel , LN_BIOZ = 1 CGMAG[2:0] = 011	V_{AVDD} = V_{DVDD} = +1.1V		158		
			V_{AVDD} = V_{DVDD} = +1.8V		178		
			V_{AVDD} = V_{DVDD} = +2.0V		185	205	
		ULP Lead On Detect	T_A = +70ºC		1.3		
			T_A = +25ºC		0.63	2.5	
Interface Supply Current	I_{OVDD}	V_{OVDD} = +1.65V, BioZ channel at 64sps (Note 7)			0.1		µA
		V_{OVDD} = 3.6V, BioZ channel at 64sps (Note 7)			0.2	1.1	
Shutdown Current	I_{SAVDD} + I_{SDVDD}	V_{AVDD} = V_{DVDD} = 2.0V	T_A = +70ºC		1.3		µA
			T_A = +25ºC		0.58	2.5	
	I_{SOVDD}	V_{OVDD} = 3.6V, V_{AVDD} = V_{DVDD} = 2.0V				1.1	
TIMING CHARACTERISTICS (NOTE 3)							
SCLK Frequency	f_{SCLK}			0		12	MHz
SCLK Period	t_{CP}			83			ns
SCLK Pulse Width High	t_{CH}			15			ns
SCLK Pulse Width Low	t_{CL}			15			ns
CSB Fall to SCLK Rise Setup Time	t_{CSS0}	To 1st SCLK rising edge (RE)		15			ns
CSB Fall to SCLK Rise Hold Time	t_{CSH0}	Applies to inactive RE preceding 1st RE		0			ns
CSB Rise to SCLK Rise Hold Time	t_{CSH1}	Applies to 32nd RE, executed write		10			ns
CSB Rise to SCLK Rise	t_{CSA}	Applies to 32nd RE, aborted write sequence		15			ns

Electrical Characteristics (continued)

(V_{DVDD} = V_{AVDD} = +1.1V to +2.0V, V_{OVDD} = +1.65V to +3.6V, f_{FCLK} = 32.768kHz, LN_BIOZ = 1, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{DVDD} = V_{AVDD} = +1.8V, V_{OVDD} = +2.5V, T_A = +25°C.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
SCLK Rise to CSB Fall	t_{CSF}	Applies to 32nd RE	100			ns
CSB Pulse-Width High	t_{CSPW}		20			ns
SDI-to-SCLK Rise Setup Time	t_{DS}		8			ns
SDI to SCLK Rise Hold Time	t_{DH}		8			ns
SCLK Fall to SDO Transition	t_{DOT}	C_{LOAD} = 20pF			40	ns
		C_{LOAD} = 20pF, V_{AVDD} = V_{DVDD} ≥ 1.8V, V_{OVDD} ≥ 2.5V			20	ns
SCLK Fall to SDO Hold	t_{DOH}	C_{LOAD} = 20pF	2			ns
CSB Fall to SDO Fall	t_{DOE}	Enable time, C_{LOAD} = 20pF			30	ns
CSB Rise to SDO Hi-Z	t_{DOZ}	Disable time			35	ns
FCLK Frequency	f_{FCLK}	External reference clock		32.768		kHz
FCLK Period	t_{FP}			30.52		µs
FCLK Pulse-Width High	t_{FH}	50% duty cycle assumed		15.26		µs
FCLK Pulse-Width Low	t_{FL}	50% duty cycle assumed		15.26		µs

Note 2: All devices are 100% production tested at T_A = +25ºC. Specifications over the operating temperature range and relevant supply voltage range are guaranteed by design and characterization.
Note 3: Guaranteed by design and characterization. Not tested in production.
Note 4: Use this setting only for V_{AVDD} = V_{DVDD} ≥ 1.65V.
Note 5: Use this setting only for V_{AVDD} = V_{DVDD} ≥ 1.55V.
Note 6: Use this setting only for V_{AVDD} = V_{DVDD} ≥ 1.45V.
Note 7: f_{SCLK} = 4MHz, burst mode, BFIT[2:0] = 111, C_{SDO} = C_{INTB} = 50pF.

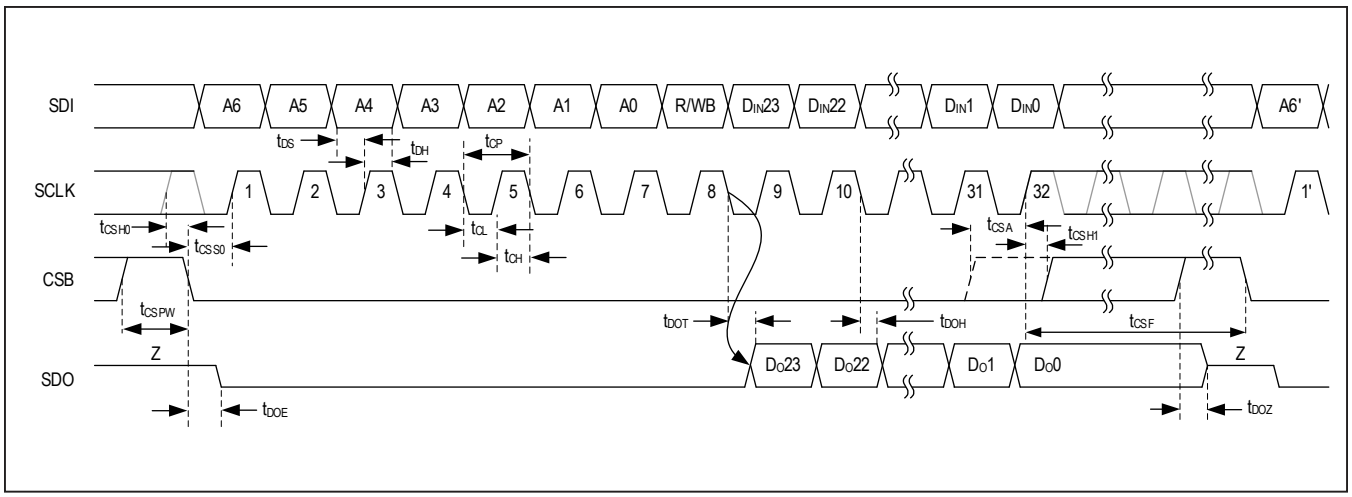


Figure 1a. SPI Timing Diagram

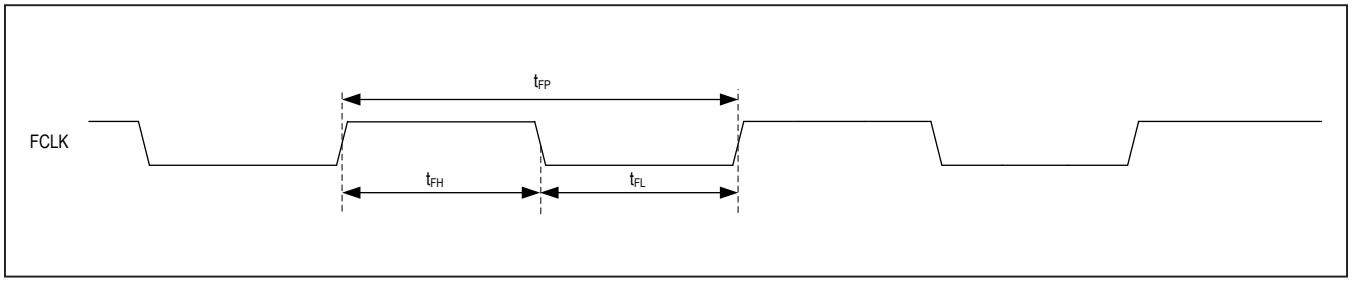
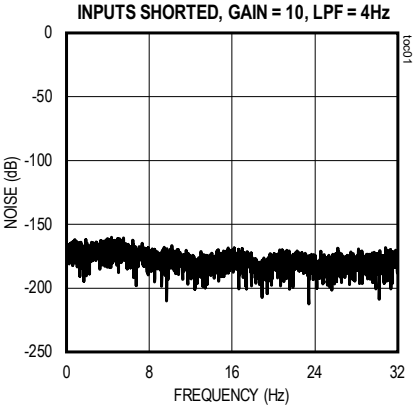


Figure 1b. FCLK Timing Diagram

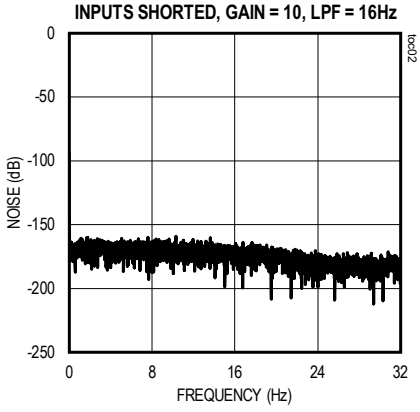
Typical Operating Characteristics

(V_{DVDD} = V_{AVDD} = 1.8V, V_{OVDD} = 2.5V, T_A = +25°C, unless otherwise noted.)

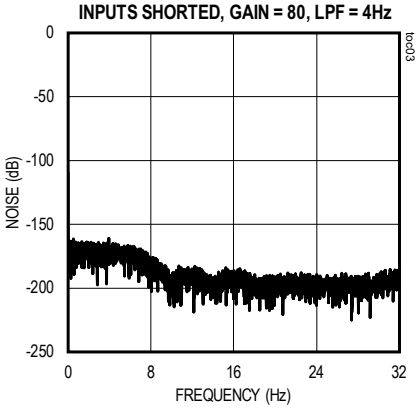
BIOZ NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 10, LPF = 4Hz



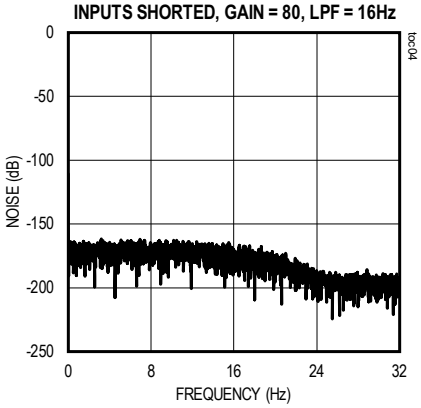
BIOZ NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 10, LPF = 16Hz



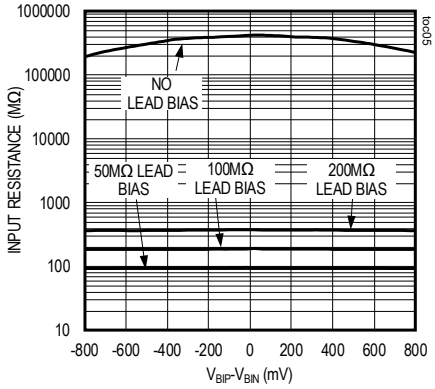
BIOZ NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 80, LPF = 4Hz



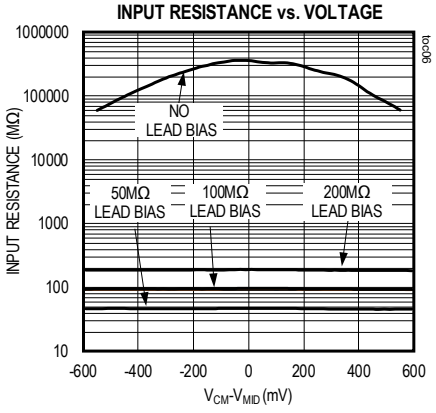
BIOZ NOISE SPECTRUM vs. FREQUENCY
INPUTS SHORTED, GAIN = 80, LPF = 16Hz



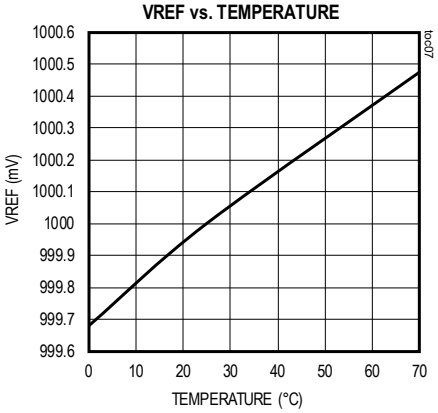
BIOZ DIFFERENTIAL INPUT
RESISTANCE vs. VOLTAGE



BIOZ COMMON-MODE
INPUT RESISTANCE vs. VOLTAGE



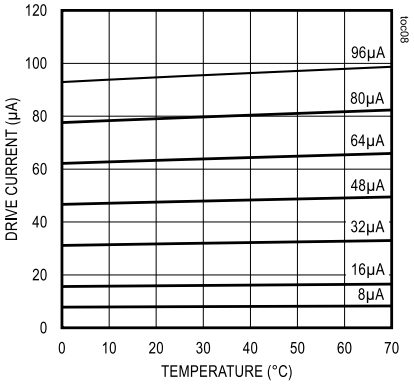
VREF vs. TEMPERATURE



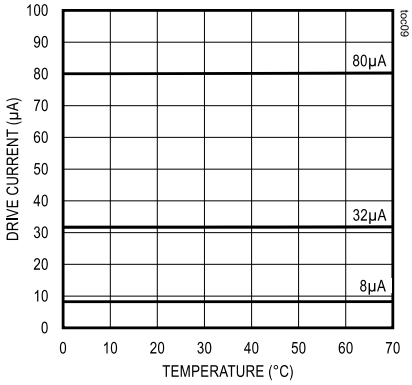
Typical Operating Characteristics (continued)

(V_{DVDD} = V_{AVDD} = 1.8V, V_{OVDD} = 2.5V, T_A = +25°C, unless otherwise noted.)

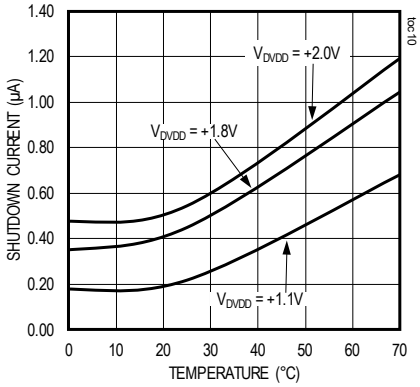
BIOZ DRIVE CURRENT vs. TEMPERATURE INTERNAL BIASING



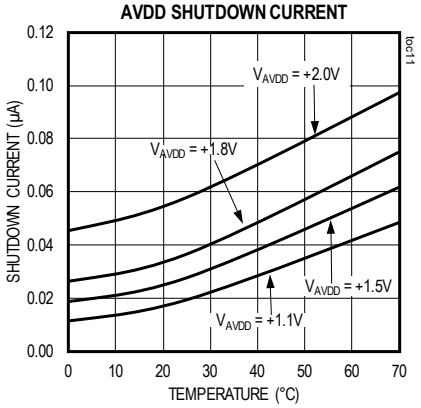
BIOZ DRIVE CURRENT vs. TEMPERATURE EXTERNAL BIASING



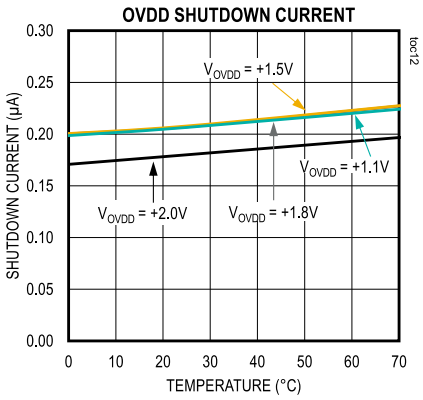
DVDD SHUTDOWN CURRENT



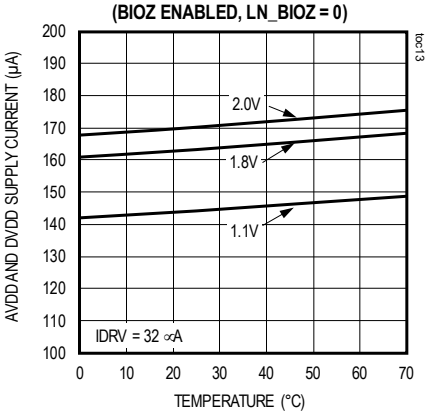
AVDD SHUTDOWN CURRENT



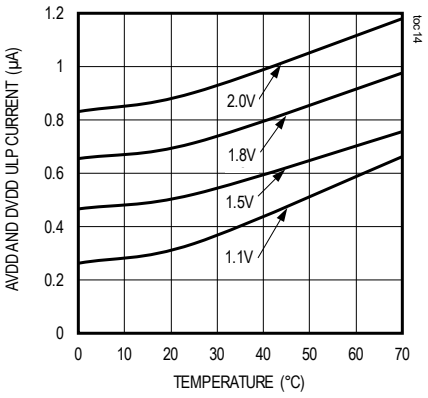
OVDD SHUTDOWN CURRENT



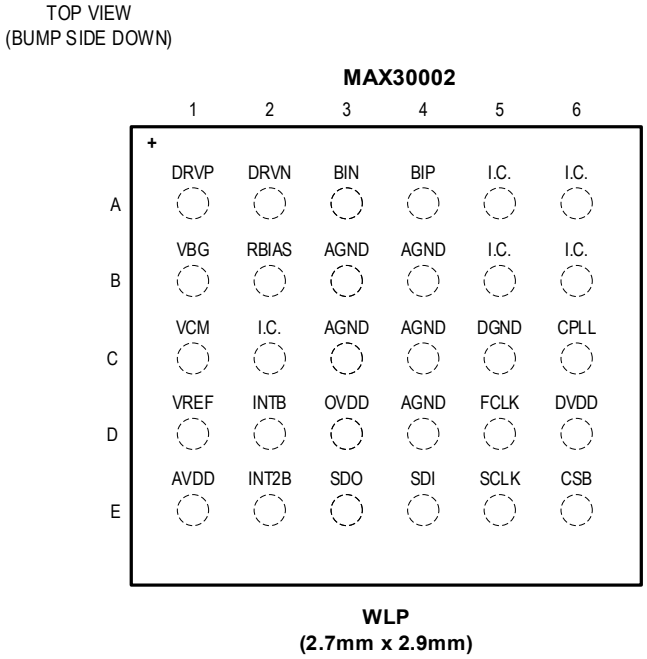
AVDD AND DVDD SUPPLY CURRENT vs. TEMPERATURE (BIOZ ENABLED, LN_BIOZ = 0)



AVDD AND DVDD ULP CURRENT vs. TEMPERATURE



Pin Configuration



WLP
(2.7mm x 2.9mm)

Pin Description

BUMP WLP	NAME	FUNCTION
A1	DRVP	Positive Output Current Source for Bio-Impedance Excitation. Requires a series capacitor between pin and electrode.
A2	DRVN	Negative Output Current Source for Bio-Impedance Excitation. Requires a series capacitor between pin and electrode.
A3	BIN	Bioimpedance Negative Input.
A4	BIP	Bioimpedance Positive Input.
A5, A6, B5, B6, C2	I.C.	Internally Connected. Connect to AGND.
B1	VBG	Bandgap Noise Filter Output. Connect a 1.0µF X7R ceramic capacitor between VBG and AGND.
B2	RBIAS	External Resistor Bias. Connect a low tempco resistor between RBIAS and AGND. If external bias generator is not used then RBIAS can be left floating.
B3, B4, C3, C4, D4	AGND	Analog Power and Reference Ground. Connect into the printed circuit board ground plane.
C1	VCM	Common Mode Buffer Output. Connect a 10µF X5R ceramic capacitor between VCM and AGND.

Pin Description (continued)

BUMP WLP	NAME	FUNCTION
C5	DGND	Digital Ground for Both Digital Core and I/O Pad Drivers. Recommended to connect to AGND plane.
C6	CPLL	PLL Loop Filter Input. Connect 1nF C0G ceramic capacitor between CPLL and AGND.
D1	VREF	ADC Reference Buffer Output. Connect a 10µF X7R ceramic capacitor between V_{REF} and AGND.
D2	INTB	Interrupt Output. INTB is an active-low status output. It can be used to interrupt an external device. INTB is three-stated when disabled.
D3	OVDD	Logic Interface Supply Voltage.
D5	FCLK	32.768kHz Clock Input. FCLK Controls the sampling of the internal sigma-delta converter and decimator and derives all the internal clocks.
D6	DVDD	Digital Core Supply Voltage. Connect to AVDD.
E1	AVDD	Analog Core Supply Voltage. Connect to DVDD.
E2	INT2B	Interrupt 2 Output. INT2B is an active-low status output. It can be used to interrupt an external device. INT2B is three-stated when disabled.
E3	SDO	Serial Data Output. SDO will change state on the falling edge of SCLK when CSB is low. SDO is three-stated when CSB is high.
E4	SDI	Serial Data Input. SDI is sampled into the device on the rising edge of SCLK when CSB is low.
E5	SCLK	Serial Clock Input. Clocks data in and out of the serial interface when CSB is low.
E6	CSB	Active-Low Chip-Select Input. Enables the serial interface.

Detailed Description

ESD Protection

BIP, BIN, DRVP, DRVN		IEC 61000-4-2 Contact Discharge (Note 8)	±8	kV
		IEC 61000-4-2 Air-Gap Discharge (Note 8)	±15	
		HMM (Human Metal Model)	±8	
All Other Pins		JEDEC JESD22-A114 HBM Transient Pulse	±2.5	kV

Note 8: ESD test performed with 1kΩ series resistor designed to withstand 8kV surge voltage.

BioZ Channel

Figure 2 illustrates the BioZ channel block diagram, excluding the ADC. The channel comprises an input MUX, a programmable analog high-pass filter, an instrumentation amplifier, a mixer, an anti-alias filter, and a programmable gain amplifier. The MUX includes several features such as ESD protection, EMI filtering, lead biasing, leads off checking, and ultra-low-power leads-on checking. The output of this analog channel drives a 20-bit Sigma-Delta ADC.

Input MUX

The BioZ input MUX shown in Figure 3 contains integrated ESD and EMI protection, DC leads off detect current sources and comparators, lead-on detect, series isolation switches, lead biasing, and a built-in programmable resistor load, for self test.

EMI Filtering and ESD Protection

EMI filtering of the BIP and BIN inputs consists of a single pole, low pass, differential, and common mode filter with the pole located at approximately 32MHz. The BIP and BIN inputs also have input clamps that protect the inputs from ESD events. The DRVP and DRVN outputs also feature ESD protection.

- ±8kV using the Contact Discharge method specified in IEC61000-4-2 ESD.
- ±15kV using the Air Gap Discharge method specified in IEC61000-4-2 ESD.
- ±8kV HMM

For IEC61000-4-2 ESD protection, use 1kΩ or larger series resistors on BIP, BIN, DRVP, and DRVN that are rated to withstand the appropriate surge voltages.

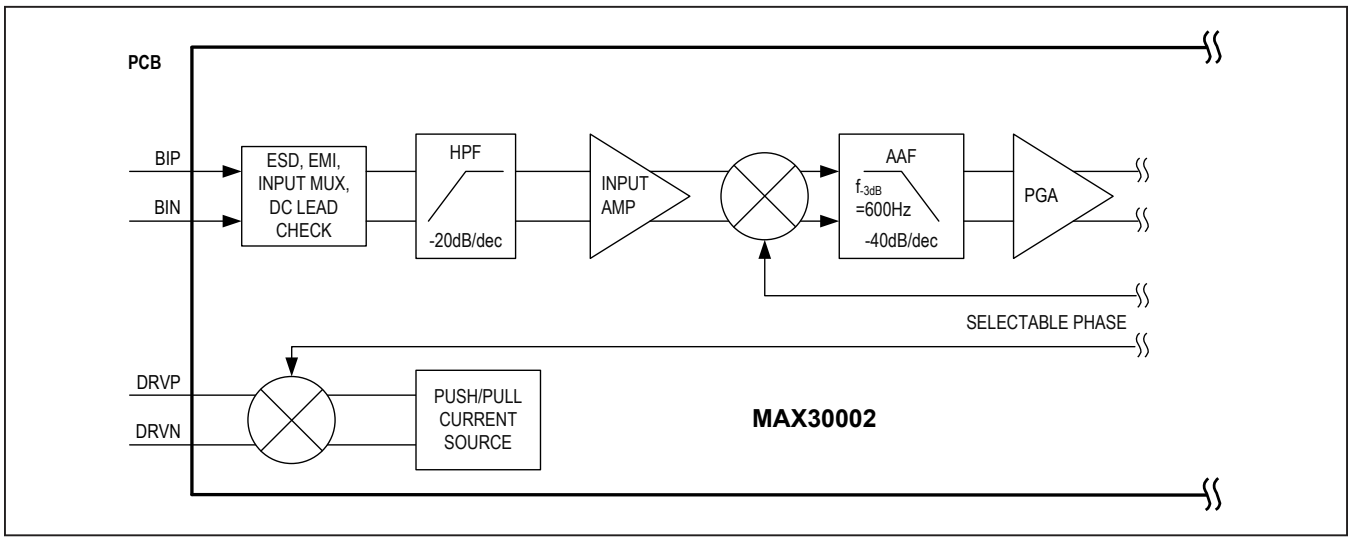


Figure 2. BioZ Channel Input Amplifier, Mixer, and PGA Excluding the ADC and Current Drive Output

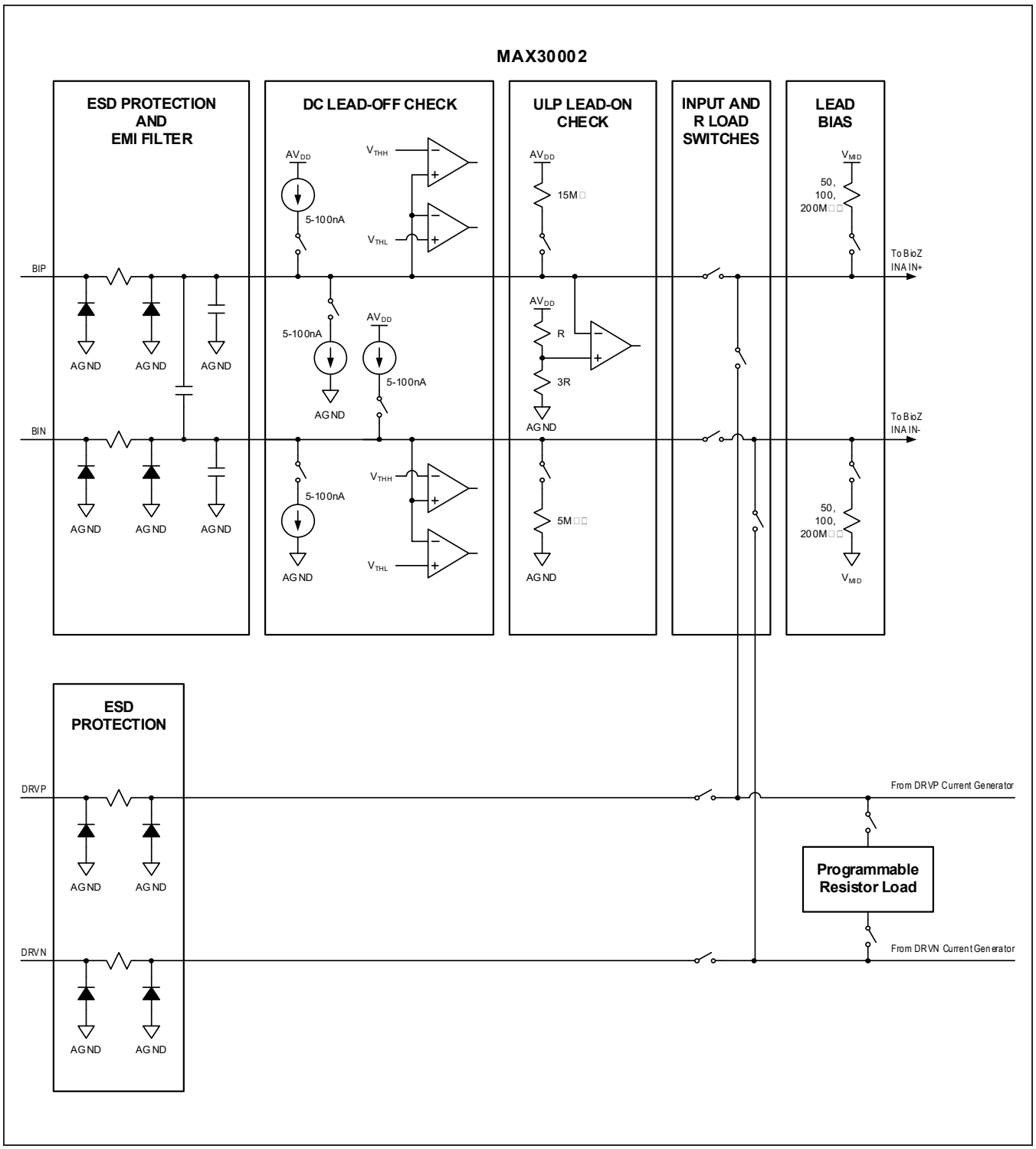


Figure 3. BioZ Input MUX

Leads-Off Detection and ULP Leads-On Detection

MAX30002 provides the capability of detecting lead off scenarios that involve two electrode and four electrode configurations through the use of digital threshold and analog threshold comparisons. There are three methods to detect lead-off for the BioZ channel. There is a compliance monitor for the current generator on the DRVP and DRVN pins detecting when the voltage on the pins is outside its operating range. The CGMON bit in the CNFG_BIOZ (0x18) register enables this function and the BCGMON, BCGMP, and BCGMN bits in the STATUS (0x01) register indicate if the DRVP and DRVN pins are out of compliance. There is a DC lead-off circuit on the BIP and BIN pins that sinks or sources a programmable DC current and window comparators with a programmable threshold to detect the condition. There is a digital AC lead-off detection monitoring the output of the BioZ ADC with programmable under and overvoltage levels performing a digital comparison. The EN_BLOFF bit in the CNFG_GEN (0x10) register enables this function and the BLOFF_HI_IT[7:0] and BLOFF_LO_IT[7:0] bits in the MNGR_DYN (0x05) register sets the digital threshold for detection. Refer to Table 1 for lead off conditions and register settings to allow detection. The 0nA setting can also be used with the V_{MID} ±300mV threshold to monitor the input compliance of the INA when DC leads-off detection is not needed.

The ULP lead-on detect operates by pulling BIN low with a pulldown resistance larger than 5MΩ and pulling BIP high with a pullup resistance larger than 15MΩ. A low-power comparator determines if BIP is pulled below a predefined threshold that occurs when both electrodes make contact with the body. When the impedance between BIP and BIN is less than 40MΩ, the LONINT status bit is asserted, and when the interrupt is enabled on either the INTB or INT2B pin, will alert the µC to a leads-on condition.

Table 1. BioZ Lead Off Detection Configurations

CONFIGURATION	CONDITION	DRVP/N	BIP/N	MEASURED SIGNAL	REGISTER SETTING TO DETECT
Two-Electrode (Shared DRV/BI)	1 Electrode Off	Rail to Rail	Rail to Rail	Rail to Rail (Saturated Inputs)	CNFG_GEN (0x10), EN_BLOFF[1:0] = 10 or 11 MNGR_DYN (0x05), BLOFF_HI_IT[7:0]
Four-Electrode (Force/Sense)	1 DRV Electrode Off, Large Body Coupling	Rail to Rail	Normal	½ Signal	CNFG_BIOZ (0x18), CGMON = 1
	1 DRV Electrode Off, Small Body Coupling	Rail to Rail	Rail to Rail	Rail to Rail (Saturated Inputs)	CNFG_GEN (0x10), EN_BLOFF[1:0] = 10 or 11 MNGR_DYN (0x05), BLOFF_HI_IT[7:0]
	1 BI (sense) Electrode Off	Normal	Floating	½ Signal	CNFG_GEN (0x10), EN_DCLOFF = 10
	Both BIP/N (sense) Electrodes Off	Normal	Floating	No Signal	CNFG_GEN (0x10), EN_BLOFF[1:0] = 01 or 11 MNGR_DYN (0x05), BLOFF_LO_IT[7:0]
	1 DRV and 1 BI Electrode Off	Rail to Rail	Wide Swing, Dependent on Body Coupling	Rail to Rail	CNFG_GEN (0x10), EN_BLOFF[1:0] = 10 or 11 MNGR_DYN (0x05), BLOFF_HI_IT[7:0]

Lead Bias

The MAX30002 limits the BIP and BIN DC input common mode range to V_{MID} ±150mV at V_{AVDD} = 1.1V or V_{MID} ±550mV (typ) at V_{AVDD} = 1.8V. This range can be maintained either through external/internal lead-biasing.

Internal DC lead-biasing consists of 50MΩ, 100MΩ, or 200MΩ selectable resistors to V_{MID} that drive the electrodes within the input common mode requirements of the BioZ channel and can drive the connected body to the proper common mode voltage level. See the EN_RBIAS[1:0], RBIASV[1:0], RBIASP, and RBIASN bits in the CNFG_GEN (0x10) register to select a configuration.

The common-mode voltage, V_{CM}, can optionally be used as a body bias to drive the body to the common-mode voltage by connecting V_{CM} to a separate electrode on the body through a 200kΩ or higher resistor to limit current into the body according to IEC 60601-1:2005, 8.7.3. If this is utilized then the internal lead bias resistors to V_{MID} can be disabled.

Programmable Resistive Load

The programmable resistive load on the DRVP/DRVN pins allows a built in self-test of the current generator (CG) and the entire BioZ channel. Refer to Figure 4 for implementation details.

Nominal resistance can be varied between 5kΩ and 625Ω. The modulation resistance is used to switch the load resistance between R_{NOM} and (R_{NOM} - R_{MOD}) at the selected modulation rate. The modulation resistance is dependent on the nominal resistance value with resolution of 247.5mΩ to 2.96Ω at the largest nominal resistance (5kΩ) and 15.3mΩ to 46.3mΩ with the smallest nominal resistance (625Ω). Refer to Table 2 for a complete listing of nominal and modulated resistor values. Modulation rate can be programmed between 62.5mHz to 4Hz.

See register CNFG_BMUX (0x17) to select the configuration for modulation rate and resistor value.

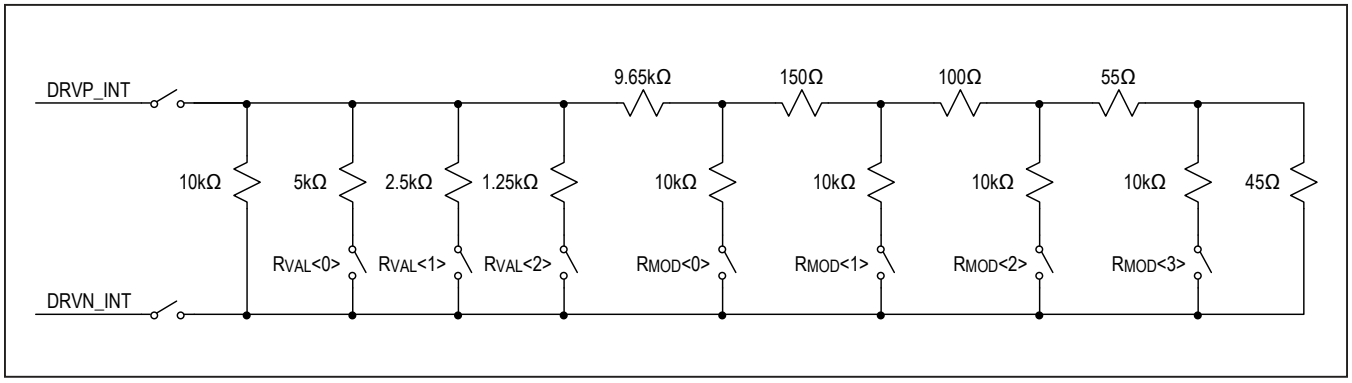


Figure 4. Programmable Resistive Load Topology

Table 2. Programmable Resistive Load Values

R_{NOM} (Ω)	R_{MOD} (mΩ)	R_{VAL}			R_{MOD}			
		<2>	<1>	<0>	<3>	<2>	<1>	<0>
5000.000	-	0	0	0	0	0	0	0
	2960.7	0	0	0	0	0	0	1
	980.6	0	0	0	0	0	1	0
	247.5	0	0	0	0	1	0	0
2500.000	—	0	0	1	0	0	0	0
	740.4	0	0	1	0	0	0	1
	245.2	0	0	1	0	0	1	0
	61.9	0	0	1	0	1	0	0
1666.667	—	0	1	0	0	0	0	0
	329.1	0	1	0	0	0	0	1
	109.0	0	1	0	0	0	1	0
	27.5	0	1	0	0	1	0	0
1250.000	—	0	1	1	0	0	0	0
	185.1	0	1	1	0	0	0	1
	61.3	0	1	1	0	0	1	0
1000.000	—	1	0	0	0	0	0	0
	118.5	1	0	0	0	0	0	1
	39.2	1	0	0	0	0	1	0
833.333	—	1	0	1	0	0	0	0
	82.3	1	0	1	0	0	0	1
	27.2	1	0	1	0	0	1	0
714.286	—	1	1	0	0	0	0	0
	60.5	1	1	0	0	0	0	1
	20.0	1	1	0	0	0	1	0
625.000	—	1	1	1	0	0	0	0
	46.3	1	1	1	0	0	0	1
	15.3	1	1	1	0	0	1	0

Current Generator

The current generator provides square-wave modulating differential current that is AC injected into the body via pins DRVP and DRVN with the bio-impedance sensed differentially through pins BIP and BIN. Two and four electrode configurations are supported for typical wet and dry electrode impedances.

Current amplitudes between 8μA_{PK} to 96μA_{PK} are selectable with current injection frequencies between 125Hz and 131.072kHz in power of two increments. See register CNFG_BIOZ (0x18) for configuration selections.

Current amplitude should be chosen so as not exceed 90mV_{P-P} at the BIP and BIN pins based on the network impedance at the current injection frequency. A 47nF DC blocking capacitor is required between both DRVP and DRVN and their respective electrodes. The current generator also includes a phase offset adjustment, which delays the drive current modulator with respect to the input mixer. The phase can be adjusted in 11.25° increments from 0° to 168.75° for injection frequencies up to f_{MSTR}. For injection frequencies of 2 x f_{MSTR} and 4 x f_{MSTR}, the phase resolution is reduced to 22.5° and 45°, respectively; see CNFG_BIOZ (0x18) for details.

Converting BioZ Samples to Ohms

BioZ samples are recorded in a 20-bit left-justified two's complement format. After converting to signed magnitude format, BioZ is calculated by the following equation:

$$BioZ\ (\Omega) = ADC \times V_{REF} / (2^{19} \times BIOZ\_CGMAG \times BIOZ\_GAIN)$$

ADC is the ADC counts in signed magnitude format, V_{REF} is 1V (typ; see *Electrical Characteristics*), BIOZ_CGMAG is 8 to 96 x 10^{-6}A, and BIOZ_GAIN is 10V/V, 20V/V, 40V/V, or 80V/V. BIOZ_CGMAG and BIOZ_GAIN are set in CNFG_BIOZ (0x18).

Current Selection and Resolution Calculation Example 1 (Two Terminal with Common Protection)

Selection of the appropriate current is accomplished by first calculating the resistive component of the network impedance at the injection frequency. Worst case electrode impedances should be used.

Given Figure 5 and a current injection frequency of 80kHz, the resistive component of the network impedance is:

$$R_{BODY} + 2R_{P1} + 2R_{P2} + 2R_S + Re\left\{\frac{2R_E}{1 + j\omega R_E C_E}\right\} = 2.7k\Omega$$

where R_{BODY} = 100Ω, R_{P1} = 1kΩ, R_{P2} = 200Ω, R_S = 100Ω, R_E = 1MΩ, C_E = 5nF. The maximum current injection is the maximum AC input differential range (90mV$_{PK}$) divided by the network impedance (2.7kΩ) or 33.3μA$_{PK}$. The closest selectable lower value is 32μA$_{PK}$.

Given the current injection value and the channel bandwidth (refer to register CNFG_BIOZ (0x18) for digital LPF selection) the resolvable impedance can be calculated by dividing the appropriate input referred noise by the current injection value. For example, with a bandwidth of 4Hz, the input referred noise with a gain of 20V/V is 0.16μV$_{RMS}$ or 1.1μV$_{P-P}$. The resolvable impedance is, therefore, 1.1μV$_{P-P}$/32μA$_{PK}$ = 34mΩ$_{P-P}$ or 5mΩ$_{RMS}$.

Current Selection and Resolution Calculation Example 2 (Four Terminal)

Selection of the appropriate current is accomplished by first calculating the resistive component of the network impedance at the injection frequency. Worst case electrode impedances should be used.

Given Figure 6 and a current injection frequency of 80kHz, the resistive component of the network impedance is:

$$R_{BODY} + 2R_{DP1} + 2R_{DP2} + 2R_S + Re\left\{\frac{2R_E}{1 + j\omega R_E C_E}\right\} = 2.7k\Omega$$

where R_{BODY} = 100Ω, R_{DP1} = 1kΩ, R_{DP2} = 200Ω, R_S = 100Ω, R_E = 1MΩ, C_E = 5nF. The maximum current injection is the maximum DRVP/N Compliance Voltage (V_{DD}-0.5V = 0.6V for V_{DD} = 1.1V) divided by the network impedance (2.7kΩ) or 222.2μA$_{PK}$. The closest selectable lower value is 96μA$_{PK}$.

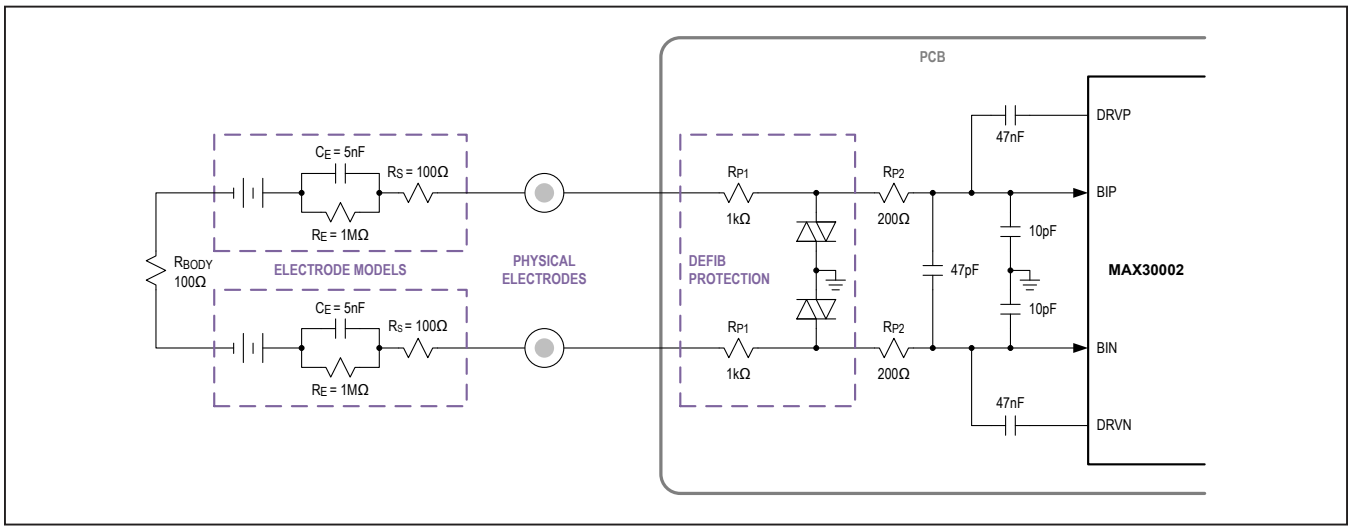


Figure 5. Example Configuration – Two Terminal with Common Protection

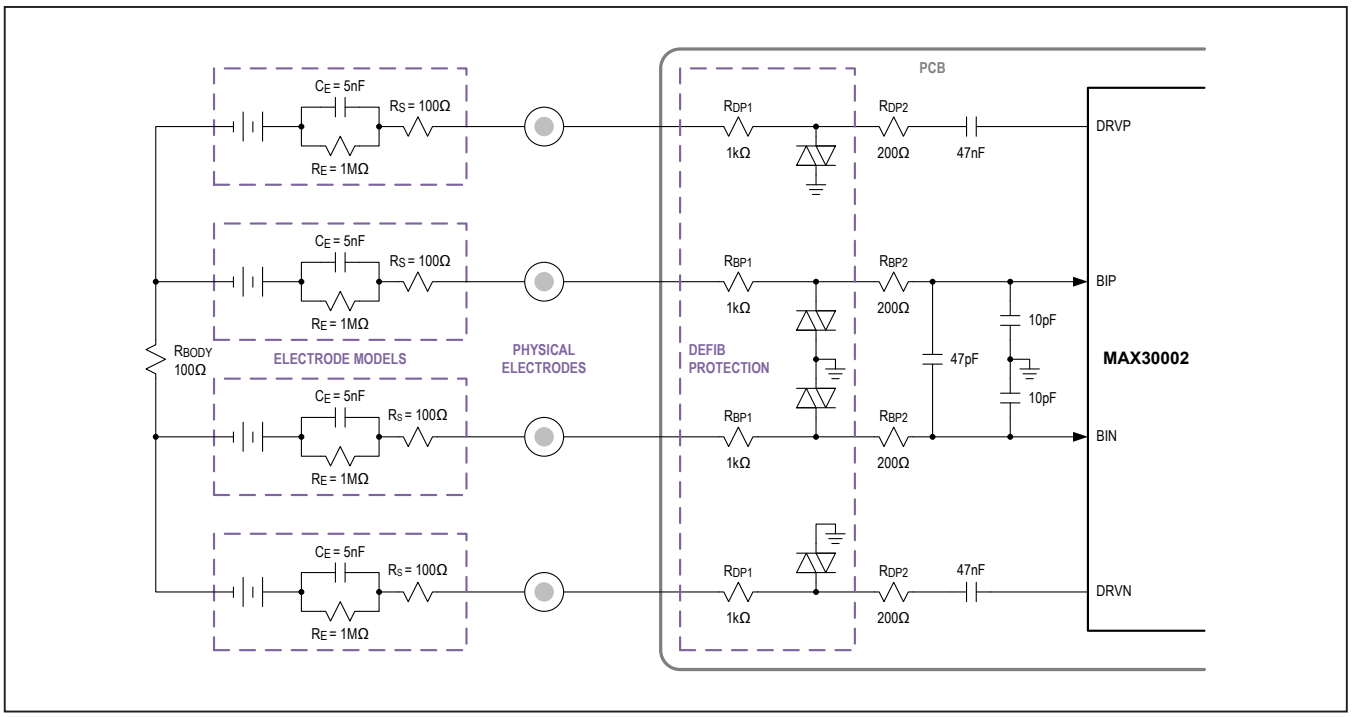


Figure 6. Example Configuration—Four Terminal

Given the current injection value and the channel bandwidth (refer to register CNFG_BIOZ (0x18) for digital LPF selection) the resolvable impedance can be calculated by dividing the appropriate input referred noise by the current injection value. For example, with a bandwidth of 4Hz, the input referred noise with a gain of 40V/V is $0.12\mu V_{RMS}$ or $0.78\mu V_{P-P}$. The resolvable impedance is therefore $0.78\mu V_{P-P}/96\mu A_{PK} = 8m\Omega_{P-P}$ or $1.2m\Omega_{RMS}$.

Filter Section

The filter section consists of an FIR decimation filter to to convert the ADC sample rate to the final data rate, followed by a programmable IIR and FIR filter to implement HPF and LPF selections, respectively.

The high-pass filter options include a fourth-order IIR Butterworth filter with a 0.05Hz or 0.5Hz corner frequency along with a pass through setting for DC coupling. Lowpass filter options include a 12-tap linear phase (constant group delay) FIR filter with 4Hz, 8Hz, or 16Hz corner frequencies. See register CNFG_BIOZ (0x18) to configure the filters. Table 3 illustrates the BioZ latency in samples and time for each ADC data rate.

Noise Measurements

Table 4 shows the noise performance of the BioZ channel of MAX30002 referred to the BioZ inputs.

Reference and Common Mode Buffer

The MAX30002 features internally generated reference voltages. The bandgap output (V_{BG}) pin requires an external 1.0µF capacitor to AGND and the reference output (V_{REF}) pin requires a 10µF external capacitor to AGND for compensation and noise filtering.

A common-mode buffer is provided to buffer 650mV which is used to drive common mode voltages for internal blocks. Use a 10µF external capacitor between V_{CM} to AGND to provide compensation and noise filtering. The common-mode voltage, V_{CM}, can optionally be used as a body bias to drive the body to the common-mode voltage by connecting V_{CM} to a separate electrode on the body through a 200kΩ or higher resistor to limit current into the body according to IEC 60601-1:2005, 8.7.3. If this is utilized then the internal lead bias resistors to V_{MID} may be disabled if the input signals are within the common-mode input range.

Table 3. BioZ Latency in Samples and Time as a Function of BioZ Data Rate and Decimation

BIOZ CHANNEL SETTINGS			LATENCY			
INPUT SAMPLE RATE (Hz)	OUTPUT DATA RATE (sps)	DECIMATION RATIO	WITHOUT LPF (INPUT SAMPLES)	WITH LPF (INPUT SAMPLES)	WITHOUT LPF(ms)	WITH LPF (ms)
32,768	64	512	3,397	6,469	103.668	197.418
32,000	62.5	512	3,397	6,469	106.156	202.156
32,000	50	640	5,189	9,029	162.156	282.156
31,968	49.95	640	5,189	9,029	162.319	282.439
32,768	32	1,024	7,557	13,701	230.621	418.121
32,000	31.25	1,024	7,557	13,701	236.156	428.156
32,000	25	1,280	9,605	17,285	300.156	540.156
31,968	24.975	1,280	9,605	17,285	300.457	540.697

Table 4. BioZ Channel Noise Performance

GAIN	BANDWIDTH	NOISE		SNR	ENOB
V/V	Hz	μV_{RMS}	μV_{P-P}	dB	Bits
10	4	0.23	1.55	101.6	16.6
	8	0.28	1.87	100.0	16.3
	16	0.35	2.34	98.0	16.0
20	4	0.16	1.10	104.9	17.1
	8	0.19	1.27	103.4	16.9
	16	0.26	1.68	100.9	16.5
40	4	0.12	0.78	107.6	17.6
	8	0.16	1.07	104.9	17.1
	16	0.22	1.48	102.0	16.7
80	4	0.11	0.72	108.3	17.7
	8	0.15	1.01	105.3	17.2
	16	0.21	1.42	102.4	16.7

SNR = 20log(V_{IN}(RMS)/V_N(RMS)), ENOB = (SNR – 1.76)/6.02

V_{INP-P} = 100mV, V_{INRMS} = 35.4mV for a gain of 10V/V. The input amplitude is reduced accordingly for high gain settings.

SPI Interface Description

32 Bit Normal Mode Read/Write Sequences

The MAX30002 interface is SPI/QSPI/Micro-wire/DSP compatible. The operation of the SPI interface is shown in Figure 1a. Data is strobed into the MAX30002 on SCLK rising edges. The device is programmed and accessed by a 32 cycle SPI instruction framed by a CSB low interval. The content of the SPI operation consists of a one byte command word (comprised of a seven bit address and a Read/Write mode indicator, i.e., A[6:0] + R/$\overline{W}$) followed by a three-byte data word. The MAX30002 is compatible with CPOL = 0/CPHA = 0 and CPOL = 1/CPHA = 1 modes of operation.

Write mode operations will be executed on the 32nd SCLK rising edge using the first four bytes of data available. In write mode, any data supplied after the 32nd SCLK rising edge will be ignored. Subsequent writes require CSB to de-assert high and then assert low for the next write command. In order to abort a command sequence, the rise of CSB must precede the updating (32nd) rising-edge of SCLK, meeting the t_{CSA} requirement.

Read mode operations will access the requested data on the 8th SCLK rising edge, and present the MSB of the requested data on the following SCLK falling edge, allowing the µC to sample the data MSB on the 9th SCLK rising edge. Configuration, Status, and FIFO data are all available via normal mode read back sequences. If more than 32 SCLK rising edges are provided in a normal read sequence then the excess edges will be ignored and the device will read back zeros.

If accessing the STATUS register or the BIOZ FIFO memory, all interrupt updates will be made and the internal FIFO read pointer will be incremented in response to the 30th SCLK rising edge, allowing for internal synchronization operations to occur. See the data tag structures used within the FIFO for means of detecting end-of-file (EOF) samples, invalid (empty samples) and other aides for efficiently using and managing normal mode read back operations.

Burst Mode Read Sequence

The MAX30002 provides commands to read back the BIOZ FIFO memory in a burst mode to increase data transfer efficiency. Burst mode uses different register addresses than the normal read sequence register addresses. The first 32 SCLK cycles operate exactly as described for the normal mode. If the µC continues to provide SCLK edges beyond the 32nd rising edge, the MSB of the next available FIFO word will be presented on the next falling SCLK edge, allowing the µC to sample the MSB of the next word on the 33rd SCLK rising edge. Any affected interrupts and/or FIFO read pointers will be incremented in response to the (30+nx24)th SCLK rising edge where n is an integer starting at 0. (i.e., on the 30th, 54th, and 78th SCLK rising-edges for a three-word, burst-mode transfer).

This mode of operation will continue for every 24 cycle sub frame, as long as there is valid data in the FIFO. See the data tag structures used within each FIFO for means of detecting end-of-file (EOF) samples, invalid (empty samples) and other aides for efficiently using and managing burst mode read back operations.

There is no burst mode equivalent in write mode.

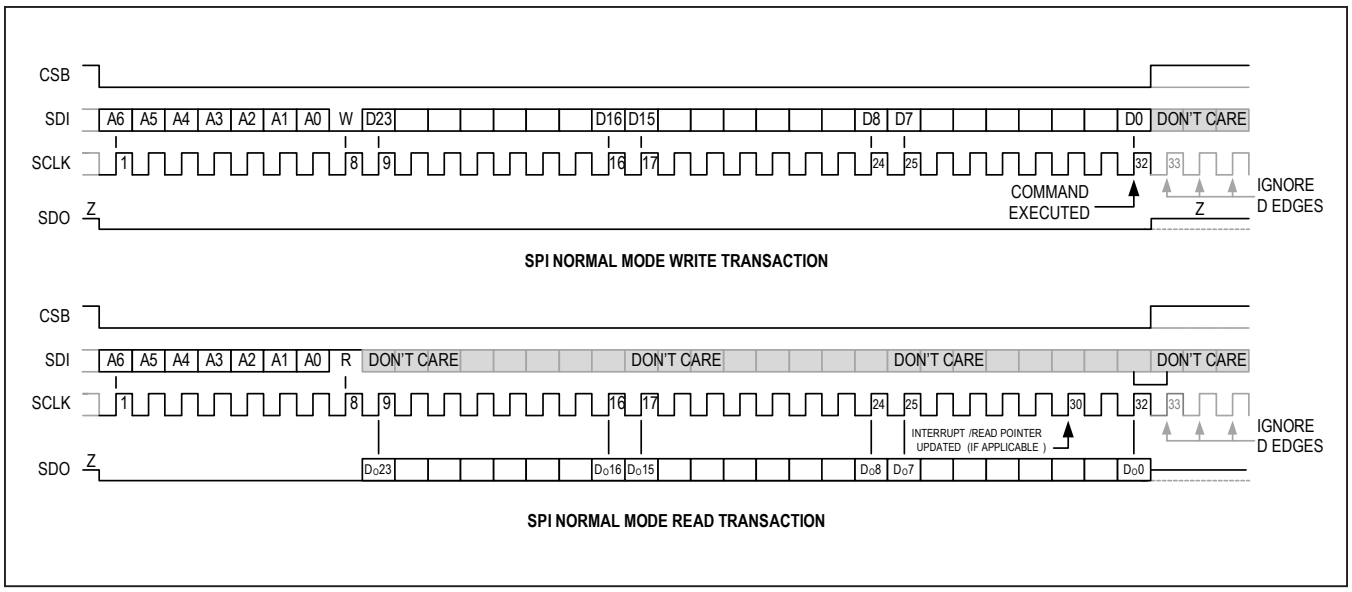


Figure 7. SPI Normal Mode Transaction Diagram

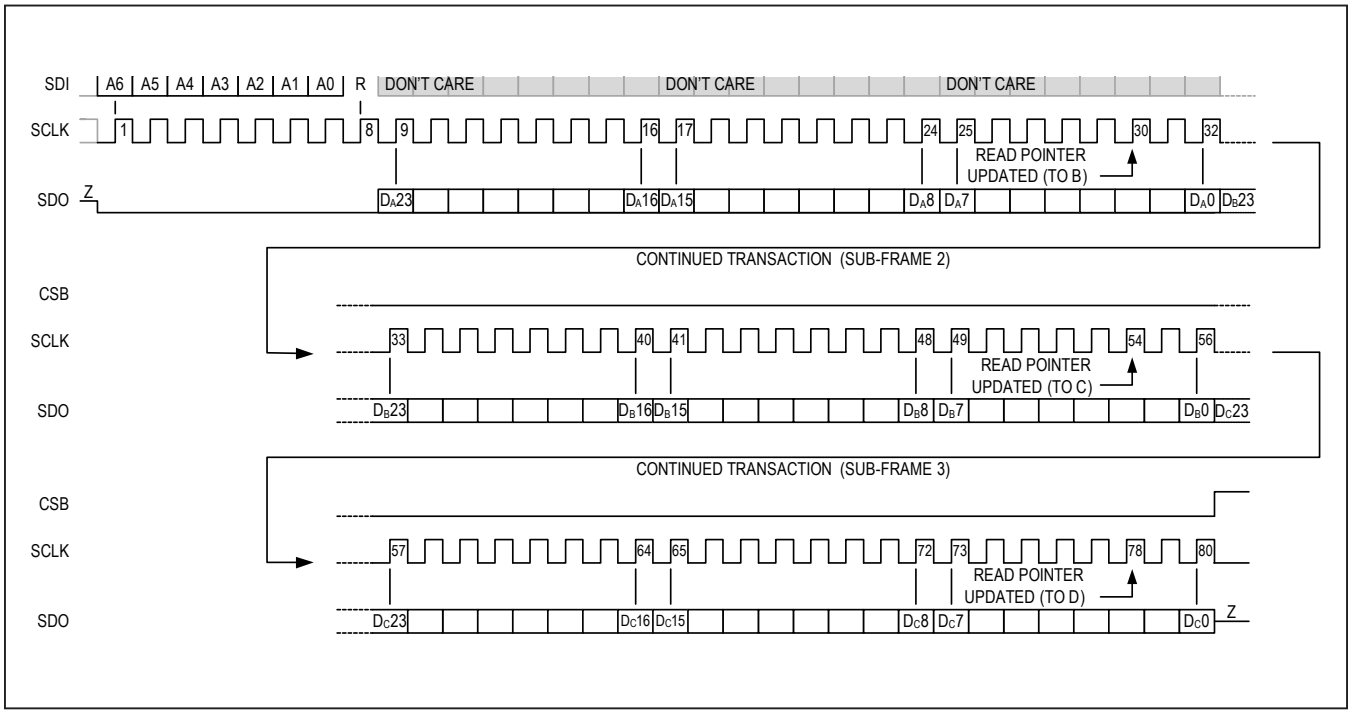


Figure 8. SPI Burst Mode Read Transactions Diagram

User Command and Register Map

REG [6:0]	NAME	R/W MODE	DATA INDEX							
			23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0
0x00	NO-OP	R/W	x / x / x	x / x / x	x / x / x	x / x / x	x / x / x	x / x / x	x / x / x	x / x / x
0x01	STATUS	R	x	x	x	DCLOFFINT	BINT	BOVF	BOVER	BUNDR
			BCGMON	x	x	x	LONINT	x	SAMP	PLLINT
			x	x	BCGMP	BCGMN	LDOFF_PH	LDOFF_PL	LDOFF_NH	LDOFF_NL
0x02 0x03	EN_INT EN_INT2	R/W	x	x	x	EN_DCLOFFINT	EN_BINT	EN_BOVF	EN_BOVER	EN_BUNDR
			EN_BCGMON	x	x	x	EN_ LONINT	x	EN_SAMP	EN_ PLLINT
			x	x	x	x	x	x	INTB_TYPE[1:0]	
0x04	MNGR_ INT	R/W	x	x	x	x	x	BFIT[2:0]		
			x	x	x	x	x	x	x	x
			x	x	x	x	CLR_PEDGE	CLR_ SAMP	SAMP_IT[1:0]	
0x05	MNGR_ DYN	R/W	x	x	x	x	x	x	x	x
			BLOFF_HI_IT[7:0]							
			BLOFF_LO_IT[7:0]							
0x08	SW_RST	W	Data Required for Execution = 0x000000							
0x09	SYNCH	W	Data Required for Execution = 0x000000							
0x0A	FIFO_ RST	W	Data Required for Execution = 0x000000							
0x0F	INFO	R	0	1	0	1	REV_ID[3:0]			
			x	x	1	0	x	x	x	x
			x	x	x	x	x	x	x	x
0x10	CNFG_ GEN	R/W	EN_ULP_LON[1:0]		FMSTR[1:0]		x	EN_BIOZ	x	x
			EN_BLOFF[1:0]		EN_DCLOFF[1:0]		IPOL	IMAG[2:0]		
			VTH[1:0]		EN_RBIAS[1:0]		RBIASV[1:0]		RBIASP	RBIASN
0x17	CNFG_ BMUX	R/W	x	x	OPENP	OPENN	CALP_SEL[1:0]		CALN_SEL[1:0]	
			x	x	CG_MODE[1:0]		EN_BIST	RNOM[2:0]		
			x	RMOD[2:0]			x	x	FBIST[1:0]	
0x18	CNFG_ BIOZ	R/W	RATE	AHPF[2:0]			EXT_RBIAS	LN_BIOZ	GAIN[1:0]	
			DHPF[1:0]		DLPF[1:0]		FCGEN[3:0]			
			CGMON	CGMAG[2:0]			PHOFF[3:0]			
0x22	BIOZ_ FIFO_ BURST	R+	BIOZ FIFO Burst Mode Read Back				See FIFO Description for details			
0x23	BIOZ_ FIFO	R	BIOZ FIFO Normal Mode Read Back				See FIFO Description for details			
0x7F	NO-OP	R/W	x/x/x	x/x/x	x/x/x	x/x/x	x/x/x	x/x/x	x/x/x	x/x/x

Note: *R/W Mode R+ denotes burst mode.*

x = Don't Care

Register Description

NO_OP (0x00 and 0x7F) Registers

No Operation (NO_OP) registers are read-write registers that have no internal effect on the device. If these registers are read back, DOUT remains zero for the entire SPI transaction. Any attempt to write to these registers is ignored without impact to internal operation.

STATUS (0x01) Register

STATUS is a read-only register that provides a comprehensive overview of the current status of the device. The first two bytes indicate the state of all interrupt bits (regardless of whether interrupts are enabled in registers EN_INT (0x02) or EN_INT2 (0x03)). All interrupt bits are active high. The last byte includes detailed status information for conditions associated with the other interrupt bits.

Table 5. STATUS (0x01) Register Map

REG	NAME	R/W	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0
0x01	STATUS	R	x	x	x	DCLOFFINT	BINT	BOVF	BOVER	BUNDR
			BCGMON	x	x	x	LONINT	x	SAMP	PLLINT
			x	x	BCGMP	BCGMN	LDOFF_PH	LDOFF_PL	LDOFF_NH	LDOFF_NL

Table 6. Status (0x01) Register Meaning

INDEX	NAME	MEANING
D[20]	DCLOFFINT	DC Lead-Off Detection Interrupt. Indicates that the MAX30002 has determined it is in a BioZ leads off condition (as selected in CNFG_GEN) for more than 90ms. Remains active as long as the leads-off condition persists, then held until cleared by STATUS read back (32nd SCLK).
D[19]	BINT	BIOZ FIFO Interrupt. Indicates BIOZ records meeting/exceeding the BIOZ FIFO Interrupt Threshold (BFIT) are available for read back. Remains active until BIOZ FIFO is read back to the extent required to clear the BFIT condition.
D[18]	BOVF	BIOZ FIFO Overflow. Indicates the BIOZ FIFO has overflowed and the data record has been corrupted. Remains active until a FIFO Reset (recommended) or SYNCH operation is issued.
D[17]	BOVER	BIOZ Over Range. Indicates the BIOZ output magnitude has exceeded the BIOZ High Threshold (BLOFF_HI_IT) for at least 100ms, recommended for use in 2 and 4 electrode BIOZ Lead Off detection. Remains active as long as the condition persists, then held until cleared by STATUS read back (32nd SCLK).
D[16]	BUNDR	BIOZ Under Range. Indicates the BIOZ output magnitude has been bounded by the BIOZ Low Threshold (BLOFF_LO_IT) for at least 1.7 seconds, recommended for use in 4 electrode BIOZ Lead Off detection. Remains active as long as the condition persists, then held until cleared by STATUS read back (32nd SCLK).
D[15]	BCGMON	BIOZ Current Generator Monitor. Indicates the DRVP and/or DRVN current generator has been in a Lead Off condition for at least 128ms, recommended for use in 4 electrode BIOZ Lead Off detection. Remains active as long as the condition persists, then held until cleared by STATUS read back (32nd SCLK).

Table 6. Status (0x01) Register Meaning (continued)

INDEX	NAME	MEANING
D[11]	LONINT	Ultra-Low Power (ULP) Leads-On Detection Interrupt. Indicates that the MAX30002 has determined it is in a leads-on condition (as selected in CNFG_GEN). LONINT is asserted whenever EN_ULP_LON[1:0] in register CNFG_GEN is set to either 01 or 10 to indicate that the ULP leads on detection mode has been enabled. The STATUS register has to be read back once after ULP leads on detection mode has been activated to clear LONINT and enable leads on detection. LONINT remains active while the leads-on condition persists, then held until cleared by STATUS read back (32nd SCLK).
D[9]	SAMP	Sample Synchronization Pulse. Issued on the BioZ base-rate sampling instant, for use in assisting µC monitoring and synchronizing other peripheral operations and data, generally recommended for use as a dedicated interrupt. Frequency is selected by SAMP_IT[1:0], see MNGR_INT for details. Clear behavior is defined by CLR_SAMP, see MNGR_INT for details.
D[8]	PLLINT	PLL Unlocked Interrupt. Indicates that the PLL has not yet achieved or has lost its phase lock. PLLINT will only be asserted when the PLL is powered up and active (BIOZ Channel enabled). Remains asserted while the PLL unlocked condition persists, then held until cleared by STATUS read back (32nd SCLK).
D[5]	BCGMP	BIOZ Current Generator Monitor Positive Output. Indicates the DRVP current generator has been in a Lead Off condition for at least 128ms. This is not strictly an interrupt bit, but is a detailed status bit, covered by the BCGMON interrupt bit.
D[4]	BCGMN	BIOZ Current Generator Monitor Negative Output. Indicates the DRVN current generator has been in a Lead Off condition for at least 128ms. This is not strictly an interrupt bit, but is a detailed status bit, covered by the BCGMON interrupt bit.
D[3]	LDOFF_PH	DC Lead Off Detection Detailed Status. Indicates that the MAX30002 has determined (as selected by CNFG_GEN): BIP is above the high threshold (V_{THH}), BIP is below the low threshold (V_{THL}), BIN is above the high threshold (VT_{HH}), BIN is below the low threshold (V_{THL}), respectively. Remains active as long as the leads-off detection is active and the leads-off condition persists, then held until cleared by STATUS read back (32nd SCLK). LDOFF_PH to LDOFF_NL are detailed status bits that are asserted at the same time as DCLOFFINT.
D[2]	LDOFF_PL	
D[1]	LDOFF_NH	
D[0]	LDOFF_NL	

EN_INT (0x02) and EN_INT2 (0x03) Registers

EN_INT and EN_INT2 are read/write registers that govern the operation of the INTB output and INT2B output, respectively. The first two bytes indicate which interrupt input bits are included in the interrupt output OR term (ex. a one in an EN_INT register indicates that the corresponding input bit is included in the INTB interrupt output OR term). See the STATUS register for detailed descriptions of the interrupt bits. The power-on reset state of all EN_INT bits is 0 (ignored by INT).

EN_INT and EN_INT2 can also be used to mask persistent interrupt conditions in order to perform other interrupt-driven operations until the persistent conditions are resolved.

INTB_TYPE[1:0] allows the user to select between a CMOS or an open-drain NMOS mode INTB output. If using open-drain mode, an option for an internal 125kΩ pullup resistor is also offered.

All INTB and INT2B types are active-low (INTB low indicates the device requires servicing by the µC); however, the open-drain mode allows the INTB line to be shared with other devices in a wired-or configuration.

In general, it is suggested that INT2B be used to support specialized/dedicated interrupts of use in specific applications, such as the self-clearing versions of SAMP or RRINT.

Table 7. EN_INT (0x02) and EN_INT2 (0x03) Register Maps

REG	NAME	R/W	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0
0x02 0x03	EN_INT EN_INT2	R/W	x	x	x	EN_DCL OFFINT	EN_BINT	EN_BOVF	EN_ BOVER	EN_ BUNDR
			EN_ BCGMON	x	x	x	EN_ LONINT	x	EN_ SAMP	EN_ PLLINT
			x	x	x	x	x	x	INTB_TYPE[1:0]	

Table 8. EN_INT (0x02 and 0x03) Register Meaning

INDEX	NAME	DEFAULT	FUNCTION
D[23:8]	EN_DCLOFFINT EN_BINT EN_BOVF EN_BOVER EN_BUNDR EN_BCGMON EN_LONINT EN_SAMP EN_PLLINT	0x0000	Interrupt Enables for interrupt bits in STATUS[23:8] 0 = Individual interrupt bit is not included in the interrupt OR term 1 = Individual interrupt bit is included in the interrupt OR term
D[1:0]	INTB_TYPE[1:0]	11	INTB Port Type (EN_INT Selections) 00 = Disabled (high impedance) 01 = CMOS Driver 10 = Open-Drain NMOS Driver 11 = Open-Drain NMOS Driver with Internal 125kΩ Pullup Resistance
		11	INT2B Port Type (EN_INT2 Selections) 00 = Disabled (high impedance) 01 = CMOS Driver 10 = Open-Drain nMOS Driver 11 = Open-Drain nMOS Driver with Internal 125kΩ Pullup Resistance

MNGR_INT (0x04)

MNGR_INT is a read/write register that manages the operation of the configurable interrupt bits in response to BIOZ FIFO conditions (see the STATUS register and BIOZ FIFO descriptions for more details).

Table 9. MNGR_INT (0x04) Register Map

REG	NAME	R/W	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0
0x04	MNGR_INT	R/W	x	x	x	x	x	BFIT[2:0]		
			x	x	x	x	x	x	x	x
			x	CLR_FAST	x	x	x	CLR_SAMP	SAMP_IT[1:0]	

Table 10. MNGR_INT (0x04) Register Functionality

INDEX	NAME	DEFAULT	FUNCTION
D[18:16]	BFIT[2:0]	011	BIOZ FIFO Interrupt Threshold (issues BINT based on number of unread FIFO records) 000 to 111 = 1 to 8, respectively (i.e. BFIT[2:0]+1 unread records)
D[2]	CLR_SAMP	1	Sample Synchronization Pulse (SAMP) Clear Behavior: 0 = Clear SAMP on STATUS Register Read Back (recommended for debug/evaluation only). 1 = Self-clear SAMP after approximately one-fourth of one data rate cycle.
D[1:0]	SAMP_IT[1:0]	00	Sample Synchronization Pulse (SAMP) Frequency 00 = issued every sample instant 01 = issued every 2nd sample instant 10 = issued every 4th sample instant 11 = issued every 16th sample instant

MNGR_DYN (0x05)

MNGR_DYN is a read/write register that manages the settings of any general/dynamic modes within the device. This register contains the interrupt thresholds for BIOZ AC Lead-Off Detection (see CNFG_GEN for more details). Unlike many CNFG registers, changes to dynamic modes do not impact FIFO operations or require a SYNCH operation (though the affected circuits may require time to settle, resulting in invalid/corrupted FIFO output voltage information during the settling interval).

Table 11. MNGR_DYN (0x05) Register Map

REG	NAME	R/W	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0
0x05	MNGR_DYN	R/W	x	x	x	x	x	x	x	x
			BLOFF_HI_IT[7:0]							
			BLOFF_LO_IT[7:0]							

Table 12. MNGR_DYN (0x05) Register Functionality

INDEX	NAME	DEFAULT	FUNCTION
D[15:8]	BLOFF_HI_IT[7:0]	0xFF	BIOZ AC Lead Off Over-Range Threshold If EN_BLOFF[1:0] = 1x and the ADC output of a BIOZ measurement exceeds the symmetric thresholds defined by ±2048*BLOFF_HI_IT for over 128ms, the BOVER interrupt bit will be asserted. For example, the default value (BLOFF_IT= 0xFF) corresponds to a BIOZ output upper threshold of 0x7F800 or about 99.6% of the full scale range, and a BIOZ output lower threshold of 0x80800 or about 0.4% of the full scale range with the LSB weight ≈ 0.4%.
D[7:0]	BLOFF_LO_IT[7:0]	0xFF	BIOZ AC Lead Off Under-Range Threshold If EN_BLOFF[1:0] = 1x and the output of a BIOZ measurement is bounded by the symmetric thresholds defined by ±32*BLOFF_LO_IT for over 128ms, the BUNDR interrupt bit will be asserted.

SW_RST (0x08)

SW_RST (Software Reset) is a write-only register/command that resets the MAX30002 to its original default conditions at the end of the SPI SW_RST transaction (i.e. the 32nd SCLK rising edge). Execution occurs only if DIN[23:0] = 0x000000. The effect of a SW_RST is identical to power-cycling the device.

Table 13. SW_RST (0x08) Register Map

REG	NAME	R/W	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0
0x08	SW_RST	W	D[23:16] = 0x00							
			D[15:8] = 0x00							
			D[7:0] = 0x00							

SYNCH (0x09)

SYNCH (Synchronize) is a write-only register/command that begins new BIOZ operations and recording, beginning on the internal MSTR clock edge following the end of the SPI SYNCH transaction (i.e. the 32nd SCLK rising edge). Execution occurs only if DIN[23:0] = 0x000000. SYNCH will reset and clear the FIFO memory and the DSP filter (to mid-scale), allowing the user to effectively set the “Time Zero” for the FIFO records. No configuration settings are impacted. For best results, users should wait until the PLL has achieved lock before synchronizing if the CNFG_GEN settings have been altered.

Once the device is initially powered up, it will need to be fully configured prior to launching recording operations. Likewise, anytime a change to CNFG_GEN or CNFG_ BIOZ registers are made there may be discontinuities in the BIOZ records and possibly changes to the size of the time steps recorded in the FIFOs. The SYNCH command provides a means to restart operations cleanly following any such disturbances.

If a FIFO overflow event occurs and a portion of the record is lost, it is recommended to use the SYNCH command to recover and restart the recording, (avoiding issues with missing data).

Table 14. SYNCH (0x09) Register Map

REG	NAME	R/W	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0
0x09	SYNCH	W	D[23:16] = 0x00							
			D[15:8] = 0x00							
			D[7:0] = 0x00							

FIFO_RST (0x0A)

FIFO_RST (FIFO Reset) is a write-only register/command that begins a new BIOZ recording by resetting the FIFO memory and resuming the record with the next available BIOZ data. Execution occurs only if DIN[23:0] = 0x000000. Unlike the SYNCH command, the operations of any active BIOZ circuitry are not impacted by FIFO_RST, so no settling/recovery transients apply. FIFO_RST can also be used to quickly recover from a FIFO overflow state.

Table 15. FIFO_RST (0x0A) Register Map

REG	NAME	R/W	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0
0x0A	FIFO_RST	W	D[23:16] = 0x00							
			D[15:8] = 0x00							
			D[7:0] = 0x00							

INFO (0x0F)

INFO is a read-only register that provides information about the MAX30002. The first nibble contains an alternating bit pattern to aide in interface verification. The second nibble contains the revision ID. The third nibble includes part ID information.

Note: Due to internal initialization procedures, this command will not read-back valid data if it is the first command executed following either a power-cycle event, or a SW_RST event.

Table 16. INFO (0x0F) Register Map

REG	NAME	R/W	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0
0x0F	INFO	R	0	1	0	1	REV_ID[3:0]			
			x	x	1	0	x	x	x	x
			x	x	x	x	x	x	x	x

Table 17. INFO (0x0F) Register Meaning

INDEX	NAME	MEANING
D[19:16]	REV_ID[3:0]	Revision ID

CNFG_GEN (0x10)

CNFG_GEN is a read/write register which governs general settings, most significantly the master clock rate for all internal timing operations. Anytime a change to CNFG_GEN is made, there may be discontinuities in the BIOZ record and possibly changes to the size of the time steps recorded in the FIFOs. The SYNCH command can be used to restore internal synchronization resulting from configuration changes. Note when EN_BIOZ is logic-low, the device is in one of two ultra-low power modes (determined by EN_ULP_LON).

Table 18. CNFG_GEN (0x10) Register Map

REG	NAME	R/W	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0
0x10	CNFG_GEN	R/W	EN_ULP_LON[1:0]		FMSTR[1:0]		x	EN_BIOZ	x	x
			EN_BLOFF[1:0]		EN_DCLOFF[1:0]		IPOL	IMAG[2:0]		
			VTH[1:0]		EN_RBIAS[1:0]		RBIASV[1:0]		RBIASP	RBIASN

Table 19. CNFG_GEN (0x10) Register Functionality

INDEX	NAME	DEFAULT	FUNCTION
D[23:22]	EN_ULP_LON [1:0]	00	Ultra-Low Power Lead-On Detection Enable 00 = ULP Lead-On Detection disabled 01 = Reserved. Do not use. 10 = BioZ ULP Lead-On Detection enabled. 11 = Reserved. Do not use. ULP mode is only active when the BioZ channel is powered down/disabled.
D[21:20]	FMSTR[1:0]	00	Master Clock Frequency. Selects the Master Clock Frequency (FMSTR), which also determines the BioZ timing characteristics. These are generated from FCLK, which is always 32.768kHz. 00 = F_{MSTR} = 32768Hz 01 = F_{MSTR} = 32000Hz 10 = F_{MSTR} = 32000Hz 11 = F_{MSTR} = 31968.78Hz
D[18]	EN_BIOZ	0	BIOZ Channel Enable 0 = BIOZ Channel disabled 1 = BIOZ Channel enabled
D[15:14]	EN_BLOFF[1:0]	00	BIOZ Digital Lead Off Detection Enable 00 = Digital Lead Off Detection disabled 01 = Lead Off Under Range Detection, 4 electrode BIOZ applications 10 = Lead Off Over Range Detection, 2 and 4 electrode BIOZ applications 11 = Lead Off Over & Under Range Detection, 4 electrode BIOZ applications AC Method, requires active BIOZ Channel , enables BOVER & BUNDR interrupt behavior. Uses BIOZ excitation current set in CNFG_BIOZ with digital thresholds set in MNGR_DYN.
D[13:12]	EN_DCLOFF	00	DC Lead-Off Detection Enable 00 = DC Lead-Off Detection disabled 01 = Reserved. Do not use. 10 = DCLOFF Detection applied to the BIP/N pins. 11 = Reserved. Do not use. DC Method, requires active selected channel, enables DCLOFF interrupt and status bit behavior. Uses current sources and comparator thresholds set below.
D[11]	DCLOFF_ IPOL	0	DC Lead-Off Current Polarity (if current sources are enabled/connected) 0 = BIP - Pullup BIN – Pulldown 1 = BIP - Pulldown BIN – Pullup
D[10:8]	IMAG[2:0]	000	DC Lead-Off Current Magnitude Selection 000 = 0nA (Disable and Disconnect Current Sources) 001 = 5nA 010 = 10nA 011 = 20nA 100 = 50nA 101 = 100nA 110 = Reserved. Do not use. 111 = Reserved. Do not use.

Table 19. CNFG_GEN (0x10) Register Functionality (continued)

INDEX	NAME	DEFAULT	FUNCTION
D[7:6]	VTH[1:0]	00	DC Lead-Off Voltage Threshold Selection 00 = V_{MID} ± 300mV 01 = V_{MID} ± 400mV 10 = V_{MID} ± 450mV 11 = V_{MID} ± 500mV
D[5:4]	EN_RBIAS[1:0]	00	Enable and Select Resistive Lead Bias Mode 00 = Resistive Bias disabled 01 = Reserved. Do not use. 10 = BioZ Resistive Bias enabled if EN_BIOZ is also enabled 11 = Reserved. Do not use. If EN_BIOZ is not asserted at the same time or prior to EN_RBIAS[1:0] being enabled, then EN_RBIAS[1:0] will remain set to 00.
D[3:2]	RBIASV[1:0]	01	Resistive Bias Mode Value Selection 00 = R_{BIAS} = 50MΩ 01 = R_{BIAS} = 100MΩ 10 = R_{BIAS} = 200MΩ 11 = Reserved. Do not use.
D[1]	RBIASP	0	Enables Resistive Bias on Positive Input 0 = BIP is not resistively connected to V_{MID} 1 = BIP is connected to V_{MID} through a resistor (selected by RBIASV).
D[0]	RBIASN	0	Enables Resistive Bias on Negative Input 0 = BIN is not resistively connected to V_{MID} 1 = BIN is connected to V_{MID} through a resistor (selected by RBIASV).

Table 20 shows BIOZ data rates that can be realized with various setting of FMSTR, along with RATE configuration bits available in the CNFG_BIOZ register. Note FMSTR also determines the timing resolution of the CAL waveform generator.

Table 20. Master Frequency Summary Table

FMSTR [1:0]	MASTER FREQUENCY (f_{MSTR}) (Hz)	BIOZ DATA RATES (B_RATE) (sps)
00	32,768	0 = 64 1 = 32
01	32,000	0 = 62.50 1 = 31.25
10	32,000	0 = 50 1 = 25
11	31,968	0 = 49.95 1 = 24.98

CNFG_BMUX(0x17)

CNFG_BMUX is a read/write register which configures the operation, settings, and functionality of the input multiplexer associated with the BIOZ channel.

Table 21. CNFG_BMUX (0x17) Register Map

REG	NAME	R/W	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0
0x17	CNFG_ BMUX	R/W	x	x	OPENP	OPENN	CALP_SEL[1:0]		CALN_SEL[1:0]	
			x	x	CG_MODE[1:0]		EN_BIST	RNOM[2:0]		
			x	RMOD[2:0]			x	x	FBIST[1:0]	

Table 22. CNFG_BMUX (0x17) Register Functionality

INDEX	NAME	DEFAULT	FUNCTION
D[21]	OPENP	1	Open the BIP Input Switch (most often used for testing and calibration) 0 = BIP is internally connected to the BIOZ channel 1 = BIP is internally isolated from the BIOZ channel
D[20]	OPENN	1	Open the BIN Input Switch (most often used for testing and calibration) 0 = BIN is internally connected to the BIOZ channel 1 = BIN is internally isolated from the BIOZ channel
D[19:18]	CALP_ SEL[1:0]	00	BIP Calibration Selection 00 = No calibration signal applied 01 = Input is connected to VMID 10 = Reserved. Do not use. 11 = Reserved. Do not use.
D[17:16]	CALN_ SEL[1:0]	00	BIN Calibration Selection 00 = No calibration signal applied 01 = Input is connected to VMID 10 = Reserved. Do not use. 11 = Reserved. Do not use.
D[13:12]	CG_ MODE[1:0]	00	BIOZ Current Generator Mode Selection 00 = Unchopped Sources with Low Pass Filter (higher noise, excellent 50/60Hz rejection, recommended for BioZ applications) 01 = Chopped Sources without Low Pass Filter (low noise, no 50/60Hz rejection, recommended for BioZ applications with digital LPF, possibly battery powered BioZ applications) 10 = Chopped Sources with Low Pass Filter (low noise, excellent 50/60Hz rejection) 11 = Chopped Sources with Resistive CM Setting (Not recommended to be used for drive currents >32µA) (low noise, excellent 50/60Hz rejection, lower input impedance)
D[11]	EN_BIST	0	BIOZ Modulated Resistance Built-In-Self-Test (RMOD BIST) Mode Enable 0 = RMOD BIST Disabled 1 = RMOD BIST Enabled To avoid body interference, the BIP/N switches should be open in this mode. When enabled, the DRVP/N isolation switches are opened and the DRVP/N-to-BIP/N internal switches are engaged. Also, the lead bias resistors are applied to the BIOZ inputs in 200MΩ mode.

Table 22. CNFG_BMUX (0x17) Register Functionality (continued)

INDEX	NAME	DEFAULT	FUNCTION
D[10:8]	RNOM[2:0]	000	BIOZ RMOD BIST Nominal Resistance Selection See RMOD BIST Settings Table for details.
D[6:4]	RMOD[2:0]	100	BIOZ RMOD BIST Modulated Resistance Selection (See RMOD BIST Settings table for details.) 000 = Modulated Resistance Value 0 001 = Modulated Resistance Value 1 010 = Modulated Resistance Value 2 011 = Reserved, Do Not Use 1xx = All SWMOD Switches Open - No Modulation (DC value = RNOM)
D[1:0]	FBIST[1:0]	00	BIOZ RMOD BIST Frequency Selection Calibration Source Frequency Selection (FCAL) 00 = $f_{MSTR}/2^{13}$ (Approximately 4 Hz) 01 = $f_{MSTR}/2^{15}$ (Approximately 1 Hz) 10 = $f_{MSTR}/2^{17}$ (Approximately 1/4 Hz) 11 = $f_{MSTR}/2^{19}$ (Approximately 1/16 Hz) Actual frequencies are determined by FMSTR selection (see CNFG_GEN for details), approximate frequencies are based on a 32,768 Hz clock (FMSTR[1:0]=00). All selections use 50% duty cycle.

Table 23. CNFG_BMUX (0x17) RMOD BIST Settings

RNOM[2:0]	RMOD[2:0]	NOMINAL RESISTANCE (Ω)	MODULATED RESISTANCE (mΩ)
000	000 001 010 1xx	5000	2960.7 980.6 247.5 Unmodulated
001	000 001 010 1xx	2500	740.4 245.2 61.9 Unmodulated
010	000 001 010 1xx	1667	329.1 109.0 27.5 Unmodulated

Table 23. CNFG_BMUX (0x17) RMOD BIST Settings (continued)

RNOM[2:0] AND SWNOM SWITCHES ENGAGED	RMOD[2:0]	NOMINAL RESISTANCE (Ω)	MODULATED RESISTANCE (mΩ)
011	000 001 1xx	1250	185.1 61.3 Unmodulated
100	000 001 1xx	1000	118.5 39.2 Unmodulated
101	000 001 1xx	833	82.3 27.2 Unmodulated
110	000 001 1xx	714	60.5 20.0 Unmodulated
111	000 001 1xx	625	46.3 15.3 Unmodulated

CNFG_BIOZ(0x18)

CNFG_BIOZ is a read/write register which configures the operation, settings, and function of the BIOZ channel, including the associated modulated current generator. Anytime a change to CNFG_BIOZ is made, there may be discontinuities in the BIOZ record and possibly changes to the size of the time steps recorded in the BIOZ FIFO. The SYNCH command can be used to restore internal synchronization resulting from configuration changes.

Table 24. CNFG_BIOZ (0x18) Register Map

REG	NAME	R/W	23/15/7	22/14/6	21/13/5	20/12/4	19/11/3	18/10/2	17/9/1	16/8/0
0x18	CNFG_BIOZ	R/W	RATE	AHPF[2:0]			EXT_RBIAS	LN_BIOZ	GAIN[1:0]	
			DHPF[1:0]		DLPF[1:0]		FCGEN[3:0]			
			CGMON	CGMAG[2:0]			PHOFF[3:0]			

Table 25. CNFG_BIOZ (0x18) Register Functionality

INDEX	NAME	DEFAULT	FUNCTION
D[23]	RATE	0	BIOZ Data Rate (also dependent on FMSTR selection, see CNFG_GEN):
			FMSTR = 00: f_{MSTR} = 32,768Hz 0 = 64sps 1 = 32sps
			FMSTR = 01: f_{MSTR} = 32,000Hz 0 = 62.50sps 1 = 31.25sps
			FMSTR = 10: f_{MSTR} = 32,000 Hz 0 = 50sps 1 = 25sps
			FMSTR = 11: f_{MSTR} = 31,968 Hz 0 = 49.95sps 1 = 24.98sps
D[22:20]	AHPF[2:0]	010	BIOZ Channel Analog High-Pass Filter Cutoff Frequency and Bypass 000 = 125Hz 001 = 300Hz 010 = 800Hz 011 = 2000Hz 100 = 3700Hz 101 = 7200Hz 11x = Bypass AHPF
D[19]	EXT_RBIAS	0	External Resistor Bias Enable 0 = Internal Bias Generator used 1 = External Bias Generator used Note: Use of the external resistor bias will improve the temperature coefficient of all biases within the product, but the main benefit is improved control of BIOZ current generator magnitude. If enabled, the user must include the required external resistor between RBIAS and GND, and the temperature coefficent achieved will be determined by the combined performance of the internal bandgap and the external resistor.
D[18]	LN_BIOZ	0	BIOZ Channel Instrumentation Amplifier (INA) Power Mode 0 = BIOZ INA is in low power mode 1 = BIOZ INA is in low noise mode
D[17:16]	GAIN[1:0]	00	BIOZ Channel Gain Setting 00 = 10V/V 01 = 20V/V 10 = 40V/V 11 = 80V/V
D[15:14]	DHPF[1:0]	00	BIOZ Channel Digital High-Pass Filter Cutoff Frequency 00 = Bypass (DC) 01 = 0.05Hz 1x = 0.50Hz

Table 25. CNFG_BIOZ (0x18) Register Functionality (continued)

INDEX	NAME	DEFAULT	FUNCTION
D[13:12]	DLPF[1:0]	01	BIOZ Channel Digital Low-Pass Filter Cutoff Frequency 00 = Bypass (Decimation only, no FIR filter) 01 = 4Hz 10 = 8Hz 11 = 16Hz (Available for 64, 62.5, 50, and 49.95sps BIOZ Rate selections only) Note: See Table 39 below. If an unsupported DLPF setting is specified, the 4Hz setting (DLPF[1:0] = 01) will be used internally; the CNFG_BIOZ register will continue to hold the value as written, but return the effective internal value when read back.
D[11:8]	FCGEN[3:0]	1000	BIOZ Current Generator Modulation Frequency 0000 = $4*f_{MSTR}$ (approximately 128000Hz) 1000 = $f_{MSTR}/64$ (approximately 500Hz) 0001 ≈ $2*f_{MSTR}$ (approximately 80000Hz) 1001 = $f_{MSTR}/128$ (approximately 250Hz) 0010 ≈ f_{MSTR} (approximately 40000Hz) 101x = $f_{MSTR}/256$ (approximately 125Hz) 0011 ≈ $f_{MSTR}/2$ (approximately 18000Hz) 11xx = $f_{MSTR}/256$ (approximately 125Hz) 0100 = $f_{MSTR}/4$ (approximately 8000Hz) 0101 = $f_{MSTR}/8$ (approximately 4000Hz) 0110 = $f_{MSTR}/16$ (approximately 2000Hz) 0111 = $f_{MSTR}/32$ (approximately 1000Hz) Actual frequencies determined by FMSTR selection, see CNFG_GEN register and table below for details.
D[7]	CGMON	0	BIOZ Current Generator Monitor 0 = Current Generator Monitors disabled 1 = Current Generator Monitors enabled, requires active BIOZ channel and Current Generators. Enables BCGMON interrupt and status bit behavior. Monitors current source compliance levels, useful in detecting DRVP/DRVN lead off conditions with 4 electrode BIOZ applications.
D[6:4]	CGMAG[2:0]	000	BIOZ Current Generator Magnitude 000 = Off (DRVP and DRVN floating, Current Generators Off) 001 = 8µA 010 = 16µA 011 = 32µA 100 = 48µA 101 = 64µA 110 = 80µA 111 = 96µA See Table 40 and 41 below for a list of allowed CGMAG settings vs. FCGEN selections.
D[3:0]	PHOFF[3:0]	0000	BIOZ Current Generator Modulation Phase Offset Phase Resolution and Offset depends on FCGEN setting: FCGEN[3:0] ≥ 0010: Phase Offset = PHOFF[3:0]*11.25° (0 to 168.75°) FCGEN[3:0] = 0001: Phase Offset = PHOFF[3:1]*22.50° (0 to 157.50°) FCGEN[3:0] = 0000: Phase Offset = PHOFF[3:2]*45.00° (0 to 135.00°)

Table 26. Supported RATE and DLPF Options

CNFG_GEN FMSTR[1:0]	RATE Sample Rate	DLPF[1:0] / Digital LPF Cut Off			
		00	01	10	11
00 = 32,768Hz	0 = 64sps	Bypass	4.096Hz	8.192Hz	16.384Hz
	1 = 32sps				4.096Hz
01 = 32,000Hz	0 = 62.5sps	Bypass	4.0Hz	8.0Hz	16.0Hz
	1 = 31.25sps				4.0Hz
10 = 32,000Hz	0 = 50sps	Bypass	4.0Hz	8.0Hz	16.0Hz
	1 = 25sps				4.0Hz
11 = 31,968Hz	0 = 49.95sps	Bypass	3.996Hz	7.992Hz	15.984Hz
	1 = 25.98sps				3.996Hz

Note: *Combinations shown in grey are unsupported and will be internally mapped to the default settings shown.*

Table 27. Actual BIOZ Current Generator Modulator Frequencies vs. FMSTR[1:0] Selection

FCGEN[3:0]	BIOZ Current Generator Modulation Frequency (Hz)			
	FMSTR[1:0] = 00 f_{MSTR} = 32,768Hz	FMSTR[1:0] = 01 f_{MSTR} = 32,000Hz	FMSTR[1:0] = 10 f_{MSTR} = 32,000Hz	FMSTR[1:0] = 11 f_{MSTR} = 31,968Hz
0000	131,072	128,000	128,000	127,872
0001	81,920	80,000	80,000	81,920
0010	40,960	40,000	40,000	40,960
0011	18,204	17,780	17,780	18,204
0100	8,192	8,000	8,000	7,992
0101	4,096	4,000	4,000	3,996
0110	2,048	2,000	2,000	1,998
0111	1,024	1,000	1,000	999
1000	512	500	500	500
1001	256	250	250	250
101x, 11xx	128	125	125	125

Table 28. Allowed CGMAG Option vs. FCGEN Selections

FCGEN[3:0]	APPROXIMATE CURRENT GENERATOR MODULATION FREQUENCY (Hz)	CGMAG[2:0] OPTIONS ALLOWED	CURRENT GENERATOR MAGNITUDE OPTIONS ALLOWED (μA_{P-P})
0000	12,8000	All	All
0001	80,000		
0010	40,000		
0011	18,000		
0100	8,000	All except 111	All except 96
0101	4,000	000, 001, 010, 011	Off, 8, 16, 32
0110	2,000	000, 001, 010	Off, 8, 16
0111	1,000	000, 001	Off, 8
1000	500		
1001	250		
101x, 11xx	125		

FIFO Memory Description

The device provides read only FIFO memory for BIOZ information. The operation of this FIFO memory is detailed in the following sections.

Table 29 summarizes the method of access and data structure within the FIFO memory.

Table 29. FIFO Memory Access and Data Structure Summary

REG	FIFO AND MODE	DATA STRUCTURE (D[23:0])																						
		23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
0x22	BIOZ Burst	BIOZ Sample Voltage Data [19:0]																				0	BTAG [2:0]		
0x23	BIOZ	BIOZ Sample Voltage Data [19:0]																				0	BTAG [2:0]		

BIOZ FIFO Memory (8 Words x 24 Bits)

The BIOZ FIFO memory is a standard circular FIFO consisting of 8 words, each with 24 bits of information. The BIOZ FIFO is independently managed by internal read and write pointers. The read pointer is updated in response to the 32nd SCLK rising edge in a normal mode read back transaction and on the (32 + n x 24)th SCLK rising edge(s) in a burst mode transaction where n = 0 to up to 31. Once a FIFO sample is marked as read, it cannot be accessed again.

The write pointer is governed internally. To aide data management and reduce µC overhead, the device provides a user-programmable BIOZ FIFO Interrupt Threshold (BFIT[2:0]) governing the BIOZ Interrupt bit (BINT). This threshold can be programmed with values from 1 to 8, representing the number of unread BIOZ FIFO entries required before the BINT bit will be asserted, alerting the µC that there is a significant amount of data in the BIOZ FIFO ready for read back (see MNGR_INT (0x04) for details).

If the write pointer ever traverses the entire FIFO array and catches up to the read pointer (due to failure of the µC to read/maintain FIFO data), a FIFO overflow will occur and data will be corrupted. The BOVF STATUS and tag bits will indicate this condition and the FIFO should be cleared before continuing measurements using either a SYNCH or FIFO_RST command—note overflow events will result in the loss of samples and thus timing information, so these conditions should not occur in well-designed applications.

Do not read beyond the last valid FIFO word to prevent possible data corruption.

BIOZ FIFO Data Structure

The data portion of the word contains the 20-bit BIOZ voltage information measured at the requested sample rate in left justified two's complement format. One bit is set to 0 and the remaining three bits of data hold important data tagging information (see details in Table 30). After converting the data portion of the sample to signed magnitude format, BioZ is calculated by the following equation:

$$BioZ\ (\Omega) = ADC \times V_{REF} / (2^{19} \times BIOZ\_CGMAG \times BIOZ\_GAIN)$$

Where:

ADC = ADC counts in signed magnitude format, V_{REF} = 1V (typ) (see the *Electrical Characteristics* section), BIOZ_CGMAG = 8 to 96 x 10^{-6}A, and BIOZ_GAIN = 10V/V, 20V/V, 40V/V, or 80V/V. BIOZ_CGMAG and BIOZ_GAIN are set in CNFG_BIOZ (0x18).

Table 30. BIOZ FIFO BIOZ Data Tags (BTAG[2:0] = D[2:0])

BTAG [2:0]	DESCRIPTION	RECOMMENDED USER ACTION	DATA VALID	TIME VALID
000	Valid Sample	Log sample into BIOZ record and increment the time step. Continue to read data from the BIOZ FIFO.	Yes	Yes
001	Over/Under Range Sample	Log sample into BIOZ record and increment the time step. Determine if the data is valid or a lead off condition. Continue to read data from the BIOZ FIFO.	?	Yes
010	Last Valid Sample (EOF)	Log sample into BIOZ record and increment the time step. Suspend read of the BIOZ FIFO until more samples are available.	Yes	Yes
011	Last Over/Under Range Sample (EOF)	Log sample into BIOZ record and increment the time step. Determine if the data is valid or a lead off condition. Suspend read of the BIOZ FIFO until more samples are available.	?	Yes
10x	Unused	-	-	-
110	FIFO Empty (exception)	Discard this sample without incrementing the time base. Suspend read of the BIOZ FIFO until more samples are available.	No	No
111	FIFO Overflow (exception)	Discard this sample without incrementing the time base. Issue a FIFO_RST command to clear the FIFOs or re-SYNCH if necessary. Note the corresponding halt and resumption in all the FIFOs.	No	No

BIOZ Data Tags (BTAG)

The final three bits in the sample are used as a data tag (BTAG[2:0] = D[2:0]) to assist in managing data transfers. The BTAG structure used is detailed below.

VALID: BTAG = 000 indicates that BIOZ data for this sample represents both a valid voltage and time step in the BIOZ record.

OVER or UNDER RANGE: BTAG = 001 indicates that BIOZ data for this sample violated selected range thresholds (see MNGR_DYN and CNFG_GEN) and that the voltage information in the sample should be evaluated to see if it is valid or indicative of a leads-off condition. Note that while the voltage data may be invalid, samples of this type do represent valid time steps in the BIOZ record.

VALID EOF: BTAG = 010 indicates that BIOZ data for this sample represents both a valid voltage and time step in the BIOZ record, and that this is the last sample currently available in the BIOZ FIFO (End-of-File, EOF). The µC should wait until further samples are available before requesting more data from the BIOZ FIFO.

OVER or UNDER RANGE EOF: BTAG = 011 indicates that BIOZ data for this sample violated selected range thresholds (see MNGR_DYN and CNFG_GEN) and that the voltage information in the sample should be evaluated to see if it is valid or indicates a leads-off condition. Note that while the voltage data may be invalid, samples of this type do represent valid time steps in the BIOZ record. This is also the last sample currently available in the BIOZ FIFO (End-of-File, EOF). The µC should wait until further samples are available before requesting more data from the BIOZ FIFO.

EMPTY: BTAG = 110 is appended to any requested read back data from an empty FIFO. The presence of this tag alerts the user that this FIFO data does not represent a valid sample or time step. Note that if handled properly by the µC, an occurrence of an empty tag will not compromise the integrity of a continuous FIFO record – this tag only indicates that the read back request was either premature or unnecessary.

OVERFLOW: BTAG = 111 indicates that the FIFO has overflowed and that there are interruptions or missing data in the sample records. The BIOZ Overflow (BOVF) bit is also included in the STATUS register. A FIFO_RESET is required to resolve this situation, effectively clearing the FIFO so that valid sampling going forward is assured.

Applications Information

External Filters

The BioZ filter depends on the drive frequency used in the application. Place the differential mode corner frequency several decades higher than the maximum drive frequency. Place the common mode corner frequency higher than the differential mode corner frequency but lower than the AM radio band.

Body Bias Electrode

Compliance with the common mode input range of the ECG and BioZ channels is achieved by using internal lead bias or by adding a third electrode to drive the body to V_{CM}. The body bias drive electrode improves performance in applications with high electrode impedance or high 50/60Hz coupling. Using V_{CM} drive also improves the input impedance because internal lead bias is disabled.

Typical Application Circuit

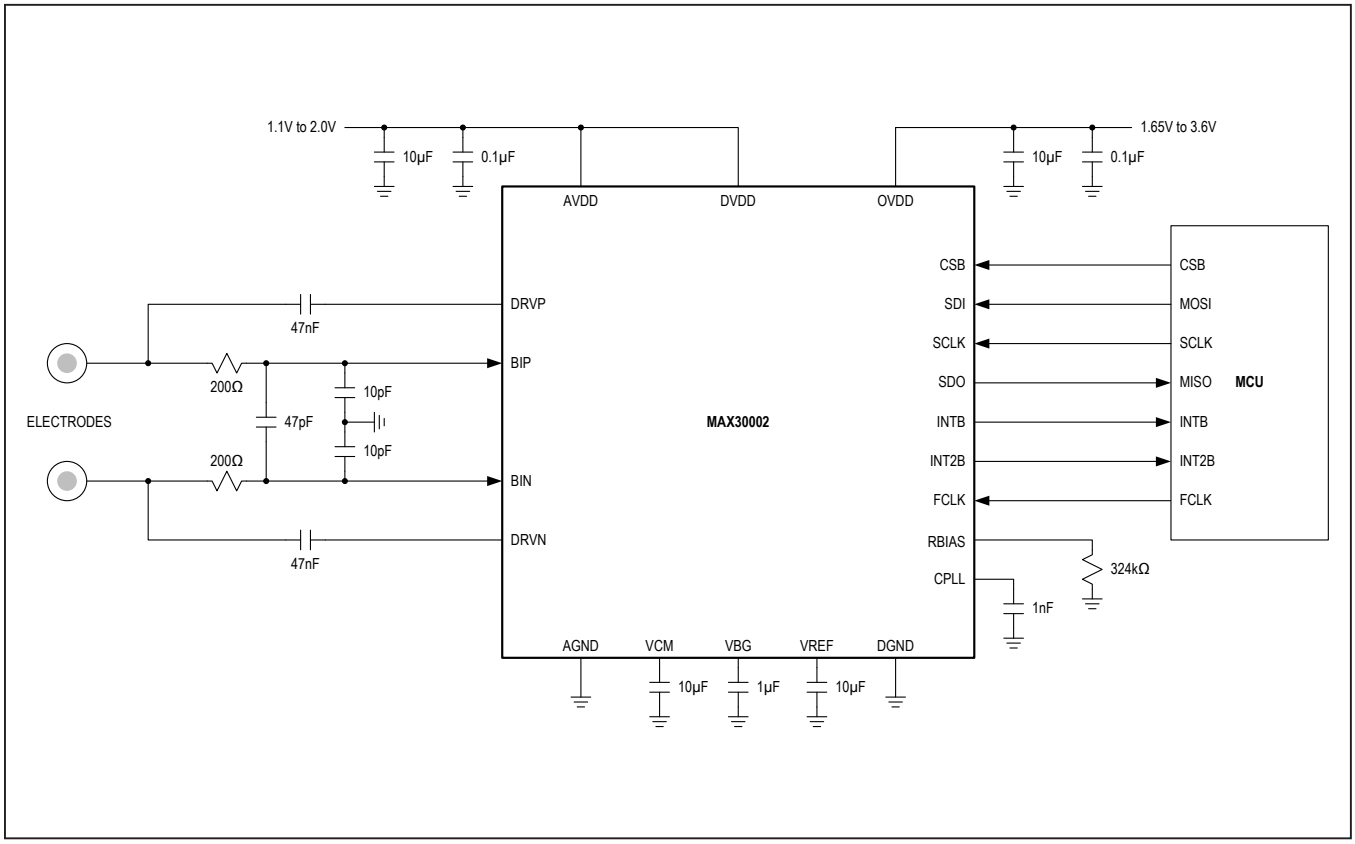


Figure 9. Two-Electrode Respiration Monitor Typical Application Circuit

Application Diagrams

See Figure 10 for an example of a clinical application for monitoring respiration using just two electrodes and with optional shared defibrillation protection circuitry. The electrode models are shown to illustrate the electrical characteristics of the physical electrodes.

Four Electrode Respiration Monitoring Application

See Figure 11 for an example of a clinical application for monitoring respiration using four electrodes and with optional defibrillation protection circuitry. The electrode models are shown to illustrate the electrical characteristics of the physical electrodes.

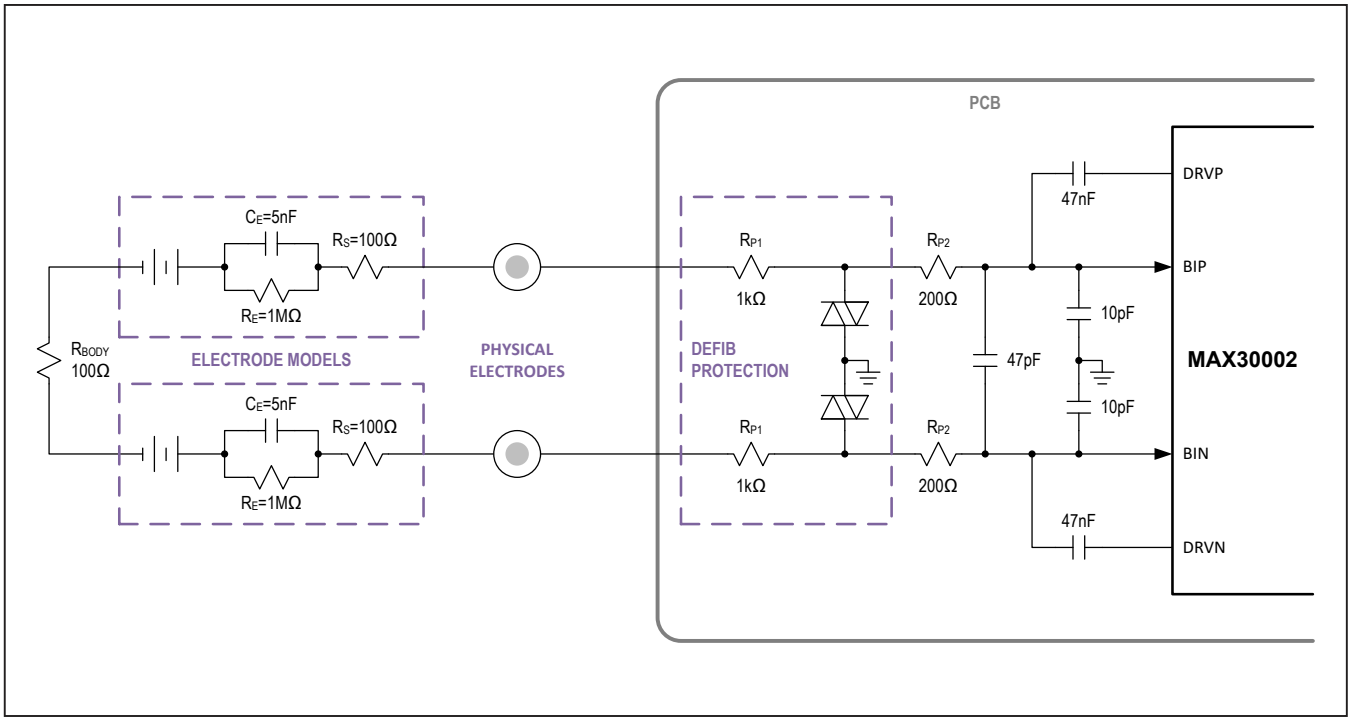


Figure 10. Two Electrode Respiration Monitoring with Optional Common Defibrillation Protection.

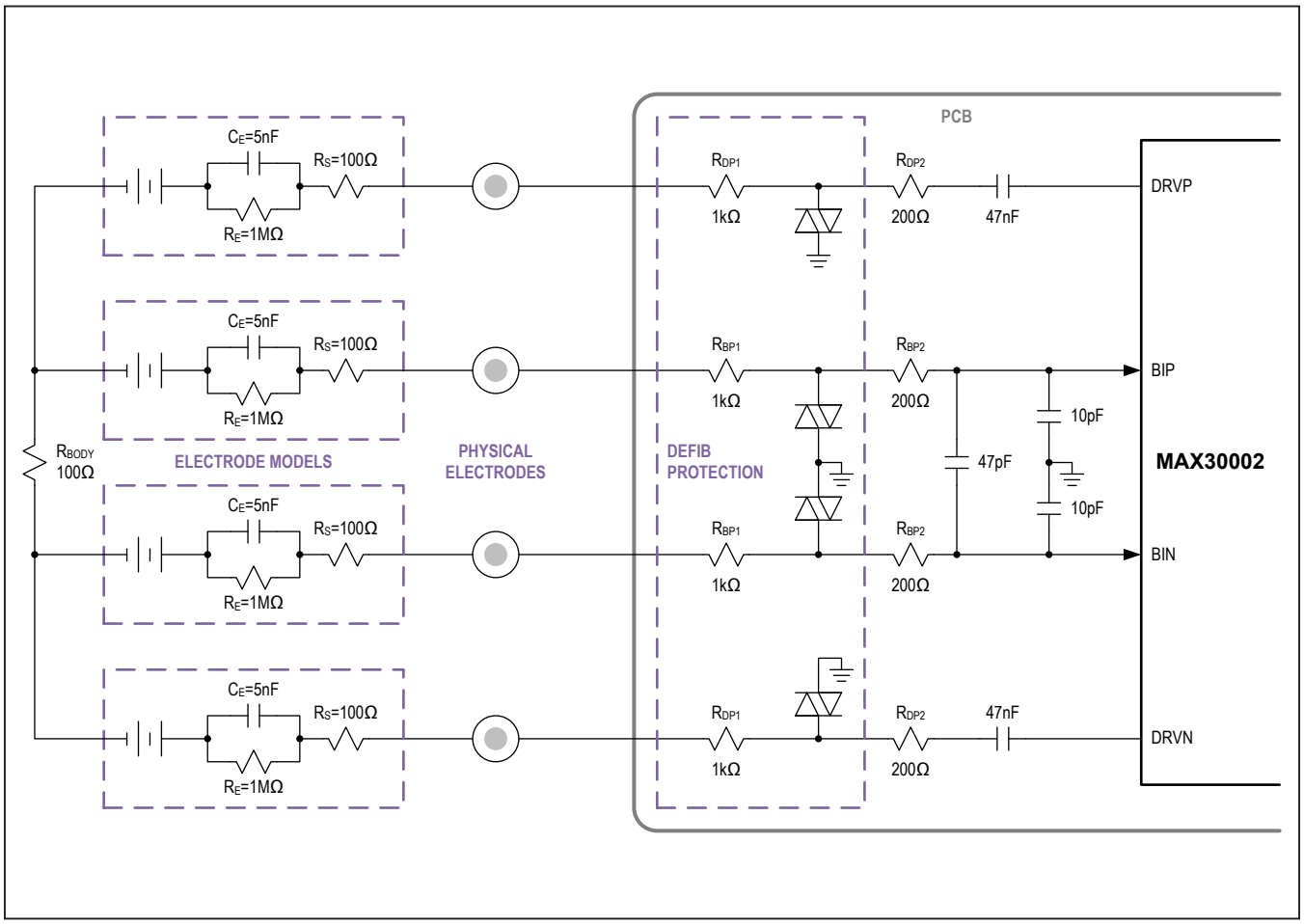


Figure 11. Four Electrode Respiration Monitoring with Optional Defibrillation Protection.

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE
MAX30002CWV+	0°C TO +70°C	30WLP
MAX30002CWV+T	0°C TO +70°C	30WLP

+Denotes lead(Pb)-free/RoHS-compliant package.
T = Tape and reel.

Chip Information

PROCESS: CMOS

Package Information

For the latest package outline information and land patterns (footprints), go to **www.maximintegrated.com/packages**. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

PACKAGE TYPE	PACKAGE CODE	OUTLINE NO.	LAND PATTERN NO.
30 WLP	W302L2+1	**21-100074**	Refer to **Application Note 1891**

Revision History

REVISION NUMBER	REVISION DATE	DESCRIPTION	PAGES CHANGED
0	3/18	Initial release	—
1	1/23	Updated Benefits and Features, General Description, Absolute Maximum Ratings, Package Thermal Characteristics, Electrical Characteristics, replaced Figure 1a, TOC 08, TOC 09, and TOC12, updated Pin Configuration, Pin Description, Detailed Description, BioZ Channel, Input MUX, EMI Filtering and ESD Protection, added ESD Protection, updated Leads-Off Detection and ULP Leads-On Detection, Lead Bias, Programmable Resistive Load, Current Generator, added Converting BIOZ Samples to Ohms, Current Selection and Resolution Calculation Example 1 (Two Terminal with Common Protection), Current Selection and Resolution Calculation Example 2 (Four Terminal), Reference and Common Mode Buffer, Table 5, Table 8, Table 13, Table 14, Table 15, BIOZ FIFO Data Structure, added Applications Information, updated Ordering Information table, and Package Information table	1, 3–8, 10–13, 15–19, 24, 26, 28, 29, 39, 40, 43