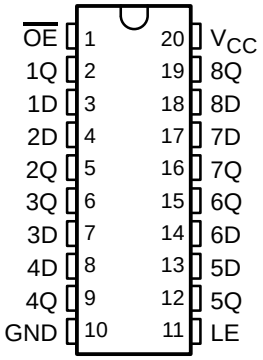
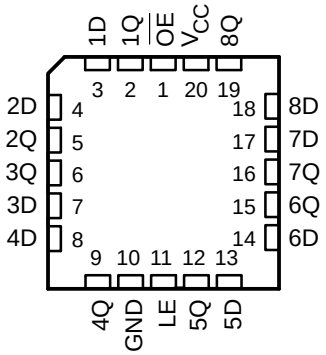
- **Operating Range 2-V to 5.5-V $V_{CC}$**
- **Latch-Up Performance Exceeds 250 mA Per JESD 17**
- **ESD Protection Exceeds JESD 22**
  - **2000-V Human-Body Model (A114-A)**
  - **200-V Machine Model (A115-A)**
  - **1000-V Charged-Device Model (C101)**

**SN54AHC373 . . . J OR W PACKAGE**
**SN74AHC373 . . . DB, DGV, DW, N, NS, OR PW PACKAGE**
**(TOP VIEW)**




**SN54AHC373 . . . FK PACKAGE**
**(TOP VIEW)**




## description/ordering information

The ’AHC373 devices are octal transparent D-type latches designed for 2-V to 5.5-V $V_{CC}$ operation.

When the latch-enable (LE) input is high, the Q outputs follow the data (D) inputs. When LE is low, the Q outputs are latched at the logic levels of the D inputs.

A buffered output-enable ($\overline{OE}$) input can be used to place the eight outputs in either a normal logic state (high or low) or the high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and increased drive provide the capability to drive bus lines without interface or pullup components.

**ORDERING INFORMATION**

| $T_A$ | PACKAGE† | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|---|---|---|---|---|
| –40°C to 85°C | PDIP – N | Tube | SN74AHC373N | SN74AHC373N |
| | SOIC – DW | Tube | SN74AHC373DW | AHC373 |
| | | Tape and reel | SN74AHC373DWR | |
| | SOP – NS | Tape and reel | SN74AHC373NSR | AHC373 |
| | SSOP – DB | Tape and reel | SN74AHC373DBR | HA373 |
| | TSSOP – PW | Tube | SN74AHC373PW | HA373 |
| | | Tape and reel | SN74AHC373PWR | |
| | TVSOP – DGV | Tape and reel | SN74AHC373DGVR | HA373 |
| –55°C to 125°C | CDIP – J | Tube | SNJ54AHC373J | SNJ54AHC373J |
| | CFP – W | Tube | SNJ54AHC373W | SNJ54AHC373W |
| | LCCC – FK | Tube | SNJ54AHC373FK | SNJ54AHC373FK |

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

## description/ordering information (continued)

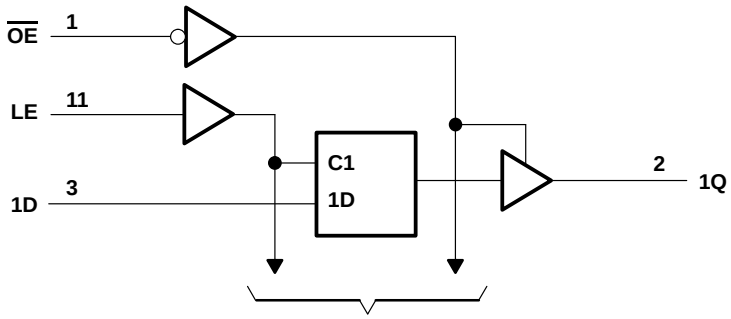
$\overline{OE}$ does not affect the internal operations of the latches. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to $V_{CC}$ through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

**FUNCTION TABLE**
**(each latch)**

| INPUTS | | | OUTPUT |
|---|---|---|---|
| $\overline{OE}$ | LE | D | Q |
| L | H | H | H |
| L | H | L | L |
| L | L | X | $Q_0$ |
| H | X | X | Z |

## logic diagram (positive logic)




## absolute maximum ratings over operating free-air temperature range (unless otherwise noted)†

Supply voltage range, $V_{CC}$ . . . . . –0.5 V to 7 V
Input voltage range, $V_I$ (see Note 1) . . . . . –0.5 V to 7 V
Output voltage range, $V_O$ (see Note 1) . . . . . –0.5 V to $V_{CC}$ + 0.5 V
Input clamp current, $I_{IK}$ ($V_I$ < 0) . . . . . –20 mA
Output clamp current, $I_{OK}$ ($V_O$ < 0 or $V_O$ > $V_{CC}$) . . . . . ±20 mA
Continuous output current, $I_O$ ($V_O$ = 0 to $V_{CC}$) . . . . . ±25 mA
Continuous current through $V_{CC}$ or GND . . . . . ±75 mA
Package thermal impedance, $\theta_{JA}$ (see Note 2): DB package . . . . . 70°C/W
DGV package . . . . . 92°C/W
DW package . . . . . 58°C/W
N package . . . . . 69°C/W
NS package . . . . . 60°C/W
PW package . . . . . 83°C/W
Storage temperature range, $T_{stg}$ . . . . . –65°C to 150°C

† Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

NOTES: 1. The input and output voltage ratings may be exceeded if the input and output current ratings are observed.
2. The package thermal impedance is calculated in accordance with JESD 51-7.

## recommended operating conditions (see Note 3)

| | | | SN54AHC373 | | SN74AHC373 | | UNIT |
|---|---|---|---|---|---|---|---|
| | | | MIN | MAX | MIN | MAX | |
| $V_{CC}$ | Supply voltage | | 2 | 5.5 | 2 | 5.5 | V |
| $V_{IH}$ | High-level input voltage | $V_{CC}$ = 2 V | 1.5 | | 1.5 | | V |
| | | $V_{CC}$ = 3 V | 2.1 | | 2.1 | | |
| | | $V_{CC}$ = 5.5 V | 3.85 | | 3.85 | | |
| $V_{IL}$ | Low-level input voltage | $V_{CC}$ = 2 V | | 0.5 | | 0.5 | V |
| | | $V_{CC}$ = 3 V | | 0.9 | | 0.9 | |
| | | $V_{CC}$ = 5.5 V | | 1.65 | | 1.65 | |
| $V_I$ | Input voltage | | 0 | 5.5 | 0 | 5.5 | V |
| $V_O$ | Output voltage | | 0 | $V_{CC}$ | 0 | $V_{CC}$ | V |
| $I_{OH}$ | High-level output current | $V_{CC}$ = 2 V | | –50 | | –50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | –4 | | –4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | –8 | | –8 | |
| $I_{OL}$ | Low-level output current | $V_{CC}$ = 2 V | | 50 | | 50 | μA |
| | | $V_{CC}$ = 3.3 V ± 0.3 V | | 4 | | 4 | mA |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 8 | | 8 | |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | $V_{CC}$ = 3.3 V ± 0.3 V | | 100 | | 100 | ns/V |
| | | $V_{CC}$ = 5 V ± 0.5 V | | 20 | | 20 | |
| $T_A$ | Operating free-air temperature | | –55 | 125 | –40 | 85 | °C |

NOTE 3: All unused inputs of the device must be held at $V_{CC}$ or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## electrical characteristics over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | $V_{CC}$ | $T_A$ = 25°C | | | SN54AHC373 | | SN74AHC373 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|
| | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $V_{OH}$ | $I_{OH}$ = –50 μA | 2 V | 1.9 | | | 1.9 | | 1.9 | | V |
| | | 3 V | 2.9 | | | 2.9 | | 2.9 | | |
| | | 4.5 V | 4.4 | | | 4.4 | | 4.4 | | |
| | $I_{OH}$ = –4 mA | 3 V | 2.58 | | | 2.48 | | 2.48 | | |
| | $I_{OH}$ = –8 mA | 4.5 V | 3.94 | | | 3.8 | | 3.8 | | |
| $V_{OL}$ | $I_{OL}$ = 50 μA | 2 V | | | 0.1 | | 0.1 | | 0.1 | V |
| | | 3 V | | | 0.1 | | 0.1 | | 0.1 | |
| | | 4.5 V | | | 0.1 | | 0.1 | | 0.1 | |
| | $I_{OL}$ = 4 mA | 3 V | | | 0.36 | | 0.5 | | 0.44 | |
| | $I_{OL}$ = 8 mA | 4.5 V | | | 0.36 | | 0.5 | | 0.44 | |
| $I_I$ | $V_I$ = 5.5 V or GND | 0 V to 5.5 V | | | ±0.1 | | ±1* | | ±1 | μA |
| $I_{OZ}$ | $V_I$ = $V_{IH}$ or $V_{IL}$, $V_O$ = $V_{CC}$ or GND | 5.5 V | | | ±0.25 | | ±2.5 | | ±2.5 | μA |
| $I_{CC}$ | $V_I$ = $V_{CC}$ or GND, $I_O$ = 0 | 5.5 V | | | 4 | | 40 | | 40 | μA |
| $C_i$ | $V_I$ = $V_{CC}$ or GND | 5 V | | 4 | 10 | | | | 10 | pF |
| $C_o$ | $V_O$ = $V_{CC}$ or GND | 5 V | | 6 | | | | | | pF |

* On products compliant to MIL-PRF-38535, this parameter is not production tested at $V_{CC}$ = 0 V.

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54AHC373 | | SN74AHC373 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 4 | | 4 | | 4 | | ns |
| $t_h$ | Hold time, data after LE↓ | 1 | | 1 | | 1 | | ns |

### timing requirements over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| | | $T_A$ = 25°C | | SN54AHC373 | | SN74AHC373 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | MIN | MAX | MIN | MAX | MIN | MAX | |
| $t_w$ | Pulse duration, LE high | 5 | | 5 | | 5 | | ns |
| $t_{su}$ | Setup time, data before LE↓ | 4 | | 4 | | 4 | | ns |
| $t_h$ | Hold time, data after LE↓ | 1 | | 1 | | 1 | | ns |

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 3.3 V ± 0.3 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC373 | | SN74AHC373 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | D | Q | $C_L$ = 15 pF | | 7.3* | 11.4* | 1* | 13.5* | 1 | 13.5 | ns |
| $t_{PHL}$ | | | | | 7.3* | 11.4* | 1* | 13.5* | 1 | 13.5 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 15 pF | | 7* | 11* | 1* | 13* | 1 | 13 | ns |
| $t_{PHL}$ | | | | | 7* | 11* | 1* | 13* | 1 | 13 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7.3* | 11.4* | 1* | 13.5* | 1 | 13.5 | ns |
| $t_{PZL}$ | | | | | 7.3* | 11.4* | 1* | 13.5* | 1 | 13.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 7* | 10* | 1* | 12* | 1 | 12 | ns |
| $t_{PLZ}$ | | | | | 7* | 10* | 1* | 12* | 1 | 12 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 9.8 | 14.9 | 1 | 17 | 1 | 17 | ns |
| $t_{PHL}$ | | | | | 9.8 | 14.9 | 1 | 17 | 1 | 17 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 9.5 | 14.5 | 1 | 16.5 | 1 | 16.5 | ns |
| $t_{PHL}$ | | | | | 9.5 | 14.5 | 1 | 16.5 | 1 | 16.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 9.8 | 14.9 | 1 | 17 | 1 | 17 | ns |
| $t_{PZL}$ | | | | | 9.8 | 14.9 | 1 | 17 | 1 | 17 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 9.5 | 13.2 | 1 | 15 | 1 | 15 | ns |
| $t_{PLZ}$ | | | | | 9.5 | 13.2 | 1 | 15 | 1 | 15 | |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | | 1.5** | | | | 1.5 | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
** On products compliant to MIL-PRF-38535, this parameter does not apply.

### switching characteristics over recommended operating free-air temperature range, $V_{CC}$ = 5 V ± 0.5 V (unless otherwise noted) (see Figure 1)

| PARAMETER | FROM (INPUT) | TO (OUTPUT) | LOAD CAPACITANCE | $T_A$ = 25°C | | | SN54AHC373 | | SN74AHC373 | | UNIT |
|---|---|---|---|---|---|---|---|---|---|---|---|
| | | | | MIN | TYP | MAX | MIN | MAX | MIN | MAX | |
| $t_{PLH}$ | D | Q | $C_L$ = 15 pF | | 5* | 7.2* | 1* | 8.5* | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 5* | 7.2* | 1* | 8.5* | 1 | 8.5 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 15 pF | | 4.9* | 7.2* | 1* | 8.5* | 1 | 8.5 | ns |
| $t_{PHL}$ | | | | | 4.9* | 7.2* | 1* | 8.5* | 1 | 8.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5.5* | 8.1* | 1* | 9.5* | 1 | 9.5 | ns |
| $t_{PZL}$ | | | | | 5.5* | 8.1* | 1* | 9.5* | 1 | 9.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 15 pF | | 5* | 7.2* | 1* | 8.5* | 1 | 8.5 | ns |
| $t_{PLZ}$ | | | | | 5* | 7.2* | 1* | 8.5* | 1 | 8.5 | |
| $t_{PLH}$ | D | Q | $C_L$ = 50 pF | | 6.5 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.5 | 9.2 | 1 | 10.5 | 1 | 10.5 | |
| $t_{PLH}$ | LE | Q | $C_L$ = 50 pF | | 6.4 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns |
| $t_{PHL}$ | | | | | 6.4 | 9.2 | 1 | 10.5 | 1 | 10.5 | |
| $t_{PZH}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 7 | 10.1 | 1 | 11.5 | 1 | 11.5 | ns |
| $t_{PZL}$ | | | | | 7 | 10.1 | 1 | 11.5 | 1 | 11.5 | |
| $t_{PHZ}$ | $\overline{OE}$ | Q | $C_L$ = 50 pF | | 6.5 | 9.2 | 1 | 10.5 | 1 | 10.5 | ns |
| $t_{PLZ}$ | | | | | 6.5 | 9.2 | 1 | 10.5 | 1 | 10.5 | |
| $t_{sk(o)}$ | | | $C_L$ = 50 pF | | | 1** | | | | 1 | ns |

* On products compliant to MIL-PRF-38535, this parameter is not production tested.
** On products compliant to MIL-PRF-38535, this parameter does not apply.

### noise characteristics, $V_{CC}$ = 5 V, $C_L$ = 50 pF, $T_A$ = 25°C (see Note 4)

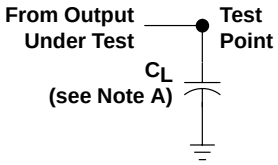
| PARAMETER | | SN74AHC373 | | UNIT |
|---|---|---|---|---|
| | | MIN | MAX | |
| $V_{OL(P)}$ | Quiet output, maximum dynamic $V_{OL}$ | | 0.8 | V |
| $V_{OL(V)}$ | Quiet output, minimum dynamic $V_{OL}$ | | –0.8 | V |
| $V_{OH(V)}$ | Quiet output, minimum dynamic $V_{OH}$ | 4.1 | | V |
| $V_{IH(D)}$ | High-level dynamic input voltage | 3.5 | | V |
| $V_{IL(D)}$ | Low-level dynamic input voltage | | 1.5 | V |

NOTE 4: Characteristics are for surface-mount packages only.

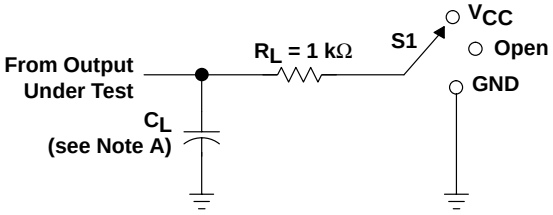
### operating characteristics, $V_{CC}$ = 5 V, $T_A$ = 25°C

| PARAMETER | | TEST CONDITIONS | | TYP | UNIT |
|---|---|---|---|---|---|
| $C_{pd}$ | Power dissipation capacitance | No load, | f = 1 MHz | 18 | pF |

## PARAMETER MEASUREMENT INFORMATION

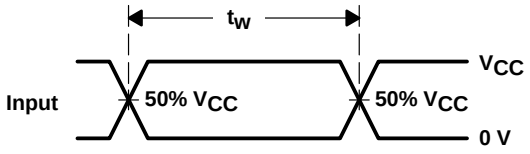



LOAD CIRCUIT FOR
TOTEM-POLE OUTPUTS

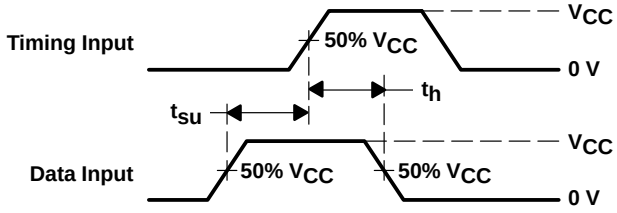



LOAD CIRCUIT FOR
3-STATE AND OPEN-DRAIN OUTPUTS

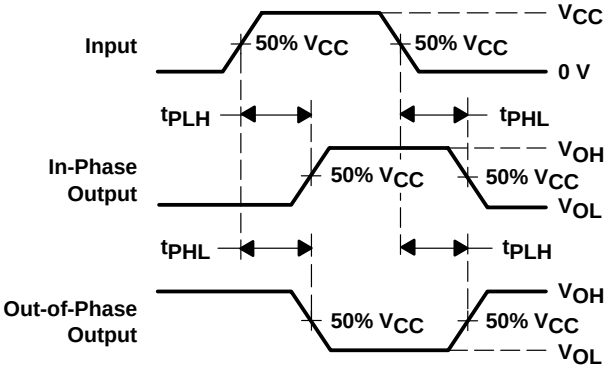
| TEST | S1 |
|---|---|
| $t_{PLH}/t_{PHL}$ | Open |
| $t_{PLZ}/t_{PZL}$ | $V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND |
| Open Drain | $V_{CC}$ |



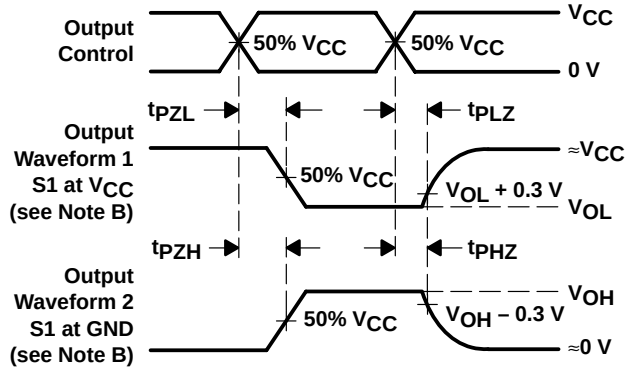

VOLTAGE WAVEFORMS
PULSE DURATION




VOLTAGE WAVEFORMS
SETUP AND HOLD TIMES




VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES
INVERTING AND NONINVERTING OUTPUTS




VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES
LOW- AND HIGH-LEVEL ENABLING

NOTES: A. $C_L$ includes probe and jig capacitance.
B. Waveform 1 is for an output with internal conditions such that the output is low except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high except when disabled by the output control.
C. All input pulses are supplied by generators having the following characteristics: PRR ≤ 1 MHz, $Z_O$ = 50 Ω, $t_r$ ≤ 3 ns, $t_f$ ≤ 3 ns.
D. The outputs are measured one at a time with one input transition per measurement.
E. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| 5962-9686601Q2A | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9686601Q2A SNJ54AHC373FK | Samples |
| 5962-9686601QRA | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-9686601QRA SNJ54AHC373J | Samples |
| 5962-9686601QSA | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-9686601QSA SNJ54AHC373W | Samples |
| SN74AHC373DBR | ACTIVE | SSOP | DB | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HA373 | Samples |
| SN74AHC373DGVR | ACTIVE | TVSOP | DGV | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HA373 | Samples |
| SN74AHC373DW | ACTIVE | SOIC | DW | 20 | 25 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AHC373 | Samples |
| SN74AHC373DWR | ACTIVE | SOIC | DW | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AHC373 | Samples |
| SN74AHC373N | ACTIVE | PDIP | N | 20 | 20 | Pb-Free (RoHS) | NIPDAU | N / A for Pkg Type | -40 to 85 | SN74AHC373N | Samples |
| SN74AHC373NSR | ACTIVE | SO | NS | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | AHC373 | Samples |
| SN74AHC373PW | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HA373 | Samples |
| SN74AHC373PWG4 | ACTIVE | TSSOP | PW | 20 | 70 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HA373 | Samples |
| SN74AHC373PWR | ACTIVE | TSSOP | PW | 20 | 2000 | Green (RoHS & no Sb/Br) | NIPDAU | Level-1-260C-UNLIM | -40 to 85 | HA373 | Samples |
| SNJ54AHC373FK | ACTIVE | LCCC | FK | 20 | 1 | TBD | POST-PLATE | N / A for Pkg Type | -55 to 125 | 5962-9686601Q2A SNJ54AHC373FK | Samples |
| SNJ54AHC373J | ACTIVE | CDIP | J | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-9686601QRA SNJ54AHC373J | Samples |

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead/Ball Finish (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| SNJ54AHC373W | ACTIVE | CFP | W | 20 | 1 | TBD | Call TI | N / A for Pkg Type | -55 to 125 | 5962-9686601QSA SNJ54AHC373W | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.



**OTHER QUALIFIED VERSIONS OF SN54AHC373, SN74AHC373 :**

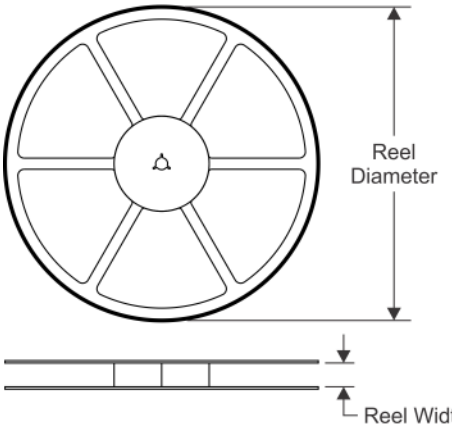
- Catalog: SN74AHC373
- Military: SN54AHC373

NOTE: Qualified Version Definitions:

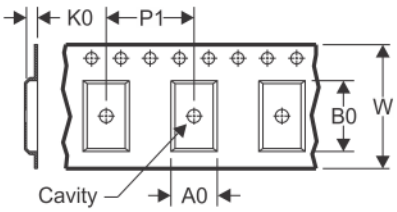
- Catalog - TI's standard catalog product
- Military - QML certified for Military and Defense Applications

## TAPE AND REEL INFORMATION

REEL DIMENSIONS

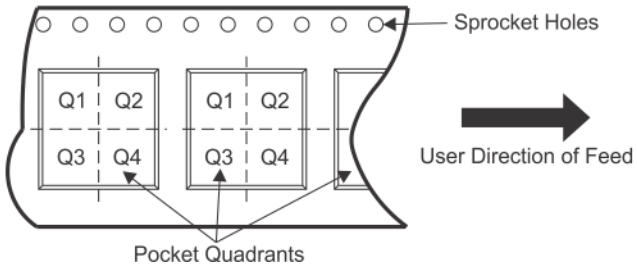



TAPE DIMENSIONS




| | |
|---|---|
| A0 | Dimension designed to accommodate the component width |
| B0 | Dimension designed to accommodate the component length |
| K0 | Dimension designed to accommodate the component thickness |
| W | Overall width of the carrier tape |
| P1 | Pitch between successive cavity centers |

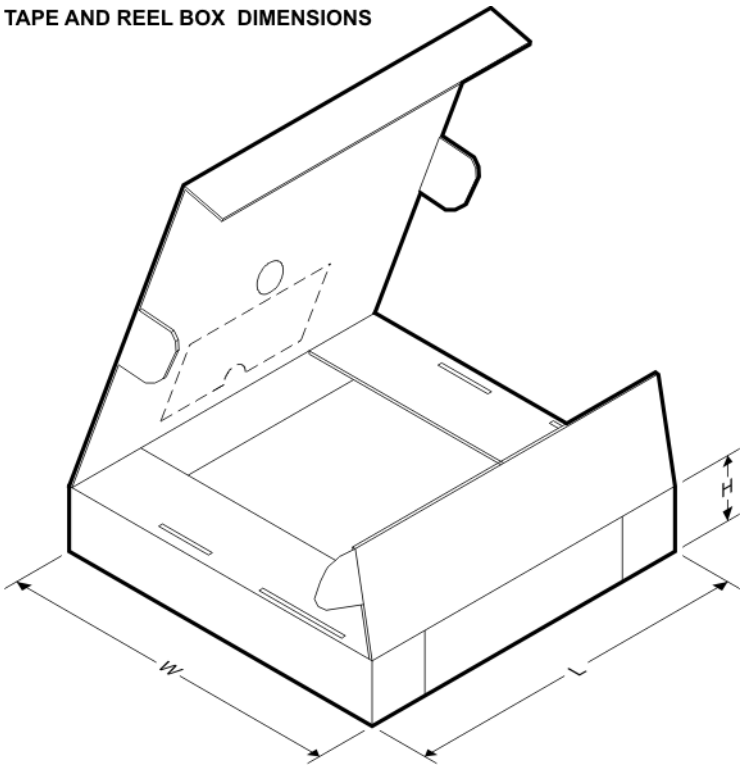
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|---|---|---|---|---|---|---|---|---|---|---|---|---|
| SN74AHC373DBR | SSOP | DB | 20 | 2000 | 330.0 | 16.4 | 8.2 | 7.5 | 2.5 | 12.0 | 16.0 | Q1 |
| SN74AHC373DGVR | TVSOP | DGV | 20 | 2000 | 330.0 | 12.4 | 6.9 | 5.6 | 1.6 | 8.0 | 12.0 | Q1 |
| SN74AHC373DWR | SOIC | DW | 20 | 2000 | 330.0 | 24.4 | 10.8 | 13.3 | 2.7 | 12.0 | 24.0 | Q1 |
| SN74AHC373NSR | SO | NS | 20 | 2000 | 330.0 | 24.4 | 8.4 | 13.0 | 2.5 | 12.0 | 24.0 | Q1 |
| SN74AHC373PWR | TSSOP | PW | 20 | 2000 | 330.0 | 16.4 | 6.95 | 7.1 | 1.6 | 8.0 | 16.0 | Q1 |

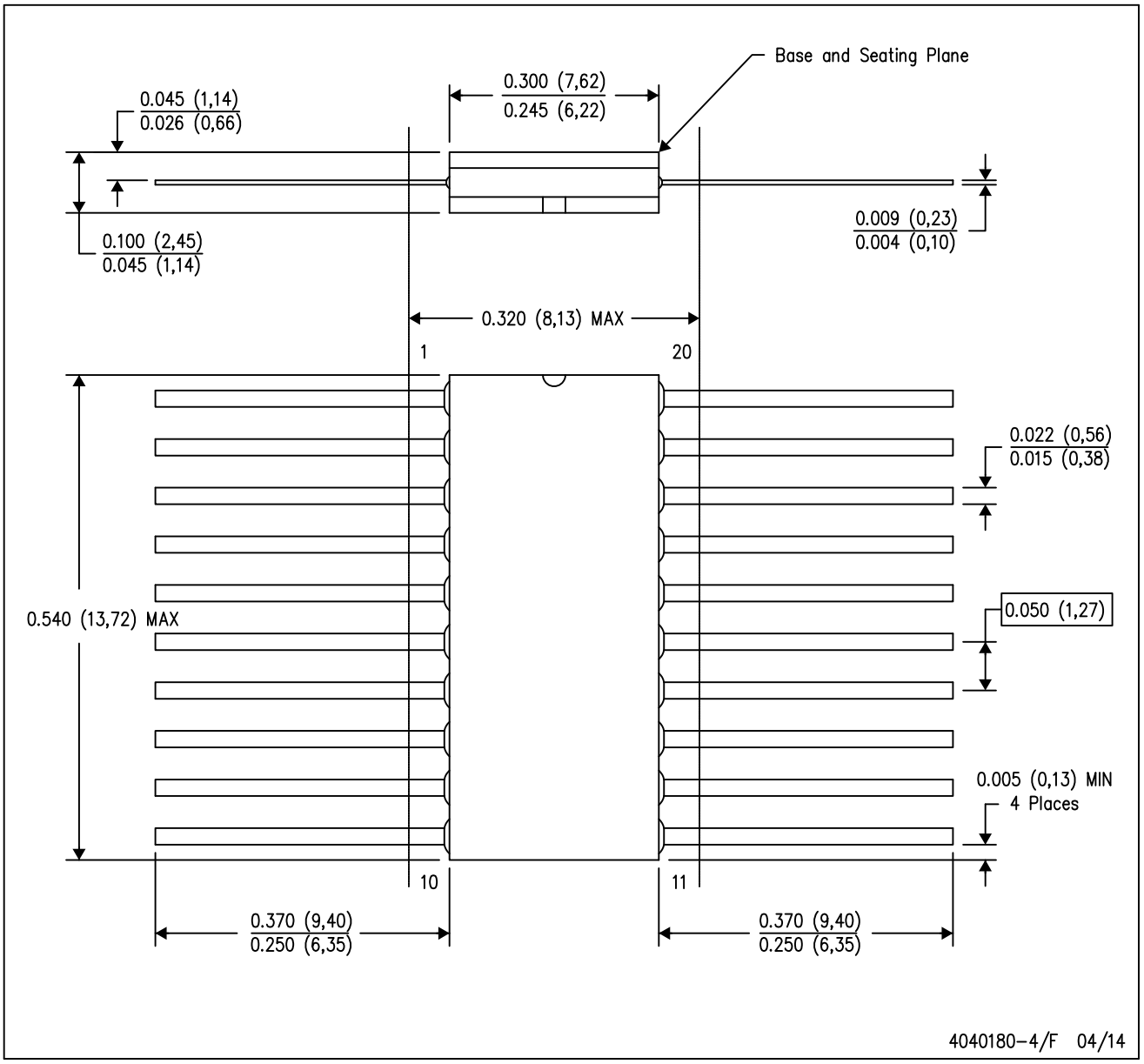
TAPE AND REEL BOX DIMENSIONS




*All dimensions are nominal

| Device | Package Type | Package Drawing | Pins | SPQ | Length (mm) | Width (mm) | Height (mm) |
|---|---|---|---|---|---|---|---|
| SN74AHC373DBR | SSOP | DB | 20 | 2000 | 367.0 | 367.0 | 38.0 |
| SN74AHC373DGVR | TVSOP | DGV | 20 | 2000 | 367.0 | 367.0 | 35.0 |
| SN74AHC373DWR | SOIC | DW | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AHC373NSR | SO | NS | 20 | 2000 | 367.0 | 367.0 | 45.0 |
| SN74AHC373PWR | TSSOP | PW | 20 | 2000 | 367.0 | 367.0 | 38.0 |

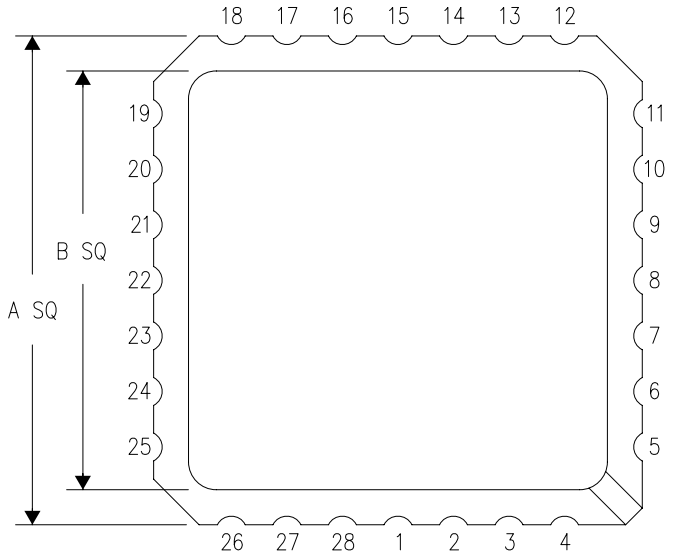
W (R–GDFP–F20) CERAMIC DUAL FLATPACK



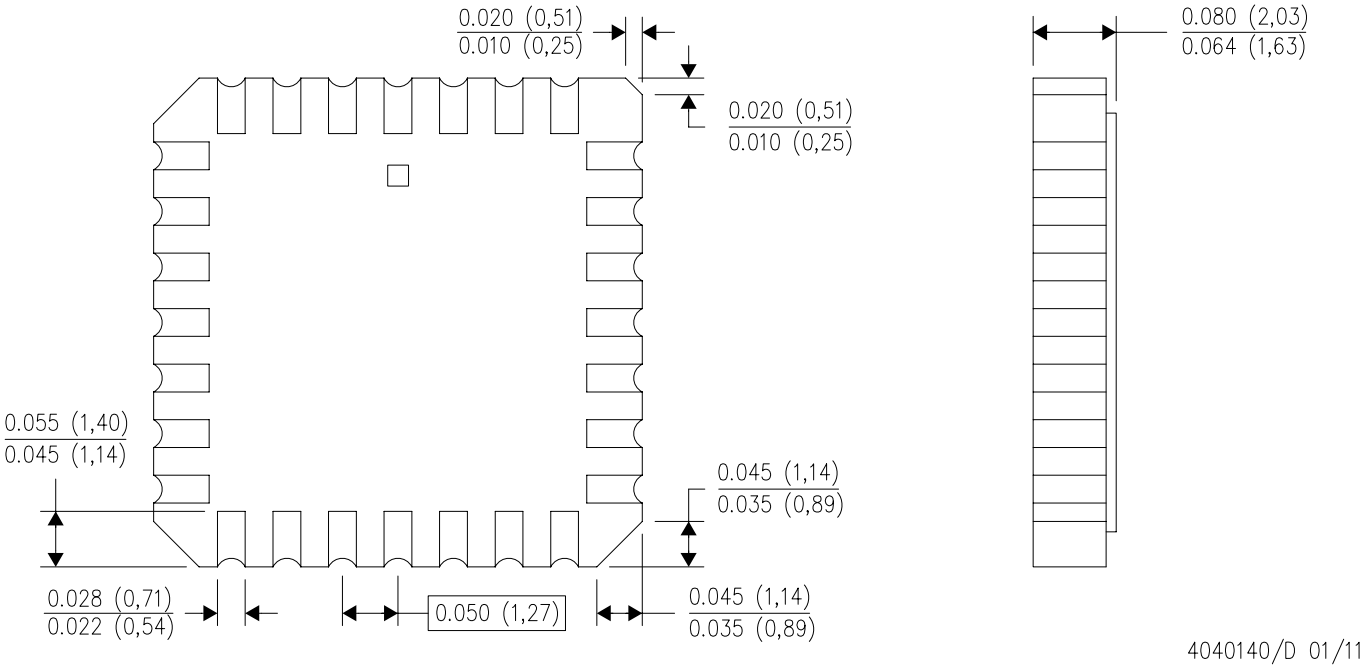

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only.
E. Falls within Mil–Std 1835 GDFP2–F20

FK (S–CQCC–N**) LEADLESS CERAMIC CHIP CARRIER

28 TERMINAL SHOWN




| NO. OF TERMINALS ** | A | | B | |
|---|---|---|---|---|
| | MIN | MAX | MIN | MAX |
| 20 | 0.342 (8,69) | 0.358 (9,09) | 0.307 (7,80) | 0.358 (9,09) |
| 28 | 0.442 (11,23) | 0.458 (11,63) | 0.406 (10,31) | 0.458 (11,63) |
| 44 | 0.640 (16,26) | 0.660 (16,76) | 0.495 (12,58) | 0.560 (14,22) |
| 52 | 0.740 (18,78) | 0.761 (19,32) | 0.495 (12,58) | 0.560 (14,22) |
| 68 | 0.938 (23,83) | 0.962 (24,43) | 0.850 (21,6) | 0.858 (21,8) |
| 84 | 1.141 (28,99) | 1.165 (29,59) | 1.047 (26,6) | 1.063 (27,0) |




4040140/D 01/11

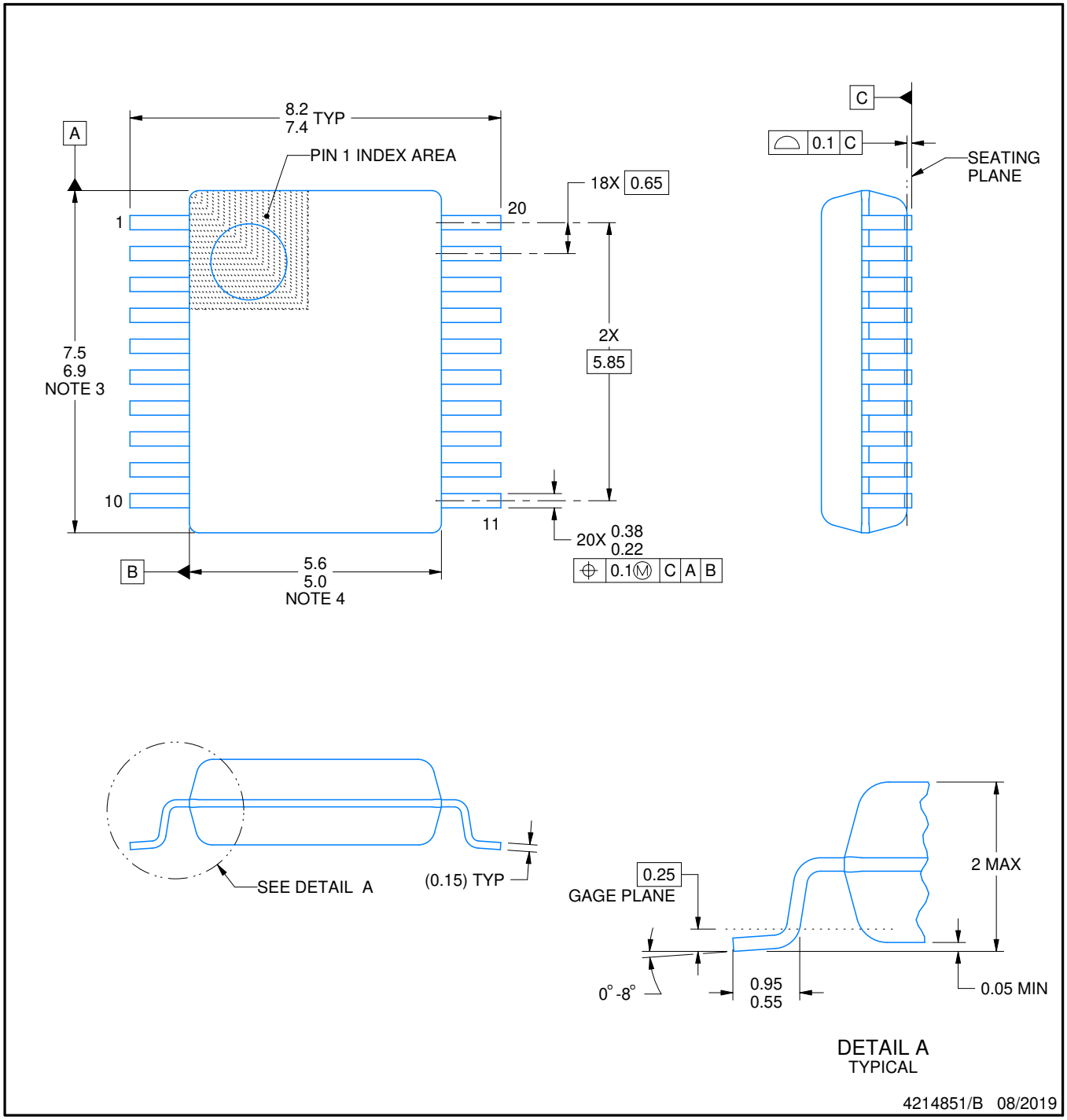
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package can be hermetically sealed with a metal lid.
D. Falls within JEDEC MS–004

# PACKAGE OUTLINE

## DB0020A

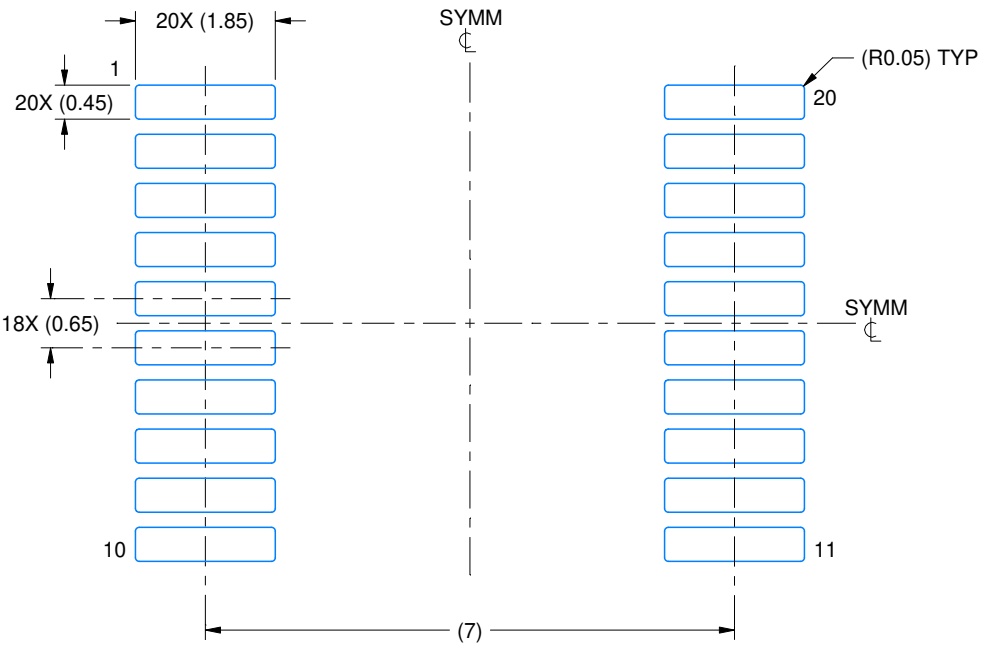
## SSOP - 2 mm max height

SMALL OUTLINE PACKAGE

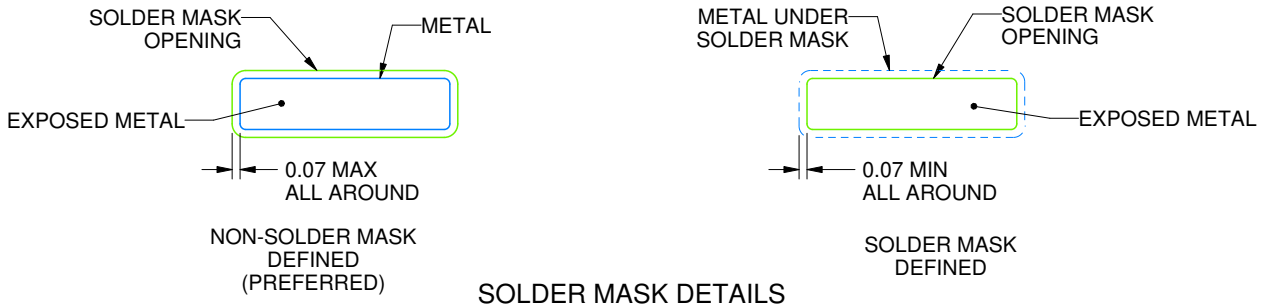



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-150.




LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

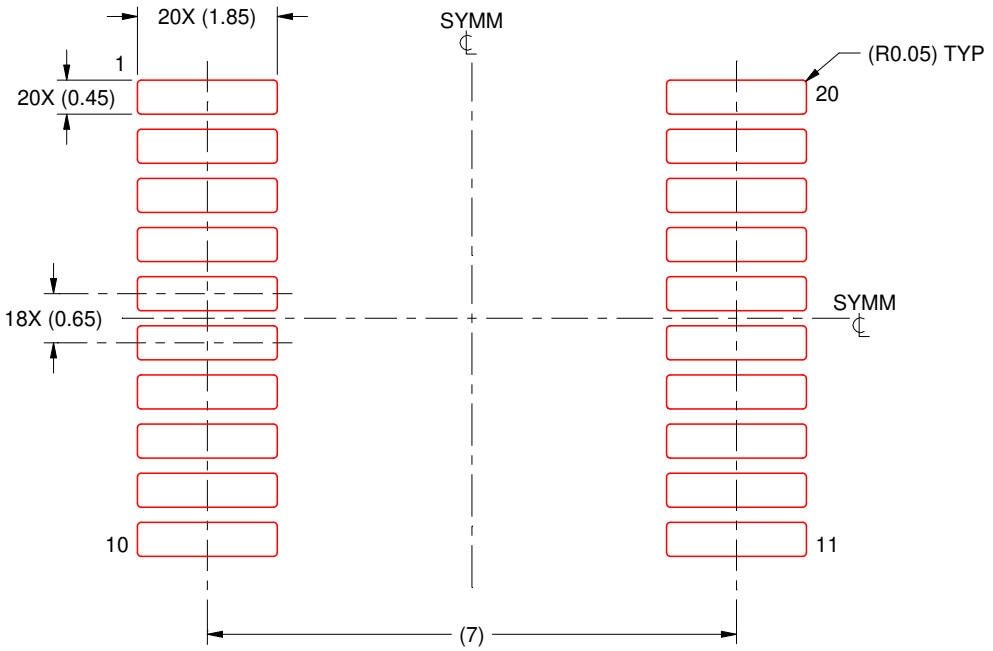



SOLDER MASK DETAILS

4214851/B 08/2019

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4214851/B 08/2019

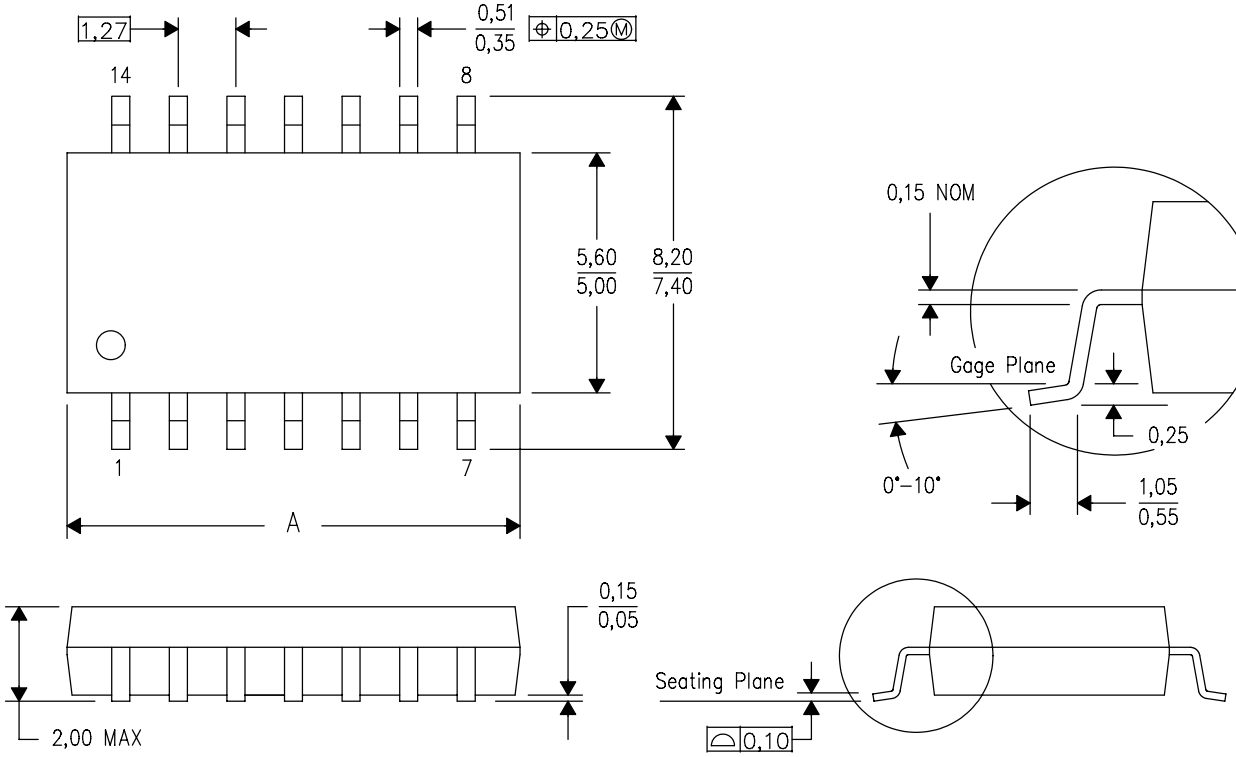
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

## MECHANICAL DATA

**NS (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE PACKAGE**

**14-PINS SHOWN**




| DIM \ PINS ** | 14 | 16 | 20 | 24 |
|---|---|---|---|---|
| A MAX | 10,50 | 10,50 | 12,90 | 15,30 |
| A MIN | 9,90 | 9,90 | 12,30 | 14,70 |

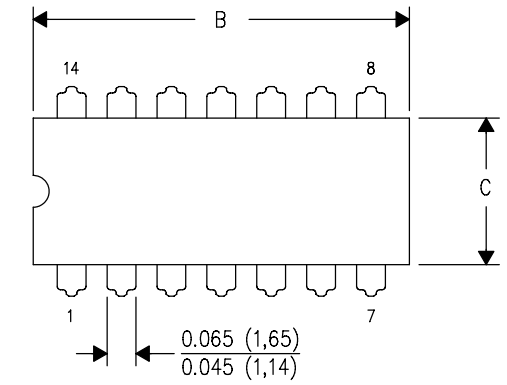
4040062/C 03/03

NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

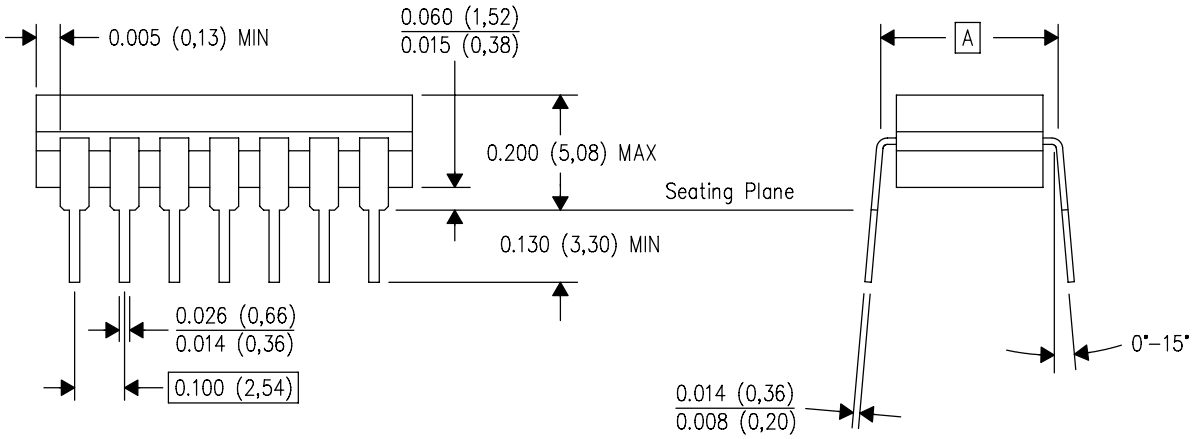
J (R–GDIP–T**)

14 LEADS SHOWN

# CERAMIC DUAL IN–LINE PACKAGE




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC | 0.300 (7,62) BSC |
| B MAX | 0.785 (19,94) | .840 (21,34) | 0.960 (24,38) | 1.060 (26,92) |
| B MIN | — | — | — | — |
| C MAX | 0.300 (7,62) | 0.300 (7,62) | 0.310 (7,87) | 0.300 (7,62) |
| C MIN | 0.245 (6,22) | 0.245 (6,22) | 0.220 (5,59) | 0.245 (6,22) |



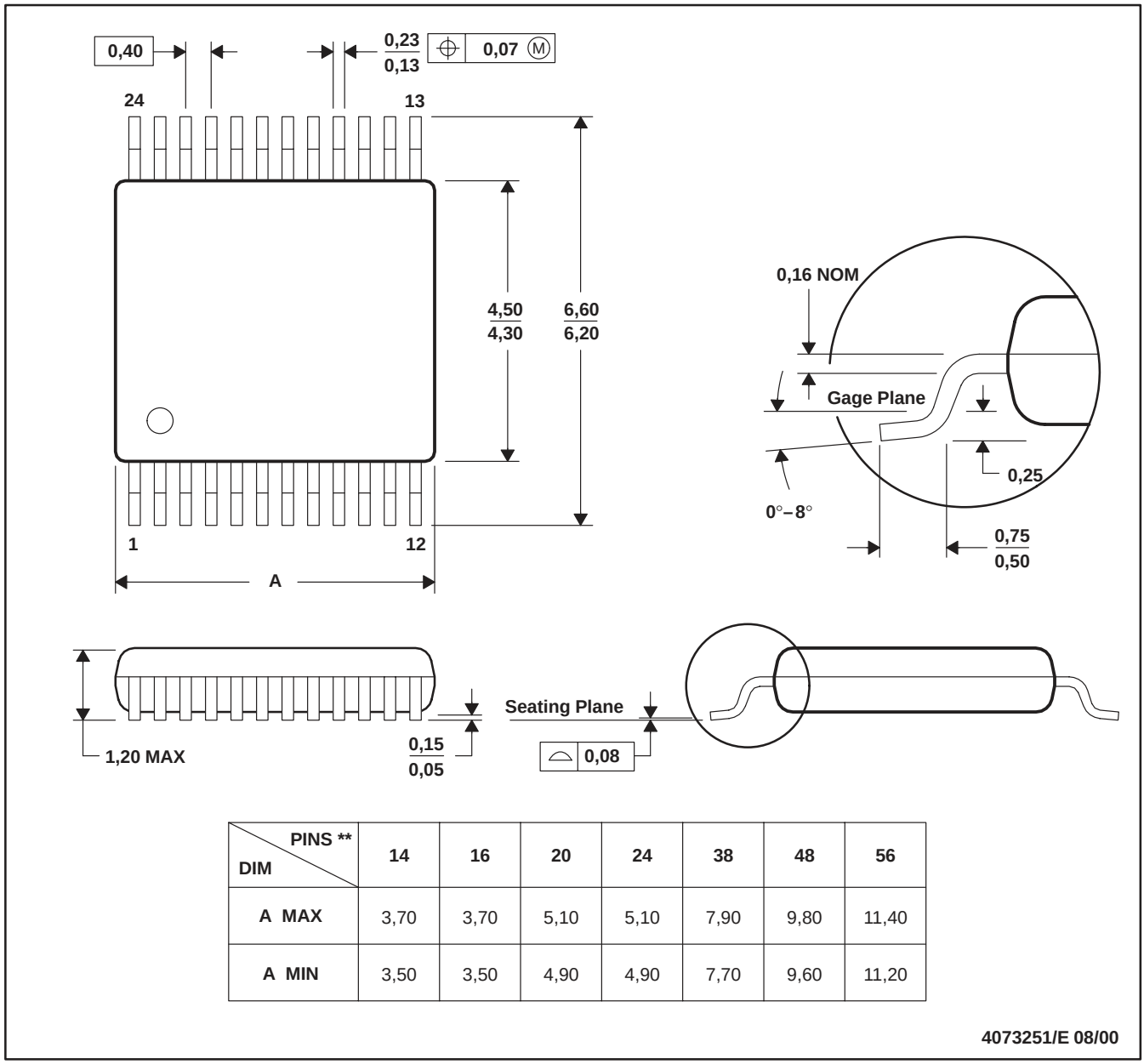

4040083/F 03/03

NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. This package is hermetically sealed with a ceramic lid using glass frit.
D. Index point is provided on cap for terminal identification only on press ceramic glass frit seal only.
E. Falls within MIL STD 1835 GDIP1–T14, GDIP1–T16, GDIP1–T18 and GDIP1–T20.

MPDS006C – FEBRUARY 1996 – REVISED AUGUST 2000

**DGV (R-PDSO-G**)** **PLASTIC SMALL-OUTLINE**

**24 PINS SHOWN**

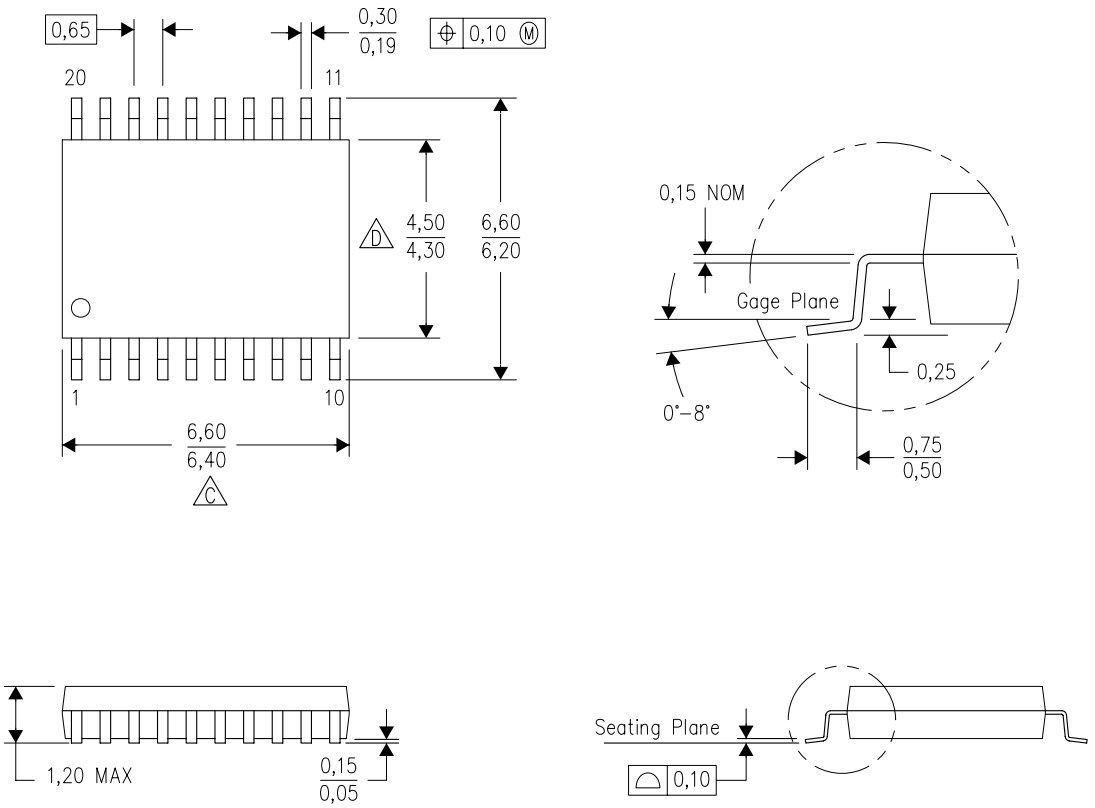



| DIM \ PINS ** | 14 | 16 | 20 | 24 | 38 | 48 | 56 |
|---|---|---|---|---|---|---|---|
| A MAX | 3,70 | 3,70 | 5,10 | 5,10 | 7,90 | 9,80 | 11,40 |
| A MIN | 3,50 | 3,50 | 4,90 | 4,90 | 7,70 | 9,60 | 11,20 |

**4073251/E 08/00**

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
D. Falls within JEDEC: 24/48 Pins – MO-153
14/16/20/56 Pins – MO-194

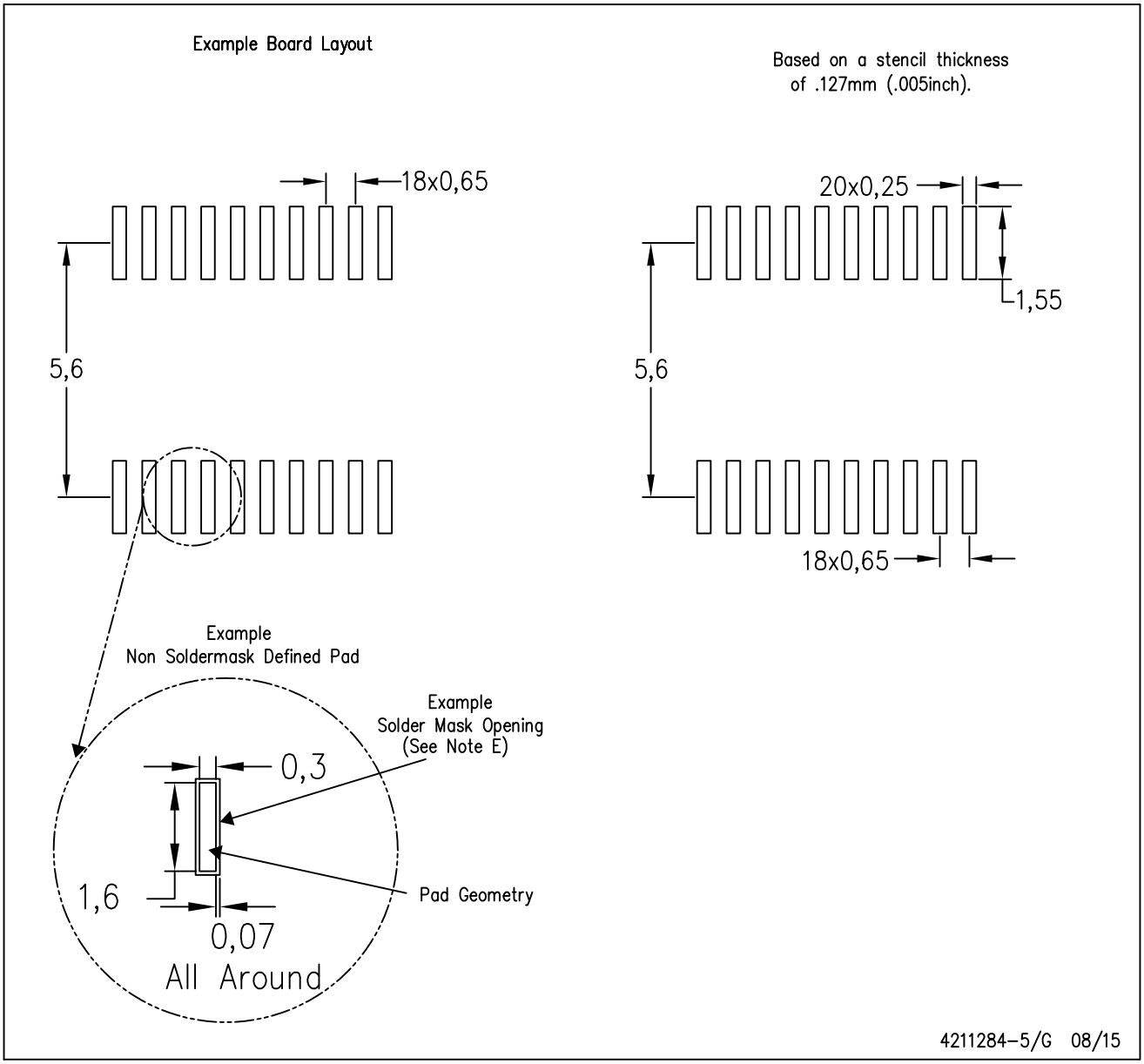
PW (R–PDSO–G20) PLASTIC SMALL OUTLINE




4040064–5/G 02/11

NOTES:
A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M–1994.
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
E. Falls within JEDEC MO–153

PW (R–PDSO–G20) PLASTIC SMALL OUTLINE

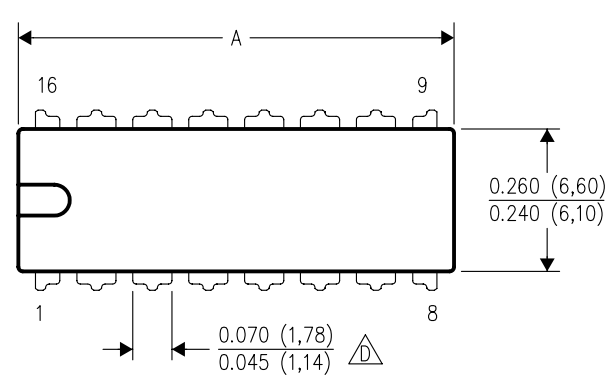



NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate design.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

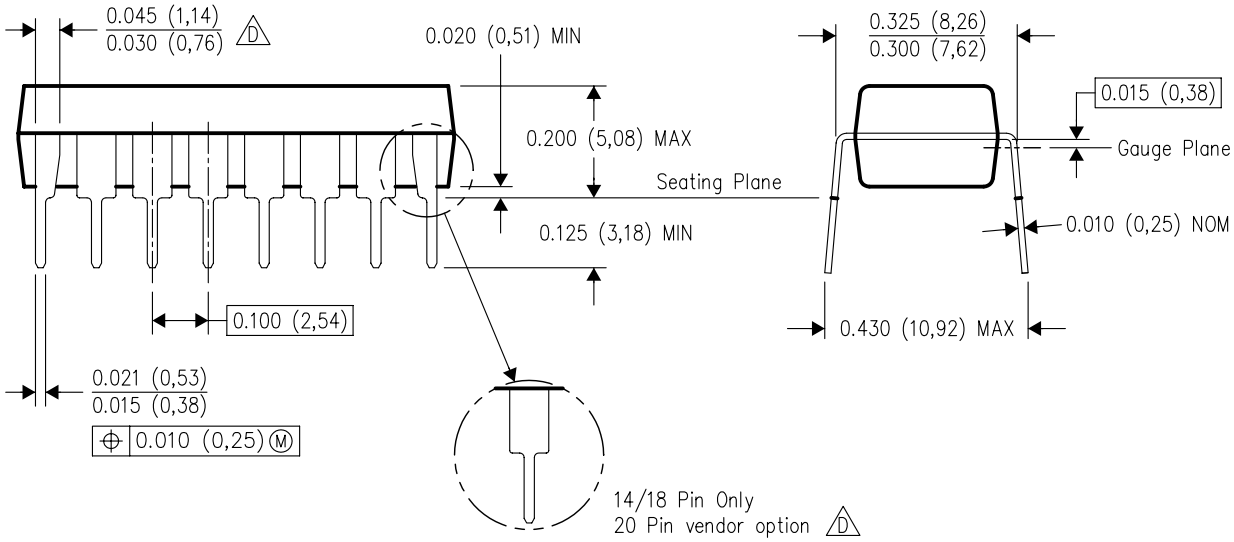
## N (R–PDIP–T**)

## PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN




| DIM \ PINS ** | 14 | 16 | 18 | 20 |
|---|---|---|---|---|
| A MAX | 0.775 (19,69) | 0.775 (19,69) | 0.920 (23,37) | 1.060 (26,92) |
| A MIN | 0.745 (18,92) | 0.745 (18,92) | 0.850 (21,59) | 0.940 (23,88) |
| MS–001 VARIATION (C) | AA | BB | AC | AD |




4040049/E 12/2002

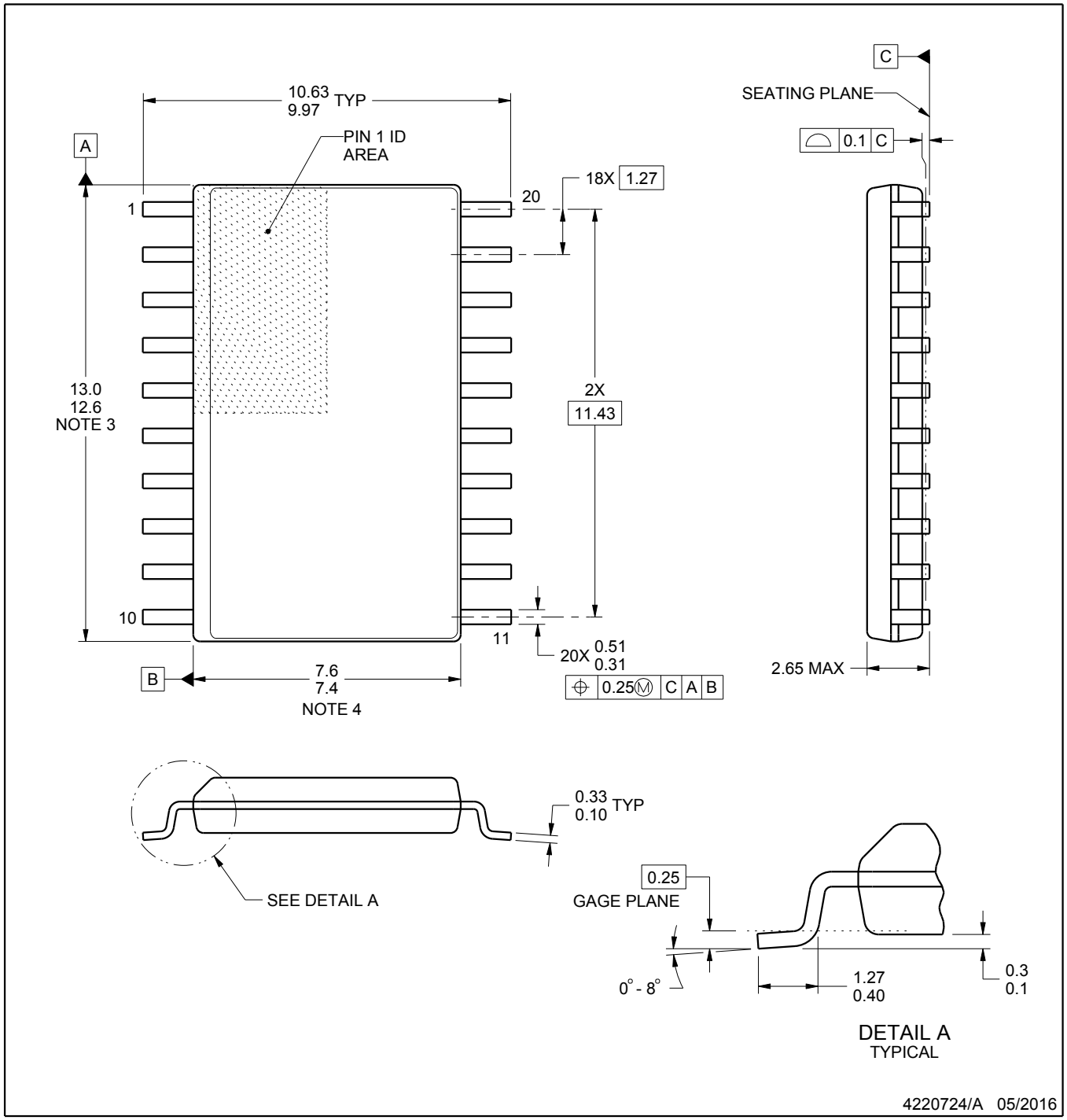
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

# PACKAGE OUTLINE

## DW0020A

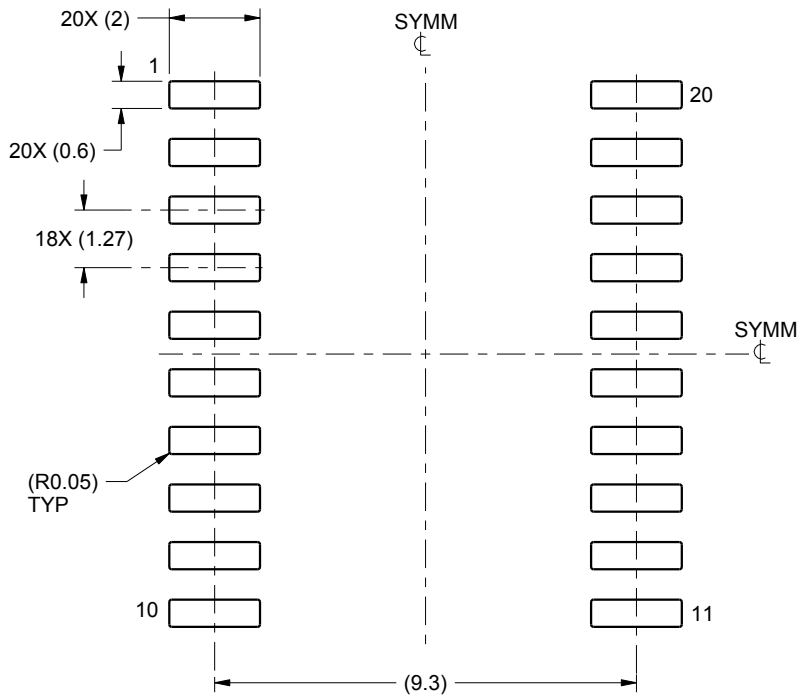
## SOIC - 2.65 mm max height

SOIC

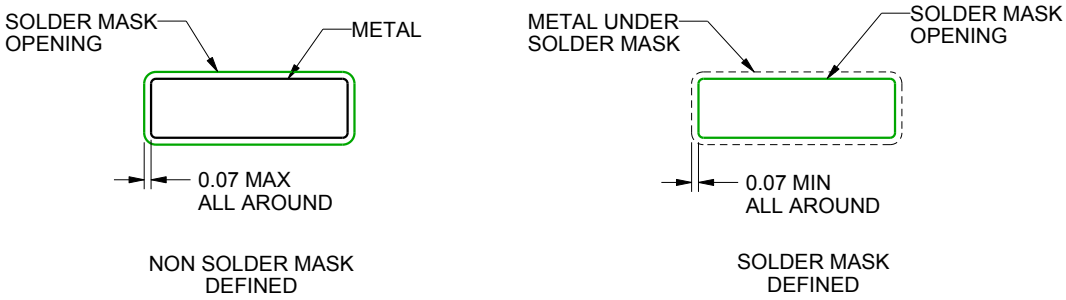



NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.43 mm per side.
5. Reference JEDEC registration MS-013.




LAND PATTERN EXAMPLE
SCALE:6X

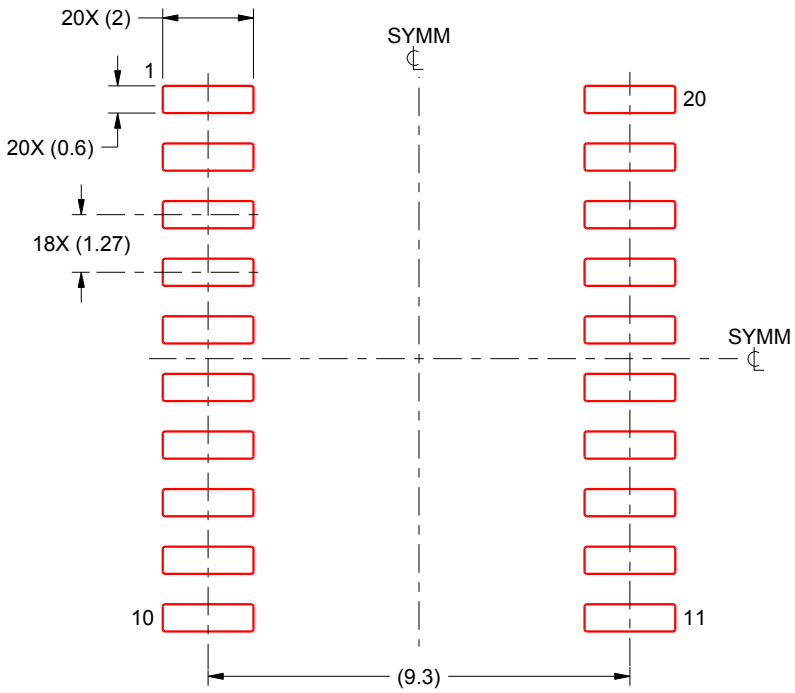



SOLDER MASK DETAILS

4220724/A 05/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.




SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:6X

4220724/A 05/2016

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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