



NX138BKM

60 V, N-channel Trench MOSFET

1 September 2020

Product data sheet

1. General description

N-channel enhancement mode Field-Effect Transistor (FET) in a leadless ultra small DFN1006-3 (SOT883) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

2. Features and benefits

- Low threshold voltage
- Very fast switching
- Trench MOSFET technology
- ElectroStatic Discharge (ESD) protection > 2 kV HBM

3. Applications

- Relay driver
- High-speed line driver
- Low-side loadswitch
- Switching circuits

4. Quick reference data

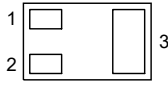
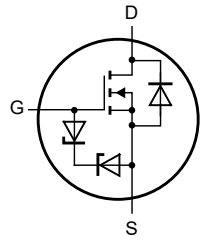
Table 1. Quick reference data

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	60	V
V_{GS}	gate-source voltage		-20	-	20	V
I_D	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}$	[1]	-	380	mA
Static characteristics						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 380\text{ mA}; T_j = 25\text{ °C}$	-	1.8	2.3	Ω

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

5. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	G	gate	 <p>Transparent top view DFN1006-3 (SOT883)</p>	 <p>017aaa255</p>
2	S	source		
3	D	drain		

6. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
NX138BKM	DFN1006-3	plastic, leadless ultra small package; 3 terminals; 0.35 mm pitch; 1 mm x 0.6 mm x 0.48 mm body	SOT883

7. Marking

Table 4. Marking codes

Type number	Marking code
NX138BKM	6R

8. Limiting values

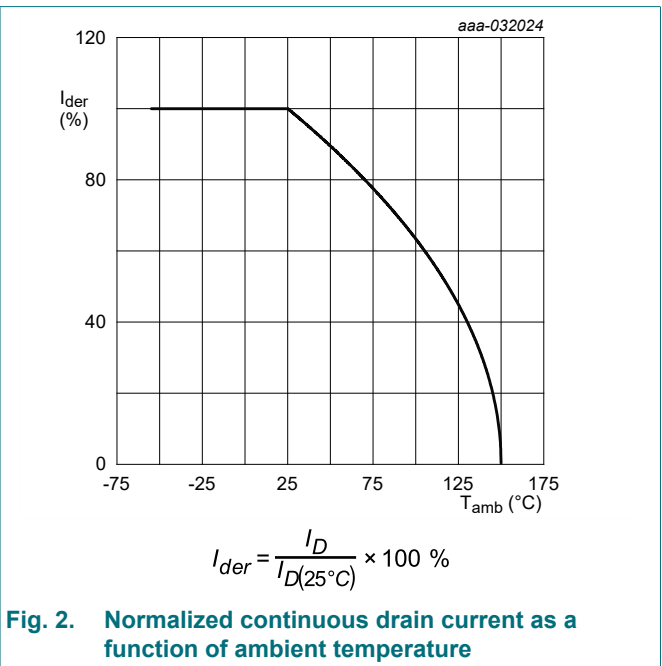
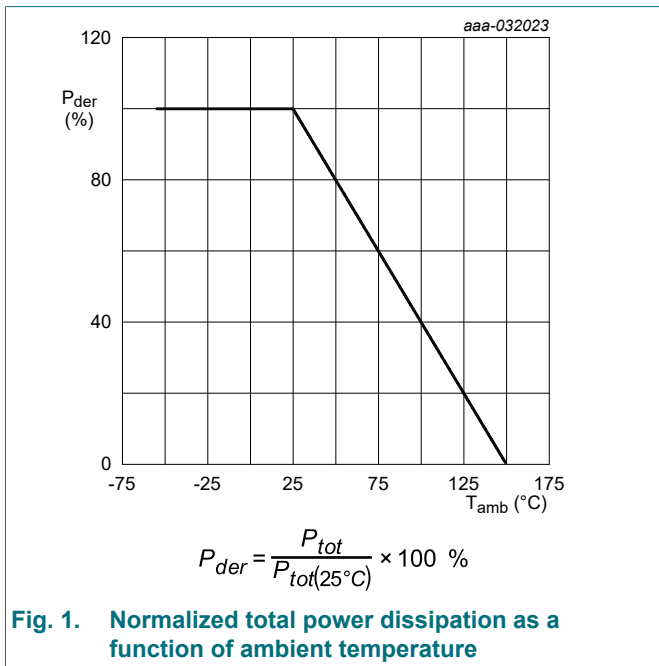
Table 5. Limiting values

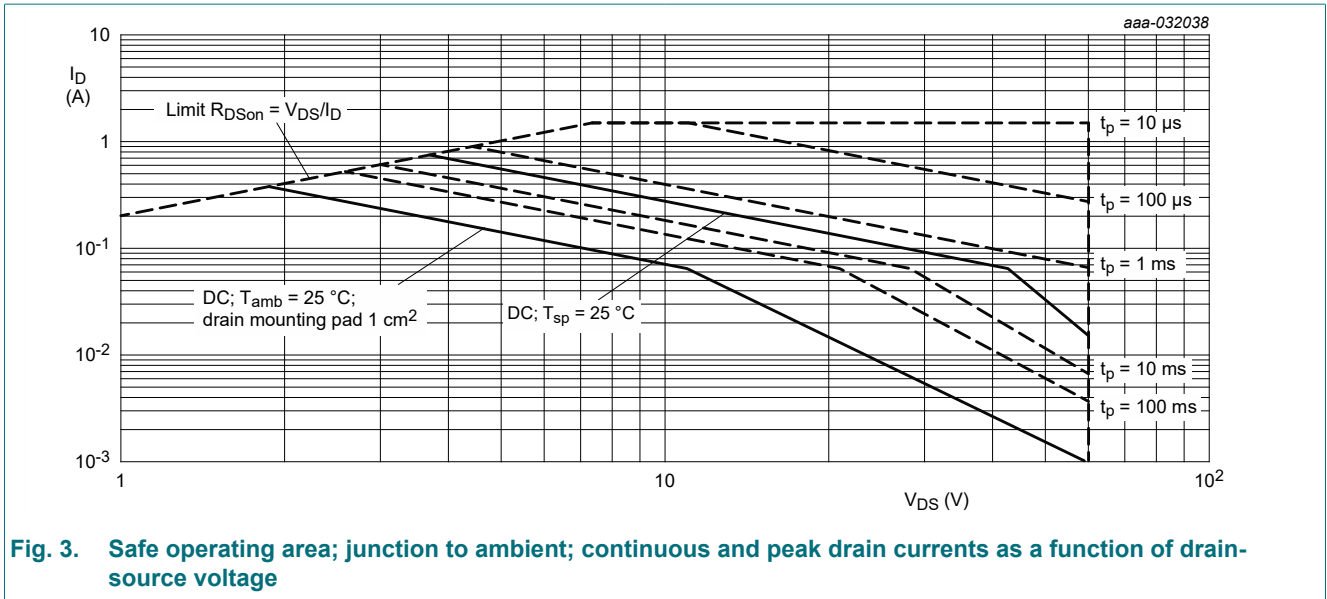
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V _{DS}	drain-source voltage	T _j = 25 °C		-	60	V
V _{GS}	gate-source voltage			-20	20	V
I _D	drain current	V _{GS} = 10 V; T _{amb} = 25 °C	[1]	-	380	mA
		V _{GS} = 10 V; T _{amb} = 100 °C	[1]	-	240	mA
I _{DM}	peak drain current	T _{amb} = 25 °C; single pulse; t _p ≤ 10 μs		-	1.5	A
P _{tot}	total power dissipation	T _{amb} = 25 °C	[2]	-	380	mW
			[1]	-	710	mW
		T _{sp} = 25 °C		-	2.8	W
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _S	source current	T _{amb} = 25 °C	[1]	-	380	mA

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

[2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.





9. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	285	330	K/W
			[2]	-	150	175	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point			-	40	45	K/W

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and mounting pad for drain 1 cm².

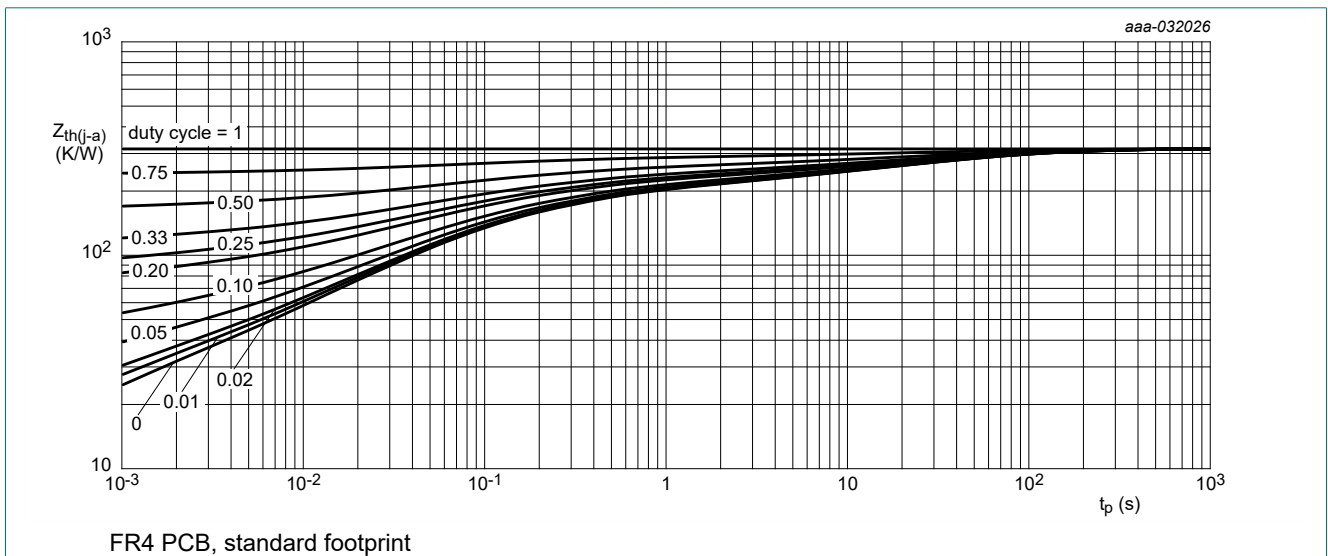


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

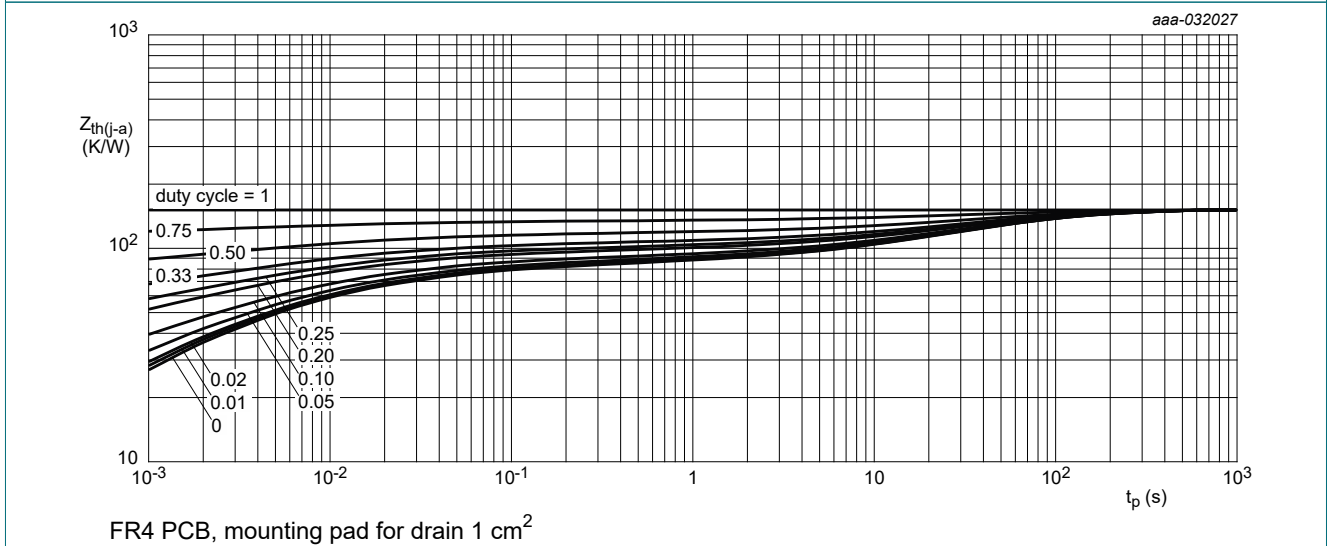


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

10. Characteristics

Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu A$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	60	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = 250 \mu A$; $V_{DS} = V_{GS}$; $T_j = 25 \text{ }^\circ C$	0.5	1	1.5	V
I_{DSS}	drain leakage current	$V_{DS} = 60 V$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	1	μA
I_{GSS}	gate leakage current	$V_{GS} = 20 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	10	μA
		$V_{GS} = -20 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	-10	μA
		$V_{GS} = 10 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	1	μA
		$V_{GS} = -10 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	-1	μA
		$V_{GS} = 5 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	500	nA
		$V_{GS} = -5 V$; $V_{DS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	-	-500	nA
R_{DSon}	drain-source on-state resistance	$V_{GS} = 10 V$; $I_D = 380 \text{ mA}$; $T_j = 25 \text{ }^\circ C$	-	1.8	2.3	Ω
		$V_{GS} = 10 V$; $I_D = 380 \text{ mA}$; $T_j = 150 \text{ }^\circ C$	-	3.9	4.9	Ω
		$V_{GS} = 5 V$; $I_D = 330 \text{ mA}$; $T_j = 25 \text{ }^\circ C$	-	2.2	2.9	Ω
		$V_{GS} = 2.5 V$; $I_D = 260 \text{ mA}$; $T_j = 25 \text{ }^\circ C$	-	2.4	4.8	Ω
g_{fs}	forward transconductance	$V_{DS} = 5 V$; $I_D = 380 \text{ mA}$; $T_j = 25 \text{ }^\circ C$	-	0.7	-	S
Dynamic characteristics						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 30 V$; $I_D = 380 \text{ mA}$; $V_{GS} = 10 V$; $T_j = 25 \text{ }^\circ C$	-	0.5	0.7	nC
Q_{GS}	gate-source charge		-	0.1	-	nC
Q_{GD}	gate-drain charge		-	0.1	-	nC
C_{iss}	input capacitance	$V_{DS} = 30 V$; $f = 1 \text{ MHz}$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	20	-	pF
C_{oss}	output capacitance		-	3.1	-	pF
C_{rss}	reverse transfer capacitance		-	2	-	pF
$t_{d(on)}$	turn-on delay time		$V_{DS} = 30 V$; $I_D = 380 \text{ mA}$; $V_{GS} = 10 V$; $R_{G(ext)} = 6 \Omega$; $T_j = 25 \text{ }^\circ C$	-	7.9	-
t_r	rise time	-		8.4	-	ns
$t_{d(off)}$	turn-off delay time	-		12.5	-	ns
t_f	fall time	-		5.1	-	ns
Source-drain diode						
V_{SD}	source-drain voltage	$I_S = 380 \text{ mA}$; $V_{GS} = 0 V$; $T_j = 25 \text{ }^\circ C$	-	0.7	1.2	V

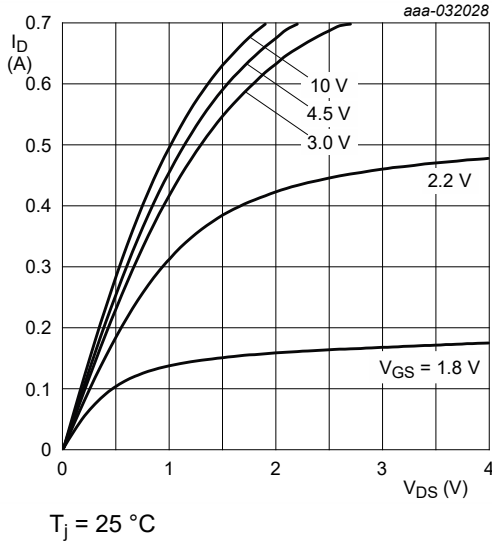


Fig. 6. Output characteristics: drain current as a function of drain-source voltage; typical values

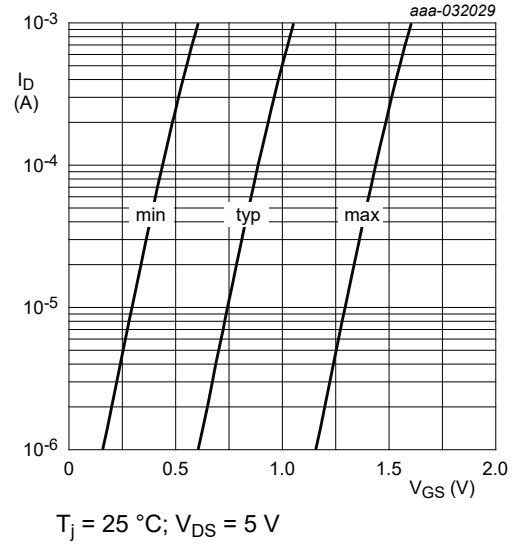


Fig. 7. Sub-threshold drain current as a function of gate-source voltage

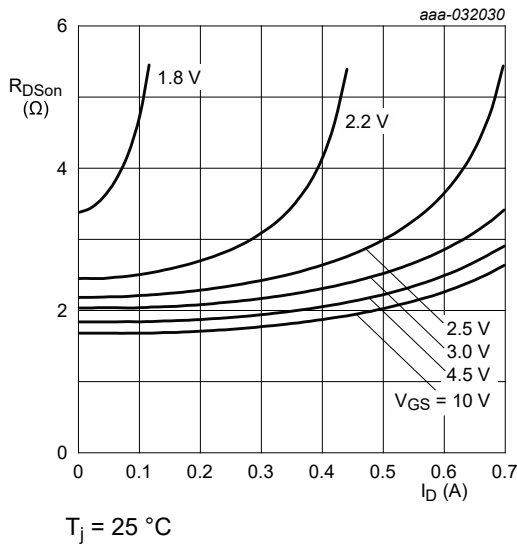


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

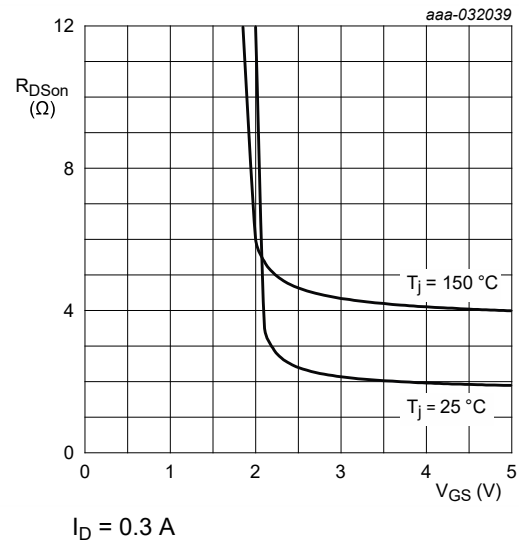


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

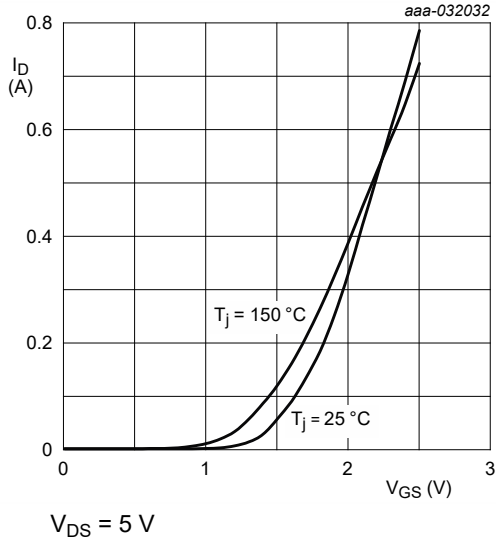


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

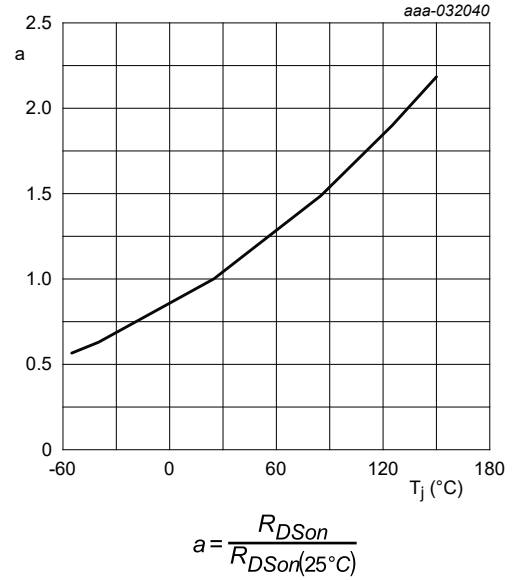


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

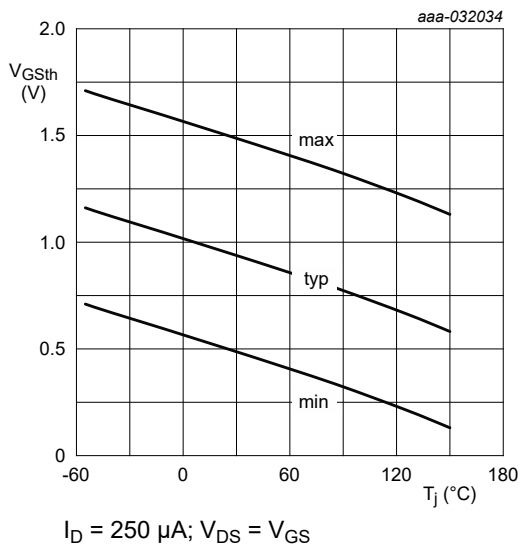


Fig. 12. Gate-source threshold voltage as a function of junction temperature

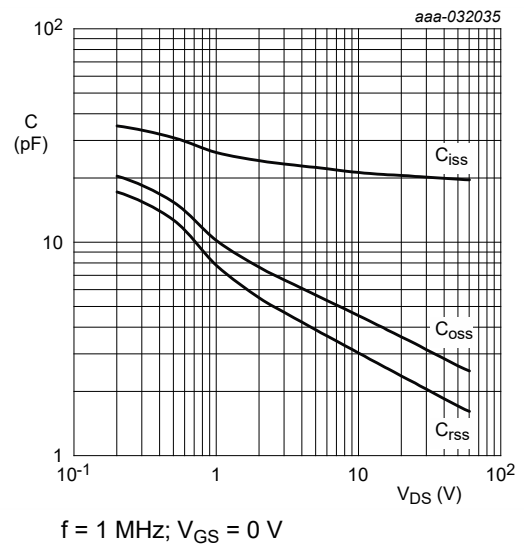
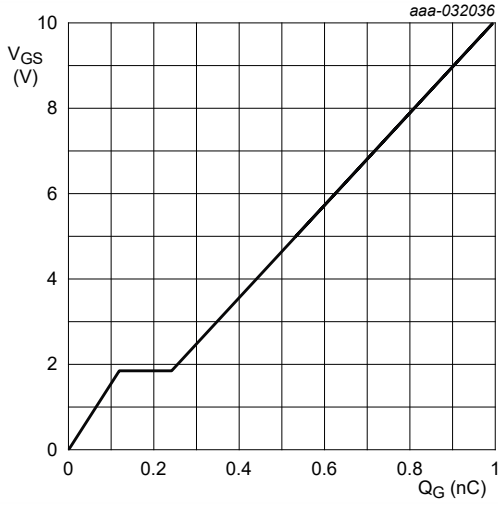


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values



$I_D = 0.2 \text{ A}; V_{DS} = 30 \text{ V}; T_j = 25 \text{ }^\circ\text{C}$

Fig. 14. Gate-source voltage as a function of gate charge; typical values

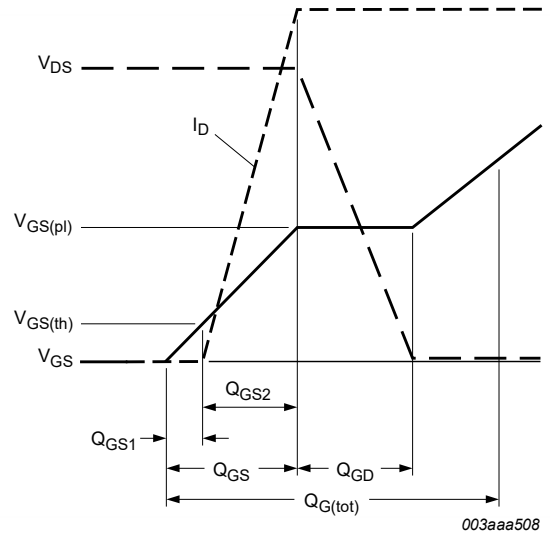
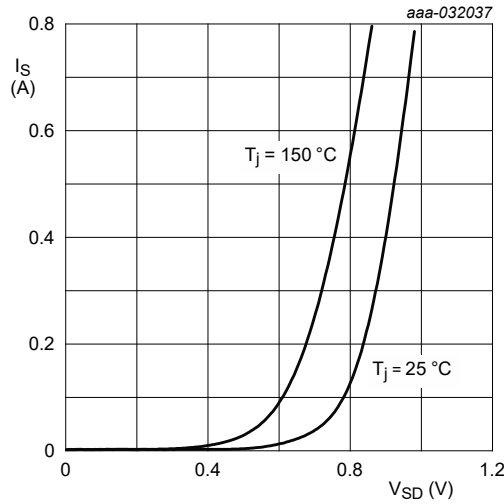


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0 \text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

11. Test information

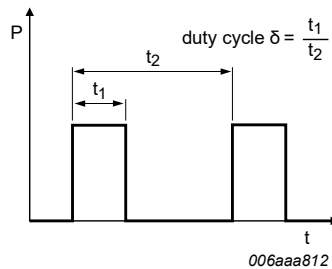


Fig. 17. Duty cycle definition

12. Package outline

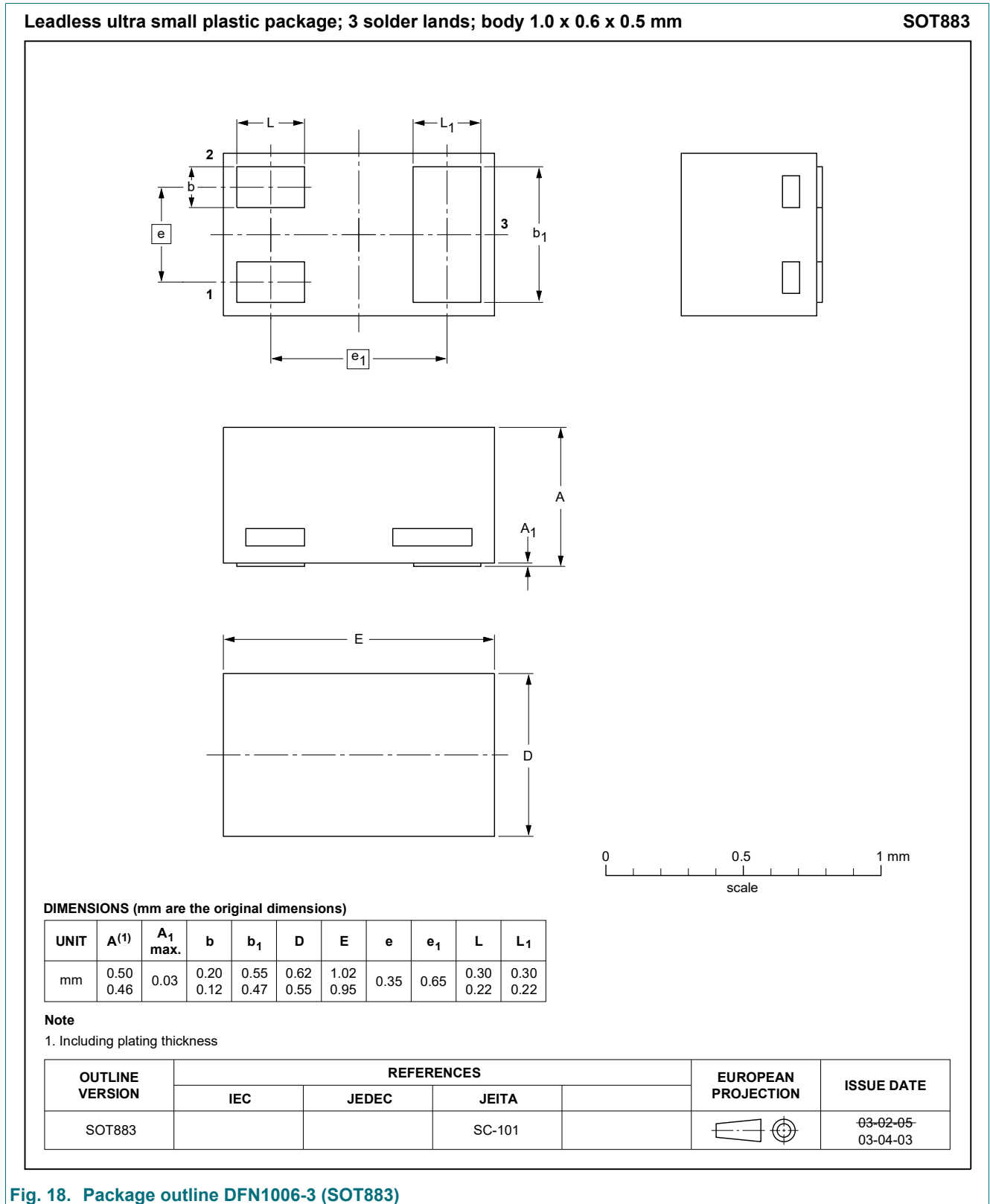


Fig. 18. Package outline DFN1006-3 (SOT883)

13. Soldering

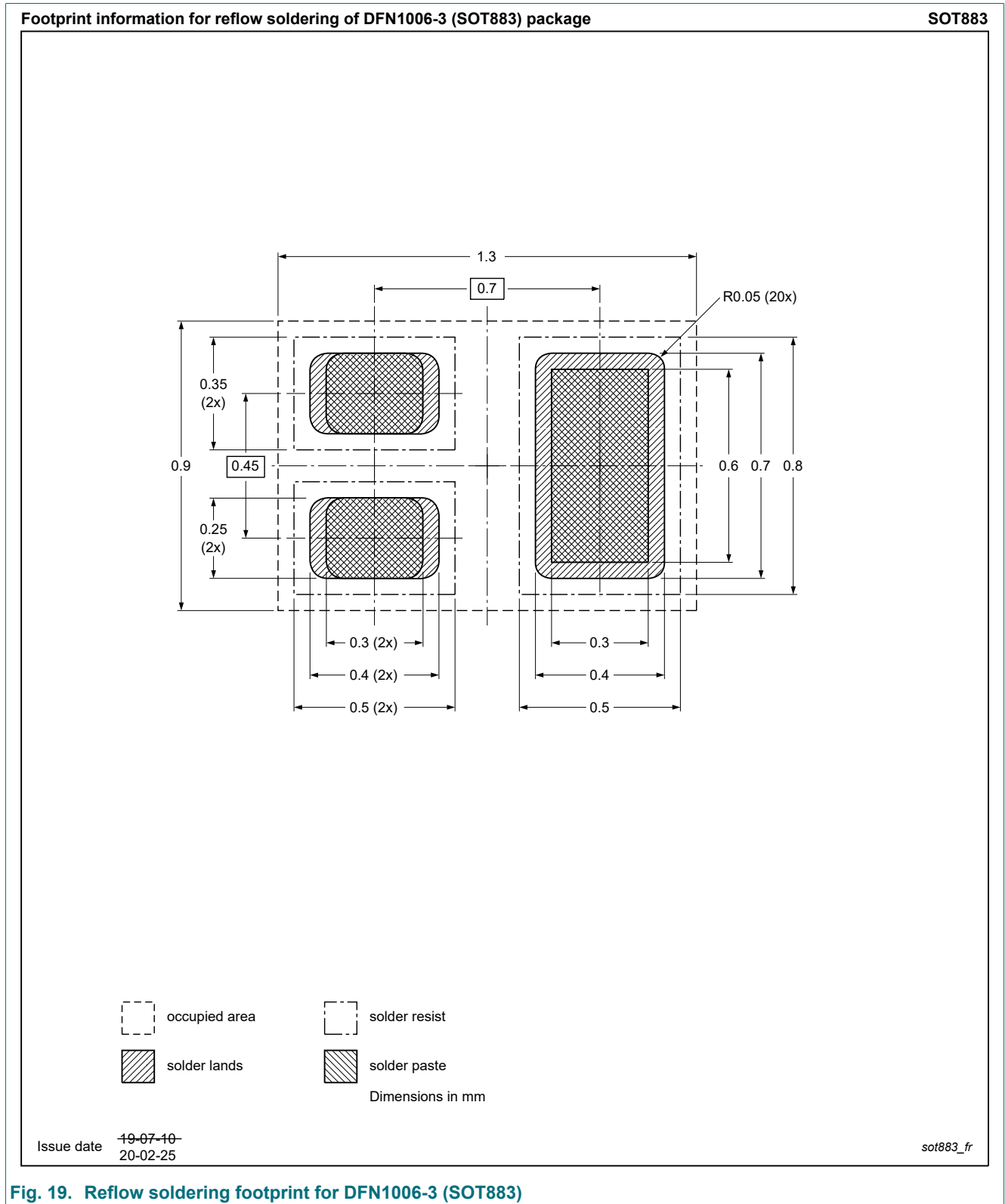


Fig. 19. Reflow soldering footprint for DFN1006-3 (SOT883)

14. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
NX138BKM v.1	20200901	Product data sheet	-	-

15. Legal information

Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
Product [short] data sheet	Production	This document contains the product specification.

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