# CSD18502KCS 40-V N-Channel NexFET™ Power MOSFET

## 1 Features

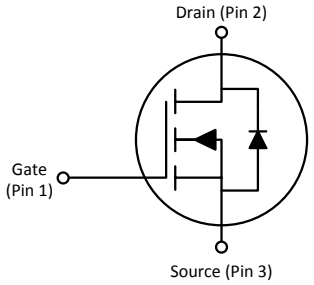
- Ultra-Low $Q_g$ and $Q_{gd}$
- Low Thermal Resistance
- Avalanche Rated
- Logic Level
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- TO-220 Plastic Package

## 2 Applications

- DC-DC Conversion
- Secondary Side Synchronous Rectifier
- Motor Control

## 3 Description

This 2.4 mΩ, 40 V, TO-220 NexFET™ power MOSFET is designed to minimize losses in power conversion applications.




### Product Summary

| $T_A$ = 25°C | | TYPICAL VALUE | | UNIT |
|---|---|---|---|---|
| $V_{DS}$ | Drain-to-Source Voltage | 40 | | V |
| $Q_g$ | Gate Charge Total (10V) | 52 | | nC |
| $Q_{gd}$ | Gate Charge Gate-to-Drain | 8.4 | | nC |
| $R_{DS(on)}$ | Drain-to-Source On Resistance | $V_{GS}$ = 4.5 V | 3.3 | mΩ |
| | | $V_{GS}$ = 10 V | 2.4 | mΩ |
| $V_{GS(th)}$ | Threshold Voltage | 1.8 | | V |

### Ordering Information(1)

| Device | Package | Media | Qty | Ship |
|---|---|---|---|---|
| CSD18502KCS | TO-220 Plastic Package | Tube | 50 | Tube |

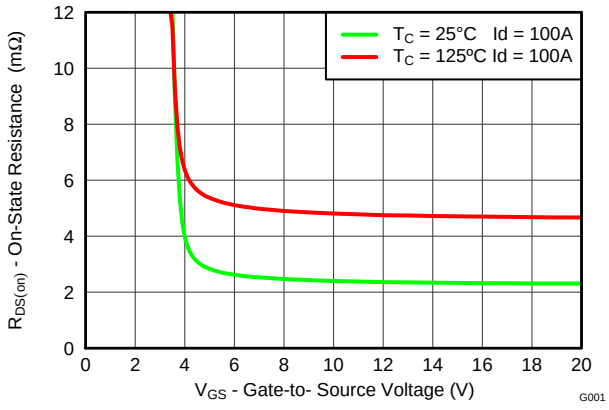
(1) For all available packages, see the orderable addendum at the end of the data sheet.

### Absolute Maximum Ratings

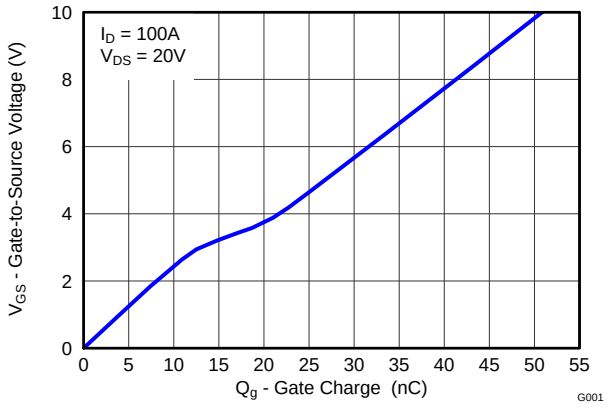
| $T_A$ = 25°C | | VALUE | UNIT |
|---|---|---|---|
| $V_{DS}$ | Drain-to-Source Voltage | 40 | V |
| $V_{GS}$ | Gate-to-Source Voltage | ±20 | V |
| $I_D$ | Continuous Drain Current (Package limited) | 100 | A |
| | Continuous Drain Current (Silicon limited), $T_C$ = 25°C | 212 | |
| | Continuous Drain Current (Silicon limited), $T_C$ = 100°C | 150 | |
| $I_{DM}$ | Pulsed Drain Current (1) | 400 | A |
| $P_D$ | Power Dissipation | 259 | W |
| $T_J$, $T_{stg}$ | Operating Junction and Storage Temperature Range | –55 to 175 | °C |
| $E_{AS}$ | Avalanche Energy, single pulse $I_D$ = 81 A, L = 0.1 mH, $R_G$ = 25 Ω | 330 | mJ |

(1) Max $R_{\theta JC}$ = 0.6°C/W, pulse duration ≤100 µs, duty cycle ≤1%

### $R_{DS(on)}$ vs $V_{GS}$




### Gate Charge



## Table of Contents



# 4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

**Changes from Revision A (October 2012) to Revision B** — **Page**

- Increased the $T_C$ = 25º continuous drain current to 212 A ... 1
- Increased the $T_C$ = 125º continuous drain current to 150 A ... 1
- Increased the pulsed drain current to 400 A ... 1
- Increased the max power dissipation to 259 W ... 1
- Increased the max operating junction and storage temperature to 175º ... 1
- Updated the pulsed current conditions ... 1
- Updated Figure 1 from a normalized $R_{\theta JA}$ to an $R_{\theta JC}$ curve ... 4
- Updated Figure 6 to extend to 175°C ... 5
- Updated Figure 8 to extend to 175°C ... 5
- Updated the SOA in Figure 10 ... 6
- Updated Figure 12 to extend to 175°C ... 6

**Changes from Original (August 2012) to Revision A** — **Page**

- Changed the Transconductance TYP value From: 149 S To: 138 S ... 3
- Changed $R_{\theta JA}$ From: 65°C/W To: 62°C/W ... 3

# 5 Specifications

## 5.1 Electrical Characteristics

($T_A$ = 25°C unless otherwise stated)

| PARAMETER | | TEST CONDITIONS | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|---|
| **STATIC CHARACTERISTICS** | | | | | | |
| $BV_{DSS}$ | Drain-to-Source Voltage | $V_{GS}$ = 0 V, $I_D$ = 250 µA | 40 | | | V |
| $I_{DSS}$ | Drain-to-Source Leakage Current | $V_{GS}$ = 0 V, $V_{DS}$ = 32 V | | | 1 | µA |
| $I_{GSS}$ | Gate-to-Source Leakage Current | $V_{DS}$ = 0 V, $V_{GS}$ = 20 V | | | 100 | nA |
| $V_{GS(th)}$ | Gate-to-Source Threshold Voltage | $V_{DS}$ = $V_{GS}$, $I_D$ = 250 µA | 1.5 | 1.8 | 2.1 | V |
| $R_{DS(on)}$ | Drain-to-Source On Resistance | $V_{GS}$ = 4.5 V, $I_D$ = 100 A | | 3.3 | 4.3 | mΩ |
| | | $V_{GS}$ = 10 V, $I_D$ = 100 A | | 2.4 | 2.9 | mΩ |
| $g_{fs}$ | Transconductance | $V_{DS}$ = 20 V, $I_D$ = 100 A | | 138 | | S |
| **DYNAMIC CHARACTERISTICS** | | | | | | |
| $C_{iss}$ | Input Capacitance | $V_{GS}$ = 0 V, $V_{DS}$ = 20 V, $f$ = 1 MHz | | 3900 | 4680 | pF |
| $C_{oss}$ | Output Capacitance | | | 900 | 1080 | pF |
| $C_{rss}$ | Reverse Transfer Capacitance | | | 21 | 26 | pF |
| $R_G$ | Series Gate Resistance | | | 1.2 | 2.4 | Ω |
| $Q_g$ | Gate Charge Total (4.5 V) | $V_{DS}$ = 20 V, $I_D$ = 100 A | | 25 | 30 | nC |
| $Q_g$ | Gate Charge Total (10 V) | | | 52 | 62 | nC |
| $Q_{gd}$ | Gate Charge Gate-to-Drain | | | 8.4 | | nC |
| $Q_{gs}$ | Gate Charge Gate-to-Source | | | 10.3 | | nC |
| $Q_{g(th)}$ | Gate Charge at $V_{th}$ | | | 7.5 | | nC |
| $Q_{oss}$ | Output Charge | $V_{DS}$ = 20 V, $V_{GS}$ = 0 V | | 52 | | nC |
| $t_{d(on)}$ | Turn On Delay Time | $V_{DS}$ = 20 V, $V_{GS}$ = 10 V, $I_{DS}$ = 100 A, $R_G$ = 0 Ω | | 11 | | ns |
| $t_r$ | Rise Time | | | 7.3 | | ns |
| $t_{d(off)}$ | Turn Off Delay Time | | | 33 | | ns |
| $t_f$ | Fall Time | | | 9.3 | | ns |
| **DIODE CHARACTERISTICS** | | | | | | |
| $V_{SD}$ | Diode Forward Voltage | $I_{SD}$ = 100 A, $V_{GS}$ = 0 V | | 0.8 | 1 | V |
| $Q_{rr}$ | Reverse Recovery Charge | $V_{DS}$= 20 V, $I_F$ = 100A, di/dt = 300A/µs | | 105 | | nC |
| $t_{rr}$ | Reverse Recovery Time | | | 48 | | ns |

## 5.2 Thermal Information

($T_A$ = 25°C unless otherwise stated)

| THERMAL METRIC | | MIN | TYP | MAX | UNIT |
|---|---|---|---|---|---|
| $R_{\theta JC}$ | Junction-to-Case Thermal Resistance | | | 0.6 | °C/W |
| $R_{\theta JA}$ | Junction-to-Ambient Thermal Resistance | | | 62 | |

## 5.3 Typical MOSFET Characteristics

($T_A$ = 25°C unless otherwise stated)

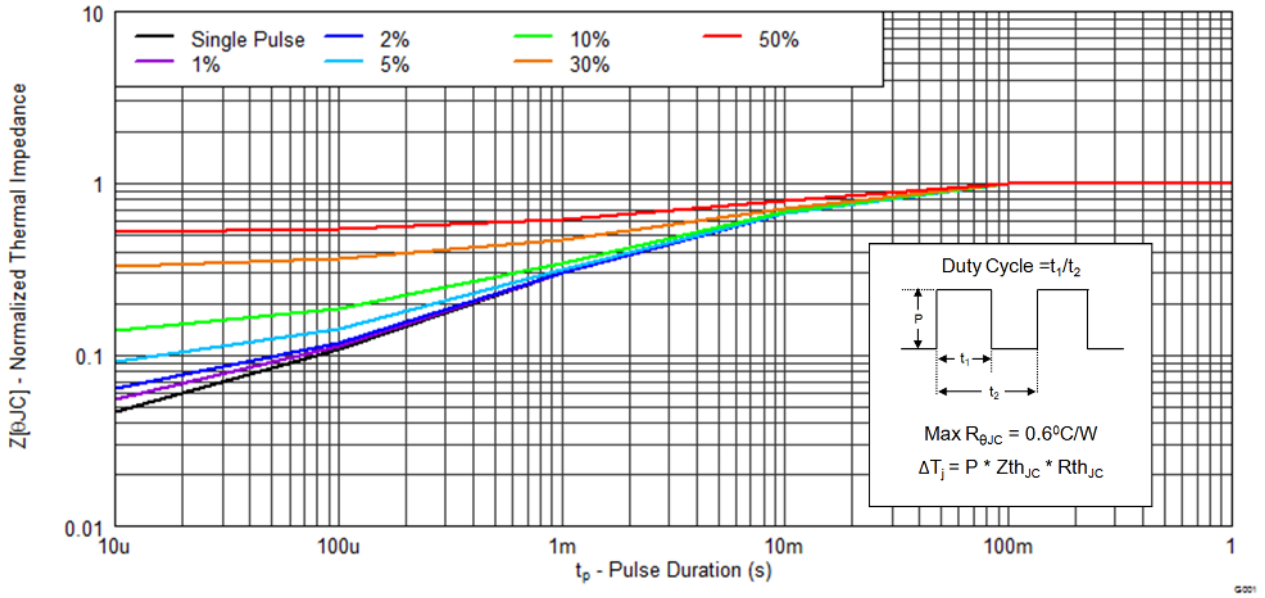



**Figure 1. Transient Thermal Impedance**

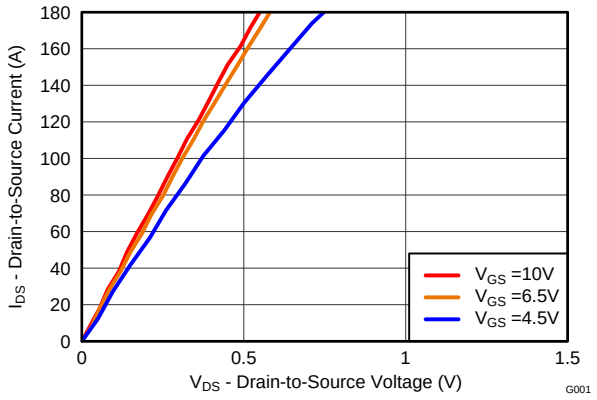



**Figure 2. Saturation Characteristics**

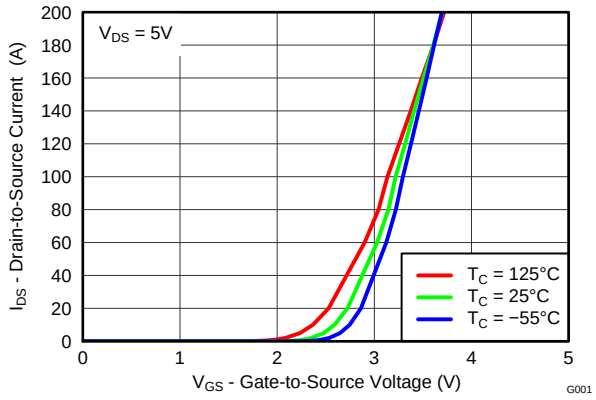



**Figure 3. Transfer Characteristics**

## Typical MOSFET Characteristics (continued)

($T_A$ = 25°C unless otherwise stated)

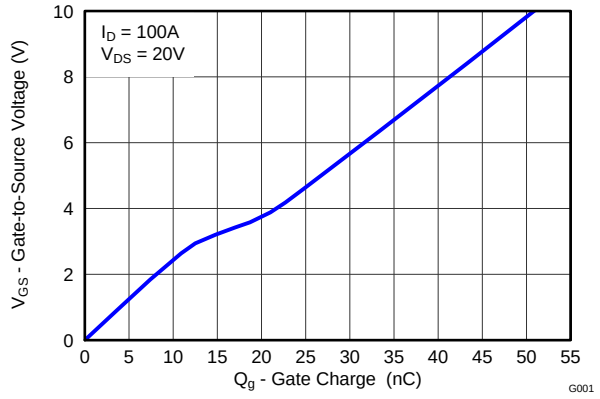



**Figure 4. Gate Charge**

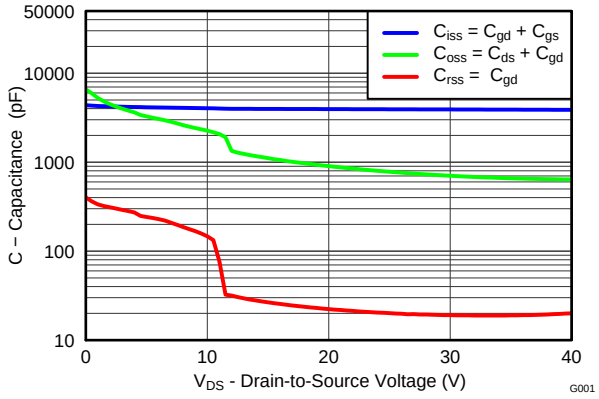



**Figure 5. Capacitance**

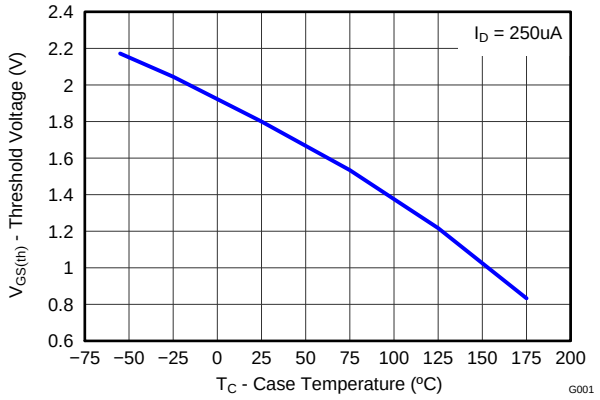



**Figure 6. Threshold Voltage vs. Temperature**

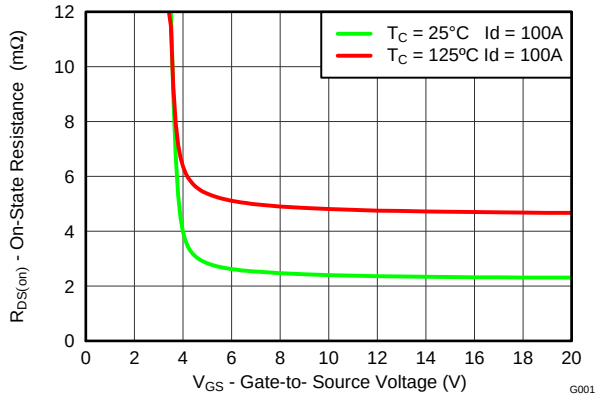



**Figure 7. On-State Resistance vs. Gate-to-Source Voltage**

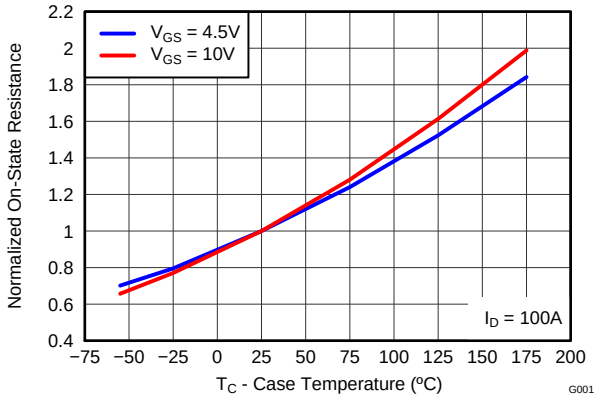



**Figure 8. Normalized On-State Resistance vs. Temperature**

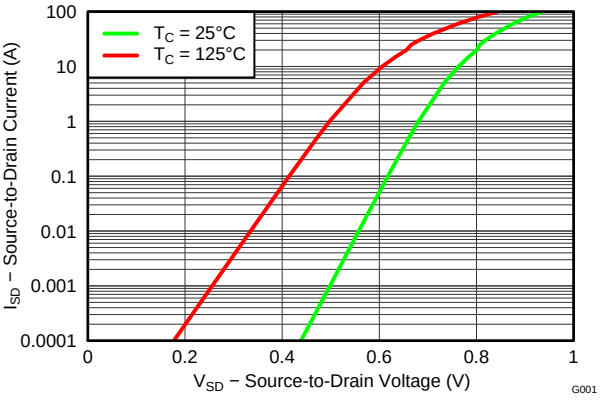



**Figure 9. Typical Diode Forward Voltage**

## Typical MOSFET Characteristics (continued)

($T_A$ = 25°C unless otherwise stated)

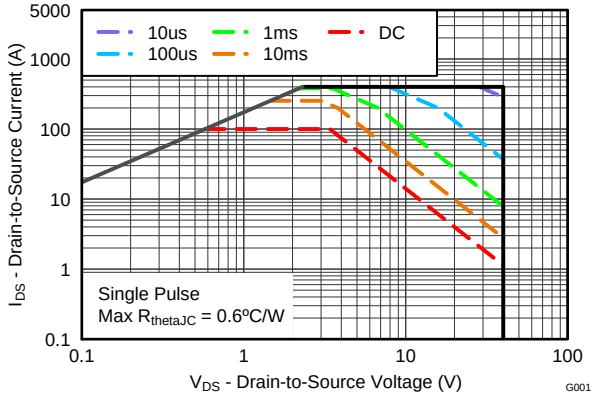



**Figure 10. Maximum Safe Operating Area**

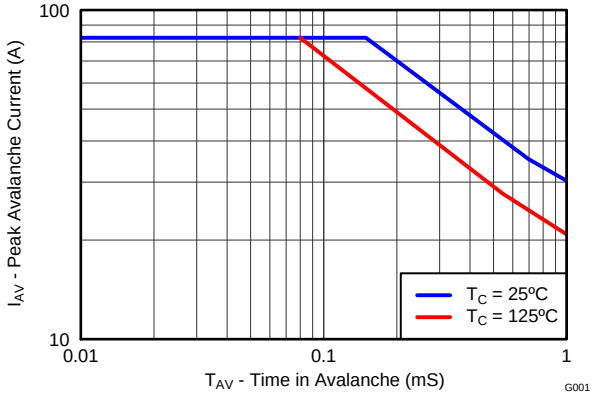



**Figure 11. Single Pulse Unclamped Inductive Switching**

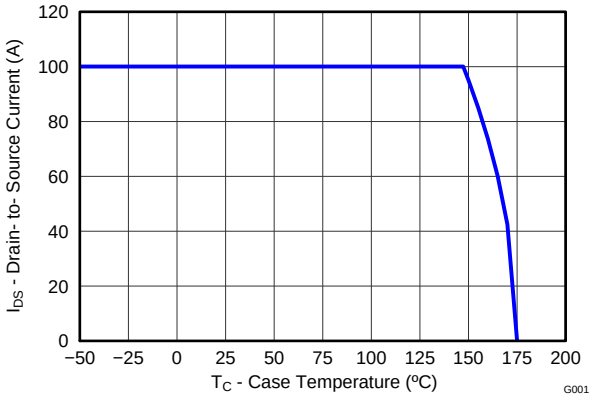



**Figure 12. Maximum Drain Current vs. Temperature**

# 6 Device and Documentation Support

## 6.1 Trademarks

NexFET is a trademark of Texas Instruments.

## 6.2 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

## 6.3 Glossary

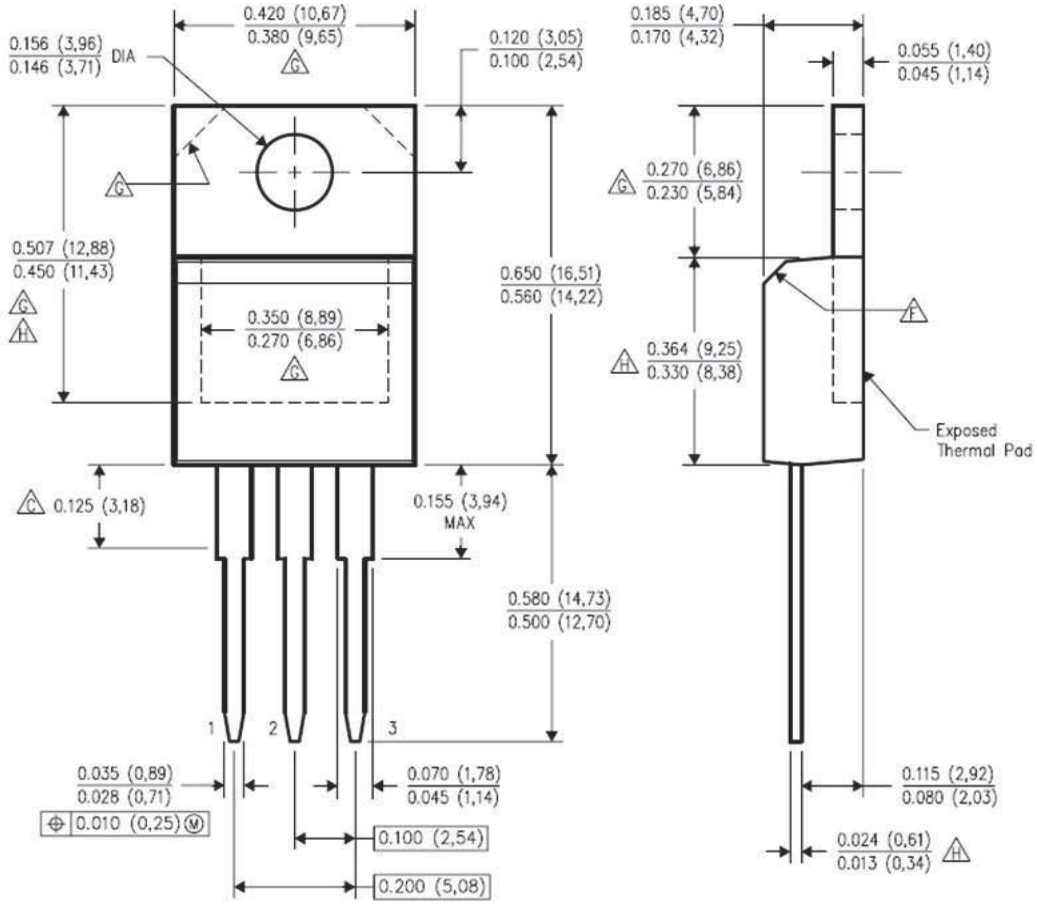
SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

# 7 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

## 7.1 KCS Package Dimensions




**Notes:**

1. All linear dimensions are in inches.
2. This drawing is subject to change without notice.
3. Lead dimensions are not controlled within 'C' area
4. All lead dimensions apply before solder dip.
5. The center lead is in electrical contact with the mounting tab.
6. The chamfer at 'F' is optional.
7. Thermal pad contour at 'G' optional with these dimensions
8. 'H' falls within JEDEC TO-220 variation AB, except minimum lead thickness, minimum exposed pad length, and maximum body length.

**Pin Configuration**

| Position | Designation |
|---|---|
| Pin 1 | Gate |
| Pin 2 / Tab | Drain |
| Pin 3 | Source |

## PACKAGING INFORMATION

| Orderable Device | Status (1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan (2) | Lead finish/ Ball material (6) | MSL Peak Temp (3) | Op Temp (°C) | Device Marking (4/5) | Samples |
|---|---|---|---|---|---|---|---|---|---|---|---|
| CSD18502KCS | ACTIVE | TO-220 | KCS | 3 | 50 | RoHS-Exempt & Green | SN | N / A for Pkg Type | -55 to 175 | CSD18502KCS | Samples |

(1) The marketing status values are defined as follows:
**ACTIVE:** Product device recommended for new designs.
**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.
**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

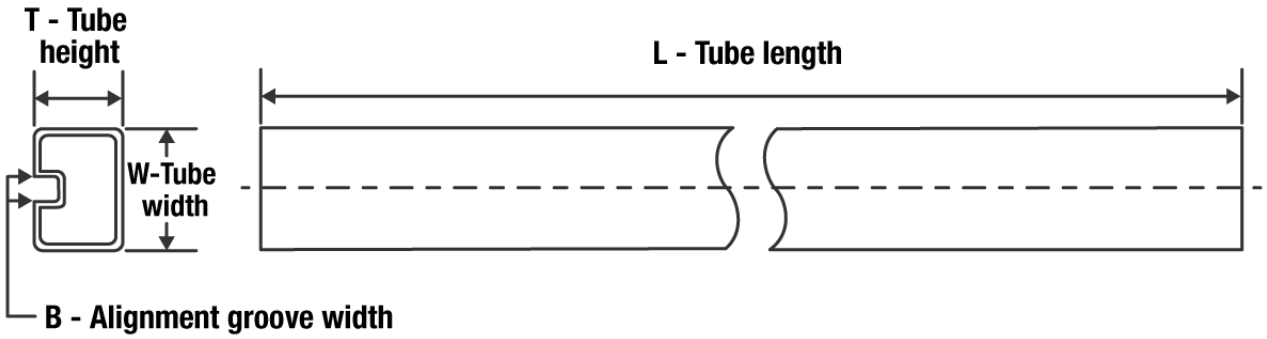
(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

## TUBE




*All dimensions are nominal

| Device | Package Name | Package Type | Pins | SPQ | L (mm) | W (mm) | T (µm) | B (mm) |
|---|---|---|---|---|---|---|---|---|
| CSD18502KCS | KCS | TO-220 | 3 | 50 | 532 | 34.1 | 700 | 9.6 |
| CSD18502KCS | KCS | TO-220 | 3 | 50 | 532 | 34.1 | 700 | 9.6 |

# IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI’s products are provided subject to TI’s Terms of Sale or other applicable terms available either on ti.com or provided in conjunction with such TI products. TI’s provision of these resources does not expand or otherwise alter TI’s applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265