3.3 V 12.288 MHz Audio Oversampling Clock Generator for USB Applications

NB3N3010B

ON Semiconductor®

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SOIC−8
D SUFFIX
CASE 751

Description

The NB3N3010B is a precision, low noise clock multiplier that generates an output frequency of 12.288 MHz. This is accomplished by using Frequency−Locked−Loop (FLL) techniques where a 4 kHz reference input is multiplied by 3072, or an 8 kHz input by 1536. The frequency multiplier is selected by the S0 pin.

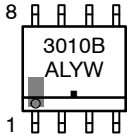
The two LVCMOS output drivers are disabled to a logic Low with the ENABLEn pin set HIGH. The NB3N3010B operates from a single +3.3 V supply, and is available in the SOIC−8 pin package. The operating temperature range is from 0°C to +85°C.

The NB3N3010B device provides the optimum combination of low cost, flexibility, and high performance. This makes it ideal for applications such as oversampling A−to−D and D−to−A converters from a low reference frequency, such as a USB start−of−frame (SOF) pulse.

Features

- Accepts 8 kHz or 4 kHz Reference Input Derived from USB Start−of−Frame
- Generates 12.288 MHz Frequency−Locked to the Reference
- Fully Integrated Frequency−Lock−Loop with Internal Loop Filter
- Low Skew Dual LVCMOS Outputs
- Very Low Phase Noise Preserves Codec Noise Floor
- Internal Voltage Regulator
- Supply Voltage Required: +3.3 V ±5%
- Temperature Range: 0°C to +85°C
- These Devices are Pb−Free, Halogen Free/BFR Free and are RoHS Compliant

MARKING DIAGRAM*



A = Assembly Location
L = Wafer Lot
Y = Year
W = Work Week
▪ = Pb−Free Package

(Note: Microdot may be in either location)

*For additional marking information, refer to Application Note AND8002/D.

ORDERING INFORMATION

Device	Package	Shipping†
NB3N3010BDR2G	SOIC−8 (Pb−Free)	2500 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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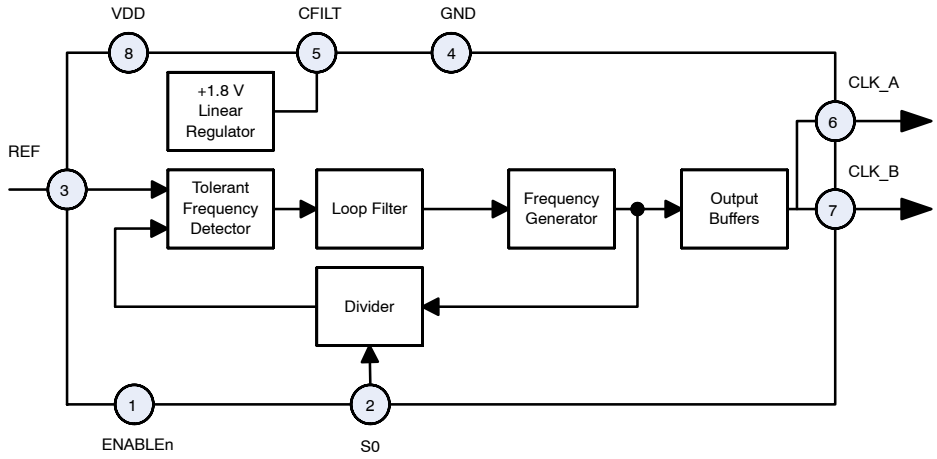

Figure 1. NB3N3010B Simplified Diagram

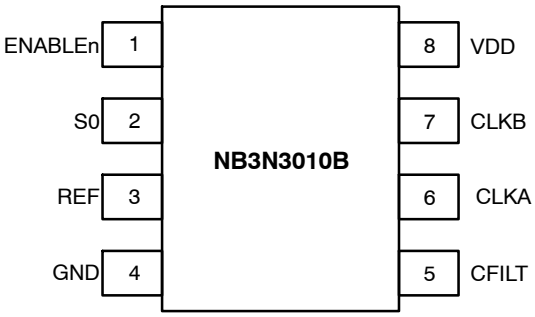

Figure 2. Pinout SOIC−8 (Top View)

Table 1. PIN DESCRIPTION

Pin	Symbol	I/O	Description
1	ENABLEn	LVTTL/ LVCMOS Input	Low active Output Enable; Defaults HIGH when left open; Internal pull−up resistor to V_{DD}.
2	S0	LVTTL/ LVCMOS Input	Frequency Select Input. See input frequency select Table 2 for details. Defaults HIGH when left open. Internal pull−up resistor to V_{DD}.
3	REF	Input	Reference Clock input
4	GND	Power Supply	Negative Supply Voltage; Ground 0 V. This pin provides GND return path to the VDD supply.
5	CFILT	Analog	Connection for external filter capacitor for internal +1.8 V regulator; see Figure 4.
6	CLKA	LVCMOS Output	Clock output, copy A (12.288 MHz)
7	CLKB	LVCMOS Output	Clock output, copy B (12.288 MHz)
8	VDD	Power Supply	Positive Supply Voltage, +3.3 V ±5%

Table 2. ATTRIBUTES

Characteristic	Value
ESD Protection Human Body Model Machine Model	 > 4 kV 400 V
R_{PU} – ENABLEn Input Pull–up Resistor R_{PU} – SO Input Pull–up Resistor	48 kΩ 48 kΩ
Moisture Sensitivity (Note 1) Pb–Free	 Level 1
Flammability Rating Oxygen Index: 28 to 34	 UL 94 V–0 @ 0.125 in
Transistor Count	12039
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

1. For additional information, see Application Note AND8003/D.

Table 3. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V_{DD}	Positive Power Supply	GND = 0 V		4.6	V
V_I	Input Voltage (VIN)	GND = 0 V		–0.3 V to V_{DD} + 0.3 V	V
T_A	Operating Temperature Range			0 to +85	°C
T_{stg}	Storage Temperature Range			–40 to +150	°C
θ_{JA}	Thermal Resistance (Junction–to–Ambient)	0 lfpm 500 lfpm	SOIC–8 SOIC–8	190 130	°C/W °C/W
θ_{JC}	Thermal Resistance (Junction–to–Case)	(Note 2)	SOIC–8	41 to 44	°C/W
T_{sol}	Wave Solder Pb–Free			265	°C

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

2. JEDEC standard multilayer board – 2S2P (2 signal, 2 power).

Table 4. DC CHARACTERISTICS V_{DD} = 3.3 V ±5%, GND = 0 V, T_A = 0°C to +85°C, Note 3.

Symbol	Characteristic	Min	Typ	Max	Unit
V_{DD}	Power Supply Voltage	3.13	3.3	3.47	V
I_{DDOEL}	Power Supply Current (operating, i.e. ENABLEn is LOW) Outputs Unloaded		21	35	mA
I_{DDOEH}	Power Supply Current (standby, i.e. ENABLEn is HIGH)		415	600	uA
V_{IH}	Input HIGH Voltage (REF, ENABLEn, S0)	2.0		V_{DD} + 0.3	V
V_{IL}	Input LOW Voltage (REF, ENABLEn, S0)	GND – 0.3		0.8	V
V_{OH}	Output HIGH Voltage (CLKA, CLKB) , I_{OH} = –12 mA	2.4			V
V_{OL}	Output LOW Voltage (CLKA, CLKB), I_{OL} = 12 mA			0.4	V

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

3. C_{FILT} capacitor must be installed; see Figure 4.

Table 5. AC CHARACTERISTICS V_{DD} = 3.3 V ±5%, GND = 0 V, T_A = 0°C to +85°C (Note 4)

Symbol	Characteristic		Min	Typ	Max	Unit
f_{out}	Output Clock Frequency: CLKA & CLKB f_{OUT} = 8 kHz x 1536 f_{OUT} = 4 kHz x 3072	 S0 = 1 S0 = 0	 12.25728 12.25728	 12.288 12.288	 12.31872 12.31872	MHz
f_{REF}	Reference Input Frequency	S0 = 1 S0 = 0	7.98 3.99	8 4	8.02 4.01	kHz
$t_{jit(per)-ref}$	Reference Input Period Jitter (pk−pk)				250	ns
t_{REFH}	Reference Input Pulse Width (high)	S0 = 1 S0 = 0	33 33		68000 136000	ns
t_{CLKH}	CLKA, CLKB output width, high		13			ns
t_{CLKL}	CLKA, CLKB output width, low		13			ns
t_r	CLKA, CLKB rise time 10% – 90%				4	ns
t_f	CLKA, CLKB fall time 90% – 10%				4	ns
$t_{jit(per)}$	CLKA, CLKB period jitter (over 10k cycles)	peak−to−peak RMS			250 20	ps
$t_{jit(cc)}$	CLK_A, CLKB cycle−to−cycle jitter (1k cycles)	peak−to−peak RMS			300 35	ps
$t_{sk(LH)}$	CLKA to CLKB output skew (low−to−high transitions)				700	ps
$t_{sk(HL)}$	CLKA to CLKB output skew (high−to−low transitions)				700	ps
	Power Valid to ENABLEn				10	ms
	ENABLEn to CLKA/CLKB			50	100	ms

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm.

4. Outputs loaded with 15 pF max to ground. C_{FILT} capacitor must be installed; see Figure 4.
5. Maximum time required after power is applied to the MCLK FLL until it is ready to accept ENABLEn active.

APPLICATION INFORMATION

Figure 1 shows the simplified block diagram of the NB3N3010B device.

The primary function of the NB3N3010B is to accept a selectable 4 kHz or 8 kHz input reference clock, REF, and then multiply it to 12.288 MHz output frequency.

Frequency Select – SO

Either of two expected input REF frequencies, 4 kHz or 8 kHz, will be multiplied by the FLL to achieve 12.288 MHz at the low−skew CLKA and CLKB outputs by selecting the S0 pin; see Table 6.

The pulse high time (T_{HI}) of the input reference signal may vary widely depending on the application. See AC specifications for details.

Output Enable – ENABLEn

A Low active output enable input pin, ENABLEn, is provided. When the ENABLEn input is High inactive, both clock outputs are driven to a logic Low.

The NB3N3010B implements a delay, specified as ENABLEn to Output Delay in the AC Specifications, from the assertion of ENABLEn to the first rising edges on the clock outputs. This delay insures that CLKA and CLKB output pulses are within specification before the output drivers are enabled. When ENABLEn transitions from Low to High (de−asserts), the current cycle of the clock outputs completes normally then the outputs will be held Low. The ENABLEn signal is asynchronous to either the REF input or CLK_x outputs.

Table 6. INPUT FREQUENCY SELECT AND OUTPUT ENABLE FUNCTIONS

ENABLEn*	S0*	f_{REF}	FLL Multiplier	CLKA & CLKB Frequency
0	L	4 kHz	3072	12.288 MHz
0	H	8 kHz	1536	12.288 MHz
1	x	x	x	Disabled Low

*Defaults High when left open.

Typical Power On Sequence

1. Power On
2. Reference Clock present; must be switching before ENABLEn goes High.
3. Output Enable, ENABLEn, High−to−Low

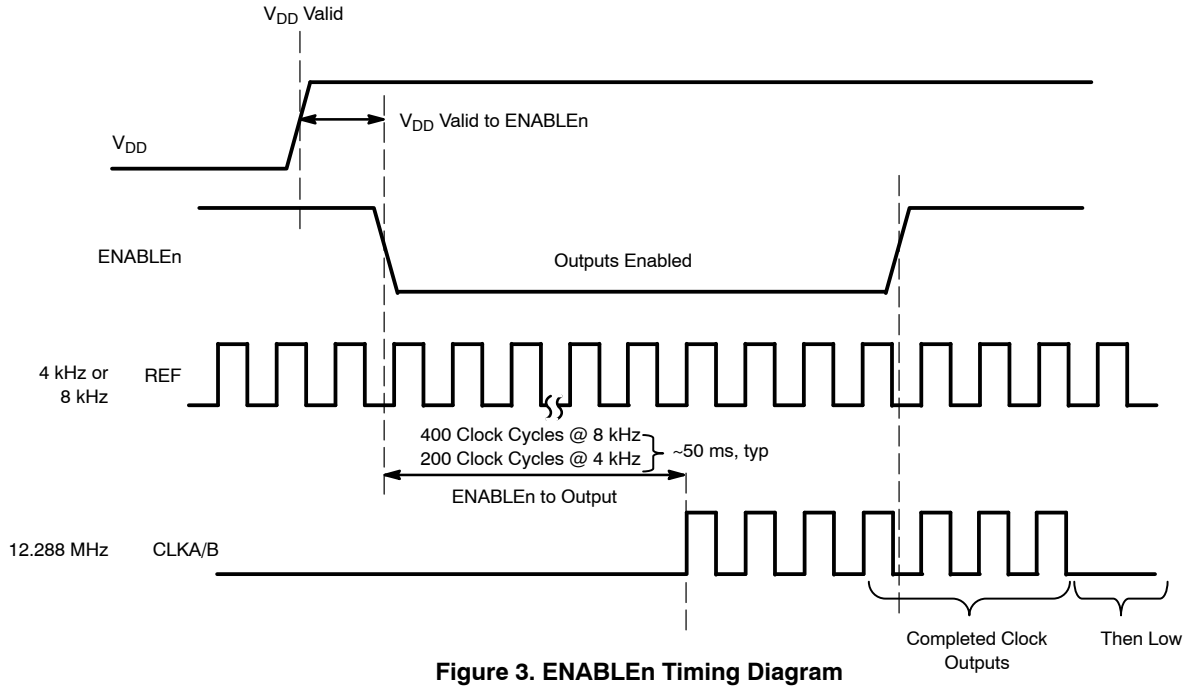

Figure 3. ENABLEn Timing Diagram

CFILT for 1.8 V Regulator

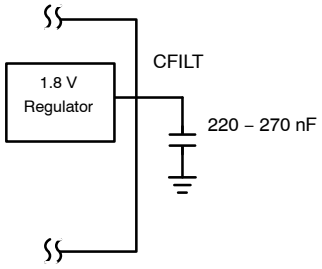

Figure 4. CFILT Capacitor

A low noise 1.8 V LDO/Regulator is integrated to provide a clean supply for the CLKA/CLKB output buffers. The LDO requires a decoupling capacitor in the range of 220 nF to 270 nF for compensation and high frequency PSR, and should be located near the device. The purpose of this design technique is to isolate the high switching noise of the digital outputs from the relatively sensitive internal analog phase−locked loop.

Figure 5. REF Input Timing Diagram

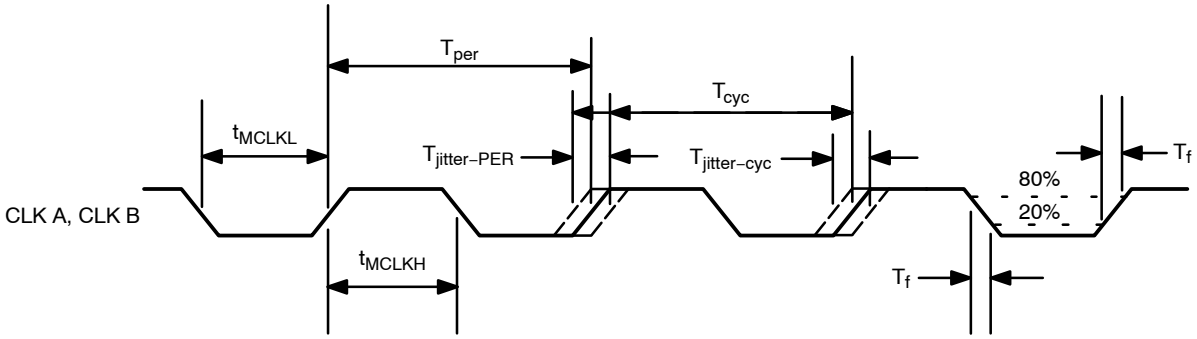

Figure 6. Clock Output Timing Diagram

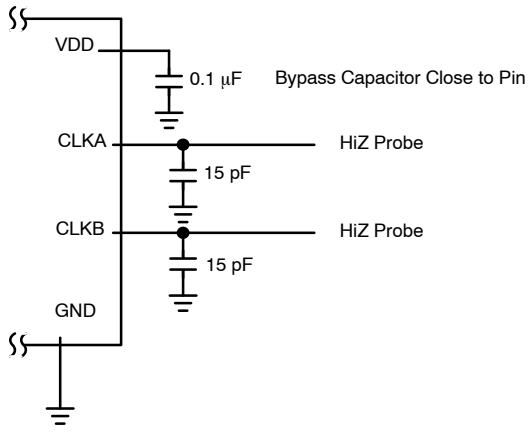

Figure 7. Test Circuit

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