HMCAD5831LP9BE

v03.0818

3-BIT 26 GSPS ANALOG-TO-DIGITAL CONVERTER W/ OVERRANGE, INHIBIT, AND 1:2 DEMUX

Typical Applications

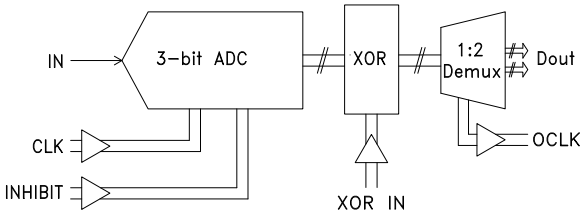
The HMCAD5831LP9BE is ideal for:

- Ultra Wideband Phased Arrays
- Radio Astronomy
- Serial Data Links
- Test Equipment for Link Diagnostics
- Spectrometers

Features

- 20 GHz Input Bandwidth
- Full Flash Architecture with Ultra-Low Latency
- Over/Under Range Bit
- Data Inhibit Function
- Data XOR Function
- 1:2 Demux Output
- Programmable Differential CML Output Swing
- 64 Lead Plastic 9 x 9 mm SMT Package: 81 mm^2

Functional Diagram



General Description

The HMCAD5831LP9BE is a wideband 3-bit analog-to-digital converter with over/under range bit. The converter operates at typical speeds of up to 26 GSPS under typical conditions with a Nyquist input. Reference ladder end voltages are set externally by the user allowing the user to customize input common mode and swing levels. ADC outputs can be forced to 0 by using the Data Inhibit function. Output data can be modulated by an external clock via the XOR CML input. The HMCAD5831LP9BE also features a 1:2 demux with half rate clock output. The output bits are binary weighted, where X2 and Y2 are the MSBs. The single-ended RF input can be AC or DC coupled and supports broadband operation.

The HMCAD5831LP9BE operates from -5V and -3.3V supplies and is available in ROHS-compliant 9 x 9 mm SMT package.

Electrical Specifications, T_A = +25 °C [1], AVEE = -5 V, OVEE = -3.3 V, Full-Scale Vin = 256 mV, Clock Input Power = 0 dBm (single ended)

Parameter	Conditions	Min.	Typ.	Max	Units
Resolution			3		bits
Sample Rate			22	26 [2]	GHz
DNL (including Overrange Bit)		-0.5		0.5	lsbs
INL (including Overrange Bit)		-0.5	±0.3	0.5	lsbs
Input Bandwidth			20		GHz
Input DC Voltage [3]			0		V
Input Voltage Swing	Can be user defined. Subject to maximum input voltage specified in the Operating Conditions table.		256	1500	mV
Input Rin			50		Ω
Clock Power, Single Ended			-3		dBm

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Electrical Specifications *(continued)*

Parameter	Conditions	Min.	Typ.	Max	Units
Clock, XOR Rin	Differential		100		Ω
Ladder Top Voltage (RTF)	Can be user defined		-0.808		V
Ladder Bottom Voltage (RBF) [4]	Can be user defined		-1.064		V
Output Amplitude [5]	Single ended, peak to peak		286		mVp-p
Output High Voltage [5]			-33		mV
Output Low Voltage [5]			-319		mV
XOR Clock Rate			156.25		MHz
XOR Input Power, Single Ended			-3		dBm
Data Inhibit Rin	Single ended		600		Ω
Data Inhibit High Voltage			200		mV
Data Inhibit Low Voltage			-200		mV
Data, Clock, OVR Bits Rout	Differential		100		Ω
Data, Clock, OVR Bits Rout	Single ended		50		Ω
Demux Ratio			1:2		
ENOB (20 GSPS)	fin = 312.5 MHz		2.9		bits
ENOB (20 GSPS)	fin = 9.6875 GHz		2.9		bits
ENOB (20 GSPS)	fin = 19.6875 GHz		2.9		bits
ENOB (26 GSPS)	fin = 406.25 MHz		2.9		bits
ENOB (26 GSPS)	fin = 12.5938 GHz		2.9		bits
SFDR (20 GSPS)	fin = 312.5 MHz		24.7		dBFS
SFDR (20 GSPS)	fin = 9.6875 GHz		25.7		dBFS
SFDR (20 GSPS)	fin = 19.6875 GHz		27.2		dBFS
Power Supply Current (-5V)			725		mA
Power Supply Current (-3.3V)			176		mA
Power	Independent of clock rate		4.2		W

[1] See Application Information section for operation over range of temperatures.
[2] Requires sufficient clock power and cooling.
[3] Input signal common mode nominally should be set to this point, but may be adjusted with RTF/RBF. See Application Information section.
[4] See Application Information section for guidance on setting reference voltages.
[5] With a single 200 Ω resistor tied from VREF1 and VREF2 to OGND. VREF1 and VREF2 are connected off chip.

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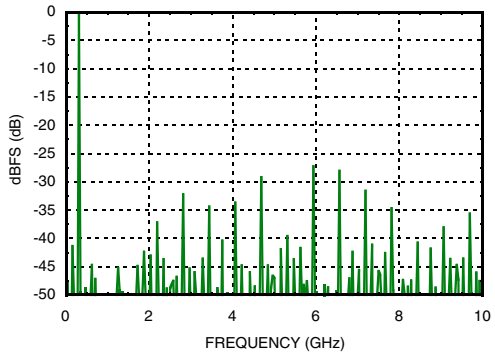
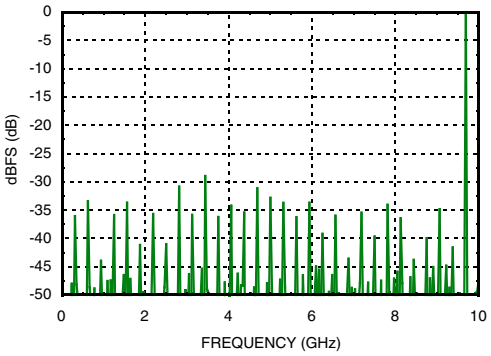
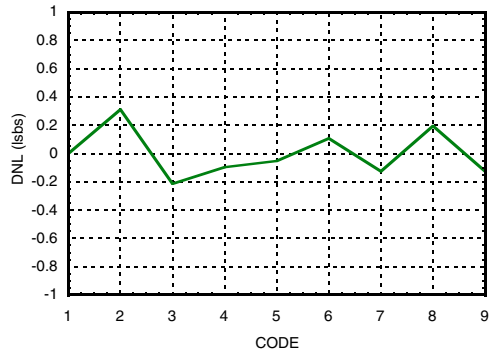
Spectral Performance FFT
(312.5 MHz input, 20 GSPS clock)



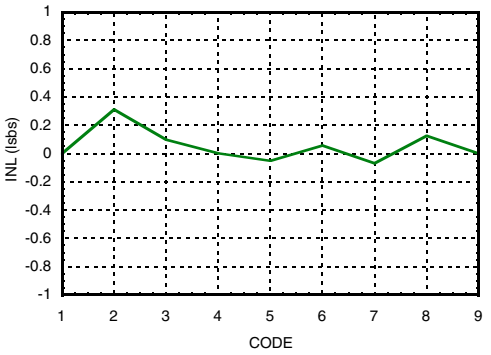
Spectral Performance FFT
(9.6875 GHz input, 20 GSPS clock)



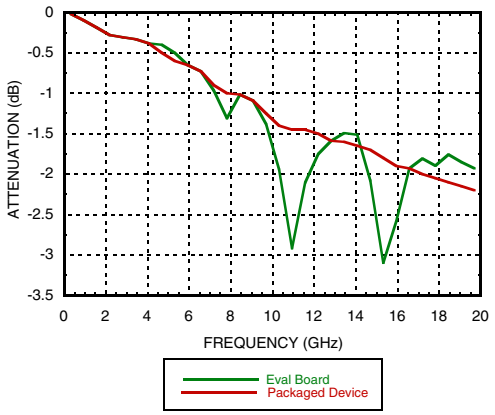
Differential Nonlinearity
(Including overrange bits)



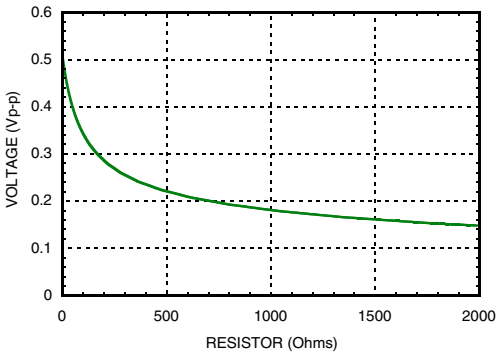
Integral Nonlinearity
(Including overrange bits)



Bandwidth [1]



VREF Resistor Value vs. Output Voltage Swing [2]



[1] This graph was made by measuring the analog input power required to get full scale on the digital output. The increase in power from DC should be equal to the attenuation. The effects of the cables and the circuit board were estimated and subtracted from the measured attenuation to determine the input attenuation of the packaged part.

[2] Single-ended voltage swing into 50 Ohm resistor.

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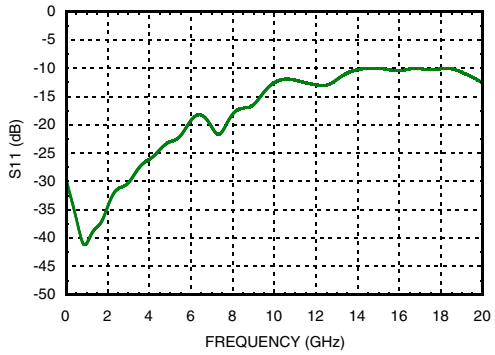
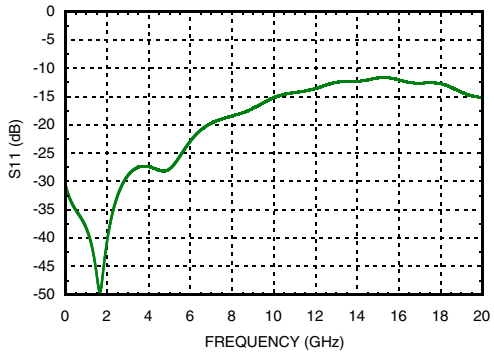
Signal S11 [1]

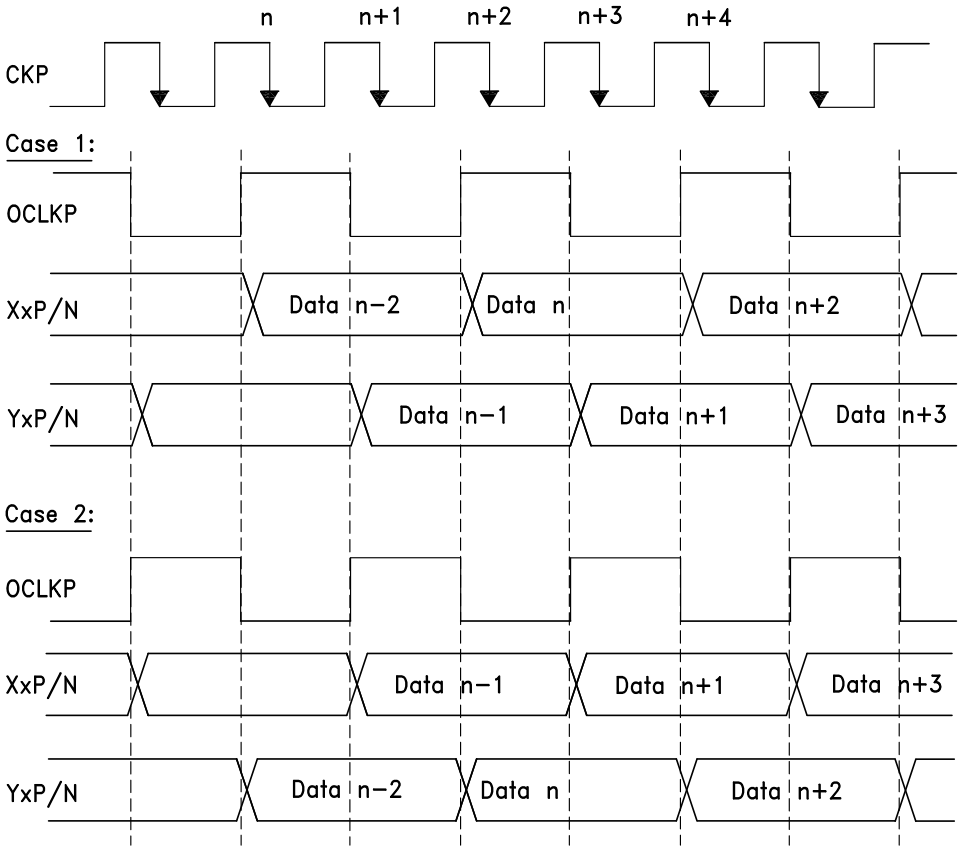


Clock S11 [1]



[1] This is S11 data taken from the input of the evaluation board. The gating function on the network analyzer was employed to remove the effects of the PCB and look only at the packaged part.

Digital Output Format and Timing Diagram



Note 1: Upon each power-up, the OCLK signal's relationship with the CK input clock may be one of two possibilities, shown above as Case 1 and Case 2. Therefore, in reference to the OCLK phase, the earlier data samples may be on the X or Y bus. The OCLK's phase relationship with the X and Y data busses is fixed: the X data bus always changes with the rising edge of OCLK and the Y bus with the falling edge.

Note 2: Latency = 1.5 sampling clock cycles + subcycle fixed delay.

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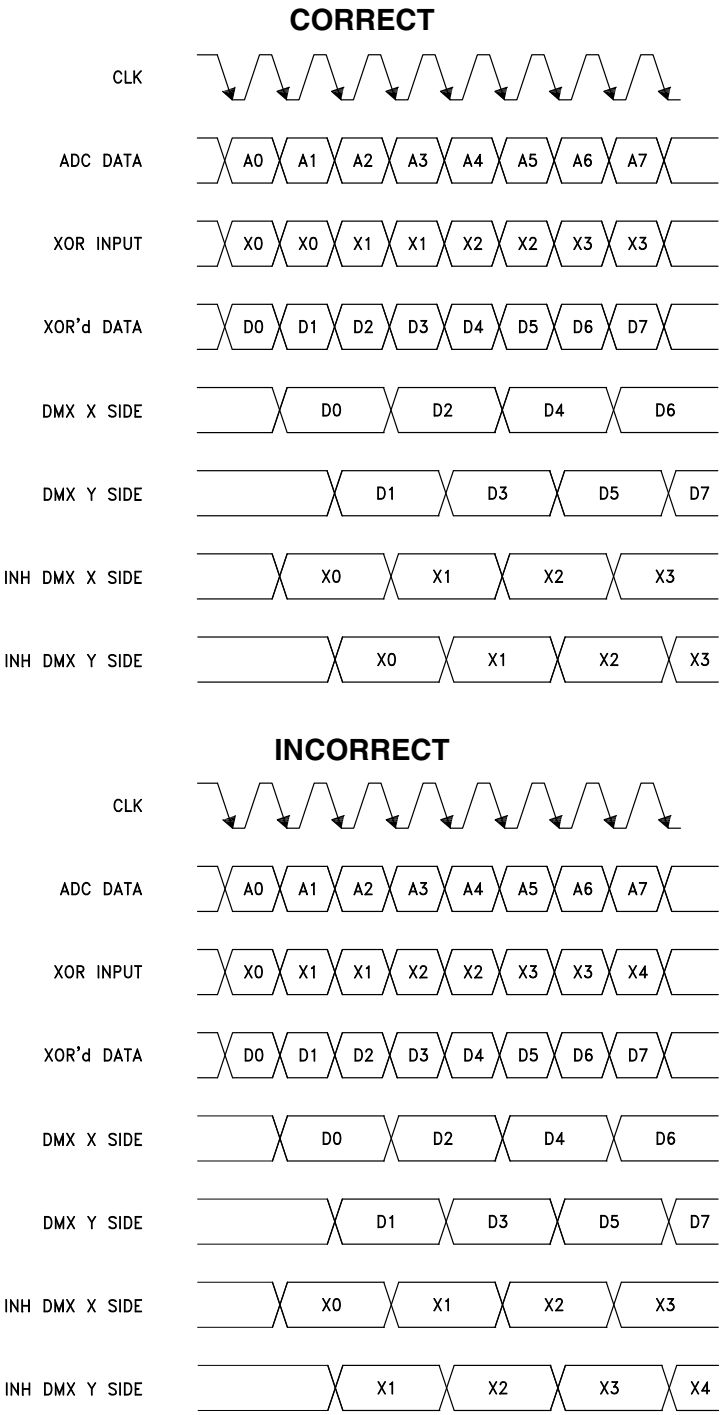
XOR Input Alignment Timing Diagrams for X Side Leading



Data
D0 = A0 xor X0
D1 = A1 xor X0
D2 = A2 xor X1
D3 = A3 xor X1
D4 = A4 xor X2
D5 = A5 xor X2

Data
D0 = A0 xor X0
D1 = A1 xor X1
D2 = A2 xor X1
D3 = A3 xor X2
D4 = A4 xor X2
D5 = A5 xor X3

In the case shown, the FPGA aligns the data with the X side leading. In the incorrect case, a 1-bit shift is caused by the 1 clock cycle delay in the XOR.

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Operating Conditions

Parameter	Description	Min.	Typ.	Max.	Units
AV_{EE}	Analog supply voltage range	-5.5	-5.0	-4.5	V
OV_{EE}	Digital and output driver supply voltage range	-3.6	-3.3	-3.0	V
V_{input}	IN, CKx, XORx, and QTx inputs voltage	-2.0		+0.5	V
V_{output}	Xxx, Yxx, and OCLKx outputs voltage	-1.5		+0.5	V
AGND-OGND		-0.3	0	+0.3	V
T_A	Ambient temperature *Limited by the Absolute Maximum junction temperature limit and depends upon the system thermal design*	-40		+85	°C

Note 1: The conditions listed in this table must be observed for the device to be functional as specified in this document. These conditions do not guarantee specific performance levels, which are listed in the DC, AC, and switching specification tables and apply under the test conditions specified therein.

Note 2: All voltages are in reference to the AGND pin of the device.

ELECTROSTATIC SENSITIVE DEVICE
OBSERVE HANDLING PRECAUTIONS

Absolute Maximum Ratings

Parameter	Description	Min.	Typ.	Max.	Units
T_J	Junction temperature			+125	°C
$T_{storage}$	Storage temperature	-65		+150	°C
$T_{operate}$	Operating temperature	-40		+85	°C
AV_{EE}	Analog supply voltage	-5.8		+0.5	V
OV_{EE}	Digital and output driver supply voltage range	-5.8		+0.5	V
V_{input}	IN, CKx, XORx, and QTx inputs voltage	V_{EE} - 0.3		AGND+0.8	V
V_{output}	Xxx, Yxx, and OCLKx outputs voltage	OV_{EE} - 0.3		OGND+0.8	V
ESD Rating	Human body model (Class 1C)		1k		V

Note 1: Operating the device beyond the limits specified in this table may cause immediate damage to the device. Functional operation of the device is further limited by the Operating Conditions. Device functionality is not implied by the Absolute Maximum Ratings.

Note 2: All voltages are in reference to AGND pin of the device.

Thermal Information

Parameter	Description	Min.	Typ.	Max.	Units
Θ_{JCb}	Thermal resistance - junction-to-case bottom pad		2.5		°C/W

Note 1: The thermal pad at the bottom of the device package must be attached to a PCB ground plane for conduction purposes as this is the most main path of heat dissipation of this device. It is also strongly recommended that the thermal pad should be connected to a metal pad on the underside of the PCB through multiple vias and that a heat sink should always be attached to this PCB metal pad.

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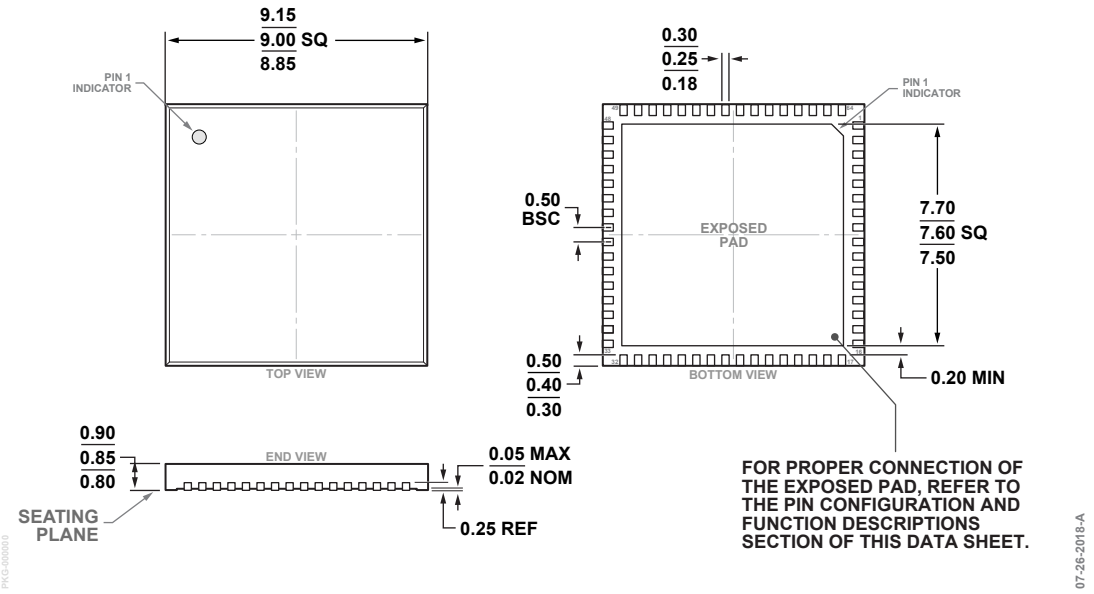
Outline Drawing



64-Lead Lead Frame Chip Scale Package [LFCSP]
9 x 9 mm Body and 0.90 mm Package Height
(CP-64-20)
Dimensions shown in millimeters

Package Information

Part Number	Package Body Material	Lead Finish	MSL Rating	Package Marking [2]
HMCAD5831LP9BE	RoHS-compliant Low Stress Injection Molded Plastic	100% matte Sn	MSL6 [1]	HAD5831 XXXX

[1] Max peak reflow temperature of 260 °C
[2] 4-Digit lot number XXXX

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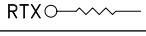
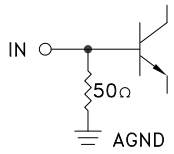
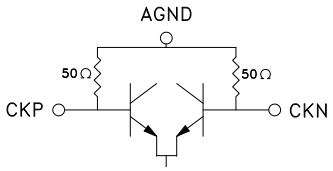
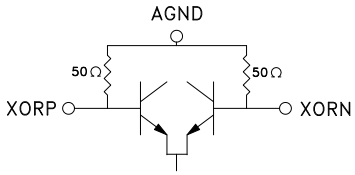
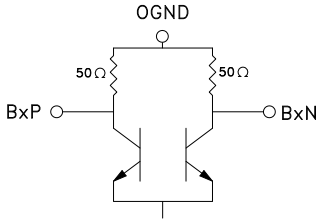
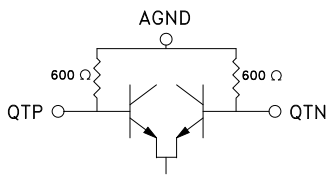
Pin Descriptions

Pin Number	Function	Description	Interface Schematic
1, 15	RTF, RBF	Reference ladder top and bottom taps	
2, 7, 9, 10, 13, 16, 17, 18, 21, 60, 63, 64	AGND	Analog ground	
3, 4, 5, 6, 14	AVEE	-5V analog rail These pins and the exposed paddle must be connected to the negative voltage supply.	
8	IN	Single-ended RF input referenced to AGND.	
11, 12	CKP, CKN	Differential clock inputs Current Mode Logic (CML) referenced to AGND. For single-ended operation, CKN must be tied to the common-mode point.	
19, 20	XORP, XORN	Differential XOR inputs Current Mode Logic (CML) referenced to AGND. For single-ended operation, XORN must be tied to the common-mode point.	
22, 23, 27, 30, 33, 36, 39, 42, 45, 48, 51, 54, 58, 59	OGND	Digital ground	
24, 25, 56, 57	OVEE	-3.3V digital rail	
26, 55	VREF2, VREF1	Output level control Output level may be increased or decreased by applying a voltage to Vref pins.	
28, 29, 31, 32	XVN, XVP, YVN, YVP	Overrange Current Mode Logic (CML) referenced to OGND. Normally ac-coupled to the digital ASIC or FPGA device.	
34, 35, 37, 38, 43, 44, 46, 47, 49, 50, 52, 53	X0N, X0P, Y0N, Y0P, X1N, X1P, Y1N, Y1P, X2N, X2P, Y2N, Y2P	Differential data outputs Current Mode Logic (CML) referenced to OGND. Normally ac-coupled to the digital ASIC or FPGA device.	
40, 41	OCLKN, OCLKP	Differential clock output Current Mode Logic (CML) referenced to OGND.	
61, 62	QTN, QTP	Differential data inhibit inputs For single-ended operation, QTN must be tied to the common-mode point.	

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Application Information

Reference Ladder

The ADC's voltage reference ladder comprises 8, 18 Ω resistors, or 144 Ω total nominal resistance. Pin 1, RTF, and pin 15, RBF, are provided for the top and bottom reference taps. These pins are driven by external supplies to establish the desired full-scale range of the ADC. The RF signal input (pin 8, IN) to the ADC, which is nominally centered at 0V (AGND), drives an internal emitter follower with a nominal VBE of -936 mV. Hence the center of full-scale range should center near -936 mV. The voltage at pin RTF is then -936 mV + $V_{full\text{-}scale}$/2. Likewise the voltage at pin RBF is -936 mV - $V_{full\text{-}scale}$/2.

As an example, if the user had a peak-to-peak input voltage swing of 256 mV centered at 0V and required the full-scale input range of the ADC to be 256 mV as well, RTF would be -936 mV + 128 mV = -772 mV. RBF would be -936 mV - 128 mV = -1.028V. Note that the diode drop, -936 mV, is dependent on temperature and process variations. RTF and RBF values in the "Electrical Specifications" table on pages 1 and 2 are shown as nominal values only.

Input Signal

The RF input is internally terminated with 50 Ohms to AGND, which should be the system RF ground. Normally, the input signal is expected to have a common-mode point at this 0V point. Because this device allows the user to set the top and bottom voltages of the reference ladder inside the device, the user has significant flexibility in adjusting the ADC span and thus the full-scale signal amplitude as well as the input signal's common-mode point.

However, it is very important to notice that there are absolute voltage level limits on the peak input signal voltage. These are indicated in the Operating Conditions table in this document. For proper operation of the device, the input signal must never swing higher than the Vinput-max or lower than Vinput-min voltages indicated in the Operating Conditions table.

The user is cautioned to also pay attention to the Absolute Maximum Ratings table as it lists the maximum input voltage beyond which damage to the device will result.

VREF Pins

Pins 26 and 55 (VREF1 and VREF2) should be connected together off chip and the pair is then connected to the OGND through a resistor. These pins are used to vary the output swing voltage. The Application Circuit shown uses a 200 Ω resistor. This provides the typical output swings listed in the Electrical Specifications table. Increasing the voltage on VREF1 and VREF2 will increase the output swing. Conversely, decreasing the VREF1 and VREF2 voltages will decrease the output swing.

Overrange Output

Pins 28, 29, 31, and 32 provide overrange output bits. This function indicates when the input signal is out of range of the reference ladder voltages. The bit will be high when either the signal is above RTF or below RBF. The overrange bit is cleared for the next clock cycle containing in-range data.

Data Inhibit

All data outputs can be forced to "0" by enabling the Data Inhibit function (pins 61 and 62). By driving the QTP pin high and the QTN pin low, the ADC core will produce all 0s. This occurs prior to the XOR function and the demux. When QTP is low and QTN is high, the chip operates normally, and these inputs must be set this way for normal operation.

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Application Information *(continued)*

Data XOR

All data outputs from the ADC core can be modulated by an external source. This allows the user to use AC coupling for output line connection to a SERDES input of an FPGA. This function occurs prior to the demux. The XOR input signal is retimed by the full rate internal clock and requires low jitter and suitable rise and fall times. Please contact Hittite Microwave for sample driver circuits. Typical modulation frequencies are 100 MHz to 300 MHz. For a square wave signal, a multiple of two divisor of the full rate internal clock should be used, e.g. 1/128th or 1/64th of the ADC clock. Due to the nature of the retiming scheme, the demux channel relationship timing can vary. This is dependent on when the XOR input is sampled relative to the full rate internal clock. See timing diagrams on page 5. For example, a nominal setup may have demux side X leading and side Y trailing. If the XOR input is shifted relative to the internal clock, side Y may lead and side X may trail. It is highly recommended that a variable delay be used to adjust the phase of the XOR input to avoid transitions that are very close to internal clock edges. See Typical Operation Example for more information. The XOR function can be used with the Data Inhibit function to produce a sync pattern for aligning the lanes of SERDES inputs. The device outputs are inverted when XOR is low.

Evaluation Board Description

EVAL01-HMC5831LP9 (131498-3) demonstrates the HMCAD5831LP9BE in an environment ready to be connected to an FPGA. Along with the ADC, the board features three other Hittite Microwave components. The clock output of the ADC is divided down by 32 (a stage of 8 and a stage of 4, U1, and U2) to produce a clock output that is 1/64th of the ADC clock input. This clock is available to drive the FPGA or other system components. The ADC XOR input has programmable delay (U4) allowing the user to fine-tune the XOR clock edges going into the ADC. The INHIBIT and D8BX inputs are 0 to +3.3V, compatible with most FPGAs. Finally, the ADC_VR pin allows the user to control the output voltage swing of the ADC. Output connectors J2 and J3 are high-performance SAMTEC connectors, part number ERF8-013-05.0-DV.

Ten-Level Operation

The HMCAD5831LP9BE can be used as a ten-level (3.32 bits) ADC by combining the regular data outputs with the Overrange Bit. The bottom code (code 0) is equal to OVR high and all the bits low. For codes 1 through 8, the ADC functions normally (with OVR low). The top code, code 9, is all bits high. Note that the INL/DNL plots include OVR in this manner.

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Application Information *(continued)*

Typical Operation Example

When using the device evaluation board, high-quality signal generator equipment must be used that provides low enough broadband phase noise to support the SNR specifications of this device at the very high signal frequencies.

The reference ladder voltages should be provided with stable, linear power supplies. As a starting point, it is recommended that the RTF and RBF voltage should be set to -772 mV and -1.028V, as described in the Reference Ladder subsection. The input signal can then be provided with the appropriate signal generator with 50 Ohm, single-ended output that is ac-coupled into the eval board's SMA connector. The signal generator output strength should be set at a low level such as -20 dBm before the output is enabled. The signal level can then be increased gradually as required, but never beyond the 256 mV full-scale swing that had been selected in this example. The Clock input can similarly be provided with an RF signal generator or a Hittite PLL/VCO device evaluation board, provided that the CKN input is set at the common-mode point – 0 V (AGND) in this case. Although higher amplitudes are possible, initially the user should keep the clock signal strength at -3 dBm or less. And, of course, care should be taken with the clock input as well to not overload the ADC.

An FPGA with suitably fast SERDES inputs can capture data from the HMCAD5831LP9BE using the following routine. The FPGA produces an INHIBIT high signal causing the ADC core to produce all 0s. The XOR input to the ADC runs at a slow clock rate and modulates the ADC output to produce a known waveform at the FPGA inputs. The FPGA then uses these signals to align the lanes. When the lanes are aligned, the INHIBIT signal goes low and the ADC produces signal data that continues to be modulated by the XOR input. The FPGA then corrects for the modulation. Note that the FPGA can generate the XOR modulation signal (in which case a PRBS sequence could be used). Depending on the phase of the XOR input modulation waveform, either demux output (X or Y) can be the leading data sample. In this case, the FPGA would need to resolve which lane is the leader. This can be accomplished by driving the ADC with a known signal, evaluating the outputs and reassembling FPGA data if necessary. It is recommended to do this on each power-up. It is also recommended to perform a routine to ensure that the XOR input waveform is properly aligned with the internal clock. This can be accomplished by sweeping the external variable delay stage.

Operation Over Full Temperature Range

The device typically consumes 4.2 watts power and thus requires careful thermal design at the system level. A heat sink of at least 25 cm^2 surface area is required under all conditions. Most of the device heat dissipation occurs on the bottom side of the package. The package has a thermal paddle on the bottom side. The PCB design must solder this paddle through a grid of several thermal vias to a metal pad on the bottom side of the PCB where the heat sink should be attached. In addition, the AVEE pins of the device and the paddle must be connected to the negative -5V supply plane. It is highly recommended that some manner of additional cooling technique should be employed in order to maximize the ambient temperature range of the device's operation.

The Electrical Specifications section lists only the performance parameters at +25 °C temperature. The performance diminishes as temperature increases. On the device evaluation board, in Hittite lab settings with minimal air flow, a temperature rise of 18-20 °C was observed between the ambient temperature and the thermal pad at the bottom of the PCB. The ultimate limit to the device's temperature capabilities is the maximum junction temperature specified in the Absolute Maximum Ratings table in this document. The thermal resistance from the device junction to the device thermal paddle is specified in the Thermal Information table. With this information and knowledge of the system's heat dissipation capabilities from the PCB pad to the ambient, one can determine the ambient temperature range the device can support.

Based on data taken on the device evaluation board under Hittite's lab conditions, it is believed that 22 GS/s maximum speed can be expected across the temperature range of -40 °C and +85 °C with reasonable system thermal design.

For price, delivery, and to place orders: Analog Devices, Inc., One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106
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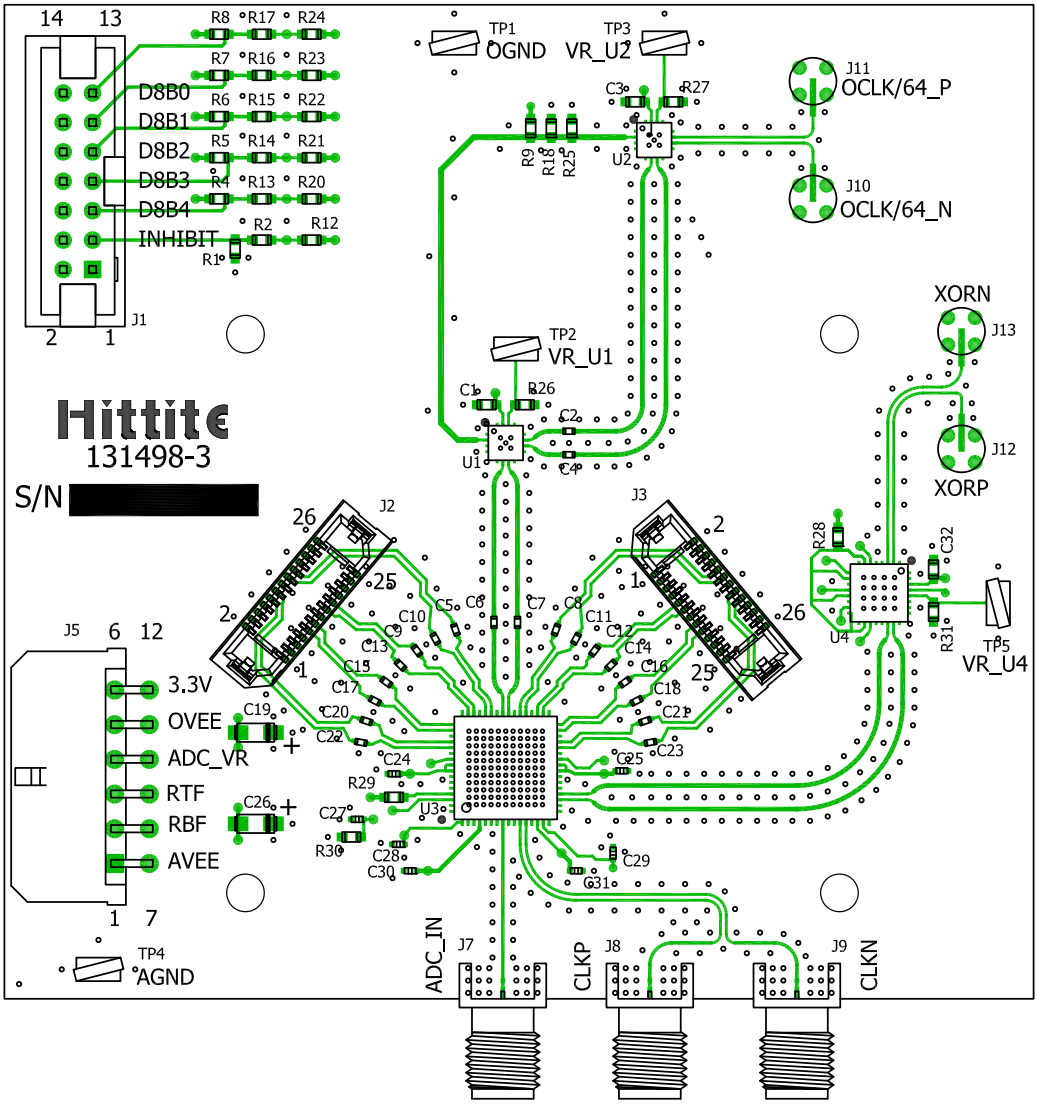
3-BIT 26 GSPS ANALOG-TO-DIGITAL CONVERTER W/ OVERRANGE, INHIBIT, AND 1:2 DEMUX

Evaluation PCB



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List of Materials for Evaluation PCB EV1HMCAD5831LP9B [1]

Item	Description
J1	14 Position Straight Header
J2, J3	Edge Rate Socket Strip, 26 Position Samtec Edge Rate ERF8-013-05.0-DV
J5	Conn Header 12 Position 3 mm 2 Rows
J7 - J9	PCN Mount k RF Connectors
J10 - J13	SMP Full Detent RF Connectors
C1, C3, C32	1000 pF Capacitor, 0603 Pkg.
C2, C4 - C18, C20 - C23	1000 pF Capacitor, 0402 Pkg
C19, C26	4.7 µF Capacitor, 1206 Pkg.
C24 - C25, C27 - C31	100 nF Capacitor 0402 Pkg.
R1, R4 - R8	33 K Ohm Resistor, 0603 Pkg.
R2, R12 - R17, R20 - R24	3.3 K Ohm Resistor, 0603 Pkg.
R18, R25, R28	1.2 K Ohm Resistor, 0603 Pkg.
R26, R27, R31	51 Ohm Resistor, 0603 Pkg.
R29	14 K Ohm Resistor, 0603 Pkg.
R30	200 Ohm Resistor, 0603 Pkg.
U1	HMC859LC3 Divide By 8, 26 GHz
U2	HMC959LC3 Divide By 4, 26 GHz
U3	HMCAD5831LP9BE 26 GSPS 3-bit ADC
U4	HMC856LC5 5-Bit Time Delay, 26 GHz
PCB [2]	131498-3 Evaluation Board

[1] Reference this number when ordering complete evaluation PCB

[2] Circuit Board Material: Arlon 25FR or Rogers 4350

The circuit board used in the application should use RF circuit design techniques. Signal lines should have 50 Ohm impedance while the package ground leads should be connected directly to the ground plane similar to that shown. The exposed metal package base must be connected to AVEE. A sufficient number of via holes should be used to connect the top and bottom ground planes. The evaluation circuit board shown is available from Analog Devices, upon request.

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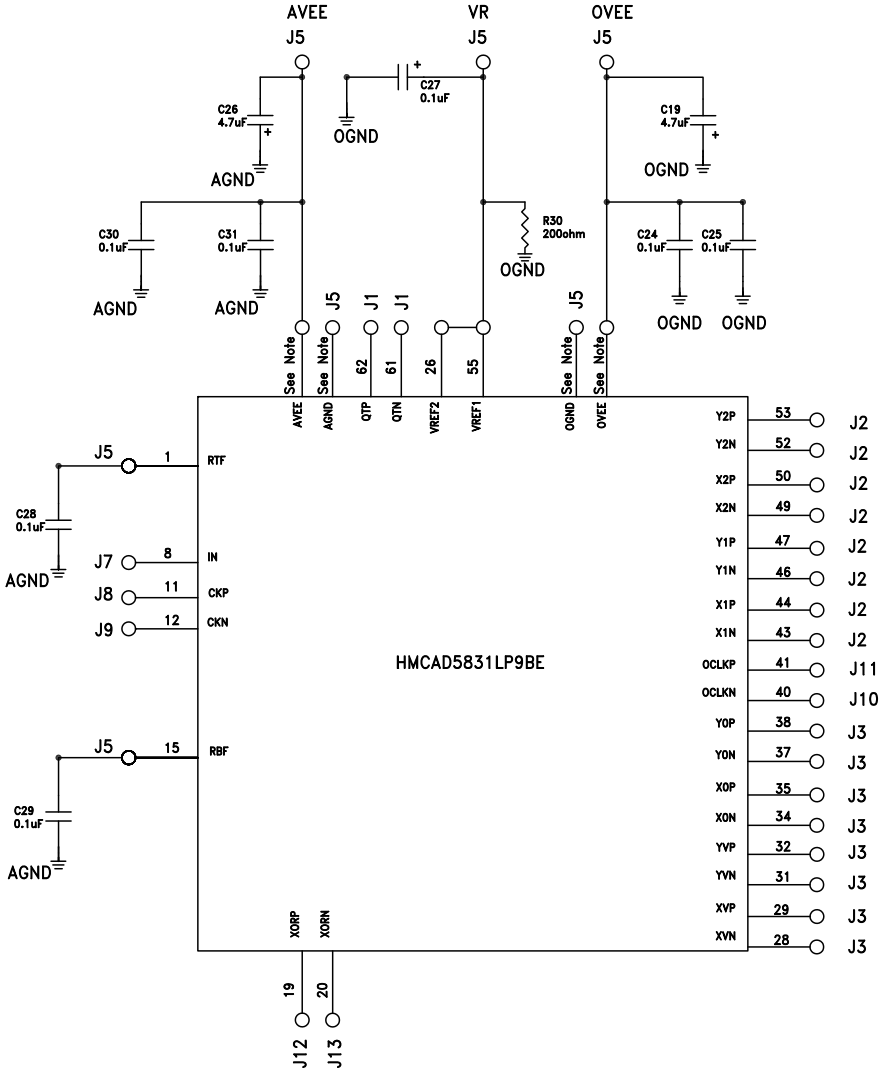
Application Circuit



Pin Number	Function	Description
2, 7, 9, 10, 13, 16, 17, 18, 21, 60, 63, 64	AGND	Analog ground
3, 4, 5, 6, 14	AVEE	-5V analog rail These pins and the exposed paddle must be connected to the negative voltage supply.
22, 23, 27, 30, 33, 36, 39, 42, 45, 48, 51, 54, 58, 59	OGND	Digital ground
24, 25, 56, 57	OVEE	-3.3V digital rail
J5		12-position MOLEX
J2, J3		SAMTEC

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