DAC8801/11EVM

This user guide describes the DAC8801/11 Evaluation Module. It covers the operating procedures and characteristics of the EVM board along with the supported device. The physical printed circuit board (PCB) layout, schematic diagram, and circuit descriptions are included.

Contents

List of Figures

List of Tables

1 Information About Cautions and Warnings

This manual contains cautions and warnings.

CAUTION

This is an example of a CAUTION statement.

A CAUTION statement describes a situation that could potentially damage this EVM board or your software or equipment.

WARNING

This is an example of a WARNING statement.

A WARNING statement describes a situation that could potentially cause HARM to you.

The information in a caution or a warning is provided for your protection. Read each caution and warning carefully.

2 Related Documentation from Texas Instruments

To obtain a copy of any of the following TI documents, call the Texas Instruments Literature Response Center at (800) 477-8924 or the Product Information Center (PIC) at (972) 644-5580. When ordering, identify this manual by its title and literature number. Updated documents can also be obtained through our website at www.ti.com.

Related Documentation

Data Sheets	Literature Number
DAC8801	SLAS403
DAC8811	SLAS411
OPA277/2277	SBOS079
INA105	SBOS145
REF102	SBVS022A

3 Questions About This or Other Data Converter EVMs

If you have questions about this or other Texas Instruments Data Converter evaluation modules, please feel free to e-mail the Data Converter Application Team at dataconvapps@list.ti.com. Include in the subject heading the product you have questions or concerns with.

4 EVM Overview

This section provides an overview of the DAC8801/11 evaluation module (EVM), and instructions on setting up and using this evaluation module.

4.1 Features

This EVM features the DAC8801/11 multiplying digital-to-analog converter (MDAC). It provides a quick and easy way to evaluate the functionality and performance of the high resolution serial input MDAC. The EVM provides the serial interface header to easily attach to any host microprocessor or TI TMS320™ DSP family base system for communication.

4.2 Power Requirements

The following sections describe the power requirements of this EVM.

4.2.1 Supply Voltage

The dc power supply for the digital section (V_{DD}) of this EVM is dedicated to 5 V via the J3-1 terminal or J6-10 terminal and is referenced to ground through the J3-2 and J6-5 terminals respectively.

The dc power supply requirements for the analog section of this EVM are as follows; the V_{CC} and V_{SS} are typically ±15 V but can range from ±4.5 V minimum to ±18 V maximum and connect through J1-3 and J1-1 respectively, or through J6-1 and J6-2 terminals. The 5VA connects through J6-3 and the -5VA connects through J6-4. All of the analog power supplies are referenced to analog ground through J1-2 and J6-6 terminals.

The V_{CC} supply sources the positive rail of the external output amplifier, U4A as well as the current-to-voltage converter amplifier, U5. The supply for the voltage reference circuit composed of U2, U3 and U4B also uses V_{CC}. The negative rail of U4 and U5 is supplied by V_{SS}, though U4 can also be selected to be connected to AGND via W5 jumper. The external output amplifier is installed as an option to provide output signal conditioning or for other output configurations desired

CAUTION

To avoid potential damage to the EVM board, make sure that the correct cables are connected to their respective terminals as labeled on the EVM board.

Stresses above the maximum listed voltage ratings may cause permanent damage to the device.

4.2.2 Reference Voltage

The externally generated ±10-VDC precision voltage reference is jumper selectable via W1. Either 10 V or –10 V can be applied to the DAC8801/11 reference input if the onboard dc source is selected. The external reference voltage source is supplied by the REF102, which is a 2.5 ppm/°C with excellent line regulation and stability. The -10-V reference is created by using the INA105. The ±10-VDC reference provides the DAC8801/11 voltage output range. An external reference source of up to ±15 VAC can be applied to the reference input via TP1 if an ac source is desired.

4.3 EVM Basic Functions

This EVM is designed primarily as a functional evaluation platform to test certain functional characteristics of the DAC8801/11 MDAC. Functional evaluation of the installed MDAC device can be accomplished with the use of any microprocessor, TI DSP or some sort of a signal/waveform generator.

The headers J2 and P2 are the connectors provided to allow the control signals and data required to interface a host processor or waveform generator to the DAC8801/11EVM using a custom built cable.

The MDAC output can be monitored through the J4 header connector. In addition, the MDAC output (via U5) can be connected to the output operational amplifier, U4A, by using a jumper across pins 5 and 6 or pins 7 and 8 of J4 header. The output operational amplifier, U4A, is configurable through J5, W5 and W15 for any desired waveform characteristic.

A block diagram of the DAC8801/11EVM is shown in Figure 1.

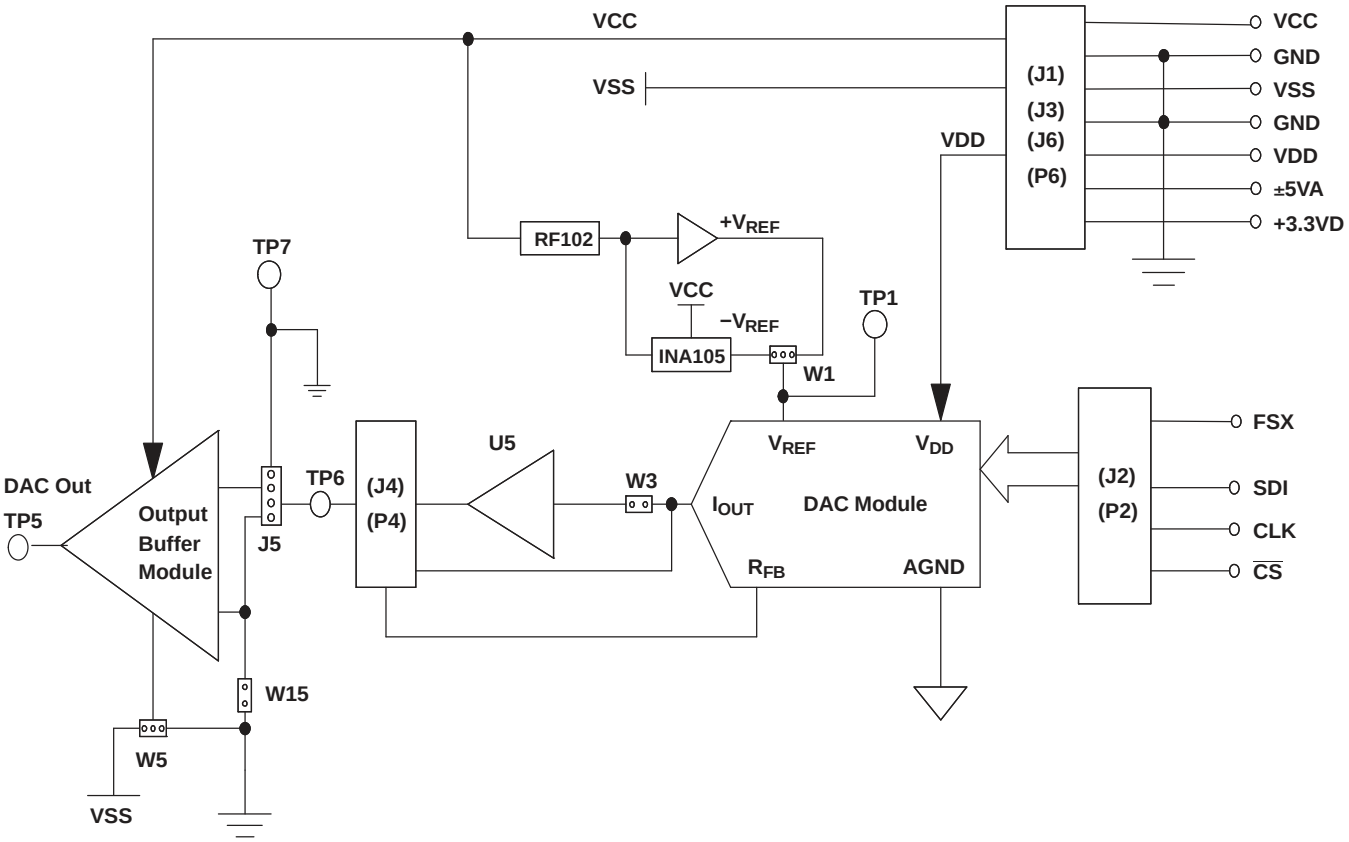

Figure 1. DAC8801/11EVM Block Diagram

5 PCB Design and Performance

This section covers the layout design of the PCB describing the physical and mechanical characteristics of the EVM. It shows the resulting performance of the EVM, which can be compared to the device specification listed in the data sheet.

5.1 PCB Layout

The DAC8801/11EVM is designed to demonstrate the performance quality of the installed MDAC device under test, as specified in the data sheet. Careful analysis of the EVM physical restrictions and factors that contributes to the EVM performance degradation is the key to a successful design implementation. The obvious attributes that contributes to the poor performance of the EVM can be avoided during the schematic design phase by properly selecting the right components and designing the circuit correctly. The circuit should include adequate bypassing, identifying and managing the analog and digital signals and knowing or understanding the components mechanical attributes.

A critical part to any design lies in the layout process. Placement of components and the proper routing of signals can greatly improve the performance of the overall system. Bypass capacitors should be placed as closely as possible to the pins and the analog and digital signals should be properly separated from each other. The power and ground planes are very important and should be carefully considered in the layout process. A solid plane is ideally preferred but sometimes impractical, so when solid planes are not possible, a split plane will do the job. When considering a split plane design, analyze the component placement and carefully split the board into its analog and digital sections starting from the device under test. The ground plane plays an important role in controlling the noise and other effects that otherwise

contributes to the error of the MDAC output. To ensure that the return currents are handled properly, route the appropriate signals only in their respective sections, meaning the analog traces should only lay directly above or below the analog section and the digital traces in the digital section. Minimize the length of the traces but use the biggest possible trace width allowable in the design. These design practice discussed can be seen in the following figures.

The DAC8801/11EVM board is constructed on a four-layer printed-circuit board using a copper-clad FR-4 laminate material. The printed-circuit board has a dimension of 43,1800 mm (1.7000 inch) × 82,5500 mm (3.2000 inch), and the board thickness is 1,5748 mm (0.0620 inch). Figure 2 through Figure 6 show the individual artwork layers.

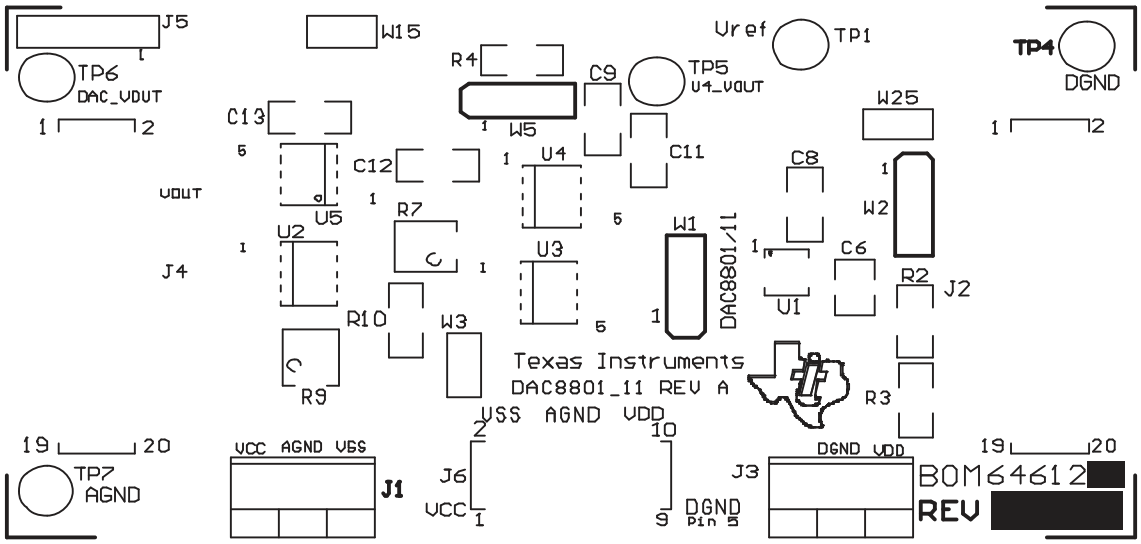

Figure 2. Top Silkscreen

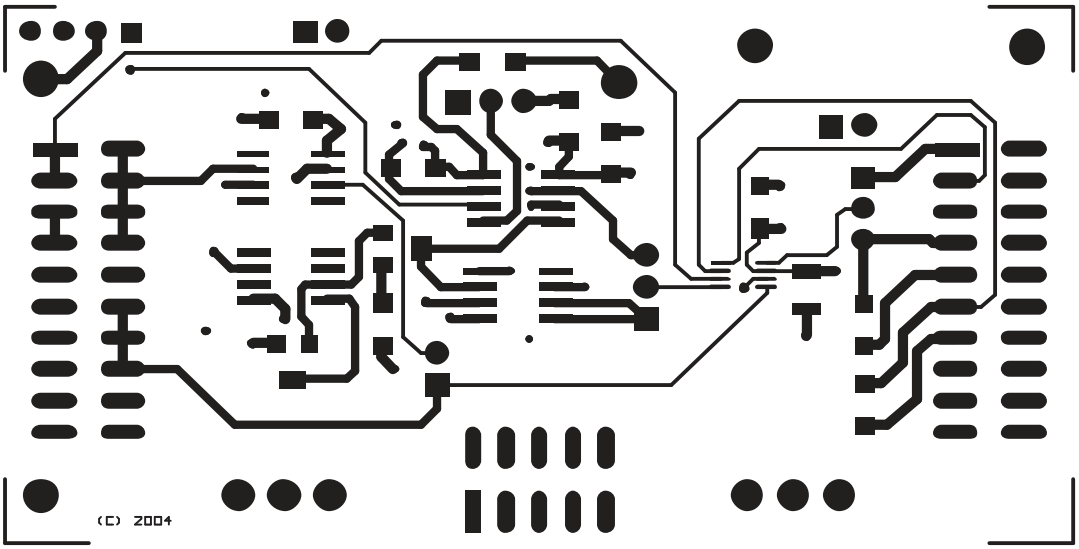

Figure 3. Layer 1 (Top Signal Plane)

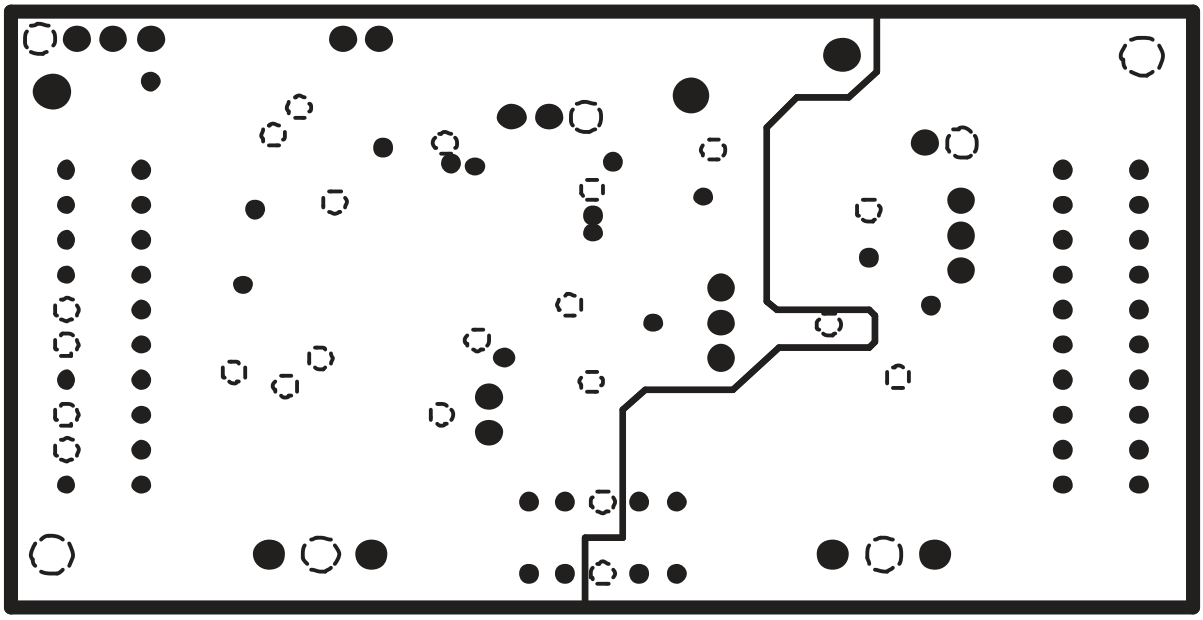

Figure 4. Layer 2 (Ground Plane)

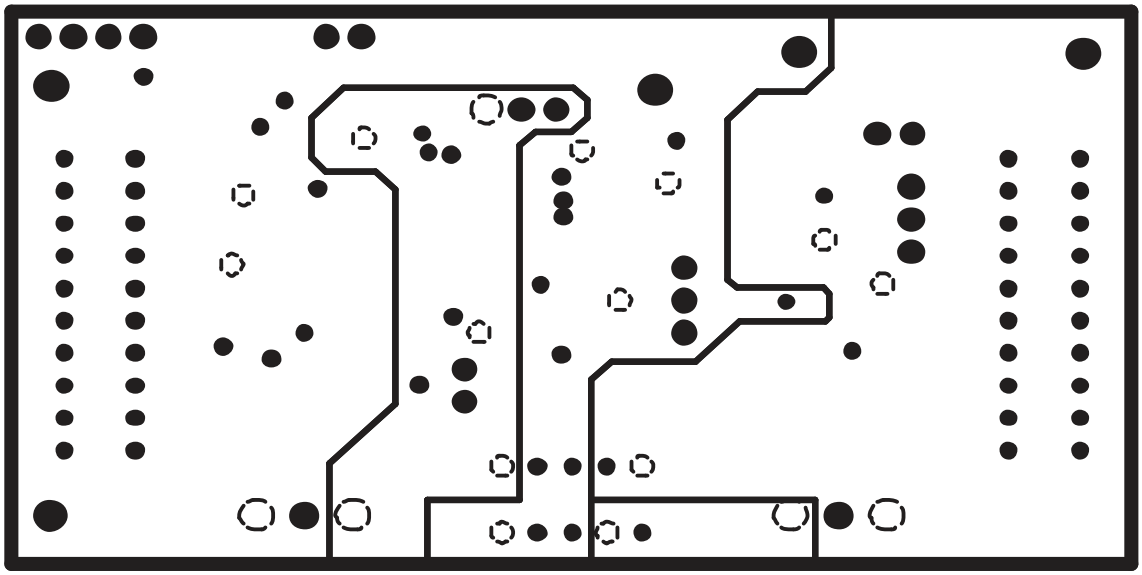

Figure 5. Layer 3 (Power Plane)

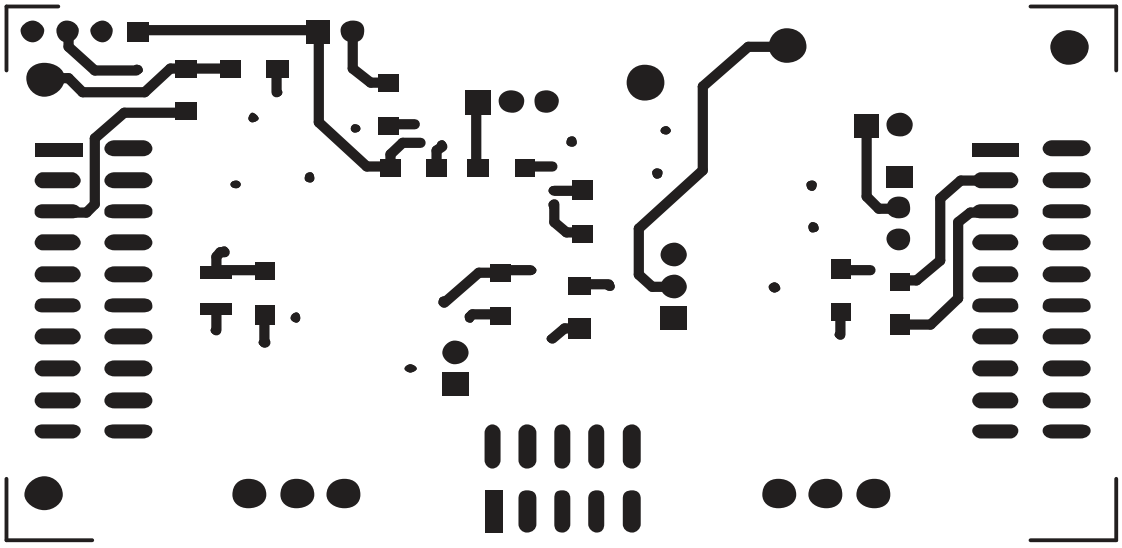

Figure 6. Layer 4 (Bottom Signal Plane)

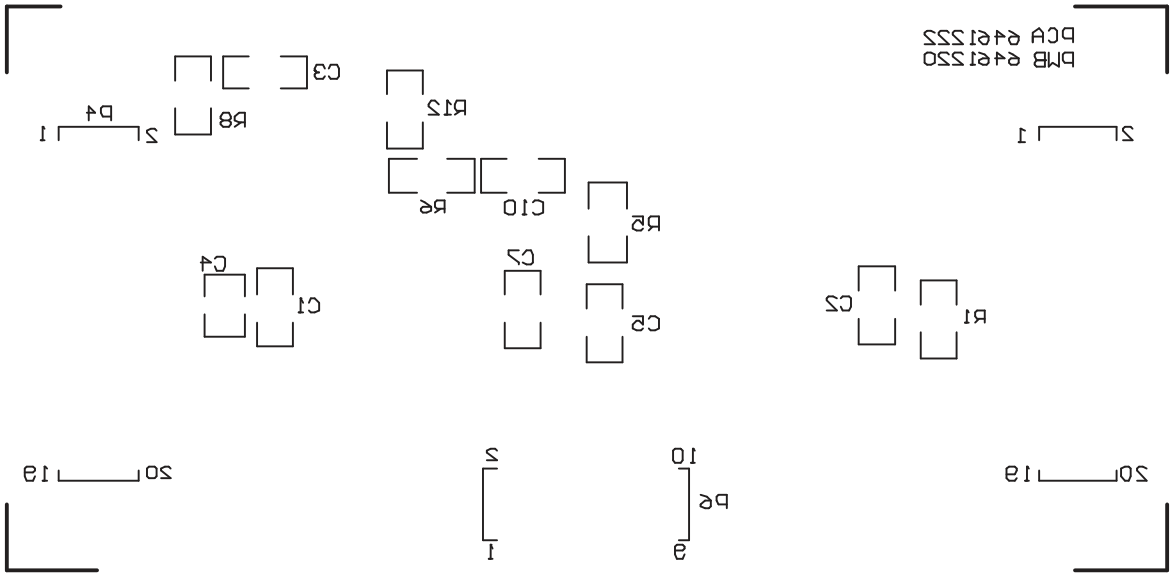

Figure 7. Bottom Silkscreen

5.2 EVM Performance Results

The EVM performance test is performed using a high density DAC bench test board, an Agilent 3458A digital multimeter and a PC running the LabVIEW® software. The EVM board is tested for all codes of the device under test (DUT) and is allowed to settle for 1 ms before the meter is read. This process is repeated for all codes to generate the measurements for INL and DNL results.

The result of the DAC8801/11EVM characterization test is shown in Figure 8. Note that the DAC8811 uses the OPA277 for the I-to-V conversion.

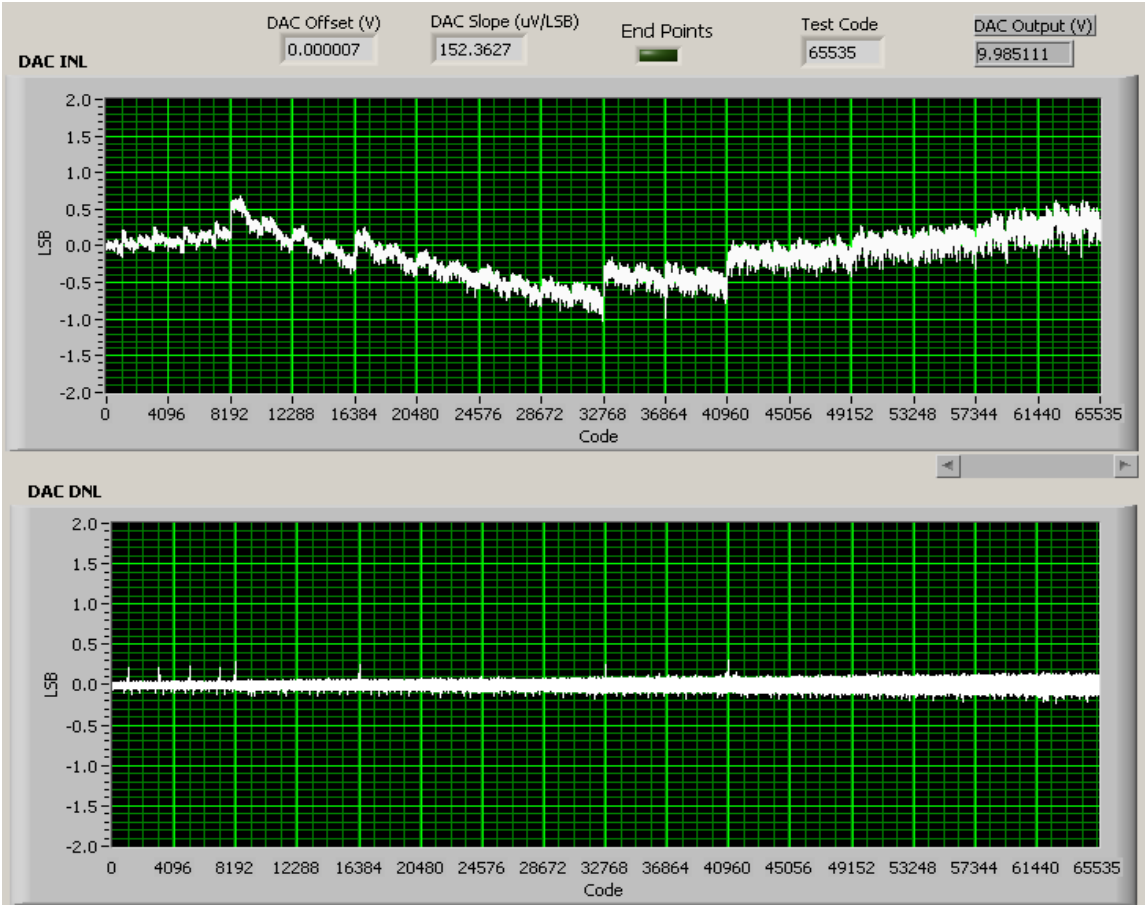

Figure 8. INL and DNL Characterization Plot for the DAC8811

6 EVM Operation

This section covers in detail the operation of the EVM to provide guidance to the user in evaluating the onboard MDAC and how to interface the EVM to a host processor.

See the specific MDAC data sheet, as listed in the *Related Documentation from Texas Instruments* section of this user guide (Section 2), for more information about the MDAC serial interface and other related topics.

The EVM board is factory tested and configured to operate in the bipolar output mode.

6.1 Factory Default Setting

The EVM board is set to its default configuration from factory as described in Table 1 to operate in unipolar voltage output operation. The default jumper settings below are shown in Figure 9.

Table 1. DAC8801/11EVM Factory Default Jumper Setting

Reference	Jumper Position	Function
W1	2-3	Routes +10V reference source to the MDAC V_{REF} input.
W2	1-2	MDAC Chip Enable is driven by $\overline{CS}$ via J2-1.
W3	1-2	MDAC I_{OUT} is connected to the I-to-V converter, U5.
W5	1-2	Negative supply rail of U4A operational amplifier is sourced by V_{SS}.
W15	OPEN	U4A operational amplifier configuration is set for 5x gain.
W25	OPEN	Chip Enable is disconnected from GND so that the control signal from W2 is allowed to drive this pin.
J4	1-2	Tie R_{FB} to MDAC V_{OUT} .
	7-8	MDAC V_{OUT} connected to J5 header via RC filter.
J5	1-2	MDAC V_{OUT} is routed to the inverting input of U4A.
	3-4	Noninverting input of U4A tied to AGND.

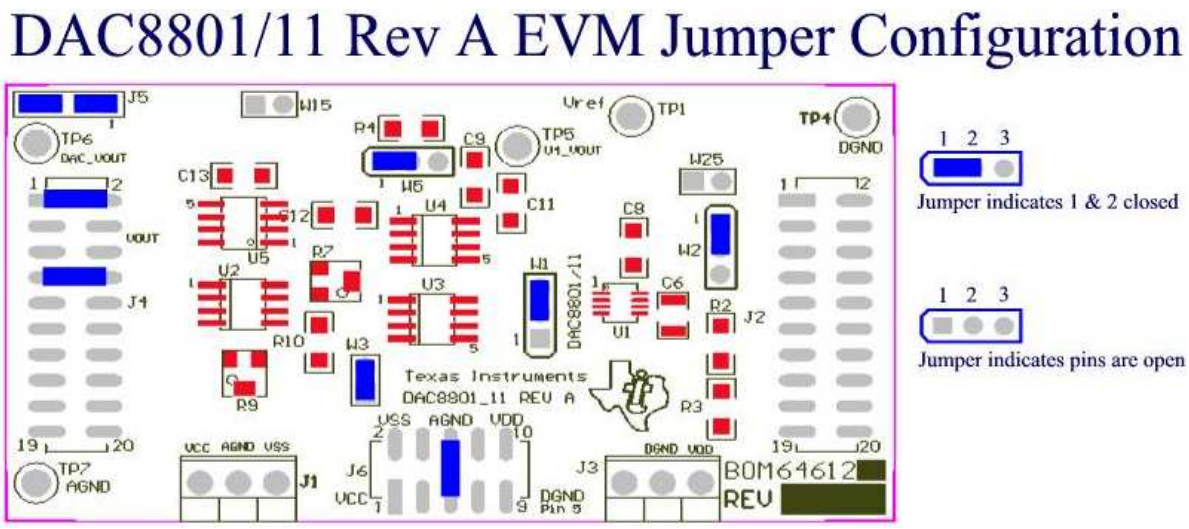

Figure 9. DAC8801/11EVM Default Jumper Setting

6.2 Host Processor Interface

The host processor drives the MDAC, so the MDACs proper operation depends on the successful configuration between the host processor and the EVM board. In addition, a properly written code is also required to operate the MDAC.

A custom cable can be made specific to the host interface platform. The EVM allows interface to the host processor through J2 header connector for the serial control signals and the serial data input. The output can be monitored through the J4 header connector.

An interface adapter card is also available for specific TI DSP starter kit as well as an MSP430 based microprocessor as mentioned in Section 4 of this manual. Using the interface card alleviates the tedious task of building customize cables and allows easy configuration of a simple evaluation system.

This MDAC EVM interfaces with any host processor capable of handling serial communication protocols or the popular TI DSP. For more information regarding the serial interface of the particular MDAC installed, refer to the specific MDAC data sheet, as listed in the *Related Documentation from Texas Instruments* section (Section 2) of this user guide.

6.3 The Output Operational Amplifiers

The EVM includes operational amplifiers for various applications. The U5 operational amplifier is used to convert the current output of the MDAC to voltage output. Though the option of voltage output is implemented, the current output, I_{OUT}, can still be monitored through J4 output header, via pins 12, 14, and 16.

The footprint of U5 is very common for most operational amplifiers; therefore, it is easy to find an operational amplifier that suits each specific application.

The following sections describe the different configurations of the output amplifier, U4A. This additional operational amplifier can be used to serve as buffer to unload the I-to-V circuit of the MDAC. It can also be used for different signal conditioning and amplification purposes desired. The EVM comes configured with the U4A operational amplifier set to a gain of five configuration. If a gain of two is desired, the inverting input of U4A can be tied to AGND (via W15) to achieve this specific configuration. In addition, the inverting input of U4A can also be connected to the MDAC voltage output (by shorting pins 1 and 2 of the J5 header) or to any voltage source through J5-1.

This buffering circuit may present some slight distortion because of the feedback resistor and capacitor. If this is the case, the user can easily configure the feedback circuit to closely match their desired wave shape by simply removing R6 and C12 and replacing it with the proper values. Additionally, C12 can be removed altogether and R6 can be replaced with a 0-Ω resistor if desired.

6.3.1 Unity Gain Output

Table 2 shows the jumper setting for the unity gain configuration of the MDAC output buffer in unipolar or bipolar supply mode.

Table 2. Unity Gain Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
J5	2-3	2-3	Routes the MDAC output to the noninverting terminal of the U4A.
W15	OPEN	OPEN	Disconnect the inverting input of operational amplifier, U4A, from AGND.
W5	2-3	1-2	Negative rail of operational amplifier is tied to AGND or powered by V_{SS}.

6.3.2 Gain of Two Output Jumper Settings

Table 3 shows the proper jumper settings of the EVM for the 2× gain output of the MDAC.

Table 3. Gain of Two Output Jumper Settings

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
J5	2-3	2-3	Routes the MDAC output to the noninverting terminal of the U4A.
W15	CLOSED	CLOSED	Inverting input of the output operational amplifier, U4A, is connected to AGND to set for a gain of 2.
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of operational amplifier, U4A, for bipolar supply mode, or ties it to AGND for unipolar supply mode.

6.4 Output Gain of Five With MDAC V_{OUT} Inverted

Table 4 shows the proper jumper settings of the EVM to achieve a gain of five with the output of the MDAC inverted.

Table 4. Jumper Settings for a Gain of Five With Inverted Output

Reference	Jumper Setting		Function
	Unipolar	Bipolar	
J5	1-2 and 3-4	1-2 and 3-4	Output of MDAC is inverted with a gain of 5. Watch for clipping in unipolar mode due to operational amplifier headroom issue.
W15	OPEN	OPEN	Disconnect the inverting input of operational amplifier, U4A, from AGND.
W5	2-3	1-2	Supplies power, V_{SS}, to the negative rail of operational amplifier, U4A, for bipolar supply mode, or ties it to AGND for unipolar supply mode.

7 Jumper Setting

Table 5 shows the function of each specific jumper setting of the EVM.

Table 5. Jumper Setting Function

Reference	Jumper Setting	Function
W1		Routes the –10-V reference to MDAC V_{REF} pin.
		Disconnect the onboard external reference and use desired source of reference via TP1.
		Routes the +10-V reference to MDAC V_{REF} pin.
W2		Chip Enable pin driven by $\overline{CS}$ pin, J2-1.
		Enable chip via W25 jumper.
		Chip Enable pin driven by FSX pin, J2-7.
W3		Disconnect the I_{OUT} from the I-to-V amplifier circuit.
		Routes the I_{OUT} to the I-to-V amplifier circuit.
W5		Negative supply rail of the output operational amplifier, U4A, is powered by V_{SS} for bipolar operation.
		Negative supply rail of the output operational amplifier, U4A, is tied to AGND for unipolar operation.

Reference	Jumper Setting	Function
W15		Disconnect the inverting input terminal of U4A from ground.
		Connect the inverting input terminal of U4A from ground.
W25		Chip Enable pin is driven via W2 jumper with either $\overline{CS}$ pin on J2-1 or FSX pin on J2-7.
		Chip Enabled and is always active.
J4		Jumper pins 1-2 or pins 3-4 together to connect the feedback resistor, R_{FB}, to the output of U5.
		Jumper pins 5-6 or pins 7-8 together to connect the MDAC V_{OUT} to J5 header via the RC filter.
J5		MDAC V_{OUT} is routed to the inverting input of U2.
		MDAC V_{OUT} is routed to the non-inverting input of U2.
		The noninverting input of U2 is tied to AGND.
		MDAC V_{OUT} is routed to the inverting input of U2 and the noninverting input of U2 is tied to AGND.
Legend:		Indicates the corresponding pins that are shorted or closed.

8 Schematic

The schematic for the DAC8801/11EVM PCB is appended to this document.

9 Using the DAC8811EVM with DXP

The DAC8811EVM is compatible with the DAC eXerciser Program (DXP) from Texas Instruments. DXP is a tool that can generate the necessary control signals required to output various signals and waveforms from the device installed on the DAC8811EVM. The DAC8811EVM-PDK kit combines the DAC8811EVM board with the DSP based modular motherboard MMB0. The kit includes the DXP software for evaluation using any available USB port on a Microsoft® Windows® XP-based computer.

DXP is a program for controlling the digital input signals such as the clock, $\overline{CS}$, and SDI. Wave tables are built into the DSP software to allow sine, ramp, triangle, and square wave signals to be generated by the DAC8811. Straight dc outputs can also be obtained.

The DAC8811EVM-PDK uses the DSP-based MMB0 to control the DAC EVM through the DXP software. For complete information about installing and configuring DXP, see the DXP User's Guide, available for download from the TI web site. This section covers the specific operation of the DAC8811EVM-PDK.

9.1 Hardware

The hardware consists of two primary components: the DAC8811EVM itself and a modular motherboard called the MMB0. The MMB0 board houses a TMS320VC5507 DSP that controls the serial interface to the device loaded on the EVM board.

The hardware must be configured such that the DAC8811EVM is plugged onto the MMB0 aligning female connectors J4, J2 and J6 (on the bottom side of the DAC8811EVM) with male connectors J7, J4 and J5 on the MMB0. The assembled hardware is shown in Figure 10.

CAUTION

Use caution when assembling the boards. It is possible to misalign the connectors and damage both the EVM and the motherboard.

CAUTION

DO NOT connect the MMB0 to your PC before installing the DXP software as described in the DXP User's Guide. Installing the software first ensures that the necessary drivers are properly loaded to run the hardware.

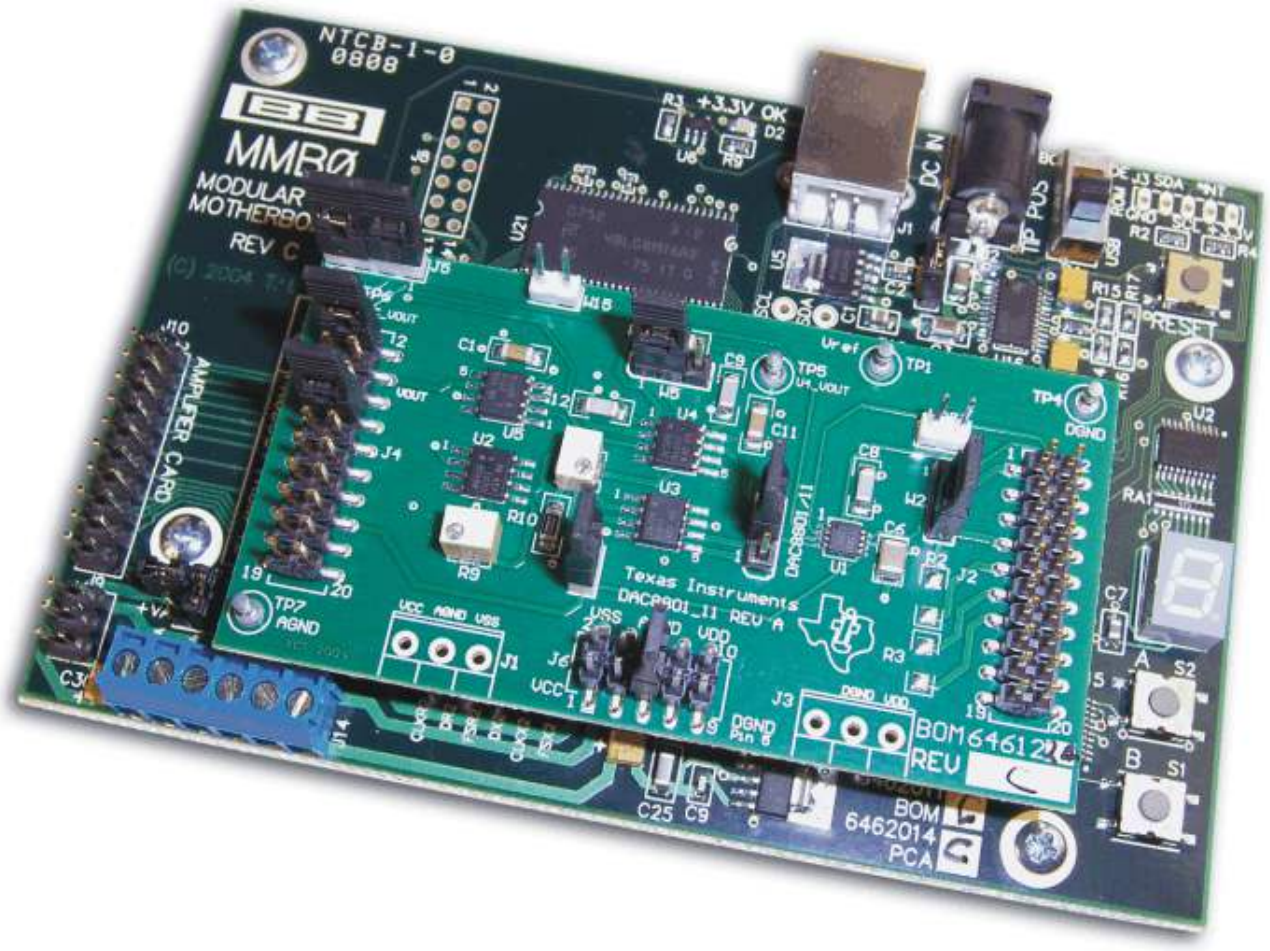

Figure 10. MMB0 with DAC8811EVM Installed

9.2 MMB0 Power Supplies

Several power connections are required for the hardware to work properly. For the MMB0, the supplied 6-V ac/dc converter is all that is necessary. Be sure that J12 on the MMB0 board is closed before connecting the ac/dc adapter to the *DC In* connector of the MMB0. This supply provides all power to the digital portion of the DAC8811EVM as well as all necessary power for the DSP. Clean, well-regulated analog power for the DAC8811EVM should be supplied externally via J14, a six-position screw terminal mounted in the lower left corner of the MMB0 board.

CAUTION

When using external power supplies applied to J14 on the MMB0, please ensure all shorting blocks from J13 are completely removed. Permanent damage to the MMB0 may occur otherwise.

From left to right, the J14 screw terminal connections are –VA, +VA, +5VA, –5VA, +5VD, and GND. The 5V from the ac/dc adapter can be connected to the +VA or the +5VA by installing a jumper across JP13A or JP13B. If the jumpers are not installed, the analog V_{SS}, V_{CC}, +5VA, and –5VA may be applied directly to the –VA, +VA, +5VA, and –5VA screw terminals at J14 on the MMB0 (referenced to the GND terminal).The DAC8811 board power requirements are described in Section 4.2 of this manual.

9.3 Software: Running DXP

Install DXP on a laptop or personal computer running Windows XP as shown in the detailed instructions in the *DXP User's Guide* (TI document SBAU146). Run the DXP program by clicking on the DXP icon on your desktop, or by browsing to your installation directory.

Before you can generate signals with DXP, a DAC EVM configuration file must be loaded. To load a configuration file, select the desired DAC from the configuration list under the *DAC* menu, as Figure 11 illustrates. Choose the DAC configuration file for the device installed on the EVM.

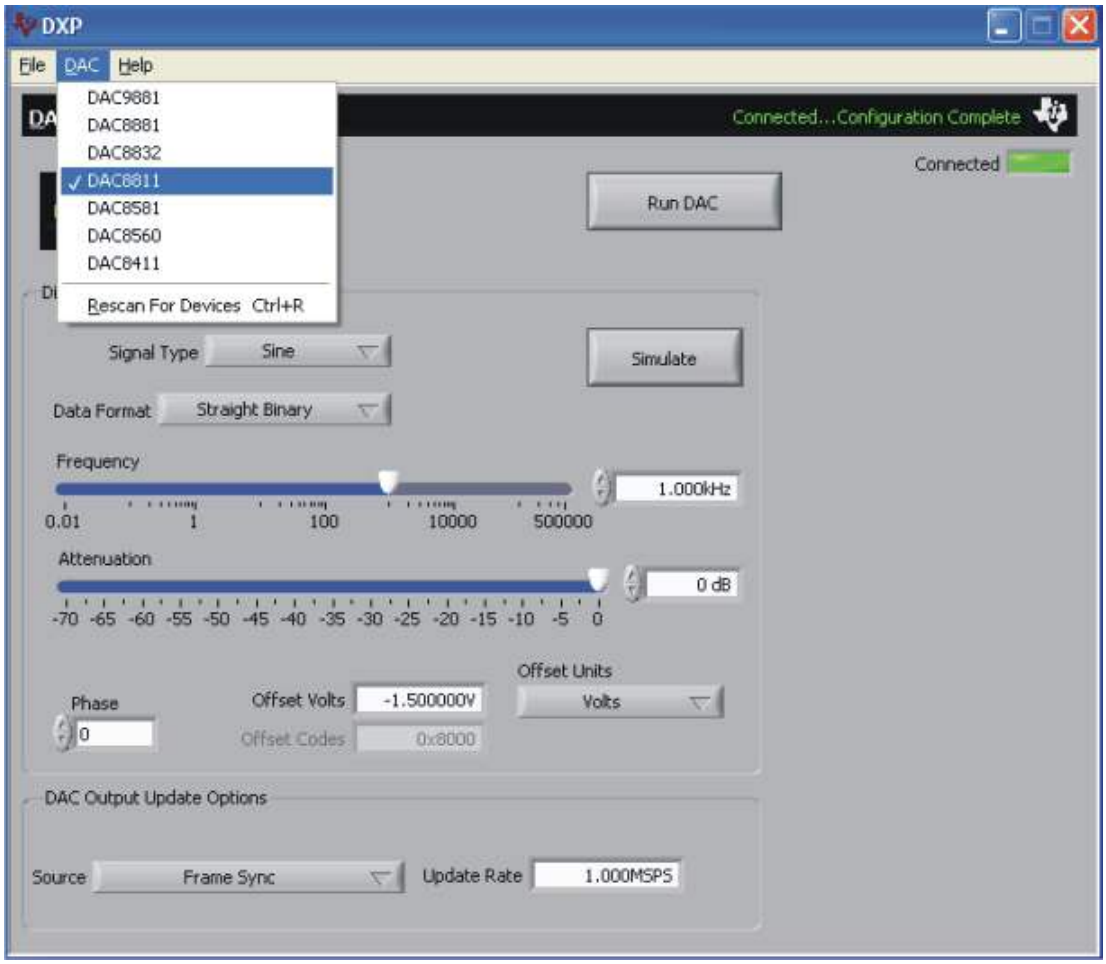

Figure 11. Loading a DAC8811EVM Configuration

The DXP software defaults to output a 1-kHz sine wave from the DAC. Other waveform options include square, sawtooth, triangle, and dc output options, as described in the DXP User's Guide. The frequency and amplitude of the output waveform are controlled by sliders on the DXP software interface. The DAC update rate can also be modified, as shown in Figure 12.

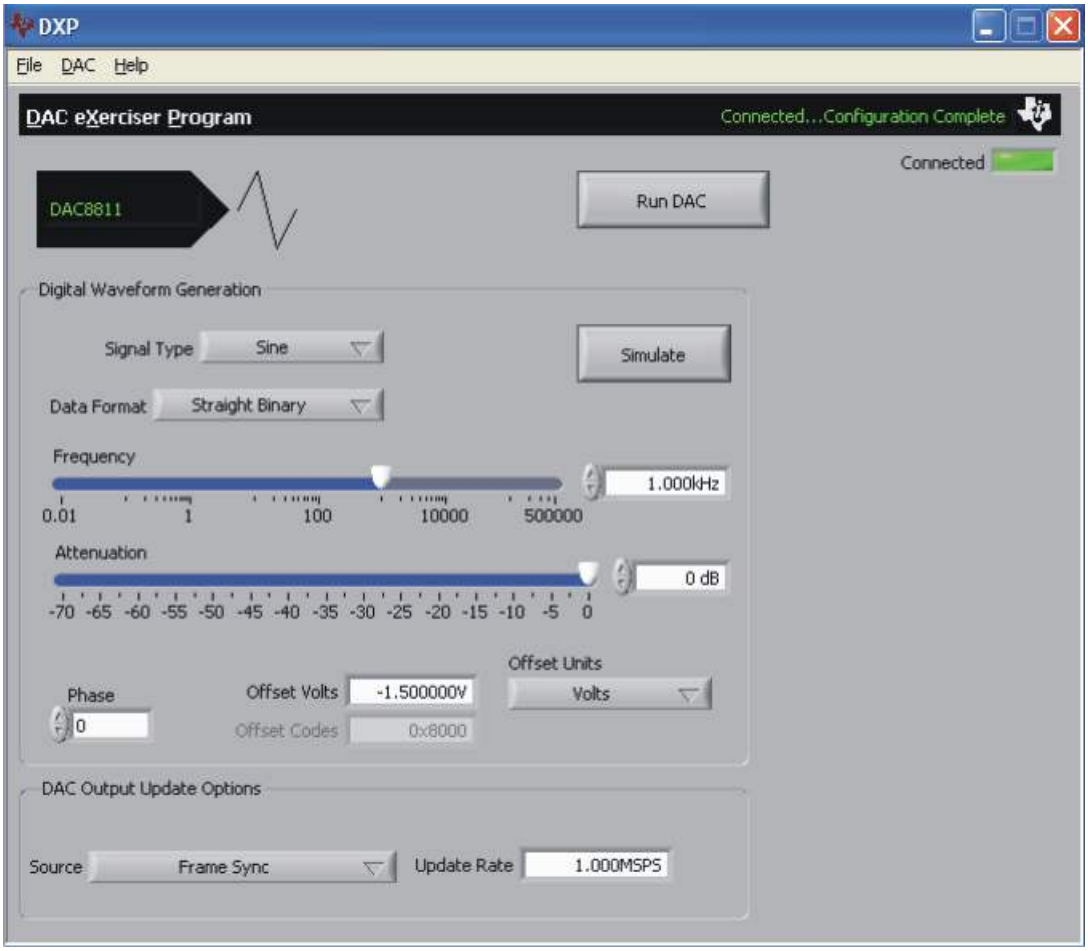

Figure 12. DAC8811EVM: Frequency/Amplitude and Update Rate Adjustments

9.4 DAC Output Update Options

The DXP software also allows the user to choose several DAC output update options, as Figure 13 shows.

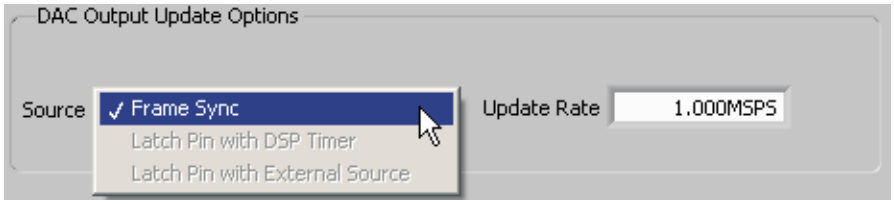

Figure 13. DAC Output Update Options

Table 6 lists the details on these options.

Table 6. Output Update Features

Options	Detailed Description
Frame Sync	The DXP software defaults to Frame Sync. The Frame Sync output of the MMB0 connects to the SYNC input of the DAC88811. The DAC output changes to the corresponding level when the DAC latch is updated via SDI. Ensure the shunt jumper on W6 is covering pins 2-3 (default is 1-2) to use this feature.
Latch with DSP Timer	N/A
Latch with External Timer	N/A
Update Rate	User input; enter the desired DAC update rate. 1MSPS is the default

10 Bill of Materials

Table 7. Parts Lists

Item #	Qty	Designator	Manufacturer	Part Number	Description
1	3	C8 C9 C10	TDK	C3216COG2A103KT	0.01µF, 1206 Multilayer ceramic capacitor
2	6	C1 C2 C5 C7 C11 C13	TDK	C3216COG1E104KT	0.1µF, 1206 Multilayer ceramic capacitor
3	1	C12	TDK	C3216COG2A102KT	1 nF, 1206 Multilayer ceramic capacitor
4	2	C4 C6	TDK	C3225X7R1E106KT	10 µF, 1210 Multilayer ceramic X5R capacitor
5	1	C3	TDK	C3216X7R1E471KT	470 pF, 50V, 1206 Multilayer ceramic capacitor SMD
6	4	R1 R2 R3 R5 (1)	Panasonic	ERJ-8GEY0R00V	0 Ω, 1/4W 1206 chip resistor
7	1	R10	Panasonic	ERJ-8ENF2002V	20 kΩ, 1/4W 1206 chip resistor
8	1	R4	Panasonic	ERJ-8GEYJ101V	100 Ω, 1/4W 1206 chip resistor
9	1	R8	Panasonic	ERJ-8GEYJ202V	2 kΩ, 5%, 1/4W 1206 chip resistor
10	2	R6 R12	Panasonic	ERJ-8ENF1002V	10 kΩ, 1/4W 1206 chip resistor
11	1	R9	Bourns	3214W-1-203E	20K Potentiometer
12	1	J5	Molex	122-03-2041	4 Position jumper_0.1" spacing
13	1	J6	Samtec	TSM-105-01-T-DV	5×2×0.1 10-pin 3A isolated power socket
14	2	J2 J4	Samtec	TSM-110-01-S-DV-M	10×2×0.1, 20 Pin 0.025"sq SMT socket
15	2	J1 J3 (1)	On-Shore Technology	ED555/3DS	3-Pin terminal connector
16	1	U1 (2)	Texas Instruments	DAC8801E/DAC8811E	14-bit/16-bit, Current output, serial input MDAC
17	1	U2	Texas Instruments	REF102AU	8-SOIC(D) precision reference, +10V
18	5	TP1 TP4 TP5 TP6 TP7	Mill-max	2348-2-01-00-00-07-0	Turret terminal test point
19	2	P2 P4 (3)	Samtec	SSW-110-22-S-D-VS-P	20-PIN 0.025"sq SMT terminal strips

(1) The following parts: J1, J3, R1, R2, and R3 are not installed.
(2) The device installed is specific to the EVM ordered.
(3) P2, P4, and P6 parts are not shown in the schematic diagram. All the P designated parts are installed in the bottom side of the PCB opposite the J designated counterpart. Example, J2 is installed on the topside while P2 is installed in the bottom side opposite of J2.

Table 7. Parts Lists (continued)

Item #	Qty	Designator	Manufacturer	Part Number	Description
20	1	P6 (3)	Samtec	SSW-105-22-F-D-VS-K	3A Isolated 10-pin power header
21	3	W3 W15 W25	Molex	22-03-2021	2 Position jumper_ 0.1" spacing
22	3	W1 W2 W5	Molex	22-03-2031	3 Position jumper_ 0.1" spacing
23	1	R7	Bourns	3214W-1-104E	100K Potentiometer
24	1	U3	Texas Instruments	INA105KU	Unity gain differential amplifier, 8 SOIC
25	1	U4	Texas Instruments	OPA2277UA	Dual high precision operational amplifier, 8SOP(D)
26	1	U5	Texas Instruments	OPA277UA	High precision operational amplifier, 8SOP(D)

Revision History		
REV	ECN Number	Approved

Note: Replace U5 amplifier with the desired amplifier that fits user's application requirements.

Use these terminals for current output

Note: R1, R2 and R3 are not populated.

Note: R8 and C3 are populated with the values as indicated. Replace R8 with 0 ohm jumper resistor and do not populate C3 if filtering is not desired.

(Max of ±15V AC or DC)

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FILE: DAC88x1_RevA.Sch	Title: DAC8801/11	
	DOCUMENTCONTROL # 6461221	REV: A
	DATE: 10-Jan-2005 SIZE:	SHEET: 1 OF: 1

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During normal operation, some circuit components may have case temperatures greater than +60°C. The EVM is designed to operate properly with certain components above +60°C as long as the input and output ranges are maintained. These components include but are not limited to linear regulators, switching transistors, pass transistors, and current sense resistors. These types of devices can be identified using the EVM schematic located in the EVM User's Guide. When placing measurement probes near these devices during operation, please be aware that these devices may be very warm to the touch.

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