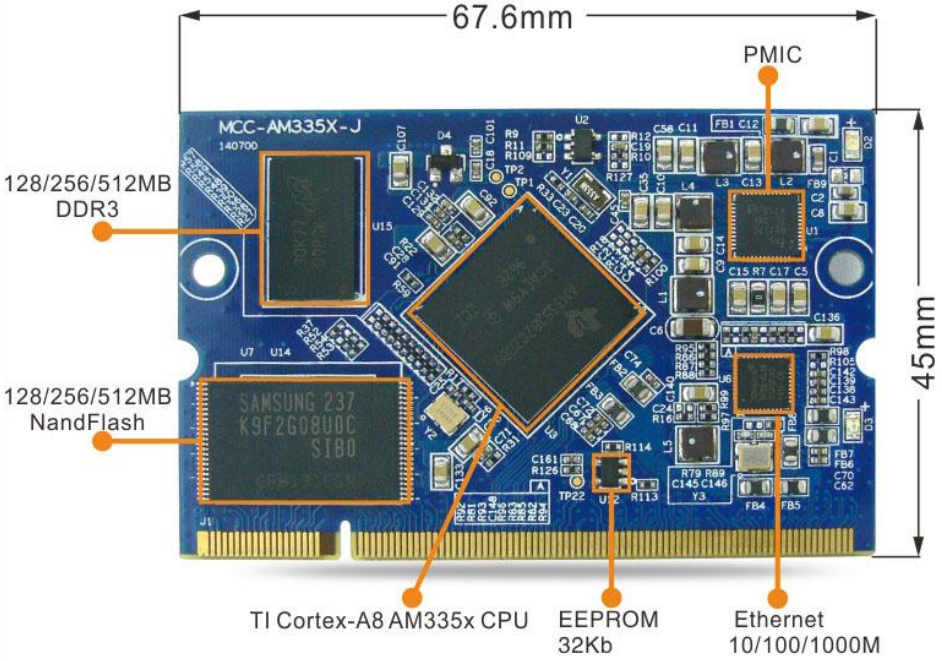
MYiR 米尔电子
Make Your Idea Real

MCC-AM335X-J CPU Module Overview

- ✓ *Up to 1GHz TI AM335x Series ARM Cortex-A8 Processors*
- ✓ *256MB DDR3 SDRAM (128MB/512MB compatible)*
- ✓ *256MB Nand Flash (128MB/512MB compatible)*
- ✓ *On-board Gigabit Ethernet PHY*
- ✓ *Power Management IC (PMIC)*
- ✓ *DDR2 SO-DIMM 200-pin Expansion Interface*
- ✓ *Ready-to-Run Linux 4.1.18 OS*
- ✓ *Supports -40 to +85 Celsius Extended Temperature Operation for Industrial Applications*

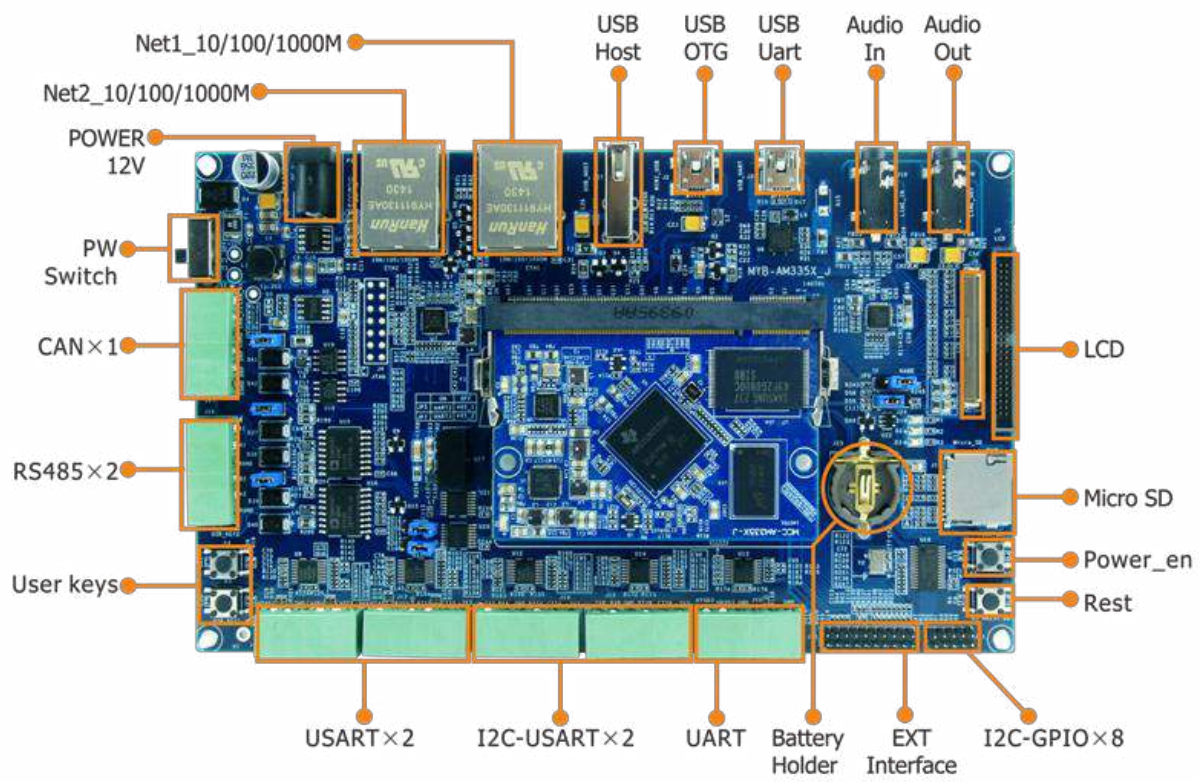
The MCC-AM335X-J CPU Module is a feature-packed System on Module (SOM) supporting the TI AM335x (AM3352, AM3354, AM3356, AM3357, AM3358 and AM3359) ARM Cortex-A8 Sitara processors which is capable of running at up to 1GHz with a rich 2D/3D graphics accelerator. It is a ready-to-run Linux controller board, supporting -40 to +85 Celsius extended temperature operation and has brought out up to two CAN bus, two Gigabit Ethernet, two USB OTG and up to six Serial ports and more other signals from one DDR2 SO-DIMM 200-pin gold finger expansion interface, thus makes it ideal for many industrial applications like game peripherals, printers, medical devices, educational terminals, intelligent charging system, intelligent vending machine, weighing system, etc.

The MCC-AM335X-J CPU Module has integrated some core components on board including the AM335x processor, 256MB DDR3 SDRAM, 256MB Nand Flash, 32Kb EEPROM, Gigabit Ethernet PHY chip as well as Power Management IC. It can also have flexible and compatible selections of AM335x CPU, 128/512MB DDR3 and 128/512MB Nand Flash to meet users' different requirements. The TI AM335x CPU consists of 6 different devices with various options including speed grades, packages, graphics and peripherals. The table below gives a brief overview of options.



MCC-AM335X-J CPU Module

MYIR also offers a low-cost, high-performance development board MYD-AM335X-J to provide an excellent evaluation platform to enable your quickly evaluation of the AM335x microprocessors and the MCC-AM335X-J CPU modules on this platform.



MYD-AM335X-J Development Board

MYD-AM335X-J Board with MY-LCD70TP-C 7-inch LCD Module

Hardware Specification

The **TI AM335x** microprocessors, based on the ARM Cortex-A8, operating at up to 1GHz, are enhanced with image, graphics processing, peripherals and industrial interface options such as EtherCAT and PROFIBUS. The device supports the following high-level operating systems (HLOSs) that are available free of charge from TI:

• Linux®

• Android™

The AM335x microprocessor contains these subsystems:

• Microprocessor unit (MPU) subsystem based on the ARM Cortex-A8 microprocessor.

• POWERVR SGX™ Graphics Accelerator subsystem for 3D graphics acceleration to support display and gaming effects.

• The Programmable Real-Time Unit and Industrial Communication Subsystem (PRU-ICSS) is separate from the ARM core, allowing independent operation and clocking for greater efficiency and flexibility.

The PRU-ICSS enables additional peripheral interfaces and real-time protocols such as EtherCAT, PROFINET, EtherNet/IP, PROFIBUS, Ethernet Powerlink, Sercos, and others.

AM335x ARM Cortex™-A8 Processors						
Core Feature	**AM3352**	**AM3354**	**AM3356**	**AM3357**	**AM3358**	**AM3359**
Package	15x15mm, 0.8mm (ZCZ)					
CPU Speed (MHz)	300, 600, 800, 1000	600, 800,1000	300, 600,800	300, 600,800	600, 800,1000	800
Core Internal Memory	64KB SRAM shared w/ Data 32KB Cache, Programmable 32KB Cache					
On-chip L2 (KB)	256					
External Memory Interface	DDR2/DDR3/DDR3L/mDDR (LPDDR), 2x16-bit, NAND ECC					
Graphics	-	3D Graphics	-		3D Graphics	
OS Support	Linux, Android, RTOS, Windows Embedded, no-OS					
Other Hardware Acceleration	Crypto Accelerator	Crypto Accelerator	2 PRU-ICSS Crypto Accelerator	2 PRU-ICSS Crypto Accelerator + EtherCAT slave support	2 PRU-ICSS Crypto Accelerator	2 PRU-ICSS Crypto Accelerator + EtherCAT slave support
10/100/1000 EMAC	2 port switch					
USB 2.0 OTG + PHY	2					
Serial Ports	6 UART, 2 SPI, 3 I2C, 2 McASP, 2 CAN, 8 Timers					
System	EDMA, WDT, RTC, 3 eQEP, 3 eCAP, JTAG, ADC (8ch)					
Parallel	3 MMC/SD/SDIO, GPIO					

AM335x Devices Key Features

Mechanical Parameters

- Dimensions: 67.6mm x 45mm
- PCB Layers: 8-layer design
- Power supply: 5V, 1.8V
- Working temperature: 0~70 Celsius (commercial grade) or -40~85 Celsius (industrial grade)

Processor

- TI AM3352, AM3354, AM3356, AM3357, AM3358, AM3359
  - Up to 1GHz ARM Cortex-A8 32-bit RISC MPU
  - NEON™ SIMD Coprocessor
  - 32KB/32KB of L1 Instruction/Data Cache with Single-Error Detection (parity)
  - 256KB of L2 Cache with Error Correcting Code (ECC)
  - SGX530 Graphics Engine
  - Programmable Real-Time Unit Subsystem

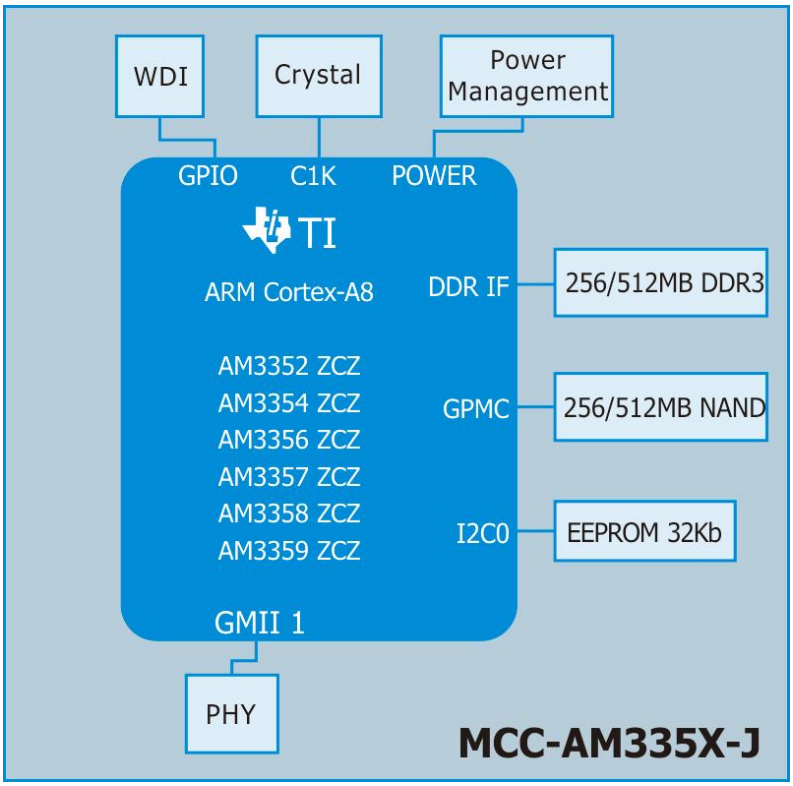
Memory

- 256MB DDR3 SDRAM (128MB/256MB compatible)
- 256MB Nand Flash (128MB/256MB compatible)
- 32Kb EEPROM

Peripherals and Signals Routed to Pins

- On-board Gigabit Ethernet PHY
- Power Management Unit (TPS65217C)
- One power indicator (Red LED)
- One user LED (Green)
- DDR2 SO-DIMM 200-pin gold finger connector (the extended signals please refer to the pinouts diagram):
  - 2 x Gigabit Ethernet
  - 2 x USB OTG
  - Up to 6 x Serial ports
  - Up to 2 x I2C
  - Up to 2 x SPI
  - Up to 2 x CAN
  - 8 x ADC
  - 2 x PWM
  - 3 x SDIO (One SDIO has multiplexed with Nand Flash signals)

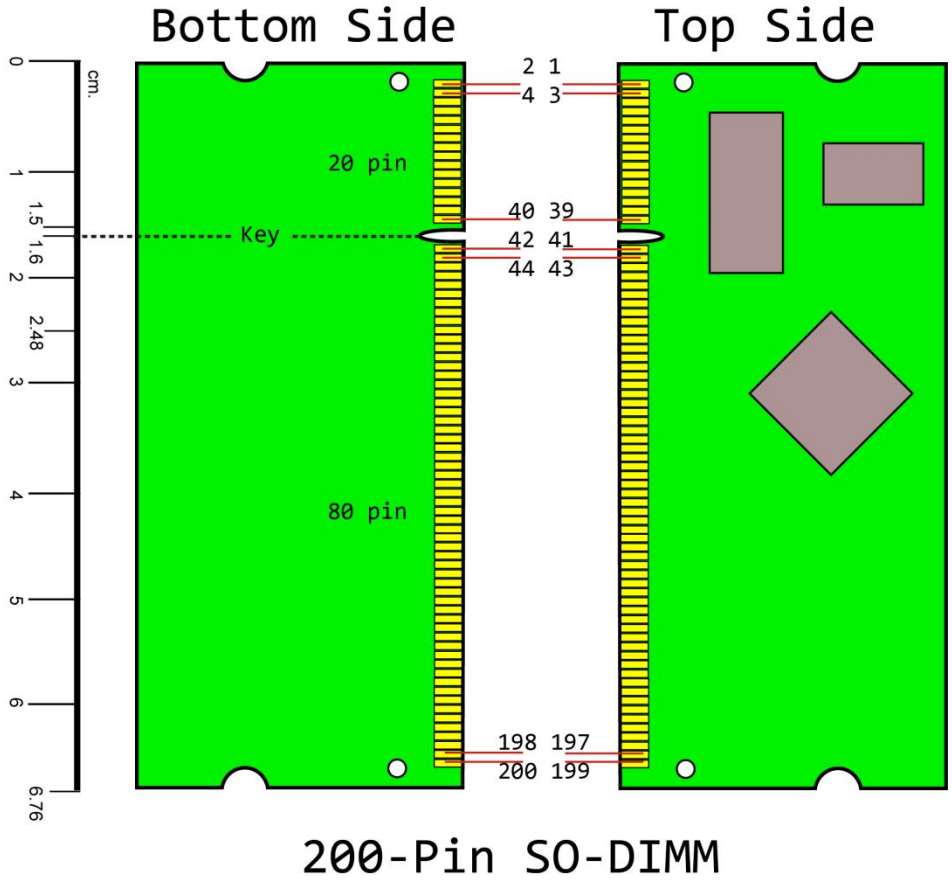
Function Block Diagram of MCC-AM335X-J CPU Module



Function Block Diagram of MCC-AM335X-J

Signals Routed to Expansion Connectors

The MCC-AM335X-J CPU Module is using the DDR2 SO-DIMM 200-pin connector as the expansion interface to connect to your next embedded design. Please refer to below table to know signals routed to the pins:



Pin Map of MCC-AM335X-J

Num	Name	BGA	Type	Description
1	+5V		PWR	5V Power suppoly
2	+5V		PWR	5V Power suppoly
3	+5V		PWR	5V Power suppoly
4	+5V		PWR	5V Power suppoly
5	GND		GND	Power Gruond
6	GND		GND	Power Gruond
7	GND		GND	Power Gruond
8	GND		GND	Power Gruond
9	NC			
10	VRTC		PWR	RTC Battery, 1.8V
11	NC			
12	VDD_3V3B		PWR	3.3V Power output, Use for outside IO level
13	NC			
14	NC			
15	LCD_DATA0	R1	I/O	LCD Data line 0

Num	Name	BGA	Type	Description
16	LCD_DATA1	R2	I/O	LCD Data line 1
17	LCD_DATA2	R3	I/O	LCD Data line 2
18	LCD_DATA3	R4	I/O	LCD Data line 3 / boot config
19	LCD_DATA4	T1	I/O	LCD Data line 4
20	LCD_DATA5	T2	I/O	LCD Data line 5
21	LCD_DATA6	T3	I/O	LCD Data line 6
22	LCD_DATA7	T4	I/O	LCD Data line 7
23	NC			
24	NC			
25	LCD_DATA8	U1	I/O	LCD Data line 8
26	LCD_DATA9	U2	I/O	LCD Data line 9
27	LCD_DATA10	U3	I/O	LCD Data line 10
28	LCD_DATA11	U4	I/O	LCD Data line 11
29	LCD_DATA12	V2	I/O	LCD Data line 12
30	LCD_DATA13	V3	I/O	LCD Data line 13
31	LCD_DATA14	V4	I/O	LCD Data line 14
32	LCD_DATA15	T5	I/O	LCD Data line 15
33	NC			
34	NC			
35	LCDPCLK	V5	O	LCD peix clock
36	LCDVSYNC	U5	O	LCD vertical Synchronization signal
37	LCDDE	R6	O	LCD Data Enable
38	LCDVHYNC	R5	O	LCD horizontal Synchronization signal
39	NC			
40	NC			
41	NC			
42	NC			
43	MMC2_CLK	V12	O	MMC2 Clock
44	MMC2_CMD	T13	O	MMC2 Command line
45	MMC2_DAT0	T12	I/O	MMC2 Data0
46	MMC2_DAT1	R12	I/O	MMC2 Data1
47	MMC2_DAT2	V13	I/O	MMC2 Data2
48	MMC2_DAT3	U13	I/O	MMC2 Data3
49	USER_BUTTON1	U10	O	User KEY 1
50	USER_BUTTON2	T10	O	User KEY 2
51	GPIO0_26	T11	O	GPIO0_26, Use for RST of SPI to IO
52	GPIO0_27	U12	O	GPIO0_27, Use for IRQ of SPI to IO
53	NC			
54	NC			
55	MMC1_DAT0	U7	I/O	EMMC/NAND Data0 (Used by nand on CoreBoard)
56	MMC1_DAT1	V7	I/O	EMMC/NAND Data1 (Used by nand on CoreBoard)
57	MMC1_DAT2	R8	I/O	EMMC/NAND Data2 (Used by nand on CoreBoard)
58	MMC1_DAT3	T8	I/O	EMMC/NAND Data3 (Used by nand on CoreBoard)
59	MMC1_DAT4	U8	I/O	EMMC/NAND Data4 (Used by nand on CoreBoard)
60	MMC1_DAT5	V8	I/O	EMMC/NAND Data5 (Used by nand on CoreBoard)

Num	Name	BGA	Type	Description
61	MMC1_DAT6	R9	I/O	EMMC/NAND Data6 (Used by nand on CoreBoard)
62	MMC1_DAT7	T9	I/O	EMMC/NAND Data7 (Used by nand on CoreBoard)
63	NC			
64	NC			
65	GMII2_TXEN	R13	O	GMII2 Transmit Enable
66	GMII2_RXDV	V14	O	GMII2 Receive Data Valid
67	GMII2_TXD3	U14	O	GMII2 Transmit Data bit 3
68	GMII2_TXD2	T14	O	GMII2 Transmit Data bit 2
69	GMII2_TXD1	R14	O	GMII2 Transmit Data bit 1
70	GMII2_TXD0	V15	O	GMII2 Transmit Data bit 0
71	NC			
72	NC			
73	GMII2_TXCLK	U15	I	GMII2 Transmit Clock
74	GMII2_RXCLK	T15	I	GMII2 Receive Clock
75	GMII2_RXD3	V16	I	GMII2 Receive Data bit 3
76	GMII2_RXD2	U16	I	GMII2 Receive Data bit 2
77	GMII2_RXD1	T16	I	GMII2 Receive Data bit 1
78	GMII2_RXD0	V17	I	GMII2 Receive Data bit 0
79	MDIO_CLK	M18	O	MDIO Clk
80	MDIO_DATA	M17	I/O	MDIO Data
81	NC			
82	NC			
83	USB1_DP	R17	DIFF	USB1 Data plus
84	USB0_DRVVBUS	F16	O	USB0 Active high VBUS control output
85	USB1_DM	R18	DIFF	USB1 Data minus
86	USB0_VBUS	P15	A	USB0 VBUS detection input
87	NC			
88	USB0_ID	P16	A	USB0 OTG ID (Micro-A or Micro-B Plug)
89	USB0_DP	N17	DIFF	USB0 Data plus
90	USB0_CE	M15	A	no connect
91	USB0_DM	N18	DIFF	USB0 Data minus
92	USB1_DRV	F15	O	USB1 Active high VBUS control output
93	NC			
94	USB1_VBUS	T18	A	USB1 VBUS detection input
95	GPMC_WAIT0			
96	USB1_ID	P17	A	USB0 ID
97	GPMC_OEn_REn	T7	O	Output Enable (active low). Also used as Read Enable (active low) for NAND protocol memories
98	GPMC_BE0n_CLE	T6	O	Lower Byte Enable (active low). Also used as Command Latch Enable for NAND protocol memories
99	GPMC_ADVn_ALE	R7	O	Address Valid or Address Latch Enable depending if NOR or NAND protocol memories are selected.
100	GPMC_WEn	U6	O	Write Enable (active low)

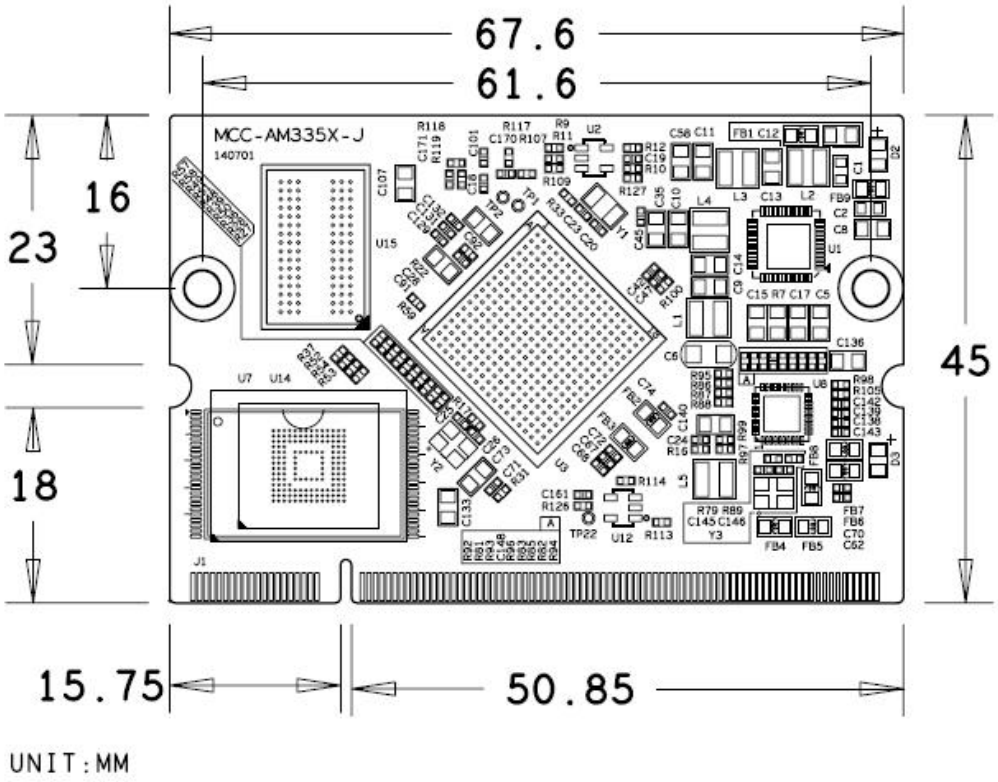
Num	Name	BGA	Type	Description
101	NC			
102	NC			
103	MMC0_CLK	G17	O	MMC0 clock
104	MMC0_DAT0	G16	I/O	MMC0 data 0
105	MMC0_CMD	G18	O	MMC0 command
106	MMC0_DAT1	G15	I/O	MMC0 data 1
107	MCASP0_AHCLKX	A14	O	McASP/I2S MCLK
108	MMC0_DAT2	F18	I/O	MMC0 data 2
109	NC			
110	MMC0_DAT3	F17	I/O	MMC0 data 3
111	NC			
112	NC			
113	NC			
114	UART1_CTS	D18	O	UART5 Clear To Send
115	NC			
116	UART1_RTS	D17	O	UART5 Require To Send
117	UART0_TX	E16	O	Dbg Uart TX
118	UART1_TX	D15	O	Uart 1 TX
119	UART0_RX	E15	I	Dbg Uart RX
120	UART1_RX	D16	I	Uart 1 RX
121	NC			
122	NC			
123	UART2_TX / UART5_RTS	J15	O	Uart 2 Transmit, use for RS485/ UART5 Require To Send
124	UART3_TX	C18	O	Uart 3 Transmit
125	UART2_RX / UART5_CTS	H17	I	Uart 2 Receive, use for RS485/UART5 Clear To Send
126	UART3_RX	C15	I	Uart 3 Receive
127	NC			
128	NC			
129	UART4_TX	E17	O	Uart 4 TX/ DCAN1 Receive
130	UART5_TX	H18	I	Uart 5 Transmit
131	UART4_RX	E18	I	Uart 4 RX/ DCAN1 Transmit
132	UART5_RX	H16	I	Uart 5 Receive
133	NC			
134	NC			
135	I2C0_SCL	C16	O	I2C0 clock (open drain with pull-up resistor on the SOM)
136	NC			
137	I2C0_SDA	C17	I/O	I2C0 data (open drain with pull-up resistor on the SOM)
138	LEDA		I	WLED driver，no connect
139	SPI0_CS0	A16	O	SPI0 Chip Select
140	SPI0_SCLK	A17	O	SPI0 Clock
141	SPI0_D1	B16	I/O	SPI0 Data 1
142	SPI0_D0	B17	O	SPI0 Data 0
143	NC			
144	NC			

Num	Name	BGA	Type	Description
145	MCASP0_ACLKX	A13	O	McASP0/ I2S Transmit Bit Clock
146	MCASP0_AHCLKR	C12	I/O	McASP0 Receive Master Clock
147	MCASP0_FSX	B13	O	McASP0 Transmit Frame Sync
148	GPIO3_16	D12	O	gpio3_16 use for Touchscreen reset
149	NC			
150	NC			
151	NC			
152	USER_LED1	B12	O	SOM LED, gpio3_18
153	NC			
154	MMC0_CD	C13	I	gpio MMC0 detection, gpio3_19
155	PWR_BUT		I	PMIC bottom input
156	MCASP0_AXR1	D13	I/O	McASP0 Serial Data (IN/OUT)
157	SYS_RESETN			Active low Power on Reset
158	EVENT_INTR0	A15	O	LCD Enable
159	EXTINTn	B18	I	External Interrupt to ARM Cortext A8 core
160	EVENT_INTR1	D14	I	NET1 INIT
161	NC			
162	NC			
163	VDD_ADC		PWR	Supply voltage range for ADC (Connected to 1.8V on CoreBoard)
164	GNDA_ADC		GND	Analog Ground
165	AIN0	B6	A	Analog Input/Output 0, used with touchscreen
166	AIN1	C7	A	Analog Input/Output 1, used with touchscreen
167	AIN2	B7	A	Analog Input/Output 2, used with touchscreen
168	AIN3	A7	A	Analog Input/Output 3, used with touchscreen
169	AIN4	C8	A	Analog Input/Output 4, used with touchscreen
170	AIN5	B8	A	Analog Input/Output 5
171	AIN6	A8	A	Analog Input/Output 6
172	AIN7	C9	A	Analog Input/Output 7
173	GNDA_ADC		GND	Analog Ground
174	GNDA_ADC		GND	Analog Ground
175	NC			
176	NC			
177	RGMII1_TRP0		DIFF	Ethernet Data 0 Positive
178	JTAG_TRSTn	B10	O	JTAG TEST RESET (ACTIVE LOW)
179	RGMII1_TRN0		DIFF	Ethernet Data 0 Negative
180	JTAG_TDI	B11	I	JTAG TEST DATA INPUT
181	RGMII1_TRP1		DIFF	Ethernet Data 1 Positive
182	JTAG_TCK	A12	I	JTAG TEST CLOCK
183	RGMII1_TRN1		DIFF	Ethernet Data 1 Negative
184	JTAG_TMS	C11	O	JTAG TEST MODE SELECT
185	NC			
186	JTAG_TDO	A11	O	JTAG TEST DATA OUTPUT
187	RGMII1_TRP2		DIFF	Ethernet Data 2 Positive
188	JTAG_EMU0	C14	I/O	JTAG Emulation Pin 0 (Used as WP singnal of eeprom on Core Board)

Num	Name	BGA	Type	Description
189	RGMII1_TRN2		DIFF	Ethernet Data 2 Negative
190	JTAG_EMU1	B14	I/O	JTAG Emulation Pin 1 (Used as WDT signal on Core Board)
191	RGMII1_TRP3		DIFF	Ethernet Data 3 Positive
192	LEDK1		I	WLED driver，no connect
193	RGMII1_TRN3		DIFF	Ethernet Data 3 Negative
194	LEDK2		I	WLED driver，no connect
195	NC			
196	NC			
197	RGMII1_ACT		O	PHY Status LED
198	RGMII1_LED_1000n		O	PHY 1000M Link LED
199	RGMII1_LED_100n		O	PHY 100M Link LED
200	NC			

Pin Outs of MCC-AM335X-J

Dimension Chart of MCC-AM335X-J CPU Module



Dimensions of MCC-AM335X-J

Software Features

MYIR's MCC-AM335X-J CPU module is preloaded with Linux 4.1.18 operating system. Many peripheral drivers are in source code to help accelerate customers' designs with a stable and reliable hardware and software platform. The software features are summarized as below:

Item	Features	Description
Bootstrap	SPL	The primary bootstrap (in source code)
	u-boot	The secondary bootstrap (in source code)
Linux kernel	Linux 4.1.18	Linux kernel customized for MYD-AM335X-J (in source code)
	USB Host USB Device USB OTG	USB Host/Device/OTG driver (in source code)
	Ethernet	Gigabit Ethernet driver (in source code)
	MMC/SD/TF	MMC/SD/TF card driver (in source code)
	NandFlash	NandFlash driver (in source code)
	CAN	CAN driver (in source code)
	RS485	RS485 driver (in source code)
	Audio	Audio driver (in source code)
	LCD Controller	LCD driver, support 4.3- and 7-inch TFT LCD (in source code)
	RTC	RTC driver (in source code)
	Touch driver	Resistive Touch driver (in source code)
	Button	Button driver (in source code)
	UART	UART driver (in source code)
	LED	LED driver (in source code)
	GPIO	GPIO driver (in source code)
	Watchdog	Watchdog driver (in source code)
	EXT UART	Extended UART driver (in source code)
	EXT GPIO	Extended GPIO driver (in source code)
File System	Buildroot	Provide tar package and ubi image file

Software Features of MCC-AM335X-J

Order Information

Product Item	Part No.
MCC-AM335X-J CPU Module	MYC-J3352-V2-256N256D-80-I
	MYC-J3358-V2-256N256D-100-I
MYD-AM335X-J Development Board	MYD-J3352-V2-256N256D-80-I
	MYD-J3358-V2-256N256D-100-I
MY-LCD43TP 4.3-inch LCD Module with resistive touch screen	MY-TFT043RV2
MY-LCD70TP 7-inch LCD Module with resistive touch screen	MY-TFT070RV2
MY-LCD70TP-C 7-inch LCD Module with capacitive touch screen	MY-TFT070CV2

Note:
1. Please specify the CPU model you prefer with the MCC-AM335X-J module, we deliver 800MHz AM3352 or 1GHz AM3358 by default, and can also supply other models for bulk orders.
2. For Price information, please contact MYIR.
3. We accept custom design based on the MCC-AM335X-J, whether reducing, adding or modifying the existing hardware according to customer's requirement.

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