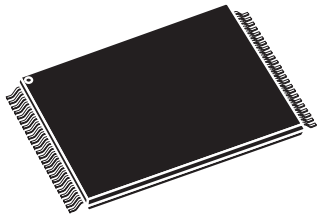
NAND08GW3F2A
NAND16GW3F2A

8-Gbit, 16-Gbit, 4224-byte page, 3 V supply, multiplane architecture, SLC NAND flash memories

Preliminary Data

Features

- High density SLC NAND flash memory
  - 8, 16 Gbits of memory array
  - Cost-effective solutions for mass storage applications
- NAND interface
  - x8 bus width
  - Multiplexed address/data
- Supply voltage: V_{DD} = 2.7 to 3.6 V
- Page size: (4096 + 128 spare) bytes
- Block size: (256K + 8K spare) bytes
- Multiplane architecture
  - Array split into two independent planes
  - All operations can be performed on both planes simultaneously
- Page read/program
  - Random access: 25 µs (max)
  - Sequential access: 25 ns (min)
  - Page program operation time: 500 µs (typ)
- Multiplane program time (2 pages): 500 µs (typ)
- Copy-back program
  - Automatic block download without latency time
- Fast block erase
  - Block erase time: 1.5 ms (typ)
  - Multiplane block erase time (2 blocks): 1.5 ms (typ)
- Status register
- Electronic signature
- Chip enable ‘don’t care’



TSOP48 12 x 20 mm (N)

- Data protection
  - Hardware program/erase locked during power transitions
- Security features
  - OTP area
  - Serial number (unique ID)
- Development tools
  - Error correction code models
  - Bad block management and wear leveling algorithm
  - HW simulation models
- Data integrity
  - 100,000 program/erase cycles (with ECC)
  - 10 years data retention
- RoHS compliant packages

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1 Description

The NANDxxGW3F2A device belongs to the 4224-byte page family of non-volatile NAND flash memories. The NANDxxGW3F2A has a density of 8 or 16 Gbits (2 x 8 Gbits). The device operates from a 3 V power supply.

The address lines are multiplexed with the data input/output signals on a multiplexed x8 input/output bus. This interface reduces the pin count and makes it possible to migrate to other densities without changing the footprint.

Each block can be programmed and erased up to 100,000 cycles (with error correction code (ECC) on). A write protect pin is available to provide hardware protection against program and erase operations.

The devices feature an open-drain, ready/busy output that identifies if the program/erase/read (P/E/R) controller is currently active. The use of an open-drain output allows the ready/busy pins of several memories to be connected to a single pull-up resistor.

For each die, the memory array is split into 2 planes of 2048 blocks each. This multiplane architecture makes it possible to program 2 pages at a time (one in each plane), to erase 2 blocks at a time (one in each plane), or to read 2 pages at a time (one in each plane) dividing by two the average program, erase, and read times.

The device has the Chip Enable ’don’t care’ feature, which allows the bus to be shared between more than one memory at the same time, as Chip Enable transition during the latency time do not stop the read operation. Program and erase operations can never be interrupted by Chip Enable transition.

The device comes with two security features:

- OTP (one time programmable) area, which is a restricted access area where sensitive data/code can be stored permanently. The access sequence and further details about this feature are subject to an NDA (non disclosure agreement)
- Serial number (unique identifier), which allows the NANDxxGW3F2A to be uniquely identified. It is subject to an NDA (non-disclosure agreement) and is, therefore, not described in the datasheet.

For more details about these security features, contact your nearest Numonyx sales office.

The device is available in TSOP48 (12 × 20 mm) package. and is shipped from the factory with block 0 always valid and the memory content bits, in valid blocks, erased to ‘1’.

Refer to the list of available part numbers and to *Table 23: Ordering information scheme* for information on how to order these options.

Table 1. Device summary

Part number	Density	Bus width	Page size	Block size	Memory array	Operating voltage (V_{DD})	Timings				Package
							Random access time (max)	Sequential access time (min)	Page program (typ)	Block erase (typ)	
NAND08GW3F2A	8 Gbits	x8	4096+128 bytes	256K + 8K bytes	64 pages x 4096 blocks	2.7 to 3.6 V	25 µs	25 ns	500 µs	1.5 ms	TSOP48
NAND16GW3F2A	16 Gbits				64 pages x 8192 blocks						

Figure 1. Logic block diagram

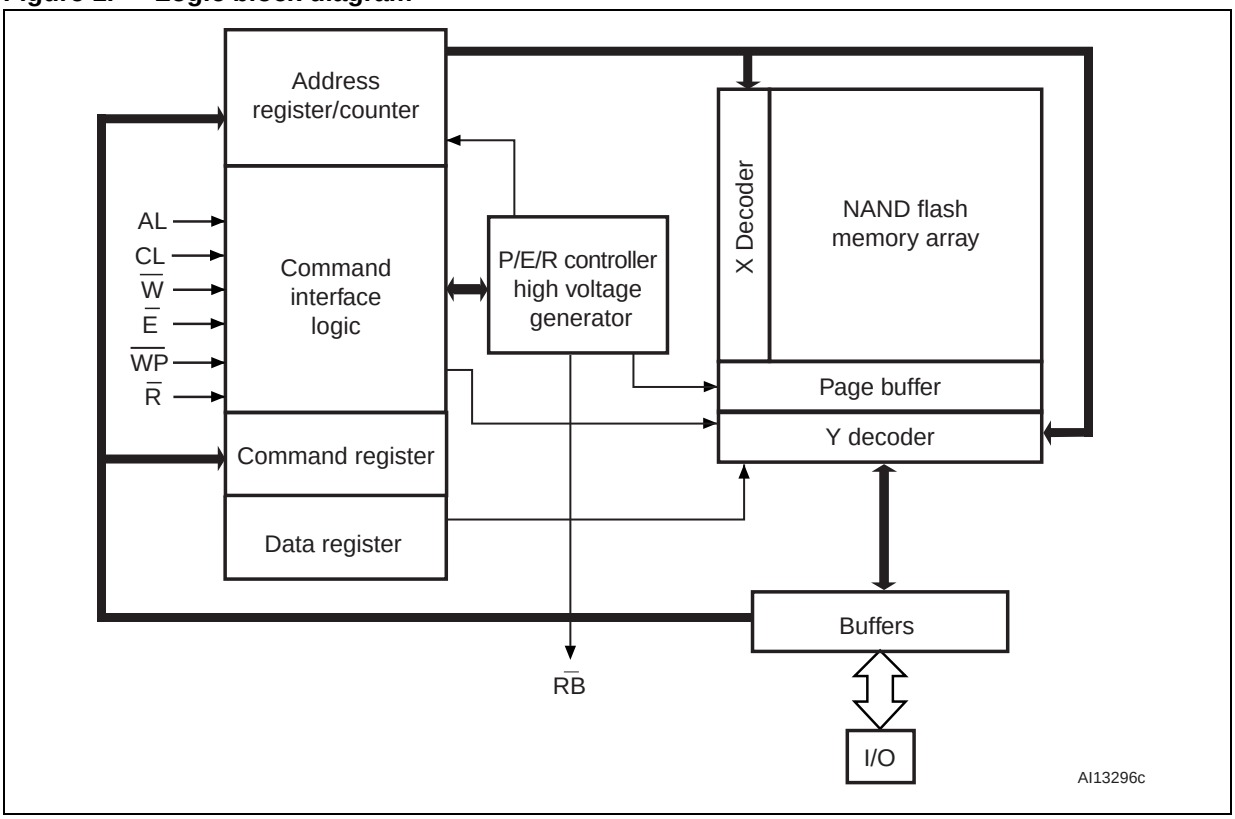


Figure 2. Logic diagram

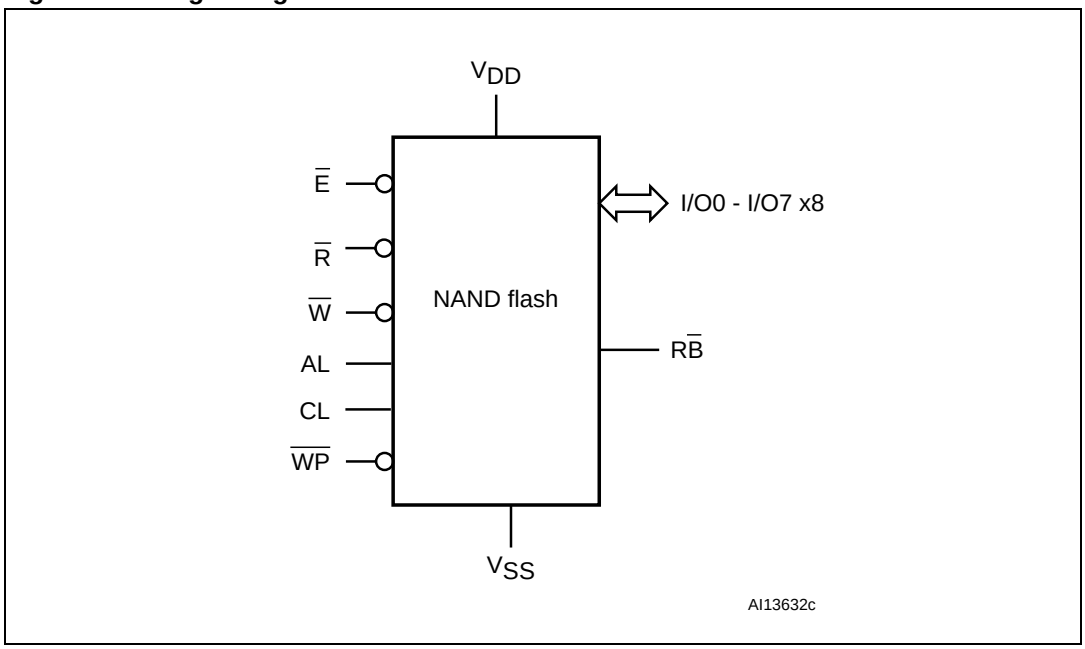
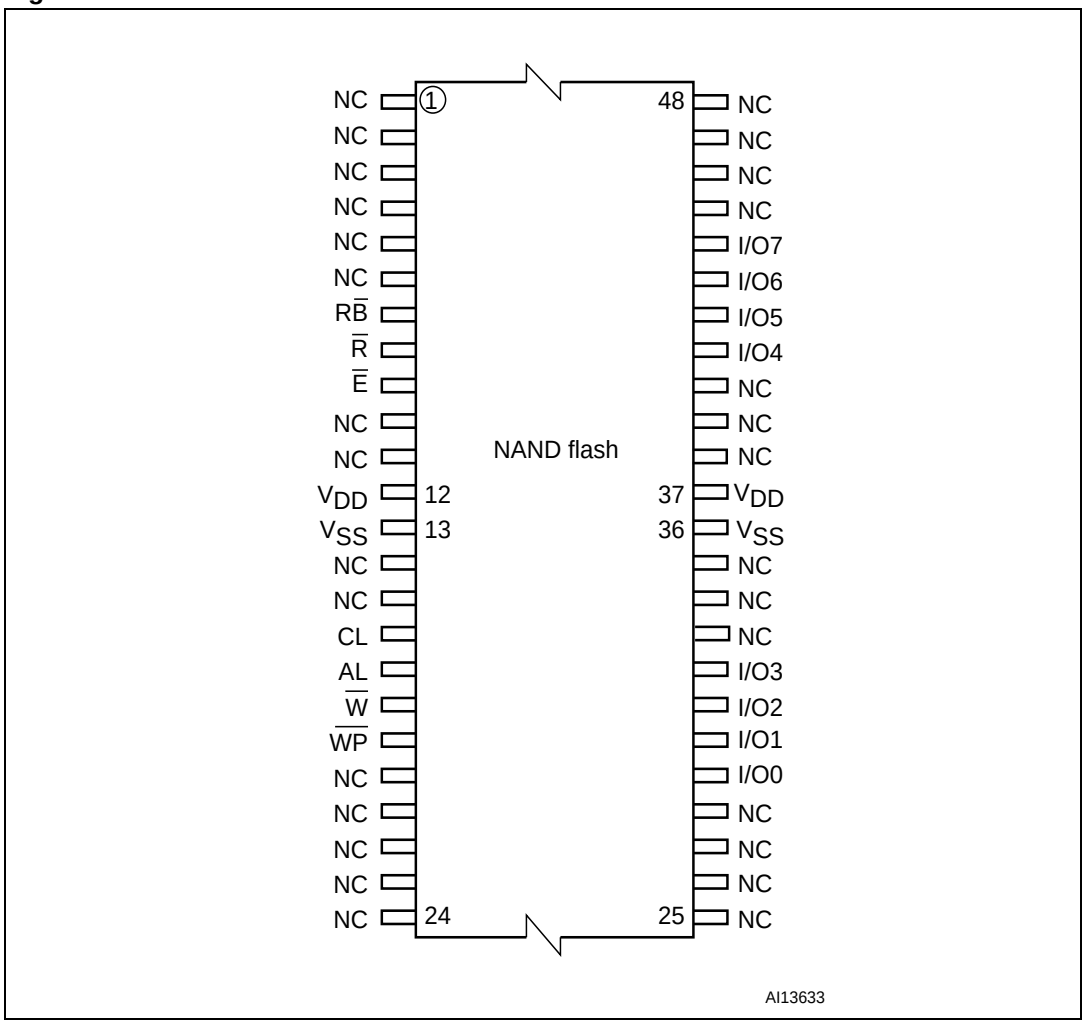


Table 2. Signal names

Signal	Function	Direction
I/O0 - I/O7	Data input/outputs	Input/output
CL	Command Latch Enable	Input
AL	Address Latch Enable	Input
$\overline{E}$	Chip Enable	Input
$\overline{R}$	Read Enable	Input
$\overline{W}$	Write Enable	Input
$\overline{WP}$	Write Protect	Input
$R\overline{B}$	Ready/Busy (open drain output)	Output
V_{DD}	Power supply	Power supply
V_{SS}	Ground	Ground
NC	No connection	–
DU	Do not use	–

Figure 3. TSOP48 connections



2 Memory array organization

The memory array is comprised of NAND structures where 32 cells are connected in series.

It is organized into blocks where each block contains 64 pages. The array is split into two areas, the main area and the spare area. The main area of the array stores data, whereas the spare area typically stores software flags or bad block identification.

The pages are split into a 4096-byte main area and a spare area of 128 bytes. Refer to *Figure 4: Memory array organization*.

2.1 Bad blocks

The NANDxxGW3F2A devices may contain bad blocks, where the reliability of blocks that contain one or more invalid bits is not guaranteed. Additional bad blocks may develop during the lifetime of the device.

The bad block information is written prior to shipping (refer to *Section 9.1: Bad block management* for more details).

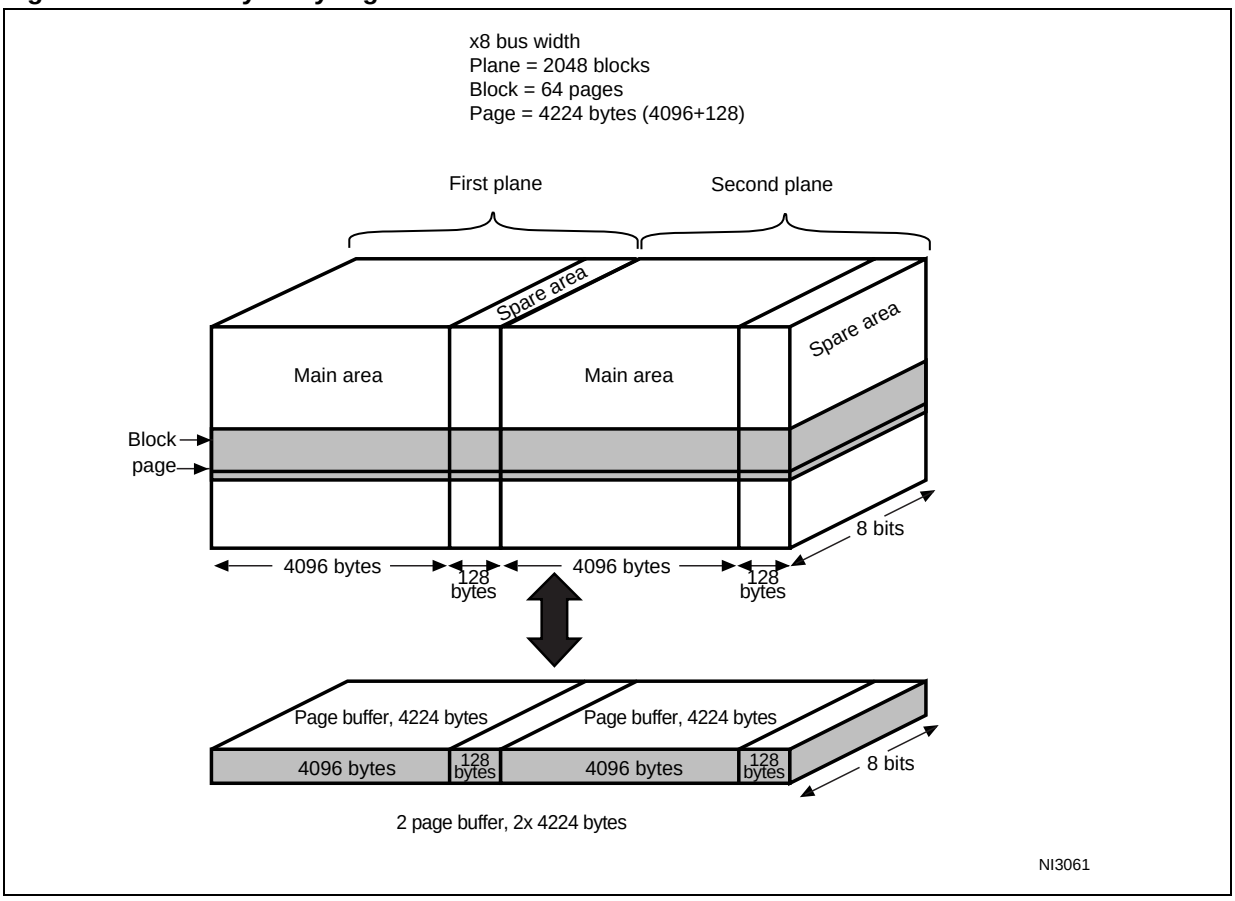
Table 3: Valid blocks shows the minimum number of valid blocks. The values shown include both the bad blocks that are present when the device is shipped and the bad blocks that could develop later on.

These blocks need to be managed using bad blocks management and block replacement (refer to *Section 9: Software algorithms*).

Table 3. Valid blocks

Density of device	Minimum	Maximum
8 Gbits	4016	4096
16 Gbits	8032	8192

Figure 4. Memory array organization



3 Signal descriptions

See *Figure 1: Logic block diagram*, and *Table 2: Signal names* for a brief overview of the signals connected to this device.

3.1 Inputs/outputs (I/O0-I/O7)

Input/outputs 0 to 7 are used to input the selected address, output the data during a read operation, or input a command or data during a write operation. The inputs are latched on the rising edge of Write Enable. I/O0-I/O7 are left floating when the device is deselected or the outputs are disabled.

3.2 Address Latch Enable (AL)

The Address Latch Enable activates the latching of the address inputs in the command interface. When AL is High, the inputs are latched on the rising edge of Write Enable.

3.3 Command Latch Enable (CL)

The Command Latch Enable activates the latching of the command inputs in the command interface. When CL is High, the inputs are latched on the rising edge of Write Enable.

3.4 Chip Enable ($\overline{E}$)

The Chip Enable input activates the memory control logic, input buffers, decoders and sense amplifiers. When Chip Enable is Low, V_{IL}, the device is selected. If Chip Enable goes High, V_{IH}, while the device is busy, the device remains selected and does not go into standby mode.

3.5 Read Enable ($\overline{R}$)

The Read Enable pin, $\overline{R}$, controls the sequential data output during read operations. Data is valid t_{RLQV} after the falling edge of $\overline{R}$. The falling edge of $\overline{R}$ also increments the internal column address counter by one.

3.6 Write Enable ($\overline{W}$)

The Write Enable input, $\overline{W}$, controls writing to the command interface, input address, and data latches. Both addresses and data are latched on the rising edge of Write Enable.

During power-up and power-down a recovery time of 10 µs (min) is required before the command interface is ready to accept a command. It is recommended to keep Write Enable High during the recovery time.

3.7 Write Protect ($\overline{WP}$)

The Write Protect pin is an input that gives a hardware protection against unwanted program or erase operations. When Write Protect is Low, V_{IL}, the device does not accept any program or erase operations.

It is recommended to keep the Write Protect pin Low, V_{IL}, during power-up and power-down.

3.8 Ready/Busy ($R\overline{B}$)

The Ready/Busy output, $R\overline{B}$, is an open-drain output that can identify if the P/E/R controller is currently active.

When Ready/Busy is Low, V_{OL}, a read, program or erase operation is in progress. When the operation completes, Ready/Busy goes High, V_{OH}.

The use of an open-drain output allows the Ready/Busy pins from several memories to be connected to a single pull-up resistor. A Low indicates that one, or more, of the memories is busy.

During power-up and power-down a minimum recovery time of 10 µs is required before the command interface is ready to accept a command. During this period the Ready/Busy signal is Low, V_{OL}.

Refer to *Section 12.1: Ready/Busy signal electrical characteristics* for details on how to calculate the value of the pull-up resistor.

3.9 V_{DD} supply voltage

V_{DD} provides the power supply to the internal core of the memory device. It is the main power supply for all operations (read, program and erase).

An internal voltage detector disables all functions whenever V_{DD} is below V_{LKO} (see *Table 19: DC characteristics*) to protect the device from any involuntary program/erase during power transitions.

Each device in a system should have V_{DD} decoupled with a 0.1 µF capacitor. The PCB track widths should be sufficient to carry the required program and erase currents.

3.10 V_{SS} ground

Ground, $V_{SS,}$ is the reference for the power supply. It must be connected to the system ground.

4 Bus operations

There are six standard bus operations that control the memory. Each of these is described in this section. See the summary in *Table 4: Bus operations*.

Typically, glitches of less than 3 ns on Chip Enable, Write Enable and Read Enable are ignored by the memory and do not affect bus operations.

4.1 Command input

Command input bus operations give commands to the memory. Commands are accepted when Chip Enable is Low, Command Latch Enable is High, Address Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal.

Only I/O0 to I/O7 are used to input commands.

See *Figure 33* and *Table 20* for details of the timings requirements.

4.2 Address input

Address input bus operations input the memory addresses. Five bus cycles are required to input the addresses (refer to *Table 5: Address insertion*).

The addresses are accepted when Chip Enable is Low, Address Latch Enable is High, Command Latch Enable is Low and Read Enable is High. They are latched on the rising edge of the Write Enable signal. Only I/O0 to I/O7 are used to input addresses.

See *Figure 34* and *Table 20* for details of the timings requirements.

4.3 Data input

Data input bus operations input the data to be programmed. Data is only accepted when Chip Enable is Low, Address Latch Enable is Low, Command Latch Enable is Low and Read Enable is High. The data is latched on the rising edge of the Write Enable signal. The data is input sequentially using the Write Enable signal.

See *Figure 35* and *Table 20* for details of the timing requirements.

4.4 Data output

Data output bus operations read the data in the memory array, the status register, the electronic signature, and the unique identifier.

Data is output when Chip Enable is Low, Write Enable is High, Address Latch Enable is Low, and Command Latch Enable is Low.

The data is output sequentially using the Read Enable signal.

If the Read Enable pulse frequency is lower then 33 MHz (t_{RLRL} higher than 30 ns), the output data is latched on the rising edge of Read Enable signal (see *Figure 36: Sequential data output after read AC waveforms*).

For higher frequencies (t_{RLRL} lower than 30 ns), the extended data out (EDO) mode must be considered. In this mode, data output is valid on the input/output bus for a time of t_{RLQX} after the falling edge of Read Enable signal (see *Figure 36: Sequential data output after read AC waveforms*).

See *Table 21: AC characteristics for operations,* for details on the timings requirements.

4.5 Write protect

Write protect bus operations protect the memory against program or erase operations. When the Write Protect signal is Low the device does not accept program or erase operations, therefore, the contents of the memory array cannot be altered. The Write Protect signal is not latched by Write Enable to ensure protection, even during power-up.

4.6 Standby

The memory enters standby mode by holding Chip Enable, $\overline{E}$, High for at least 10 µs. In standby mode, the device is deselected, outputs are disabled and power consumption is reduced.

Table 4. Bus operations

Bus operation	$\overline{E}$	AL	CL	$\overline{R}$	$\overline{W}$	$\overline{WP}$	I/O0 - I/O7
Command input	V_{IL}	V_{IL}	V_{IH}	V_{IH}	Rising	X(1)	Command
Address input	V_{IL}	V_{IH}	V_{IL}	V_{IH}	Rising	X	Address
Data input	V_{IL}	V_{IL}	V_{IL}	V_{IH}	Rising	V_{IH}	Data input
Data output	V_{IL}	V_{IL}	V_{IL}	Falling	V_{IH}	X	Data output
Write protect	X	X	X	X	X	V_{IL}	X
Standby	V_{IH}	X	X	X	X	V_{IL}/V_{DD}	X

1. $\overline{WP}$ must be V_{IH} when issuing a program or erase command.

Table 5. Address insertion(1)

Bus cycle	I/O7	I/O6	I/O5	I/O4	I/O3	I/O2	I/O1	I/O0
1st	A7	A6	A5	A4	A3	A2	A1	A0
2nd	V_{IL}	V_{IL}	V_{IL}	A12	A11	A10	A9	A8
3rd	A20	A19	A18	A17	A16	A15	A14	A13
4th	A28	A27	A26	A25	A24	A23	A22	A21
5th	V_{IL}	V_{IL}	V_{IL}	V_{IL}	V_{IL}	A31(2)	A30	A29

1. Any additional address input cycles are ignored.
2. A31 is required only for 16-Gbit devices.

Table 6. Address definitions

Address	Definition
A0 - A12	Column address
A13 - A18	Page address
A19 - A31	Block address

5 Command set

All bus write operations to the device are interpreted by the command interface. The commands are input on I/O0-I/O7 and are latched on the rising edge of Write Enable when the Command Latch Enable signal is High. Device operations are selected by writing specific commands to the command register. The two-step command sequences for program and erase operations are imposed to maximize data security.

The commands are summarized in *Table 7: Command set*.

Table 7. Command set

Function	1st cycle	2nd cycle	3rd cycle	4th cycle	Acceptable during command busy
Page Read	00h	30h			
Read for Copy Back	00h	35h			
Read ID	90h				
Reset	FFh				Yes
Page Program	80h	10h			
Multiplane Page Program	80h	11h	81h	10h	
Multiplane Read	60h	60h	30h		
Copy Back Program	85h	10h			
Multiplane Copy Back Program	85h	11h	81h	10h	
Multiplane Copy Back Read	60h	60h	35h		
Block Erase	60h	D0h			
Multiplane Block Erase	60h	60h	D0h		
Read Status Register	70h				Yes
Random Data Input	85h				
Random Data Output	05h	E0h			
Multiplane Random Data Output	00h	05h	E0h		
Cache Read	31h				
End Cache Read	3Fh				
Page Program with 2-Kbyte compatibility	80h	11h	80h	10h	
Copy Back Program with 2-Kbyte compatibility	85h	11h	85h	10h	

6 Device operations

6.1 Single plane operations

This section gives the details of the single plane device operations.

6.1.1 Page read

At power-up the device defaults to read mode. To enter read mode from another mode the Read command must be issued, see *Table 7: Command set*. Once a Read command is issued, subsequent consecutive read commands only require the confirm command code (30h).

After a first page read operation, the device stays in read mode and a second page read can be started by inputting 5 address cycles and a read confirm command.

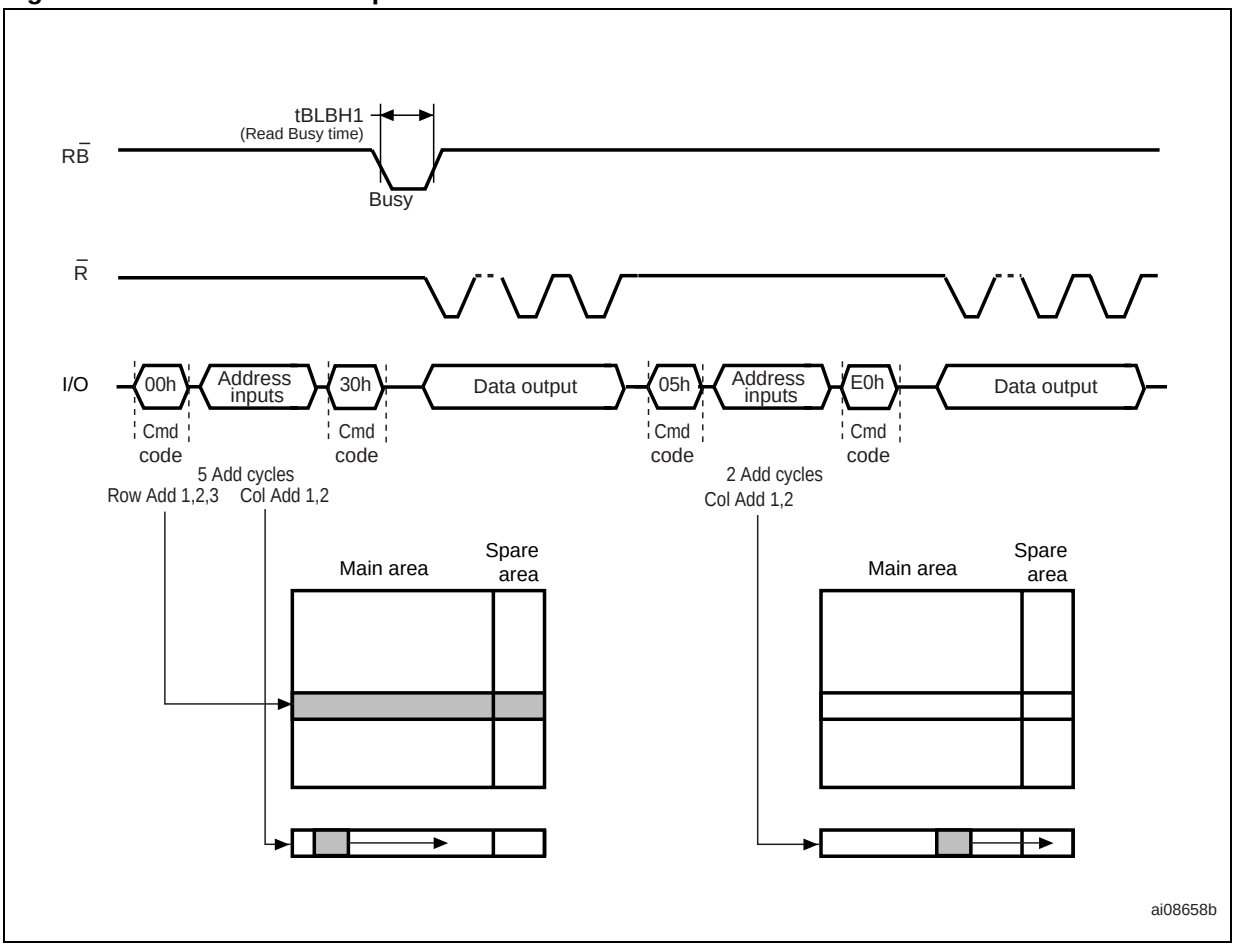
Once a read command is issued, two types of operations are available: random read and sequential page read. The random read mode is enabled when the page address is changed.

After the first random read access, the page data (4224 bytes) is transferred to the page buffer in a time of t_{WHBH} (refer to *Table 21: AC characteristics for operations* for value). Once the transfer is complete, the Ready/Busy signal goes High. The data can then be read out sequentially (from the selected column address to last column address) by pulsing the Read Enable signal (see *Figure 39: Page read operation AC waveforms*).

The device can output random data in a page, instead of the consecutive sequential data, by issuing a Random Data Output command. The Random Data Output command can be used to skip some data during a sequential data output.

The sequential operation can be resumed by changing the column address of the next data to be output, to the address which follows the Random Data Output command. The Random Data Output command can be issued as many times as required within a page.

Figure 5. Random data output



6.1.2 Cache read

The cache read operation improves the read throughput by reading data using the cache register. As soon as the user starts to read one page, the device automatically loads the next page into the cache register.

A Read Page command is issued prior to the first Cache Read command in a cache read sequence. Once the Read Page command execution is terminated, the Cache Read command can be issued as follows:

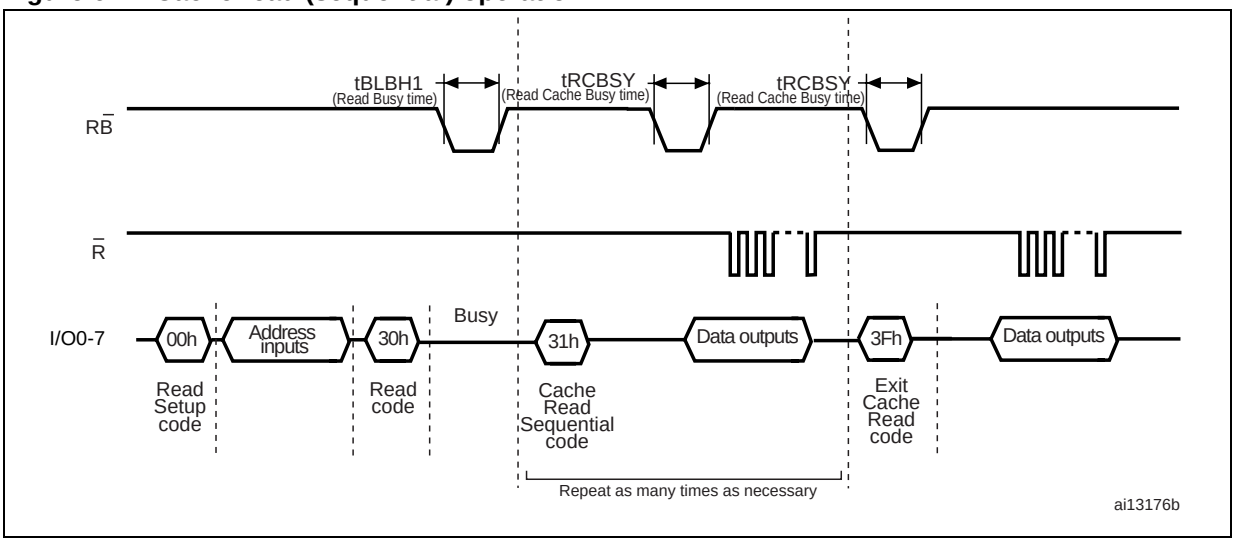
1. Issue a Sequential Cache Read command to copy the next page in sequential order to the cache register
2. Issue a Random Cache Read command to copy the page addressed in this command to the cache register.

The two commands can be used interchangeably, in any order. When there are no more pages to be read, the final page is copied into the cache register by issuing the Exit Cache Read command. A Cache Read command must not be issued after the last page of the device is read. Data output only starts after issuing the 31st command for the first time. See *Figure 6: Cache read (sequential) operation* and *Figure 6.1.3: Page program* for examples of the two sequences.

After the Sequential Cache Read or Random Cache Read command has been issued, the Ready/Busy signal goes Low and the status register bits are set to SR5='0' and SR6='0' for a period of cache read busy time, t_{RCBSY}, while the device copies the next page into the cache register.

After the cache read busy time has passed, the Ready/Busy signal goes High and the status register bits are set to SR5='0' and SR6='1', signifying that the cache register is ready to download new data. data of the previously read page can be output from the page buffer by toggling the Read Enable signal. Data output always begins at column address 00h, but the Random Data Output command is also supported.

Figure 6. Cache read (sequential) operation



6.1.3 Page program

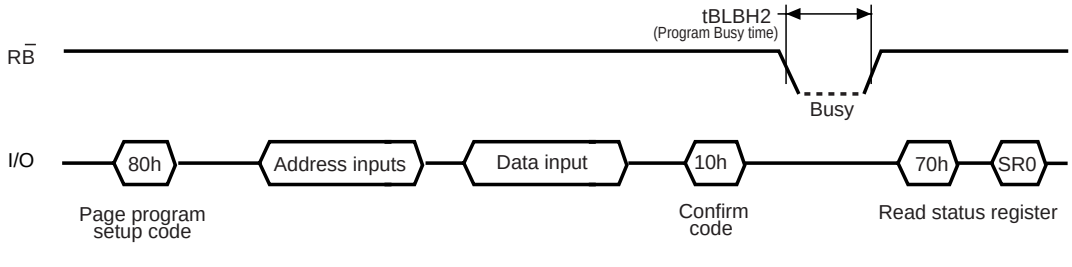
The page program operation is the standard operation to program data to the memory array. Generally, data is programmed sequentially, however, the device does support random input within a page.

The memory array is programmed by page, however, partial page programming is allowed where any number of bytes (1 to 4224) can be programmed.

The maximum number of consecutive partial page program operations on the same page is 8 (see *Table 15: Program and erase times and program erase endurance cycles*). After exceeding this a Block Erase command must be issued before any further program operations can take place in that page (see *Figure 7: Page program operation*).

Within a given block, the pages must be programmed sequentially and random page address programming is not allowed.

Figure 7. Page program operation



Once the program operation has started the status register can be read using the Read Status Register command. During program operations the status register only flags errors for bits set to '1' that have not been successfully programmed to '0'.

During the program operation, only the Read Status Register and Reset commands are accepted; all other commands are ignored. Once the program operation has completed, the P/E/R controller bit SR6 is set to '1' and the Ready/Busy signal goes High.

The device remains in read status register mode until another valid command is written to the command interface.

Sequential input

To input data sequentially the addresses must be sequential and remain in one block.

For sequential input, each page program operation comprises five steps:

1. One bus cycle is required to set up the Page Program (sequential input) command (see *Table 7: Command set*)
2. Five bus cycles are then required to input the program address (refer to *Table 5: Address insertion*)
3. The data is loaded into the data registers
4. One bus cycle is required to issue the Page Program Confirm command to start the P/E/R controller. The P/E/R controller only starts if the data has been loaded in step 3
5. The P/E/R controller then programs the data into the array.

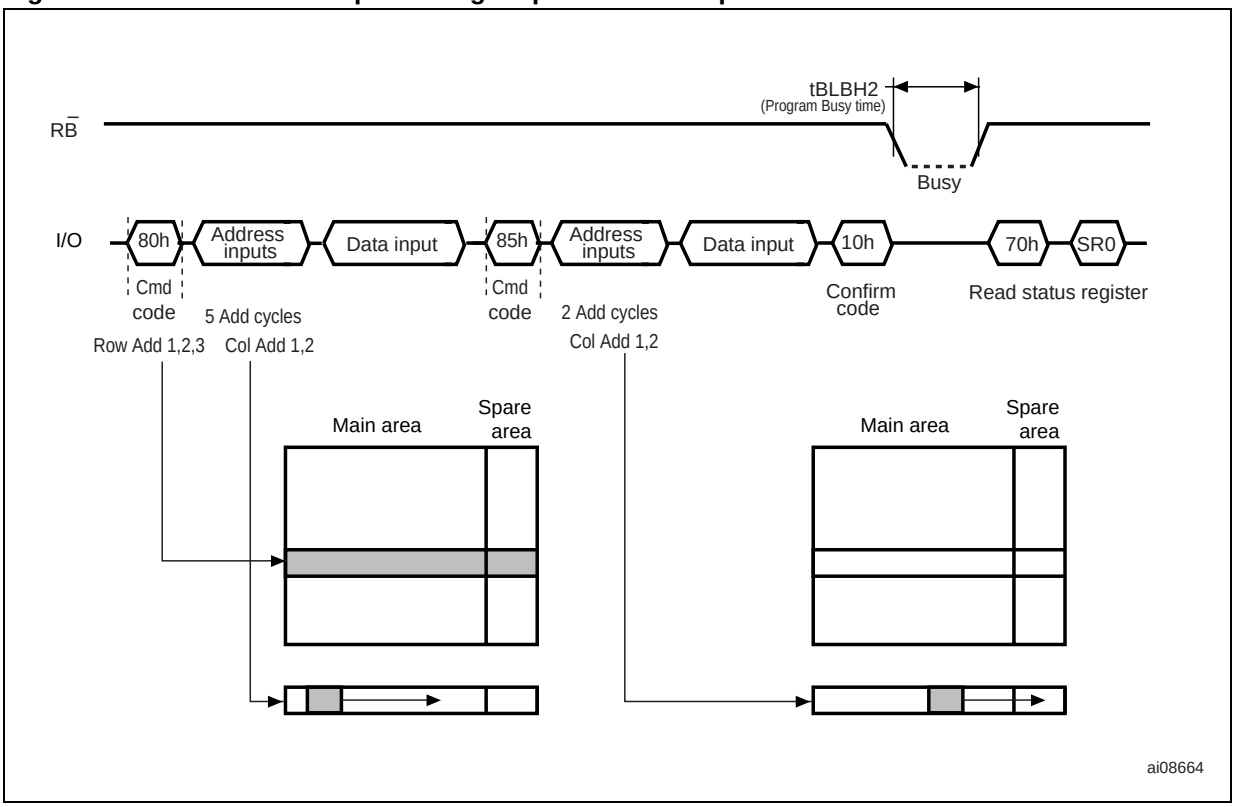
Random data input

During a sequential input operation, the next sequential address to be programmed can be replaced by a random address issuing a Random Data Input command. The following two steps are required to issue the command:

1. One bus cycle is required to setup the Random Data Input command (see *Table 7*).
2. Two bus cycles are then required to input the new column address (refer to *Table 5*).

Random data input operations can be repeated as often as required in any given page.

Figure 8. Random data input during sequential data input



6.1.4 Block erase

Erase operations are done one block at a time. An erase operation sets all the bits in the addressed block to ‘1’. All previous data in the block is lost.

An erase operation consists of three steps (refer to *Figure 9: Block erase operation*):

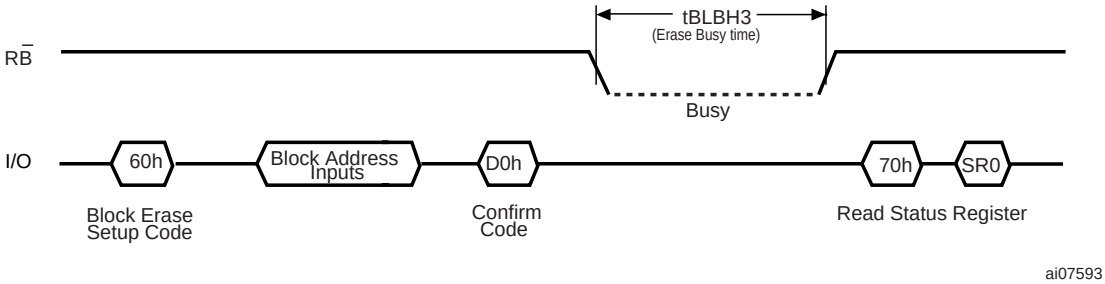
1. One bus cycle is required to setup the Block Erase command. Only addresses A19 to A30 are valid while the addresses A13 to A18 are ignored
2. Three bus cycles are then required to load the address of the block to be erased. Refer to *Table 6: Address definitions* for the block addresses of each device
3. One bus cycle is required to issue the Block Erase Confirm command to start the P/E/R controller.

The erase operation is initiated on the rising edge of Write Enable, $\overline{W}$, after the Confirm command is issued. The P/E/R controller handles block erase and implements the verify process.

During the block erase operation, only the Read Status Register and Reset commands are accepted; all other commands are ignored.

Once the program operation has completed, the P/E/R controller bit SR6 is set to ‘1’ and the Ready/Busy signal goes High. If the operation completes successfully, the write status bit SR0 is ‘0’, otherwise it is set to ‘1’ (refer to *Section 6.5: Read status register*).

Figure 9. Block erase operation



6.1.5 Copy-back program

The copy-back program with read for copy-back operation is configured to quickly and efficiently rewrite data stored in one page without data reloading when the bit error is not in data stored.

Since the time-consuming re-loading cycles are removed, the system performance is improved. The benefit is especially obvious when a portion of a block is updated and the rest of the block also needs to be copied to the newly-assigned free block. The copy-back operation is a sequential execution of read for copy-back and copy back program with the destination page address. A read operation with a 35h command in the address of the source page moves the entire 4224 bytes into the internal data buffer. When the device returns to the ready state ($R\overline{B}$ High), optional readout of data is allowed by pulsing $\overline{R}$ to check ECC (see *Figure 11: Copy back program operation (with readout of data)*). The next bus write cycle of the command is given to input the target page address.

The actual programming operation begins after the Program Confirm command (10h) is issued. Once the program process starts, the Read Status Register command (70h) may be entered to read the status register. The system controller can detect the completion of a program cycle by monitoring the $R\overline{B}$ output, or the status bit (I/O6) of the status register. When the copy back program is complete, the write status bit (I/O0) can be checked. The command register remains in read status command mode until another valid command is written to the command register. During the copy back program, data modification is possible using Random Data Input command (85h) as shown in *Figure 12: Copy back program operation with random data input*.

The copy back program operation is only allowed within the same memory plane (A19 and A31 fixed for source and target address).

Figure 10. Copy back program operation (without readout of data)

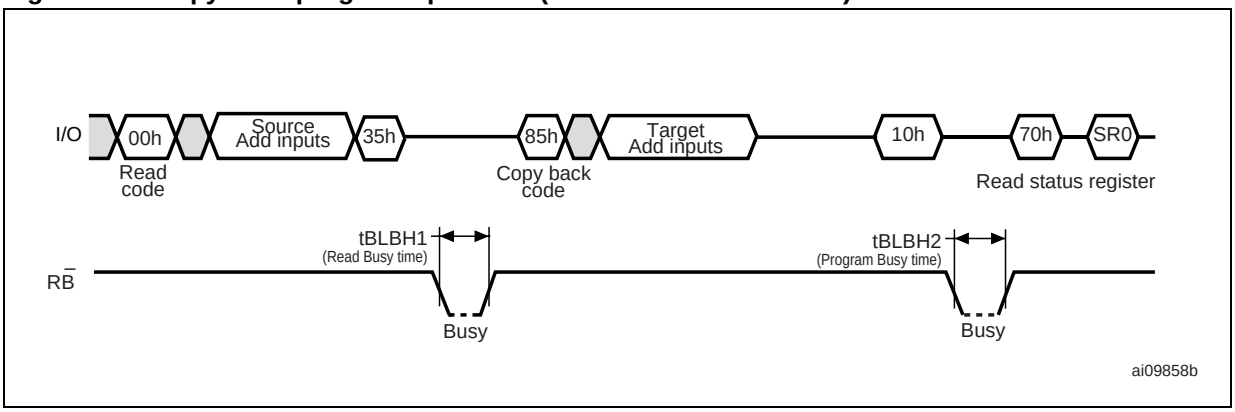


Figure 11. Copy back program operation (with readout of data)

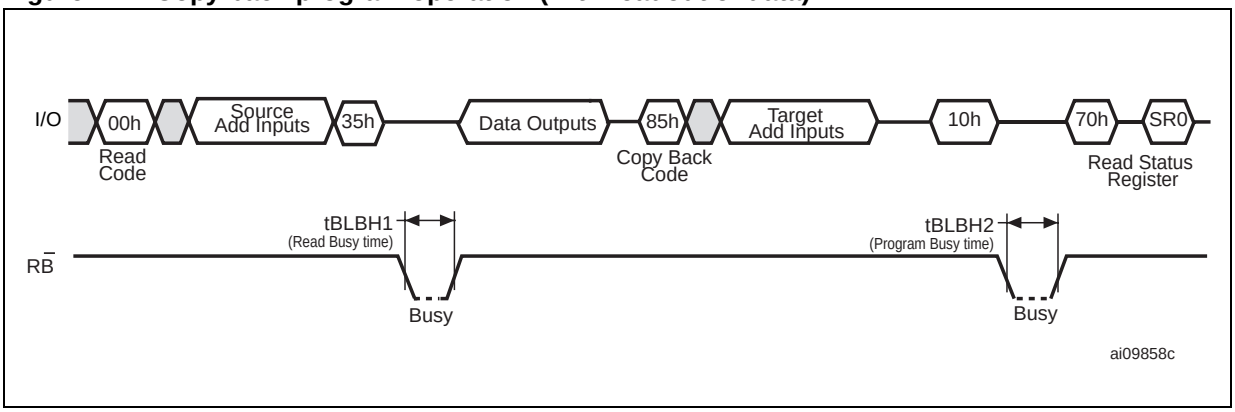
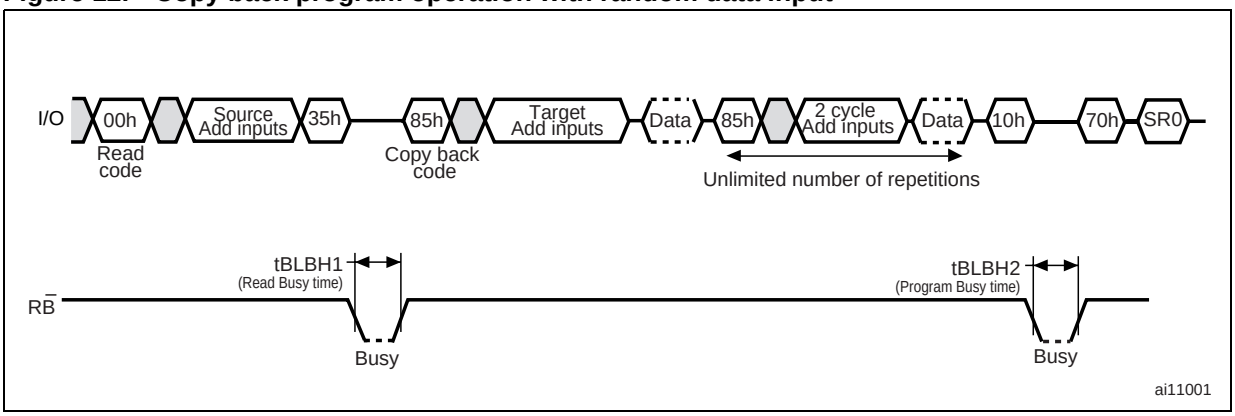


Figure 12. Copy back program operation with random data input



6.2 Multiplane operations

6.2.1 Multiplane page read

The multiplane page read operation is an extension of a page read operation for a single plane. Since the device is equipped with two memory planes, a read of two pages (one for each plane) is enabled by activating two sets of 4224-byte page registers (one for each plane). The multiplane page read operation is initiated by repeating twice the command 60h, followed by 3-address cycles, and then by one 30h Read Confirm command (only 3-address cycles are needed because the multiplane page read operation addresses the whole page starting form the first byte). In this case only the same page of the same block can be selected from each plane.

After the Read Confirm command (30h) the 8448 bytes of data within the selected two pages are transferred into the data registers in less than 25 µs (t_{WHBH}). The system controller can detect the completion of data transfer (t_{WHBH}) by monitoring the output of the R$\overline{B}$ pin.

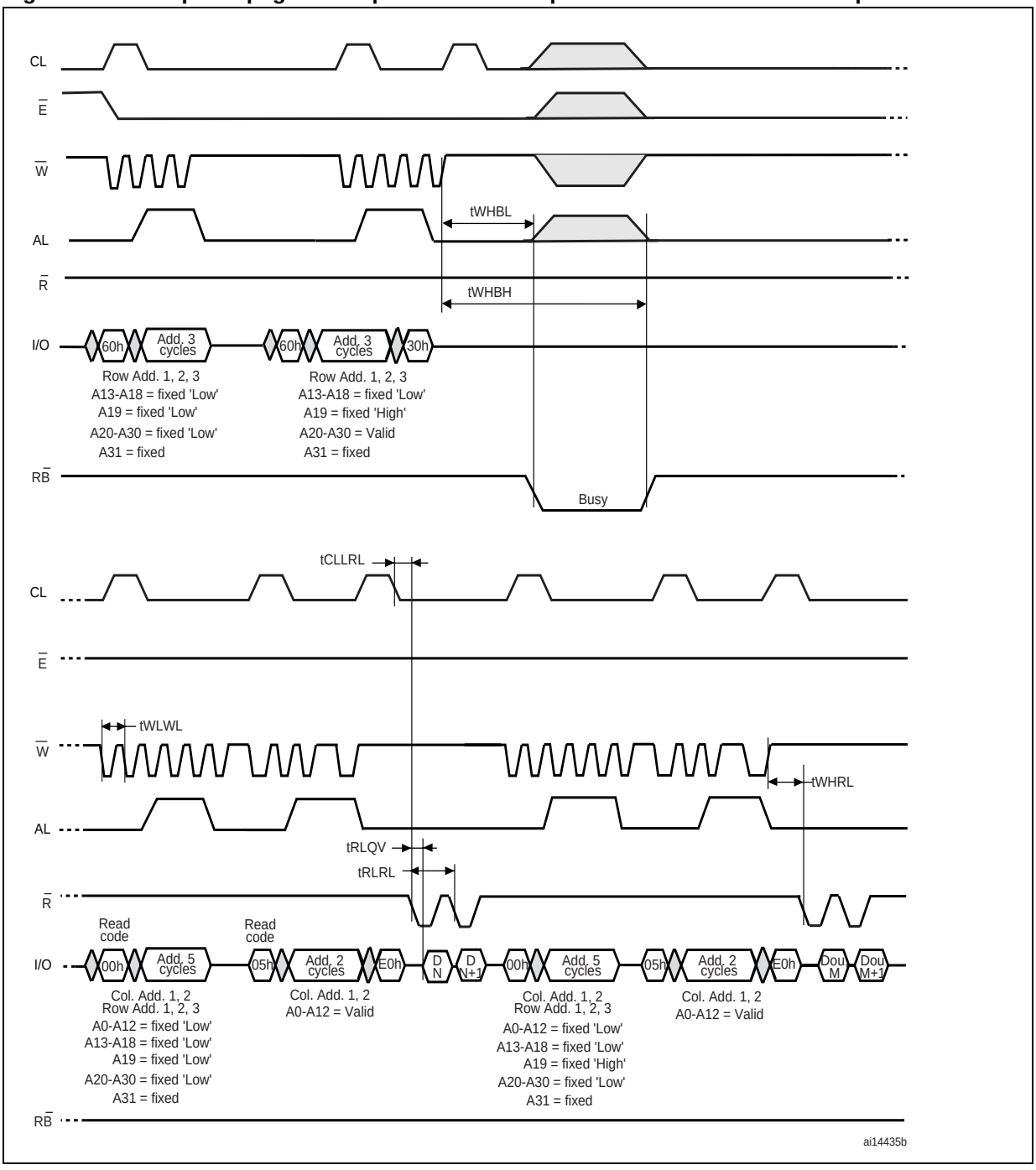
Once the data is loaded into the data registers, the data of first plane must be read by issuing the command 00h with 5 address cycles (all 00h), the command 05h with a 2-column address, the command E0h, and then by toggling Read Enable, $\overline{R}$. If the 2-column address is 00h, then the read output starts from the beginning of the page, otherwise the data output starts from selected column for random data output (see *Figure 13: Multiplane page read operation with sequential and random data output*).

The data of the second plane must be read using the following command sequence: command 00h with 5 address cycles (all 00h except A19 = 1 and A31= fixed), command 05h with a 2-column address, E0h, and then toggling Read Enable, $\overline{R}$. If the 2-column address is 00h, then the read output starts from the beginning of the page, otherwise the data output starts from selected column for random data output.

To execute multiple random data outputs within the same 2 selected pages, the command sequence is: command 00h with 5 address cycles, command 05h with a 2-column address, and finally E0h. In 5 address cycles A19=0 allows random read in the first plane page, while A19=1 allows random read in the second plane page (*Figure 13: Multiplane page read operation with sequential and random data output*).

Restrictions and details about the multiplane page read operation are shown in *Figure 13: Multiplane page read operation with sequential and random data output*. The multiplane page read operation must be used in the block that has been programmed with multiplane page program.

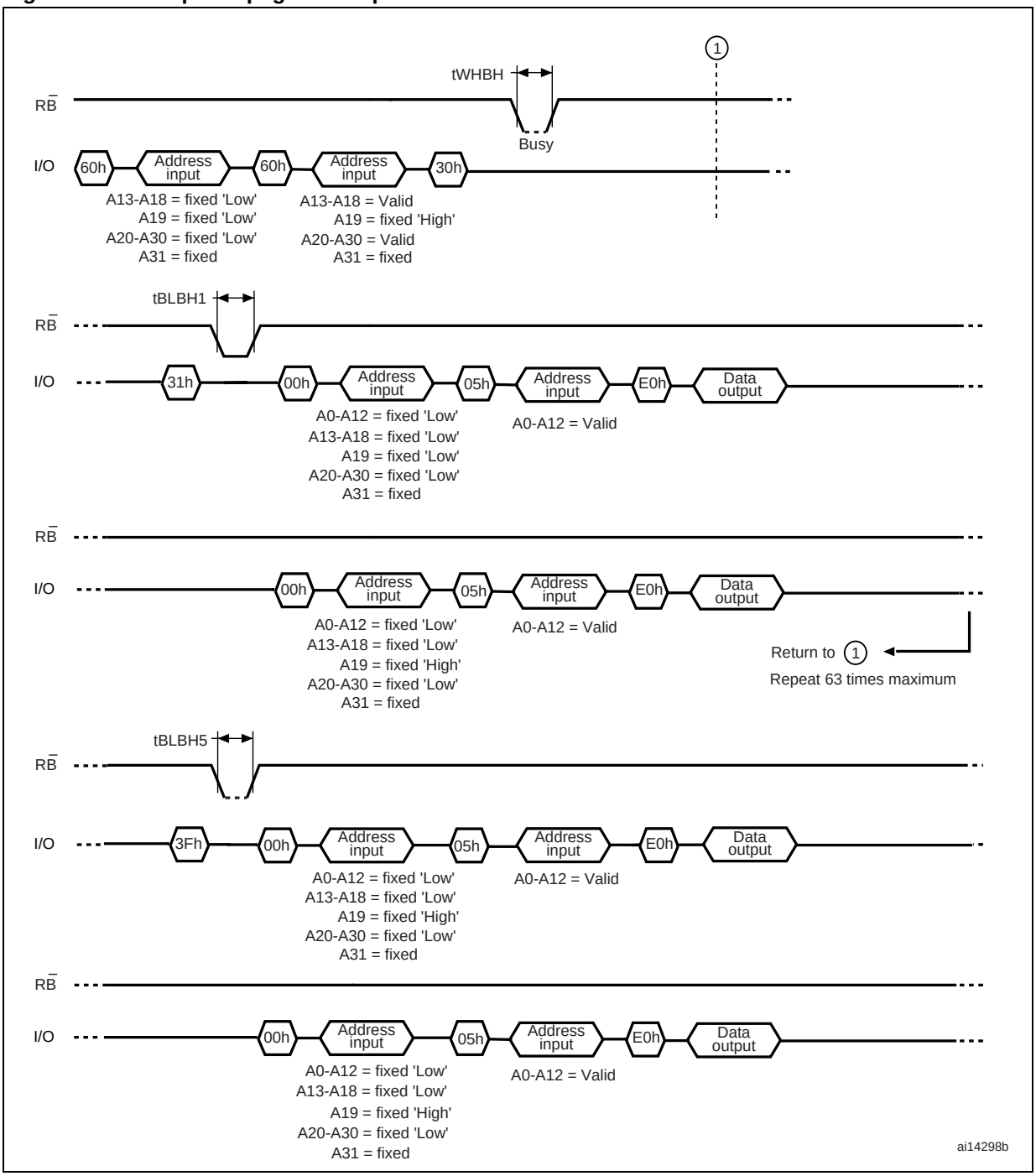
Figure 13. Multiplane page read operation with sequential and random data output



6.2.2 Multiplane cache read

NANDxxGW3F2A devices have a multiplane page read with cache operation, which enables much higher speed read operation compared to page read operation. The restrictions for this operation are shown in *Figure 14: Multiplane page read operation with cache read*.

Figure 14. Multiplane page read operation with cache read



6.2.3 Multiplane page program

The devices support multiplane page program, that allows the programming of two pages in parallel, one in each plane.

A multiplane page program operation requires two steps:

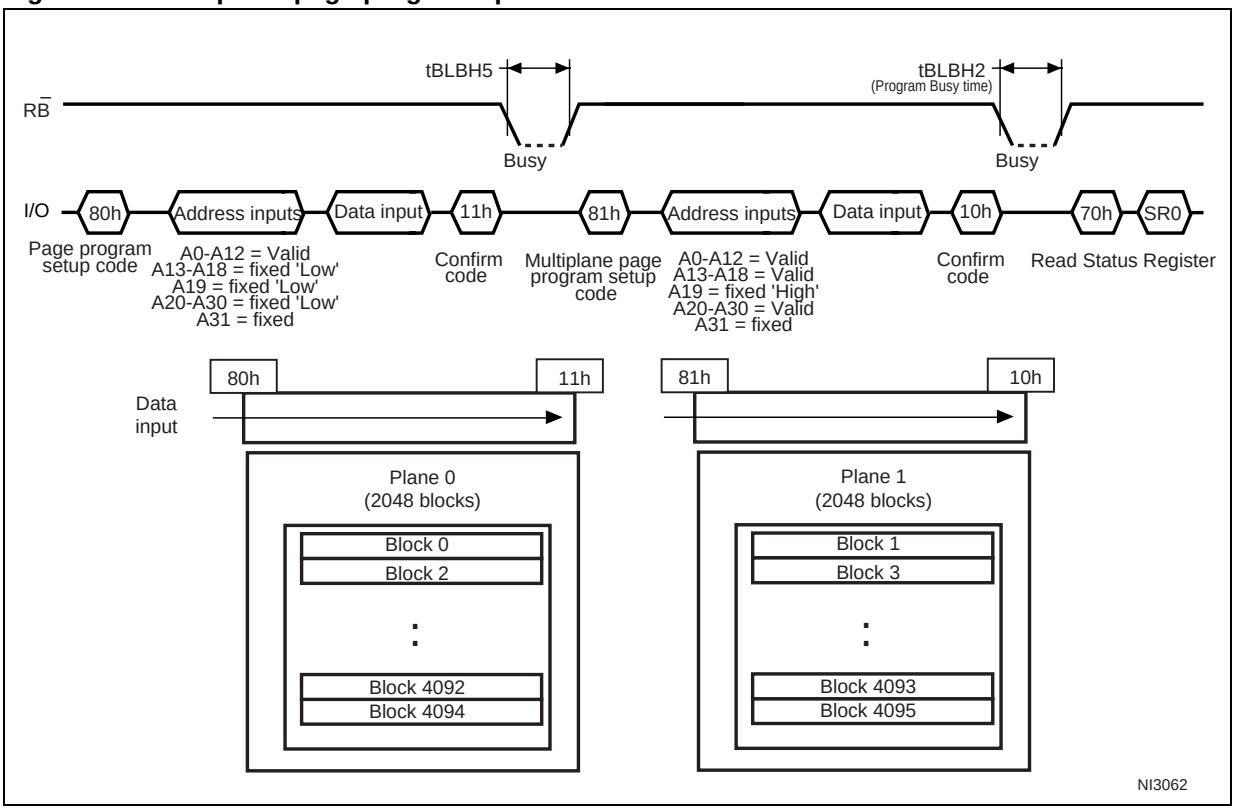
1. The first step loads serially up to two pages of data (8448 bytes) into the data buffer. It requires:
   - One clock cycle to set up the Page Program command (see *Section : Sequential input*)
   - Five bus write cycles to input the first page address and data. The address of the first page must be within the first plane (A19 = 0)
   - One bus write cycle to issue the page program confirm code. After this the device is busy for a time of t_{BLBH5}
   - When the device returns to the ready state (ready/busy high), a multiplane page program setup code must be issued, followed by the second page address (5 write cycles) and data. The address of the second page must be within the second plane (A19=1), and A18 to A13 must be the address bits loaded during the first address insertion
2. The second step programs, in parallel, the two pages of data loaded into the data buffer into the appropriate memory pages. It is started by issuing a Program Confirm command.

As for standard page program operations, the device supports random data input during both data loading phases.

Once the multiplane page program operation has started, maintaining a delay of t_{BLBH5}, the status register can be read using the Read Status Register command.

If the first or second page program fails, the fail bit of the status register is set: the device supports a pass/fail status of each plane (I/O0: total; I/O1: plane0; I/O2: plane1).

Figure 15. Multiplane page program operation



1. No command between 11h and 81h is permitted except 70h and FFh.

6.2.4 Multiplane erase

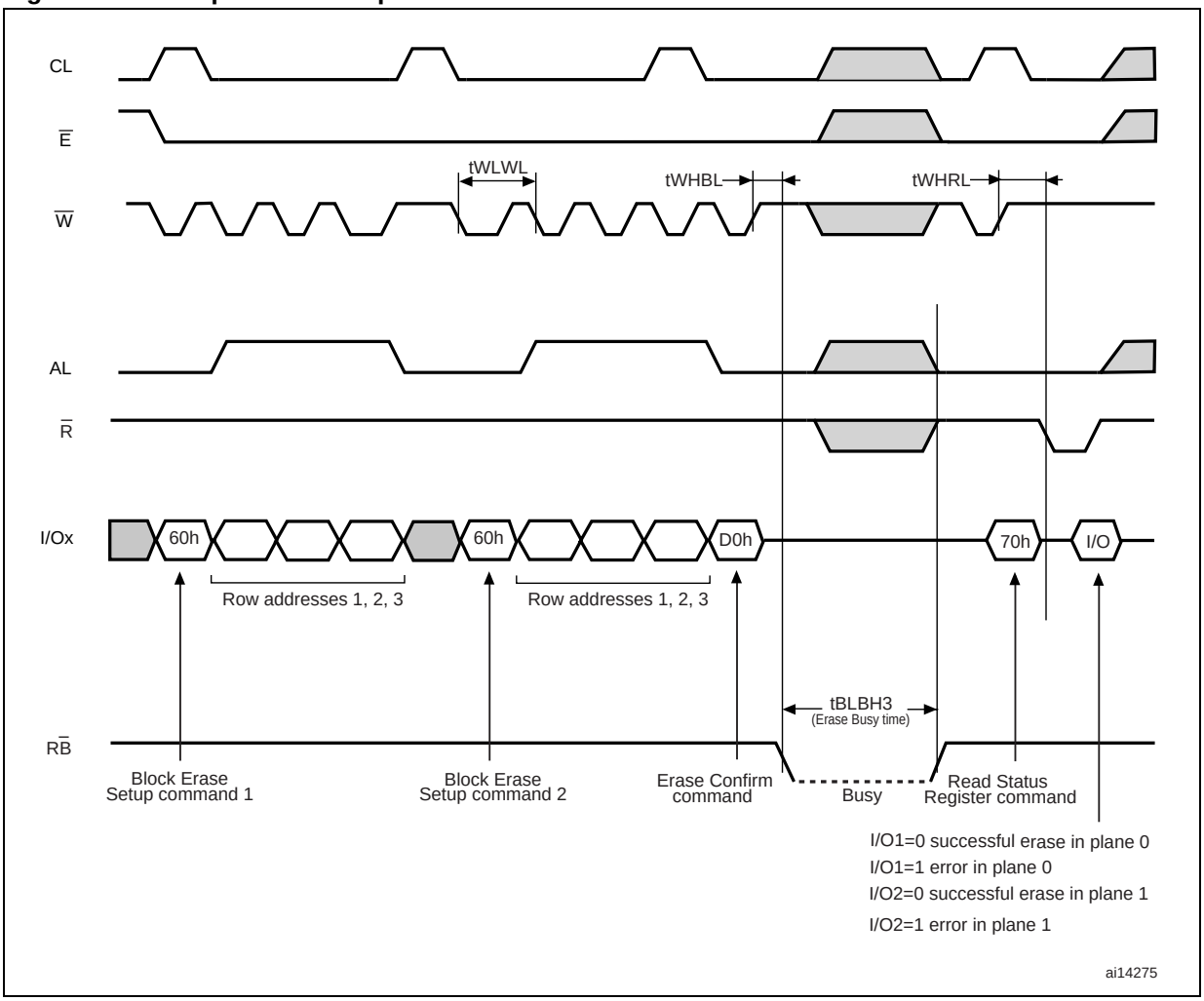
The multiplane erase operation allows the erasure of two blocks in parallel, one in each plane (refer to *Figure 16: Multiplane erase operation* for details of the sequence).

The Block Erase Setup command (60h) must be issued two times, each time followed by the 1st and 2nd block address cycles, respectively (3 cycles for each time). As for block erase operation, the Erase Confirm command (D0h) makes this operation start. No dummy busy time is required between the first and second block address cycles insertion.

Address limitation required for a multiplane program applies also to multiplane erase. The operation progress can also be checked as for multiplane program operation.

If the first or second block erase fails, the fail bit of the status register is set: the device supports a pass/fail status of each plane (I/O0: total; I/O1: plane0; I/O2: plane1).

Figure 16. Multiplane erase operation



6.2.5 Multiplane copy back program

The two-plane copy back program operation is an extension of the copy back program operation for a single plane with 4224-byte page registers. As for the single plane copy back, a multiplane read operation with ‘35h’ command (multiplane read for copy back) and the address of the source pages moves the whole 4224-byte of each page into the internal data buffer of each plane. Since the device is equipped with two memory planes, activating the two sets of 4224-byte page registers enables a simultaneous programming of two pages. *Figure 17: Multiplane copy back program operation* and *Figure 18: Multiplane copy back program operation with random data input* show the details of the command sequence for the multiplane copy back operation in standard operation mode. *Figure 19* to *22* show the new multiplane copy back program flows introduced to reduce the buffer size (8 Kbytes) required by the host to perform the multiplane copy back program operation. The sequences of data out followed by data input for each plane can be performed an indefinite number of times, depending on the buffer size used by the host. *Figure 19* shows the sequence when the host is equipped with a 4-Kbyte buffer size, while *Figure 22* shows the sequence when the host is equipped with a 2-Kbyte buffer size. The multiplane copy back program operation is allowed in the same die in stacked devices (A31 is fixed between source and target addresses).

Figure 17. Multiplane copy back program operation

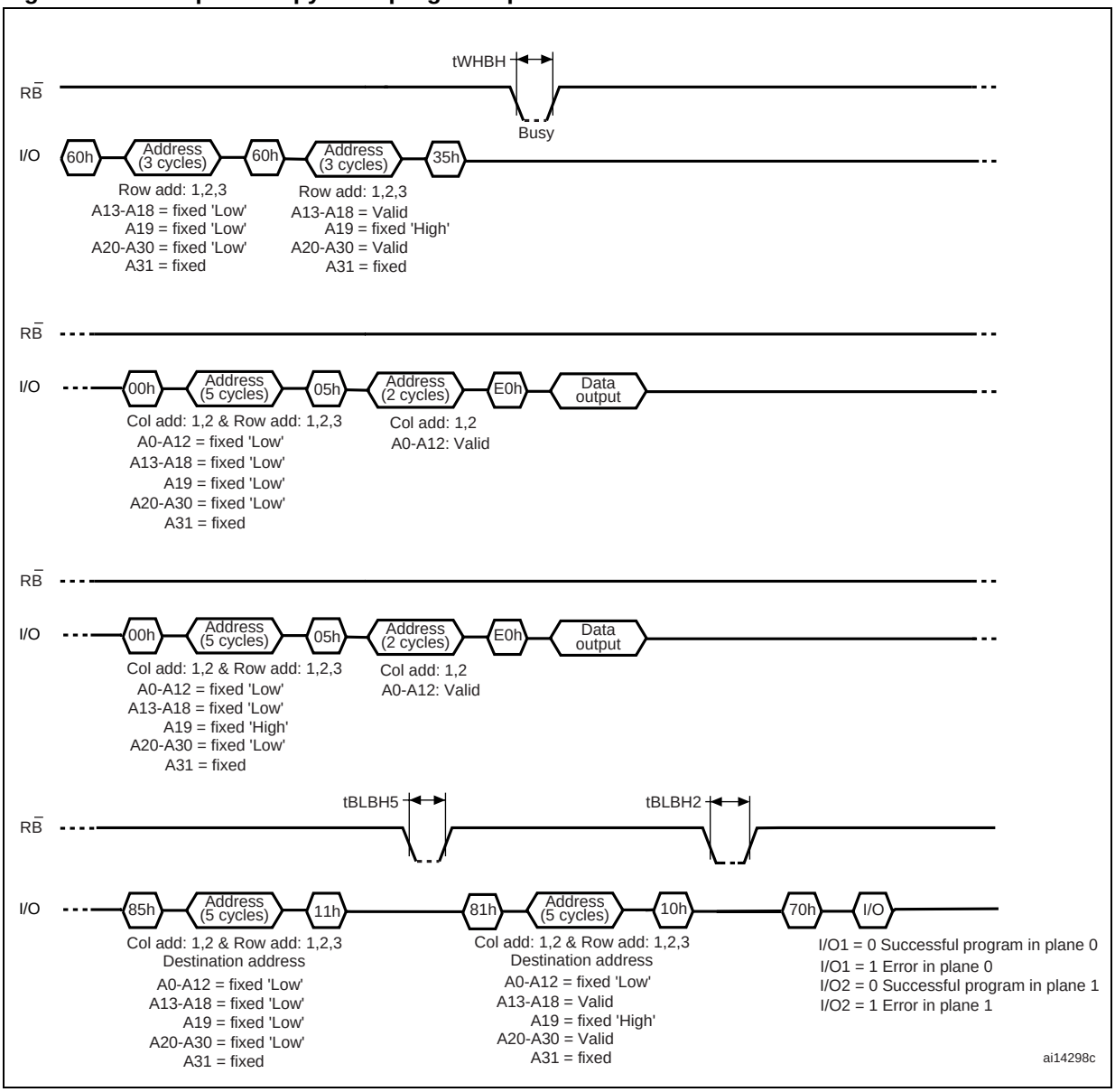


Figure 18. Multiplane copy back program operation with random data input

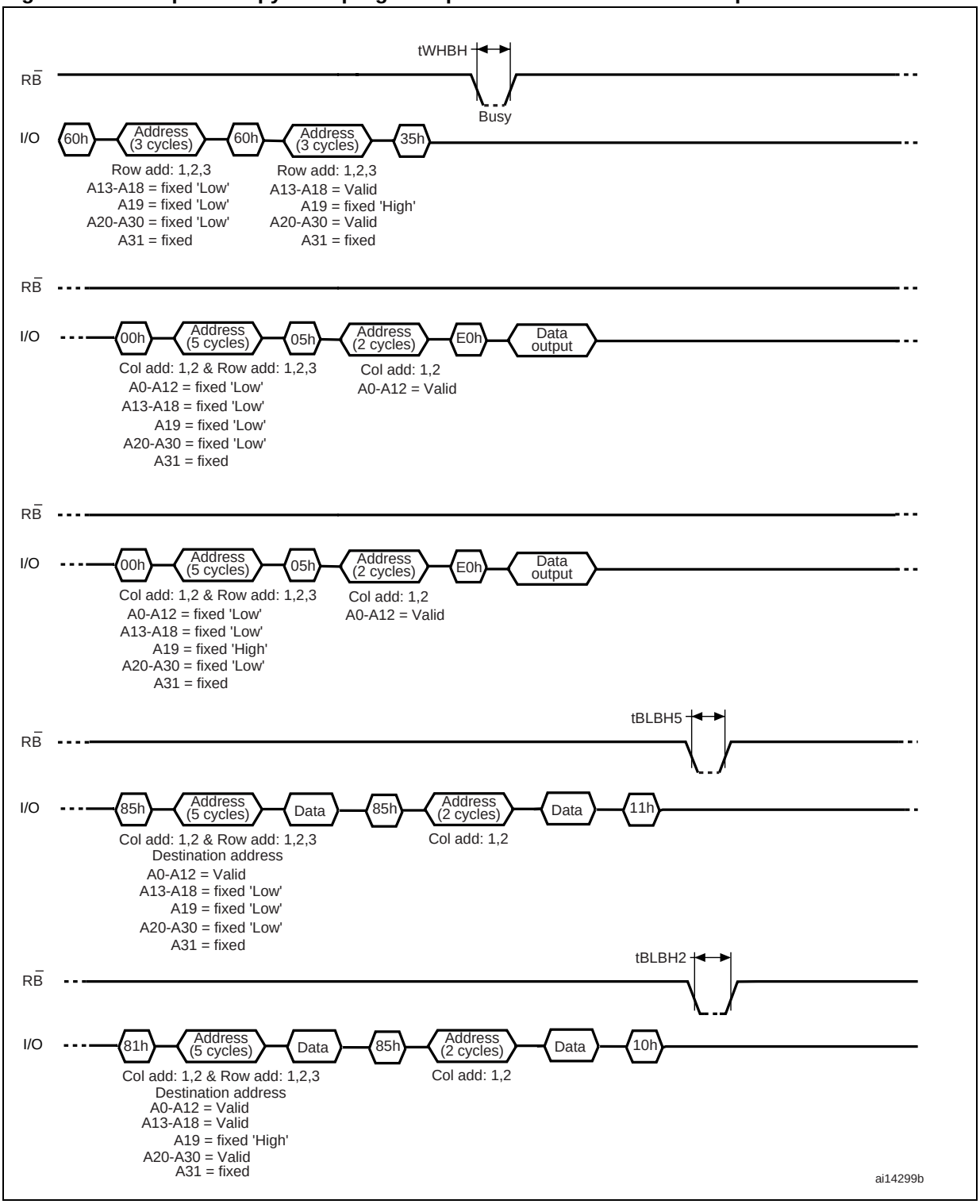


Figure 19. Multiplane copy back operation sequence

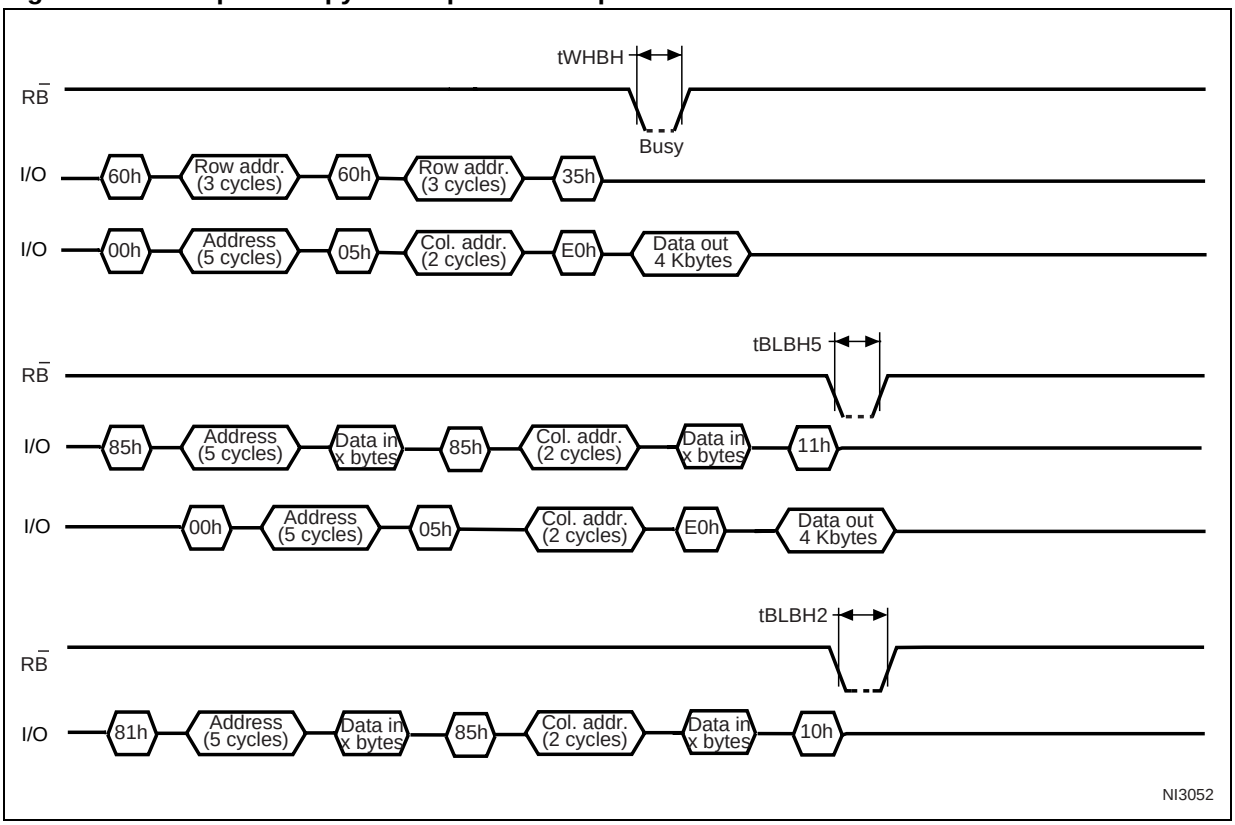


Figure 20. Multiplane copy back operation flow

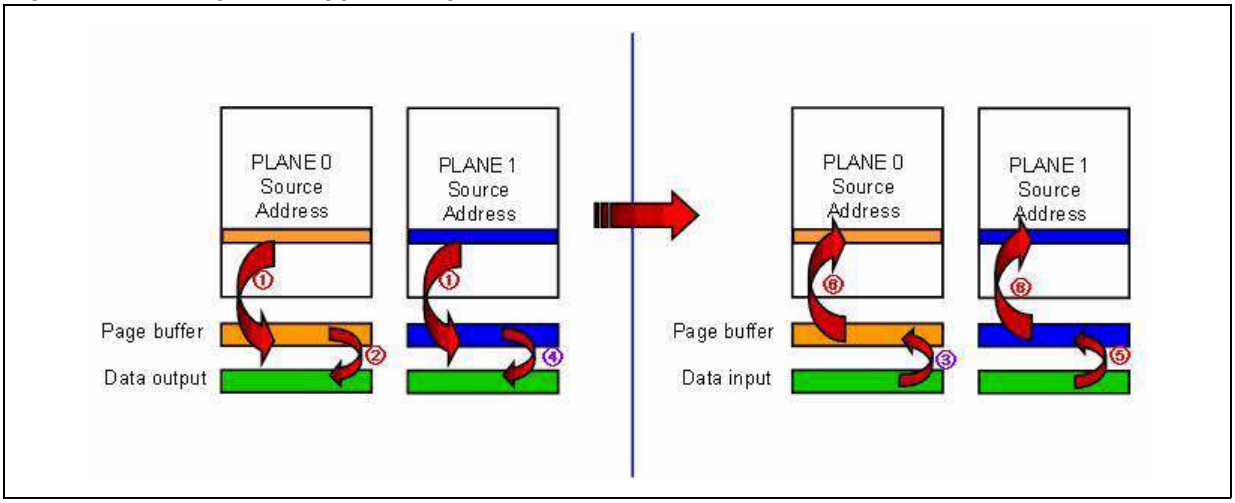


Figure 21. New multiplane copy back operation sequence

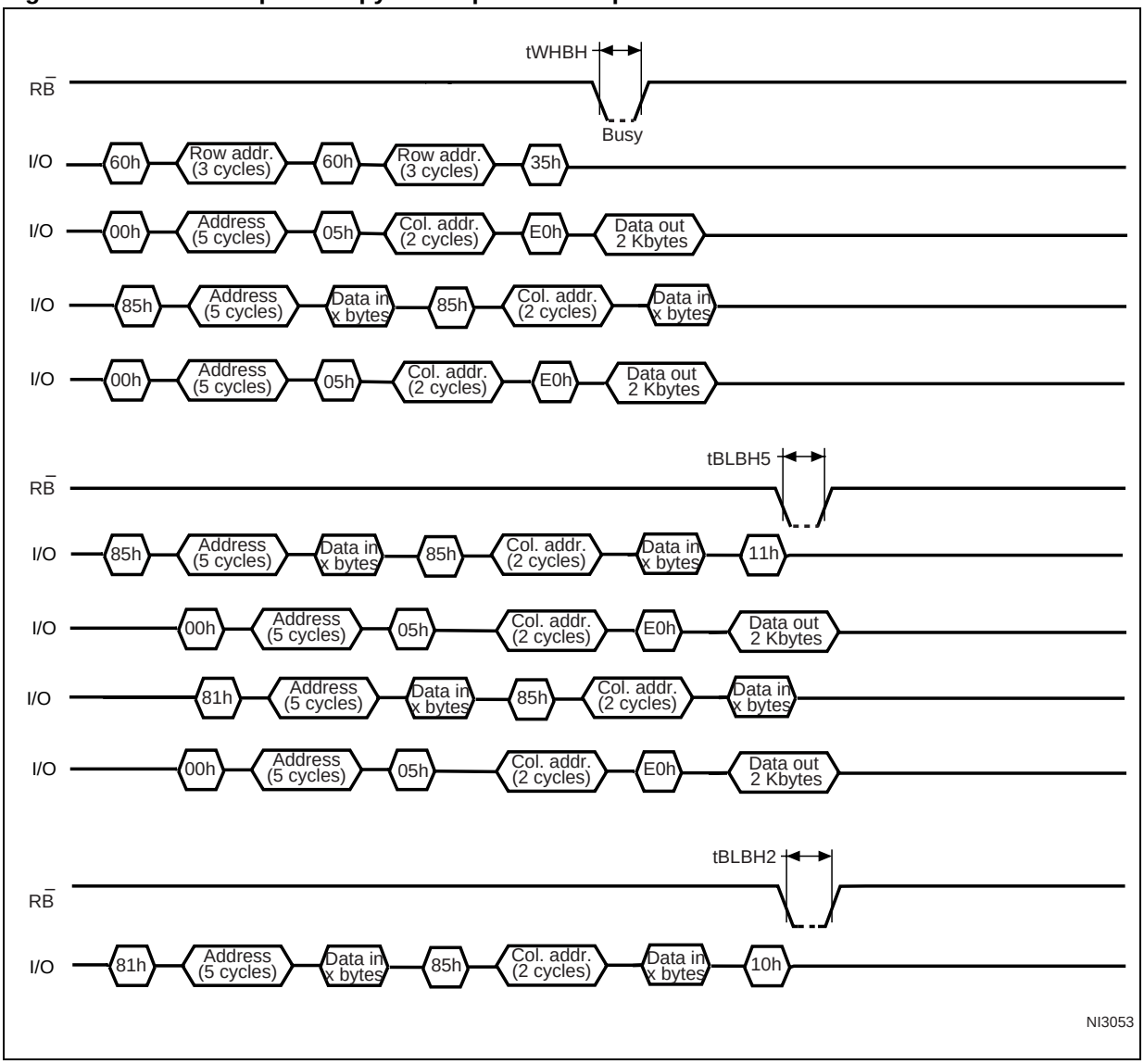
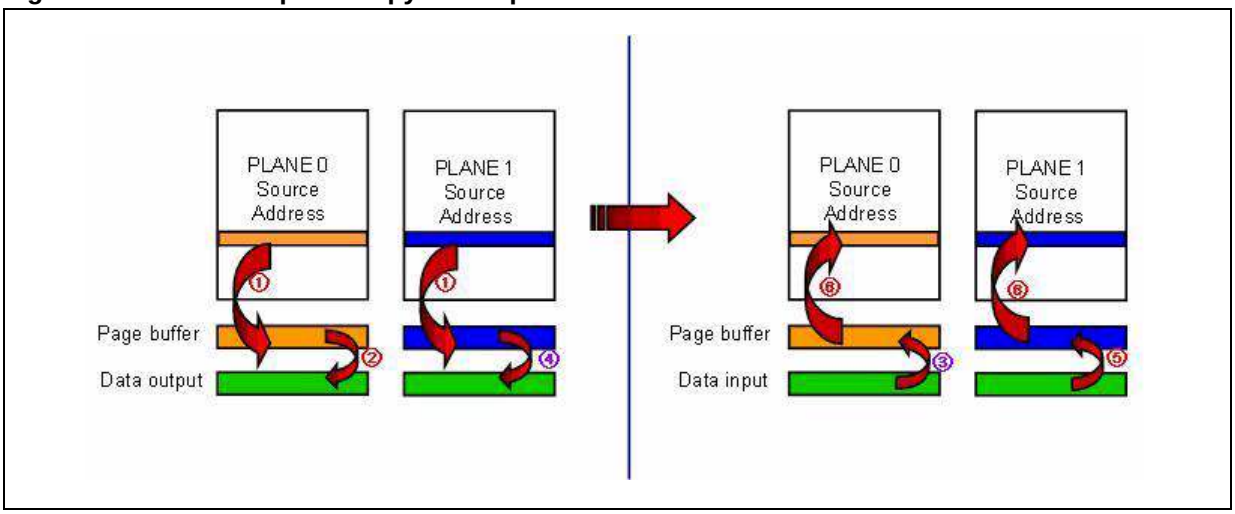


Figure 22. New multiplane copy back operation flow

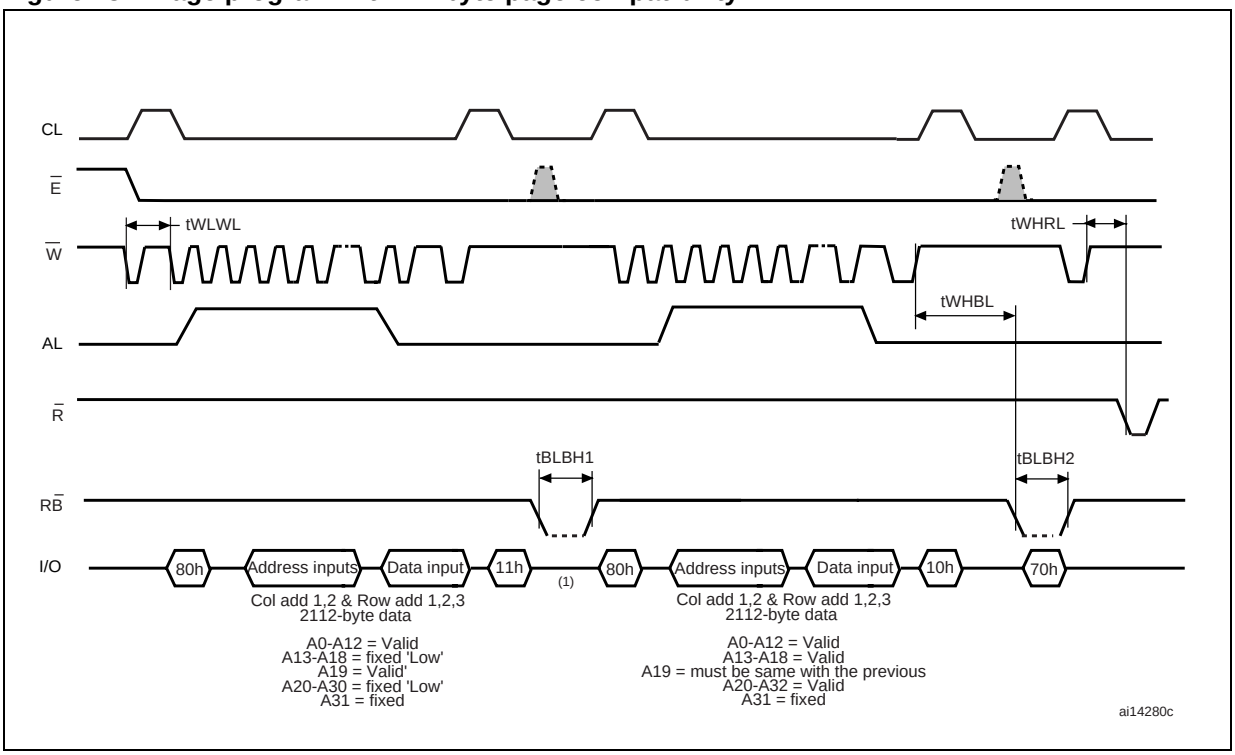


6.3 2-Kbyte page backward compatibility

6.3.1 Page program with 2-Kbyte page compatibility

A special page program operation is provided for 2-Kbyte compatibility, as shown in *Figure 23: Page program with 2-Kbyte page compatibility*.

Figure 23. Page program with 2-Kbyte page compatibility

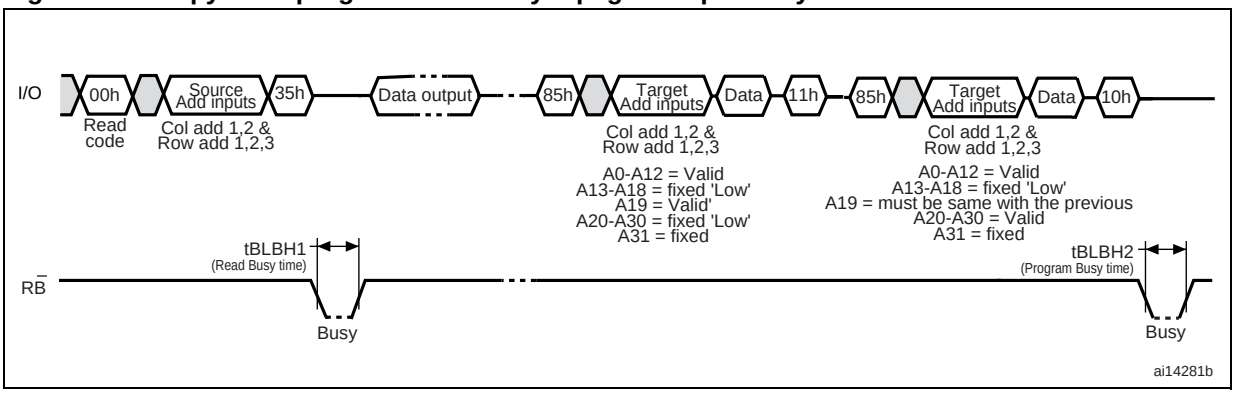


1. Any command between 11h and 80h is not allowed, except 70h/F1h and FFh.

6.3.2 Copy back program with 2-Kbyte page compatibility

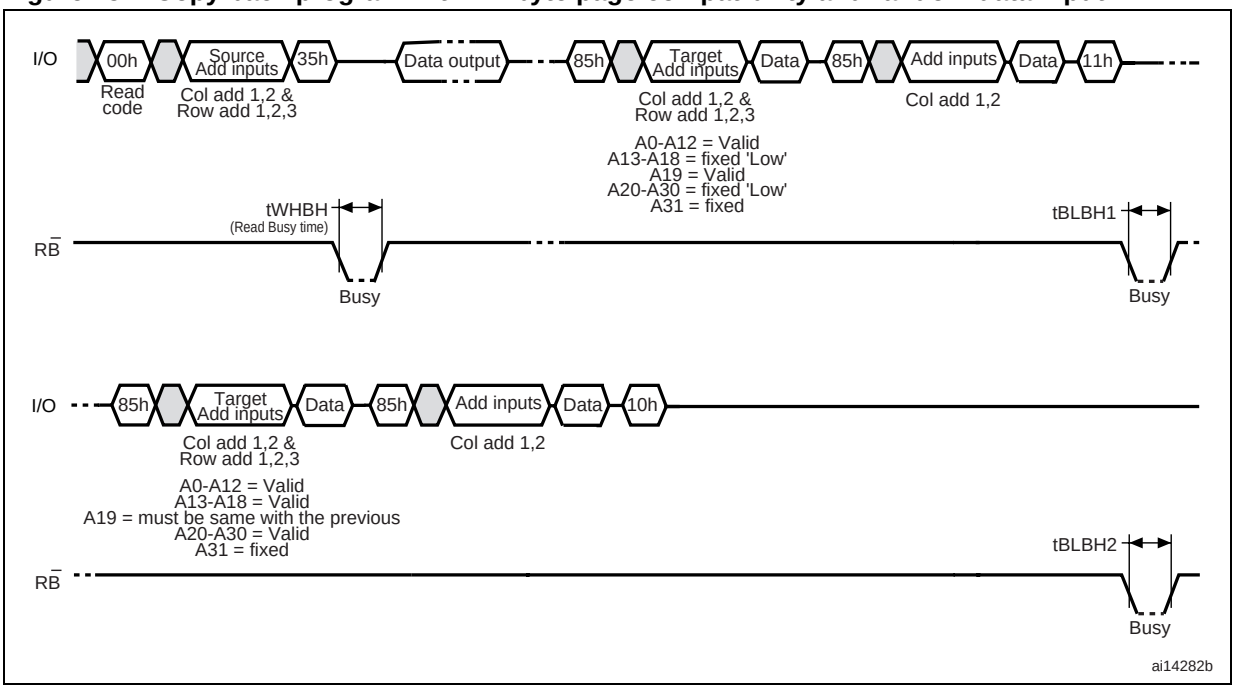
A special copy back program operation is provided for 2-Kbyte page compatibility as shown in *Figure 24: Copy back program with 2-Kbyte page compatibility* and *Figure 25: Copy back program with 2-Kbyte page compatibility and random data input*.

Figure 24. Copy back program with 2-Kbyte page compatibility



1. Copy back program operation is allowed only within the same memory plane.
2. On the same plane, it is not allowed to operate a copy-back program from an odd address page (source page) to an even address page (target page) or from an even address page (source page) to an odd address page (target page). Therefore, the copy-back program is permitted only between odd address pages or even address pages.
3. Any command between 11h and 85h is not allowed, except 70h/F1h and FFh.

Figure 25. Copy back program with 2-Kbyte page compatibility and random data input



1. Copy back program operation is allowed only within the same memory plane.
2. On the same plane, it is not allowed to operate a copy-back program from an odd address page (source page) to an even address page (target page) or from an even address page (source page) to an odd address page (target page). Therefore, the copy-back program is permitted only between odd address pages or even address pages.
3. Any command between 11h and 85h is not allowed, except 70h/F1h and FFh.

6.4 Reset

The Reset command reset the command interface and status register. If the Reset command is issued during any operation, the operation is aborted. If it is a program or erase operation that is being aborted, the contents of the memory locations being modified are no longer valid as the data is partially programmed or erased.

If the device has already been reset, then the new Reset command is not accepted.

The Ready/Busy signal goes Low for t_{BLBH4} after the Reset command is issued. The value of t_{BLBH4} depends on the operation that the device was performing when the command was issued. Refer to *Table 21: AC characteristics for operations* for the values.

6.5 Read status register

The device contains a status register that provides information on the current or previous program or erase operation. The various bits in the status register convey information and errors on the operation.

The status register is read by issuing the Read Status Register command. The status register information is present on the output data bus (I/O0-I/O7) on the falling edge of Chip Enable, or Read Enable, whichever occurs last. When several memories are connected in a system, the use of Chip Enable and Read Enable signals allows the system to poll each device separately, even when the Ready/Busy pins are common-wired. It is not necessary to toggle the Chip Enable or Read Enable signals to update the contents of the status register.

After the Read Status Register command has been issued, the device remains in read status register mode until another command is issued. Therefore, if a Read Status Register command is issued during a random read cycle a new read command must be issued to continue with a page read operation.

Refer to *Table 8* which summarizes status register bits and should be read in conjunction with the following text descriptions.

Table 8. Status register bits

I/O	Page program (SP/DP)	Block erase (SD/DP)	Page read	Definition
0	Pass/fail	Pass/fail	NA	Pass: ‘0’, Fail: ‘1’
1	Plane 0: pass/fail	Plane 0 Pass/fail	NA	Plane 0: Pass: ‘0’, Fail: ‘1’
2	Plane 1: pass/fail	Plane 1 Pass/fail	NA	Plane 1: Pass: ‘0’, Fail: ‘1’
3	NA	NA	NA	–
4	NA	NA	NA	–
5	Ready/busy	Ready/busy	Ready/busy	Busy: ‘0’; Ready:’1’
6	Ready/busy	Ready/busy	Ready/busy	Busy: ‘0’, Ready: ‘1’
7	Write protect	Write protect	Write protect	Protected: ‘0’, Not protected: ‘1’

6.5.1 Write protection bit (SR7)

The write protection bit can identify if the device is protected or not. If the write protection bit is set to ‘1’ the device is not protected and program or erase operations are allowed. If the write protection bit is set to ‘0’ the device is protected and program or erase operations are not allowed.

6.5.2 P/E/R controller bit (SR6)

Status register bit SR6 acts as a P/E/R controller bit, which indicates whether the P/E/R controller is active or inactive. When the P/E/R controller bit is set to ‘0’, the P/E/R controller is active (device is busy); when the bit is set to ‘1’, the P/E/R controller is inactive (device is ready).

6.5.3 Error bit (SR0)

The error bit identifies if any errors have been detected by the P/E/R controller. The error bit is set to ‘1’ when a program or erase operation has failed to write the correct data to the memory. If the error bit is set to ‘0’, the operation has completed successfully.

6.6 Read electronic signature

The device contains a manufacturer code and device code. The following three steps are required to read these codes:

1. One bus write cycle to issue the Read Electronic Signature command (90h)
2. One bus write cycle to input the address (00h)
3. Four bus read cycles to sequentially output the data (as shown in *Table 10: Electronic signature*).

Table 9. Device identifier codes

Device identifier cycle	Description
1st	Manufacturer code
2nd	Device identifier
3rd	Internal chip number, cell type, etc.
4th	Page size, block size, spare size organization
5th	Multiplane information

Table 10. Electronic signature

Root part number	Byte/word 1	Byte/word 2	Byte 3 (see *Table 11*)	Byte 4 (see *Table 12*)	Byte 5 (see *Table 13*)
	Manufacturer code	Device code			
NAND08GW3F2A	20h	D3h	10h	A6h	34h
NAND16GW3F2A	20h	D5h	51h	A6h	38h

Table 11. Electronic signature byte 3

I/O	Definition	Value	Description
I/O1-I/O0	Die/package	0 0 0 1 1 0 1 1	1 2 4 8
I/O3-I/O2	Cell type	0 0 0 1 1 0 1 1	2-level cell 4-level cell 8-level cell 16-level cell
I/O5-I/O4	Number of simultaneously programmed pages	0 0 0 1 1 0 1 1	1 2 4 8
I/O6	Interleaved programming between multiple devices	0 1	Not supported Supported
I/O7	Write cache	0 1	Not supported Supported

Table 12. Electronic signature byte 4

I/O	Definition	Value	Description
I/O1-I/O0	Page size (without spare area)	0 0 0 1 1 0 1 1	1 Kbyte 2 Kbytes 4 Kbytes 8 Kbytes
I/O2	Spare area size (byte/512 byte)	0 1	8 16
I/O7, I/O3	Serial access time	0 0 0 1 1 0 1 1	50 ns 30 ns 25 ns Reserved
I/O5-I/O4	Block size (without spare area)	0 0 0 1 1 0 1 1	64 Kbytes 128 Kbytes 256 Kbytes 512 Kbytes
I/O6	Organization	0 1	x8 x16

Table 13. Electronic signature byte 5

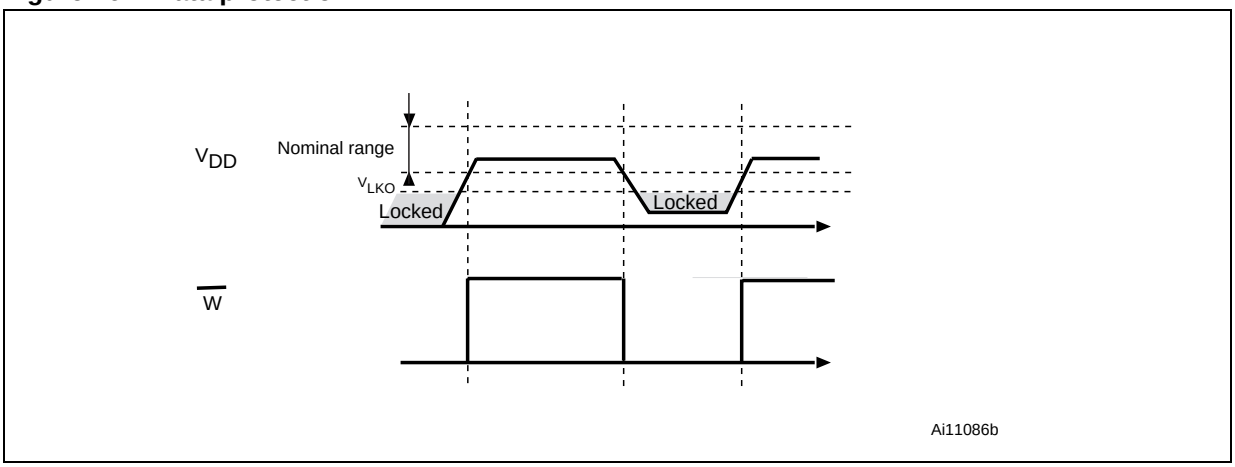
I/O	Definition	Value	Description
I/O1 - I/O0	Reserved	0 0	
I/O3 - I/O2	Plane number	0 0 0 1 1 0 1 1	1 plane 2 planes 4 planes 8 planes
I/O6 - I/O4	Plane size (without redundant area)	0 0 0 0 0 1 0 1 0 0 1 1 1 0 0 1 0 1 1 1 0 1 1 1	512 Mbits 1 Gbit 2 Gbits 4 Gbits 8 Gbits Reserved Reserved Reserved
I/O7	Reserved	0	

7 Data protection

The device has hardware features to protect against spurious program and erase operations. An internal voltage detector disables all functions whenever V_{DD} is below the V_{LKO} threshold. It is recommended to keep $\overline{WP}$ at V_{IL} during power-up and power-down.

In the V_{DD} range from V_{LKO} to the lower limit of nominal range, the $\overline{WP}$ pin should be kept Low (V_{IL}) to guarantee hardware protection during power transitions, as shown in *Figure 26*.

Figure 26. Data protection



8 Write protect operation

Erase and program operations are automatically reset when $\overline{WP}$ goes Low (t_{VLWH}= 100 ns). Erase and program operations are enabled and disabled as shown in *Figure 27*, *Figure 28*, *Figure 29*, and *Figure 30*.

If $\overline{WP}$ goes Low after the device has gone busy, the internal reset is executed and program/erase operation exits. The device becomes ready again after the internal reset sequence is executed. To avoid any corruption of stored data, $\overline{WP}$ must not go Low after the Confirm command.

Figure 27. Program enable waveform

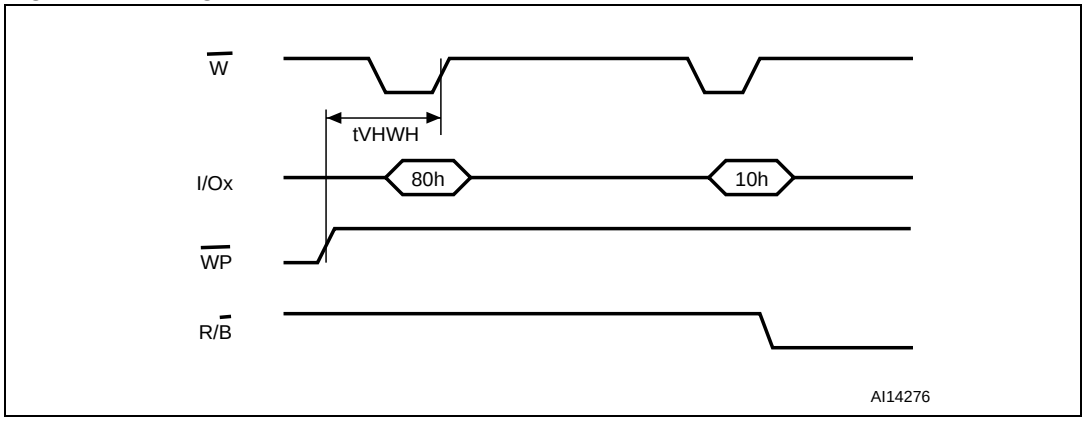


Figure 28. Program disable waveform

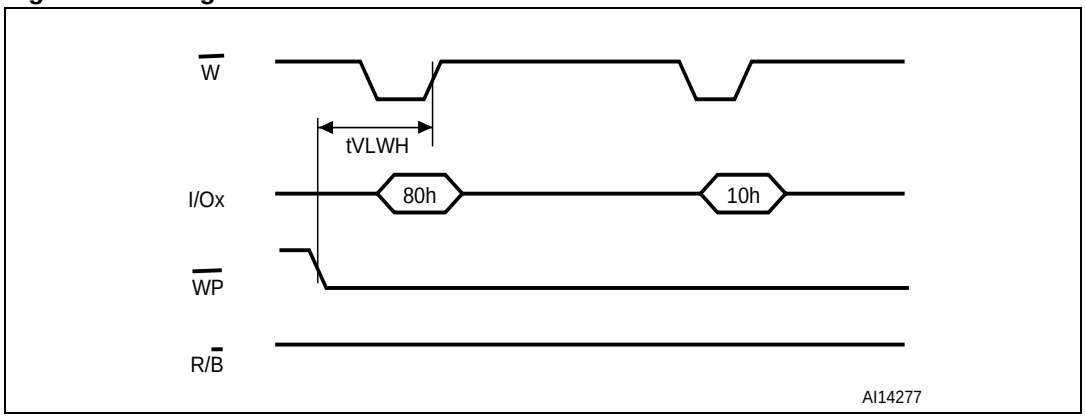


Figure 29. Erase enable waveform

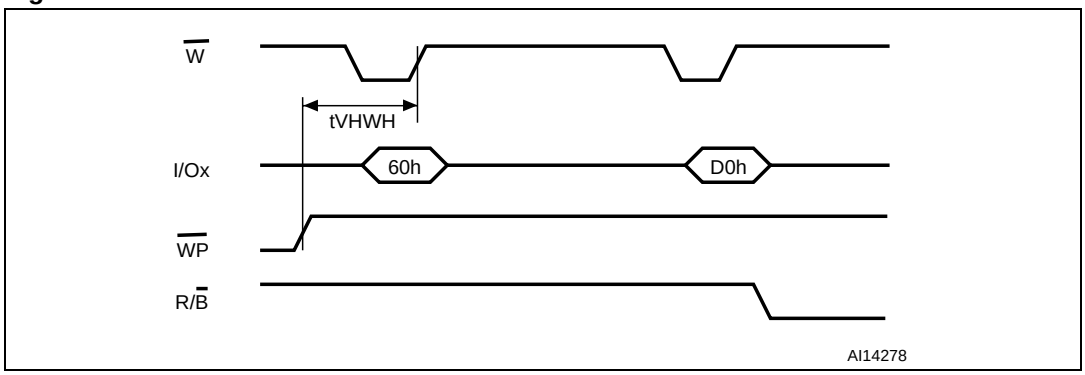
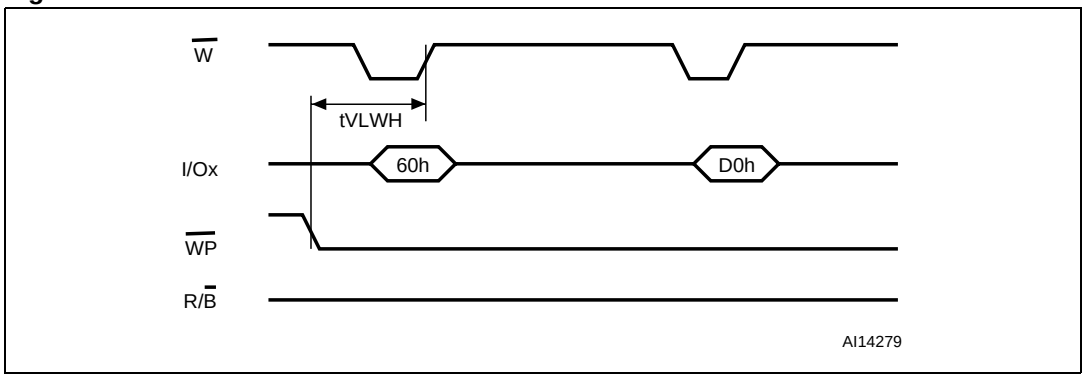


Figure 30. Erase disable waveform



9 Software algorithms

This section provides information on the software algorithms that Numonyx recommends implementing to manage the bad blocks and extend the lifetime of the NAND device.

NAND flash memories are programmed and erased by Fowler-Nordheim tunneling using high voltage. Exposing the device to high voltage for extended periods can cause the oxide layer to be damaged. For this reason, the number of program and erase cycles is limited (see *Table 15: Program and erase times and program erase endurance cycles* for value). To extend the number of program and erase cycles and to increase data retention, it is recommended to implement garbage collection and wear-leveling while the implementation of error correction code algorithms is mandatory.

To help integrate a NAND memory into an application, Numonyx can provide a full range of software solutions: file system, sector manager, drivers, and code management.

Contact the nearest Numonyx sales office or visit www.numonyx.com for more details.

9.1 Bad block management

Devices with bad blocks have the same quality level and the same AC and DC characteristics as devices where all the blocks are valid. A bad block does not affect the

performance of valid blocks because it is isolated from the bit line and common source line by a select transistor.

The devices are supplied with all the locations inside valid blocks erased (FFh). The bad block information is written prior to shipping. Any block, where the 1st and 6th bytes, in the spare area of the first page, does not contain FFh is a bad block.

The bad block information must be read before any erase is attempted as the bad block Information may be erased. For the system to be able to recognize the bad blocks based on the original information it is recommended to create a bad block table following the flowchart shown in *Figure 31: Bad block management flowchart.*

9.2 NAND flash memory failure modes

The NANDxxGW3F2A may contain bad blocks, where the reliability of blocks that contain one or more invalid bits is not guaranteed. Additional bad blocks may develop during the lifetime of the devices.

To implement a highly reliable system, all the possible failure modes must be considered:

- Program/erase failure

  in this case, the block has to be replaced by copying the data to a valid block. These additional bad blocks can be identified as attempts to program or erase them and give errors in the status register.

  Because the failure of a page program operation does not affect the data in other pages in the same block, the block can be replaced by re-programming the current data and copying the rest of the replaced block to an available valid block. The Copy Back Program command can be used to copy the data to a valid block. See *Figure 8: Random data input during sequential data input* for more details.

- Read failure

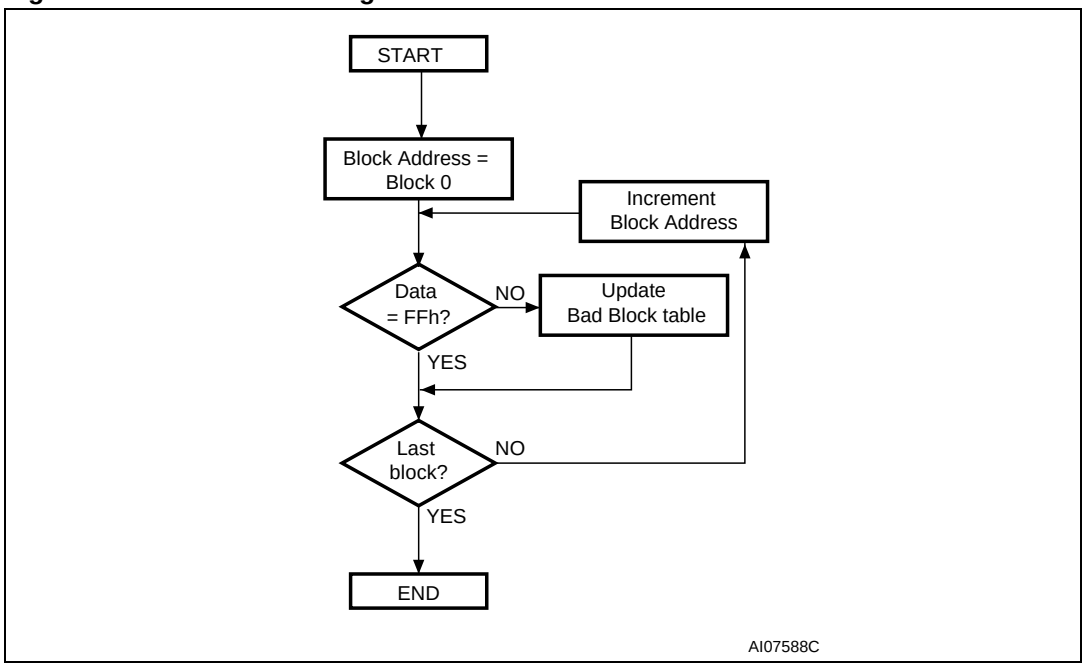
  in this case, ECC correction must be implemented. To efficiently use the memory space, it is recommended to recover single-bit errors in read by ECC, without replacing the whole block.

Refer to *Table 14* for the procedure to follow if an error occurs during an operation.

Table 14. Block failure

Operation	Procedure
Erase	Block replacement
Program	Block replacement or ECC (with 1 bit/528 bytes)
Read	ECC (with 1 bit/528 bytes)

Figure 31. Bad block management flowchart

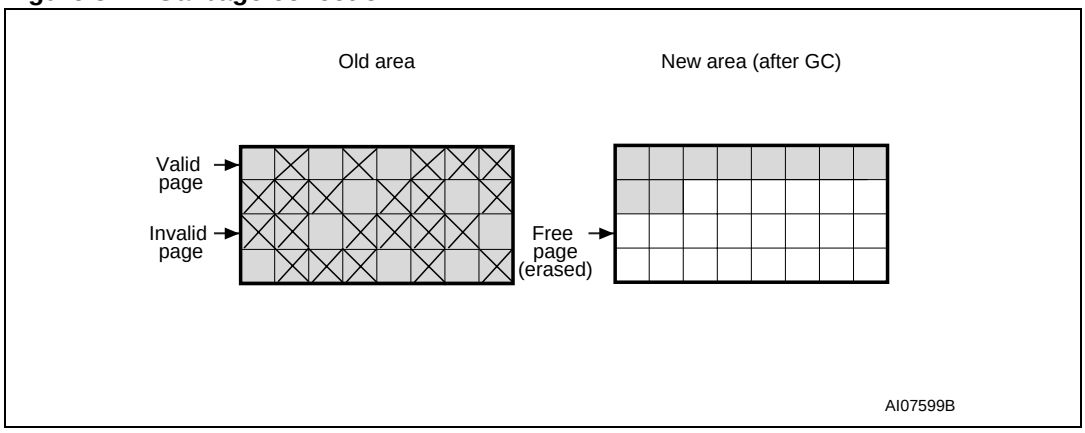


9.3 Garbage collection

When a data page needs to be modified, it is faster to write to the first available page and mark the previous page as invalid. After several updates it is necessary to remove invalid pages to free some memory space.

To free this memory space and allow further program operations, it is recommended to implement a garbage collection algorithm. In a garbage collection software the valid pages are copied into a free area and the block containing the invalid pages is erased (see *Figure 32*).

Figure 32. Garbage collection



9.4 Wear-leveling algorithm

For write-intensive applications, it is recommended to implement a wear-leveling algorithm to monitor and spread the number of write cycles per block.

In memories that do not use a wear-leveling algorithm, not all blocks get used at the same rate. The wear-leveling algorithm ensures that equal use is made of all the available write cycles for each block.

There are two wear-leveling levels:

1. First level wear-leveling, where new data is programmed to the free blocks that have had the fewest write cycles
2. Second level wear-leveling, where long-lived data is copied to another block so that the original block can be used for more frequently changed data.

The second level wear-leveling is triggered when the difference between the maximum and the minimum number of write cycles per block reaches a specific threshold.

9.5 Hardware simulation models

9.5.1 Behavioral simulation models

Denali software corporation models are platform-independent functional models designed to assist customers in performing entire system simulations (typical VHDL/Verilog). These models describe the logic behavior and timings of NAND flash devices, and, therefore, allow software to be developed before hardware.

9.5.2 IBIS simulations models

I/O buffer information specification (IBIS) models describe the behavior of the I/O buffers and electrical characteristics of flash devices.

These models provide information such as AC characteristics, rise/fall times, and package mechanical data, all of which are measured or simulated at voltage and temperature ranges wider than those allowed by target specifications.

IBIS models are used to simulate PCB connections and can be used to resolve compatibility issues when upgrading devices. They can be imported into SPICETOOLS.

10 Program and erase times and endurance cycles

Table 15 shows the program and erase times and the number of program/erase cycles per block.

Table 15. Program and erase times and program erase endurance cycles

Parameters	Min	Typ	Max	Unit
Page program time		500	700	µs
Block erase time		1.5	2	ms
Cache read busy time (t_{RCBSY})	–	3	t_{WHBH} (t_R)	µs
Program/erase cycles (per block (with ECC)	100,000			cycles
Data retention	10			years
Number of partial program cycles (NOP) within the same page (main array or spare array)			8	cycles

11 Maximum ratings

Stressing the device above the ratings listed in *Table 16: Absolute maximum ratings* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these or any other conditions above those indicated in the operating sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

Table 16. Absolute maximum ratings

Symbol	Parameter	Value		Unit
		Min	Max	
T_{BIAS}	Temperature under bias	– 50	125	°C
T_{STG}	Storage temperature	– 65	150	°C
V_{IO}(1)	Input or output voltage	– 0.6	4.6	V
V_{DD}	Supply voltage	– 0.6	4.6	V

1. Minimum voltage may undershoot to –2 V for less than 20 ns during transitions on input and I/O pins. Maximum voltage may overshoot to V_{DD} + 2 V for less than 20 ns during transitions on I/O pins.

12 DC and AC parameters

This section summarizes the operating and measurement conditions as well as the DC and AC characteristics of the device. The parameters in the following DC and AC characteristics tables are derived from tests performed under the measurement conditions summarized in *Table 17: Operating and AC measurement conditions*. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 17. Operating and AC measurement conditions

Parameter	Min	Max	Units
Supply voltage (V_{DD})	2.7	3.6	V
Ambient temperature (T_A)	–40	85	°C
Load capacitance (C_L) (1 TTL GATE and C_L)	50		pF
Input pulses voltages	0	V_{DD}	V
Input and output timing ref. voltages	1.5		V
Output circuit resistor R_{ref}	8.35		kΩ
Input rise and fall times	5		ns

Table 18. Capacitance(1)

Symbol	Parameter	Test condition	Typ	Max	Unit
C_{IN}	Input capacitance	V_{IN} = 0 V		10	pF
$C_{I/O}$	Input/output capacitance	V_{IL} = 0 V		10	pF

1. T_A = 25 °C, f = 1 MHz. C_{IN} and $C_{I/O}$ are not 100% tested.

Table 19. DC characteristics(1)

Symbol	Parameter		Test conditions	Min	Typ	Max	Unit
I_{DD1}	Operating current	Sequential read	t_{RLRL} minimum $\overline{E}$ = V_{IL}, I_{OUT} = 0 mA	–	15	30	mA
I_{DD2}		Program	–	–	15	30	mA
I_{DD3}		Erase	–	–	15	30	mA
I_{DD4}	Standby current (TTL)		E = V_{IH}, $\overline{WP}$ = 0/V_{DD}			1	mA
I_{DD5}	Standby current (CMOS)		$\overline{E}$ = V_{DD}-0.2, $\overline{WP}$ = 0/V_{DD}	–	10	50	µA
I_{LI}	Input leakage current		V_{IN} = 0 to 3.6 V	–	–	±10	µA
I_{LO}	Output leakage current		V_{OUT} = 0 to 3.6 V	–	–	±10	µA
V_{IH}	Input high voltage		–	0.8 x V_{DD}	–	V_{DD} + 0.3	V
V_{IL}	Input low voltage		–	-0.3	–	0.2 x V_{DD}	V
V_{OH}	Output high voltage level		I_{OH} = -400 µA	2.4	–	–	V
V_{OL}	Output low voltage level		I_{OL} = 2.1 mA	–	–	0.4	V
I_{OL} ($R\overline{B}$)	Output low current ($R\overline{B}$)		V_{OL} = 0.4 V	8	10		mA
V_{LKO}	V_{DD} supply voltage (erase and program lockout)		–	–	–	2	V

1. Standby and leakage currents refer to a single die device. For a multiple die device, their value must be multiplied for the number of dice of the stacked device, while the active power consumption depends on the number of dice concurrently executing different operations.

Table 20. AC characteristics for command, address, data input

Symbol	Alt. symbol	Parameter			Value	Unit
t_{ALLWH}	t_{ALS}	Address Latch Low to Write Enable High	AL setup time	Min	12	ns
t_{ALHWH}		Address Latch High to Write Enable High				
t_{CLHWH}	t_{CLS}	Command Latch High to Write Enable High	CL setup time	Min	12	ns
t_{CLLWH}		Command Latch Low to Write Enable High				
t_{DVWH}	t_{DS}	Data Valid to Write Enable High	Data setup time	Min	12	ns
t_{ELWH}	t_{CS}	Chip Enable Low to Write Enable High	$\overline{E}$ setup time	Min	20	ns
t_{WHALH}	t_{ALH}	Write Enable High to Address Latch High	AL hold time	Min	5	ns
t_{WHALL}		Write Enable High to Address Latch Low				
t_{WHCLH}	t_{CLH}	Write Enable High to Command Latch High	CL hold time	Min	5	ns
t_{WHCLL}		Write Enable High to Command Latch Low				
t_{WHDX}	t_{DH}	Write Enable High to Data Transition	Data hold time	Min	5	ns
t_{WHEH}	t_{CH}	Write Enable High to Chip Enable High	$\overline{E}$ hold time	Min	5	ns
t_{WHWL}	t_{WH}	Write Enable High to Write Enable Low	$\overline{W}$ High hold time	Min	10	ns
t_{WLWH}	t_{WP}	Write Enable Low to Write Enable High	$\overline{W}$ pulse width	Min	12	ns
t_{WLWL}	t_{WC}	Write Enable Low to Write Enable Low	Write cycle time	Min	25	ns

Table 21. AC characteristics for operations

Symbol	Alt. symbol	Parameter		Value			Unit
				Min	Typ	Max	
t_{ALLRL1}	t_{AR}	Address Latch Low to Read Enable Low	Read electronic signature	10			ns
t_{ALLRL2}			Read cycle	10			ns
t_{BHRL}	t_{RR}	Ready/Busy High to Read Enable Low		20			ns
t_{BLBH1}	t_{RBSY}	Ready/Busy Low to Ready/Busy High	Read busy time			25	µs
t_{BLBH2}	t_{PROG}		Program busy time		500	700	µs
t_{BLBH3}	t_{BERS}		Erase busy time		1.5	2	ms
t_{BLBH4}	t_{RST}	Reset Busy time, during ready				5	µs
		Reset Busy time, during read				20	µs
		Reset Busy time, during program				20	µs
		Reset Busy time, during erase				50	µs
t_{BLBH5}	t_{CBSY}	Dummy Busy time for multiplane operations			1	2	µs
t_{CLLRL}	t_{CLR}	Command Latch Low to Read Enable Low		10			ns
t_{DZRL}	t_{IR}	Data Hi-Z to Read Enable Low		0			ns
t_{EHQZ}	t_{CHZ}	Chip Enable High to Output Hi-Z				50	ns
t_{ELQV}	t_{CEA}	Chip Enable Low to Output Valid				25	ns
t_{RHRL}	t_{REH}	Read Enable High to Read Enable Low	Read Enable High hold time	10			ns
t_{EHQX}	t_{COH}	Chip Enable High to Output Hold		15			ns
t_{RHQX}	t_{RHOH}	Read Enable High to Output Hold		15			ns
t_{RLQX}	t_{RLOH}	Read Enable Low to Output Hold (EDO mode)		5			ns
t_{RHQZ}	t_{RHZ}	Read Enable High to Output Hi-Z				100	ns
t_{RLRH}	t_{RP}	Read Enable Low to Read Enable High	Read Enable pulse width	12			ns
t_{RLRL}	t_{RC}	Read Enable Low to Read Enable Low	Read cycle time	25			ns
t_{RLQV}	t_{REA}	Read Enable Low to Output Valid	Read Enable access time			20	ns
			Read ES access time(1)				
t_{WHBH}	t_{R}	Write Enable High to Ready/Busy High	Read busy time			25	µs
t_{WHBL}	t_{WB}	Write Enable High to Ready/Busy Low				100	ns
t_{WHRL}	t_{WHR}	Write Enable High to Read Enable Low		80			ns
t_{WHWH}(2)	t_{ADL}	Last Address latched on Data Loading time during program operations		70			ns
t_{VHWH}(3)	t_{WW}	Write protection time		100			ns
t_{VLWH}(3)				100			ns

1. ES = electronic signature.
2. t_{WHWH} is the delay from Write Enable rising edge during the final address cycle to Write Enable rising edge during the first data cycle.
3. $\overline{WP}$ High to $\overline{W}$ High during program/erase enable operations or $\overline{WP}$ Low to $\overline{W}$ High during program/erase disable operations.

Figure 33. Command latch AC waveforms

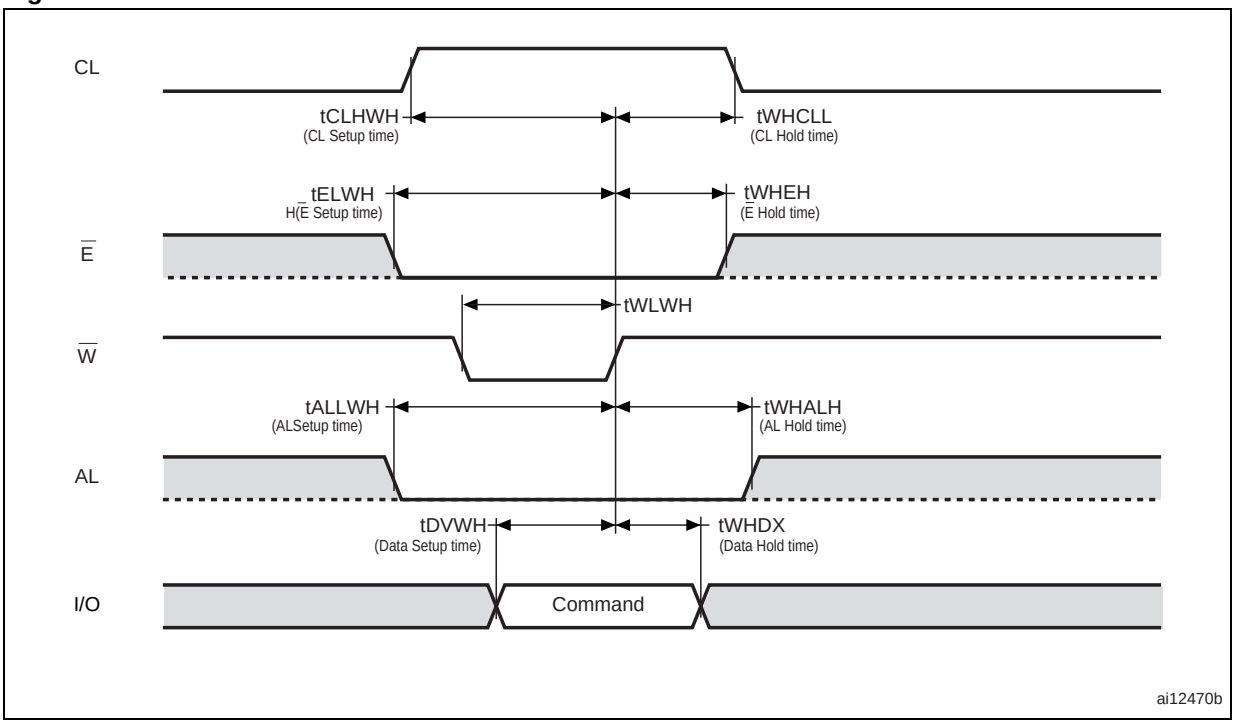


Figure 34. Address latch AC waveforms

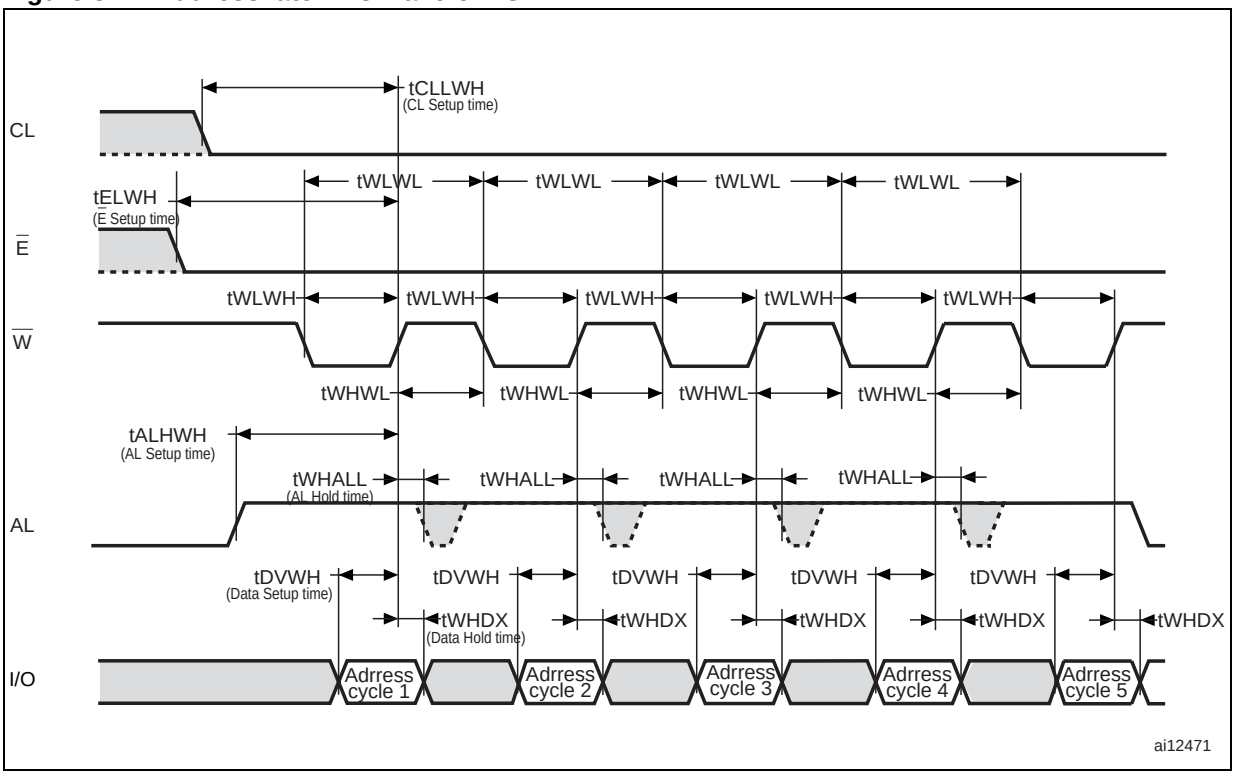


Figure 35. Data input latch AC waveforms

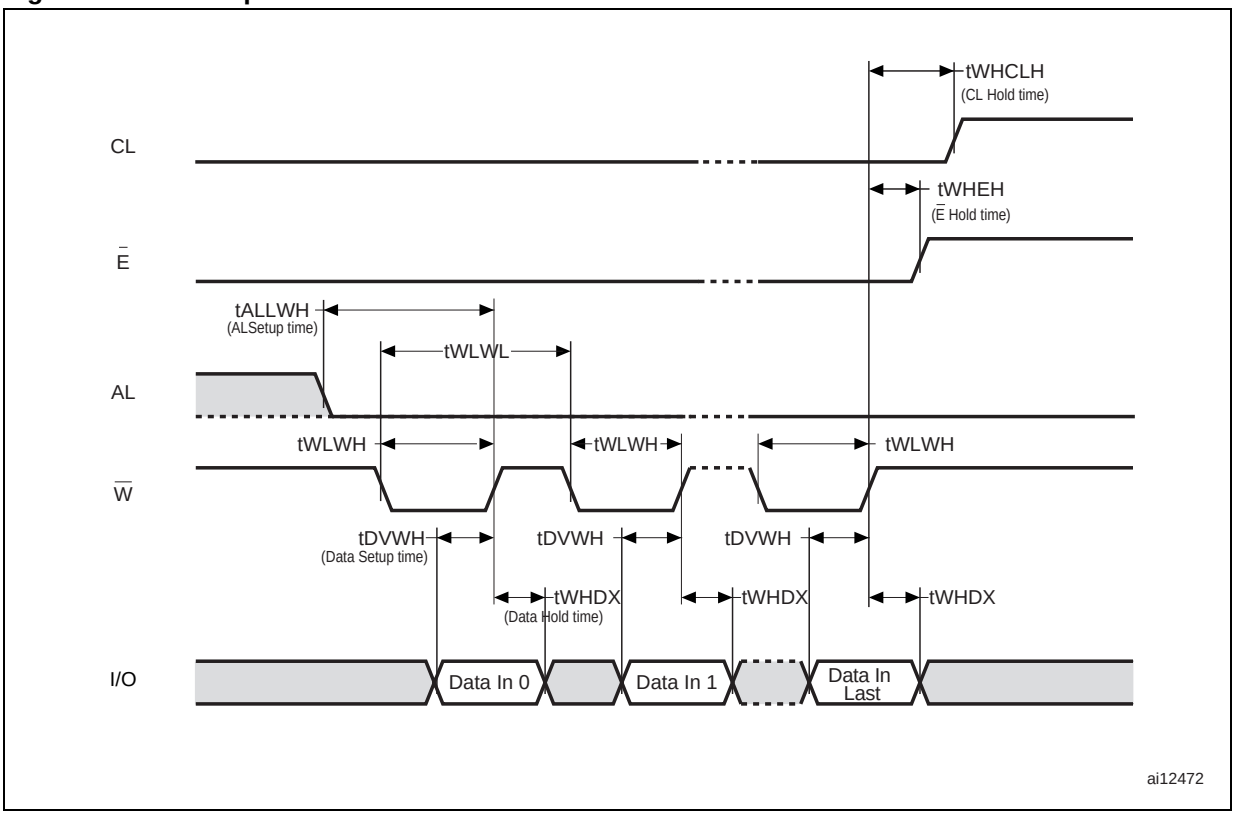
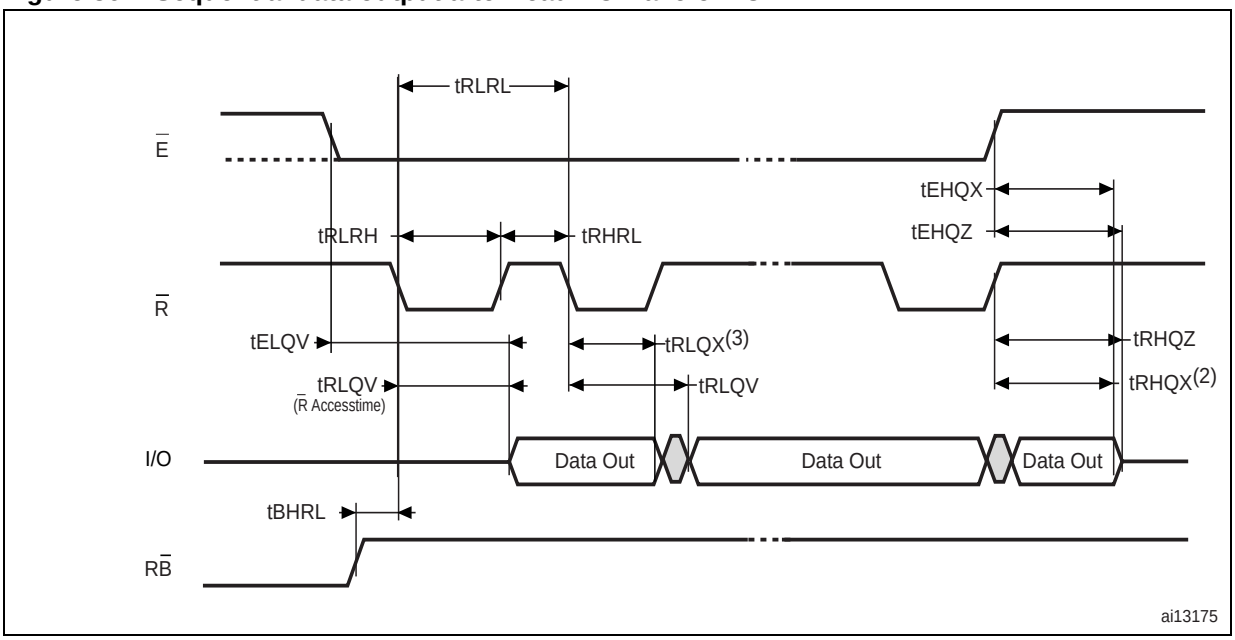


Figure 36. Sequential data output after read AC waveforms



1. CL and AL are Low, V_{IL}, and $\overline{W}$ is High, V_{IH}.
2. t_{RHQX} is applicable for frequencies lower than 33 MHz (for instance, t_{RLRL} lower than 30 ns).
3. t_{RLQX} is applicable for frequencies higher than 33 MHz (for instance, t_{RLRL} lower than 30 ns).

Figure 37. Read status register AC waveforms

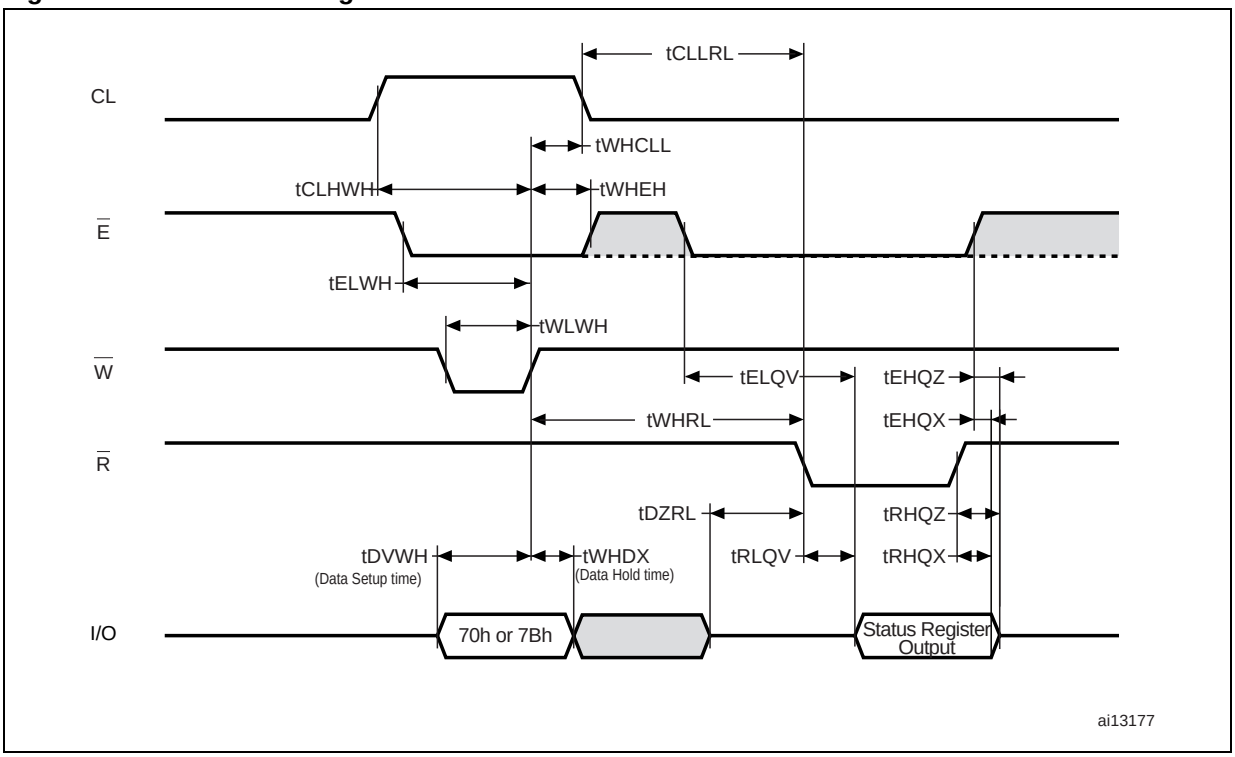
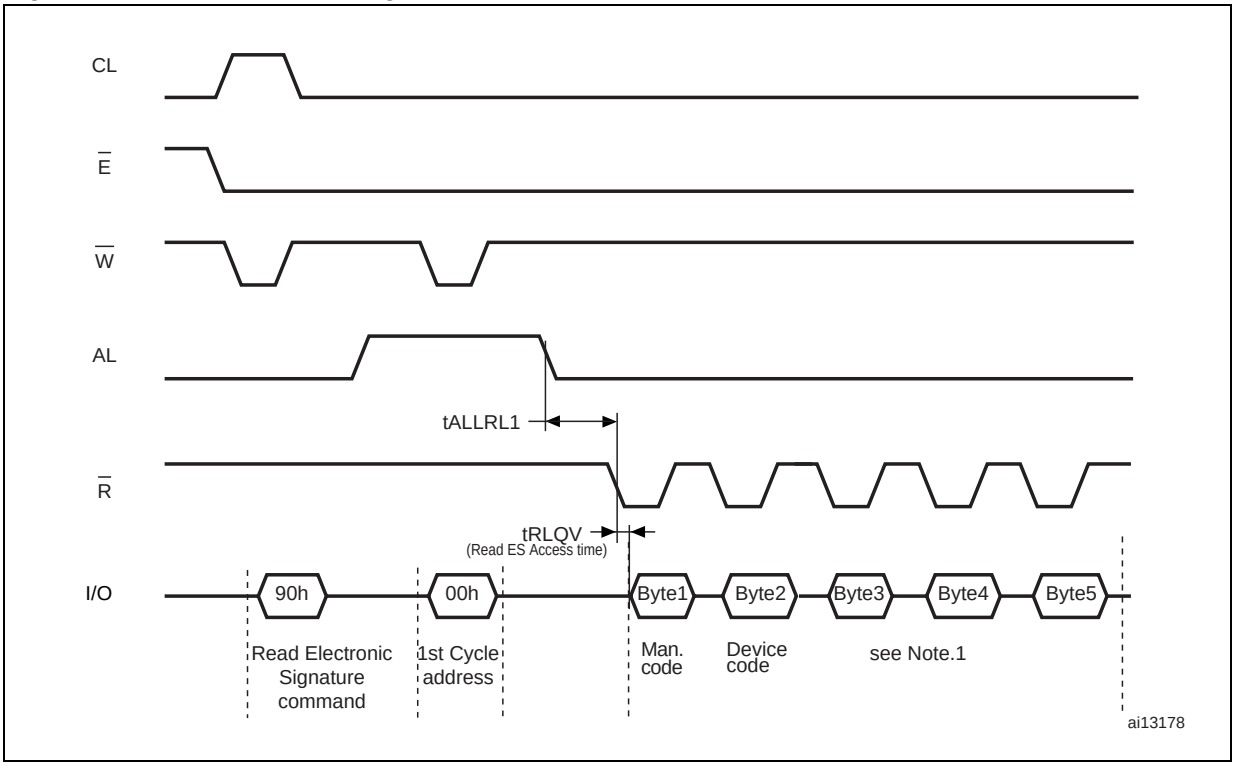


Figure 38. Read electronic signature AC waveforms



1. Refer to *Table 10* for the values of the manufacturer and device codes, and to *Table 11*, *Table 12*, and *Table 13* for the information contained in byte 3, byte 4, and byte 5.

Figure 39. Page read operation AC waveforms

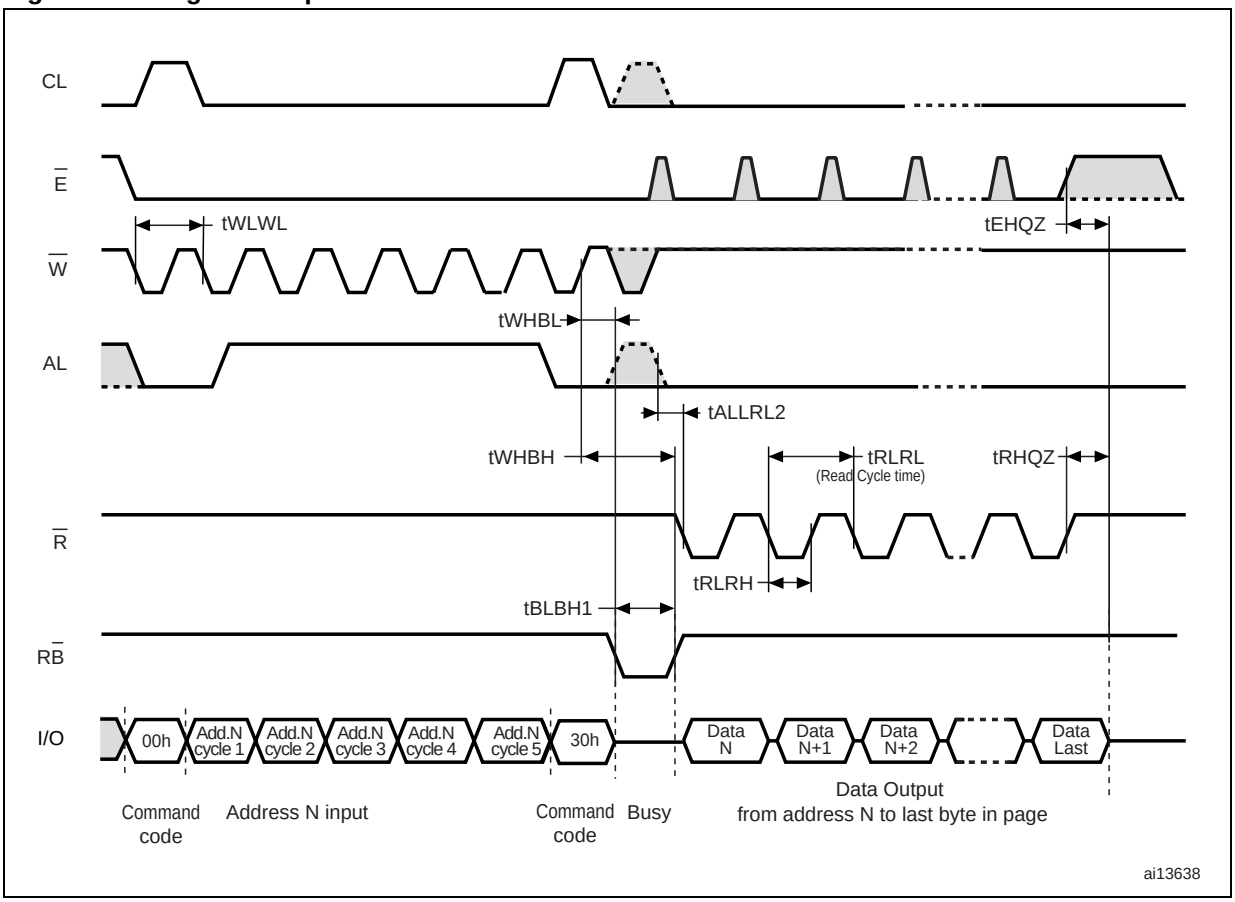


Figure 40. Page program AC waveforms

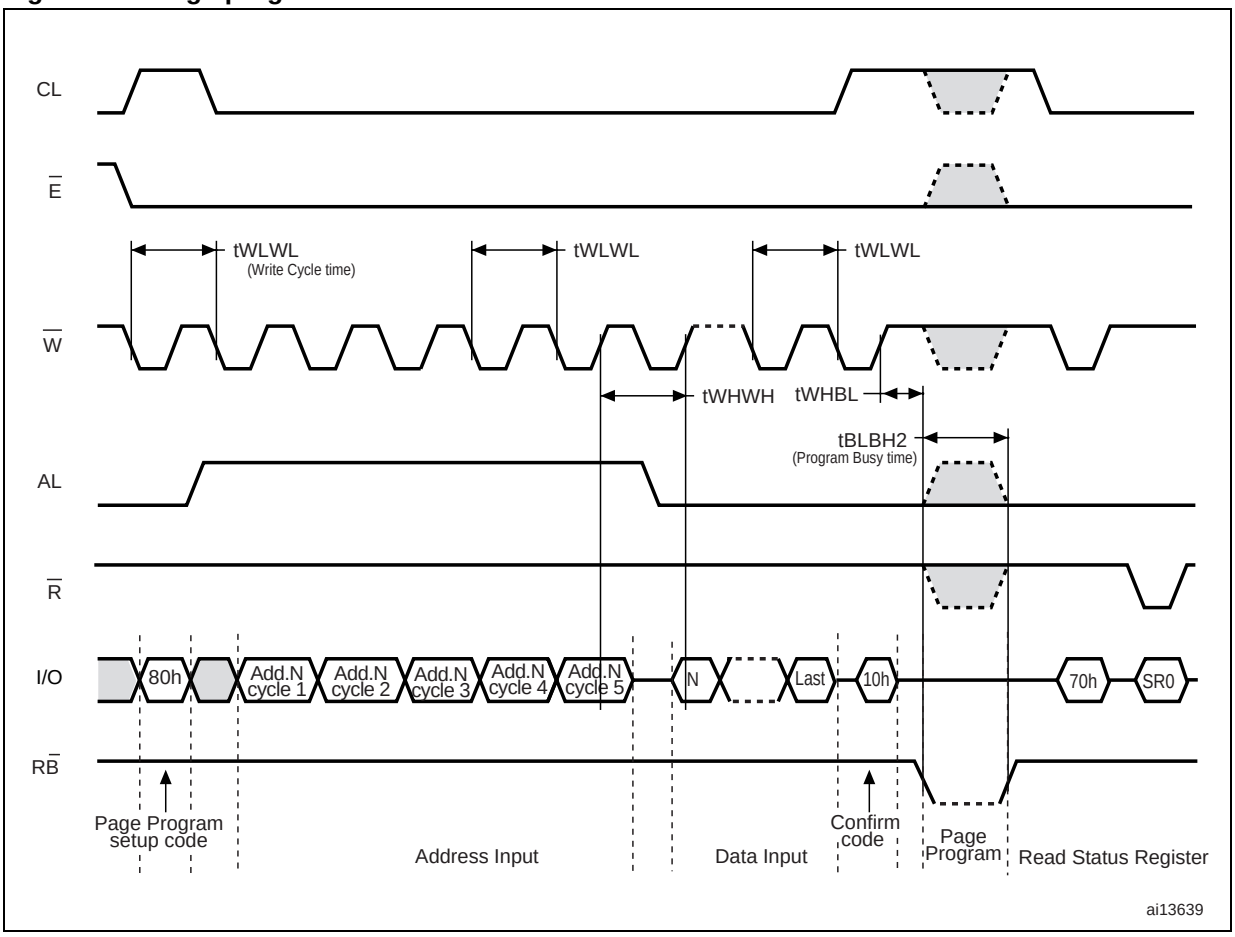


Figure 41. Block erase AC waveforms

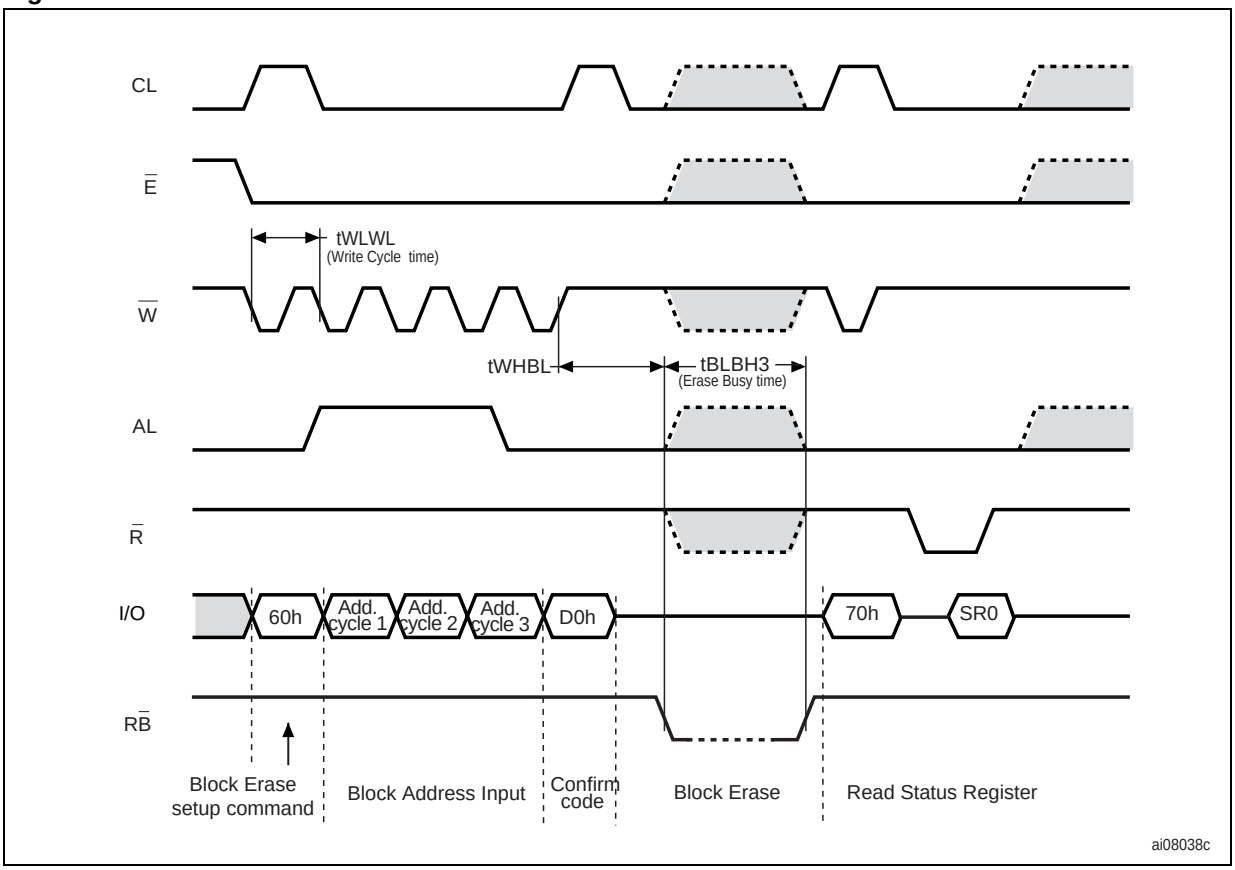
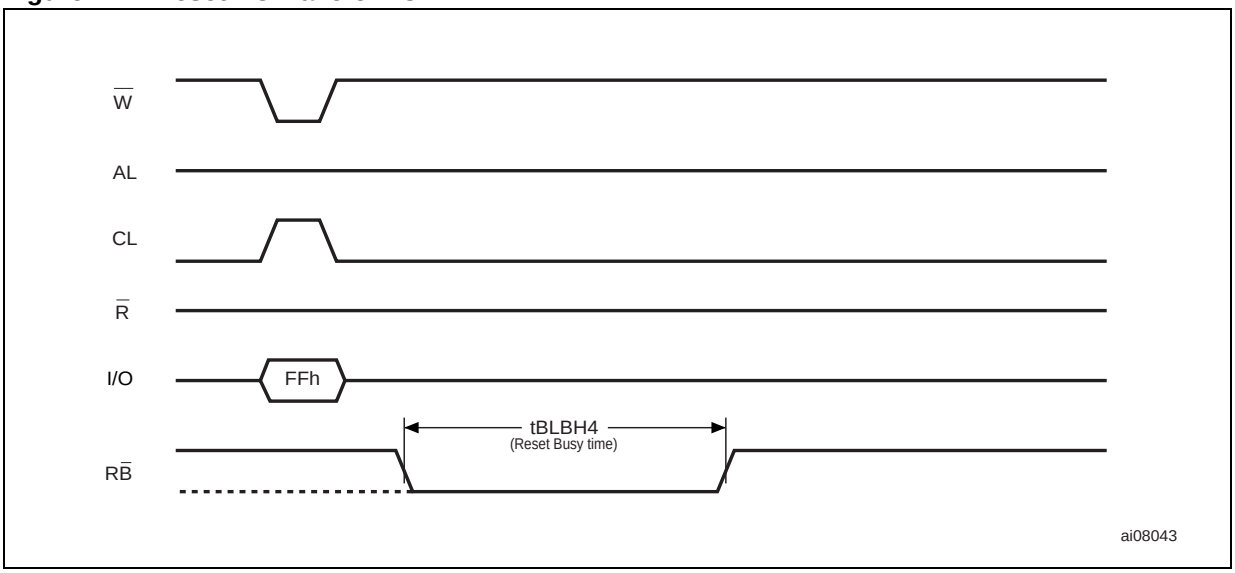


Figure 42. Reset AC waveforms



12.1 Ready/Busy signal electrical characteristics

Figure 44, *Figure 43* and *Figure 45* show the electrical characteristics for the Ready/Busy signal. The value required for the resistor R_P can be calculated using the following equation:

$$R_P min = \frac{(V_{DDmax} - V_{OLmax})}{I_{OL} + I_L}$$

So,

$$R_P min = \frac{3.2V}{8mA + I_L}$$

where I_L is the sum of the input currents of all the devices tied to the Ready/Busy signal. R_P max is determined by the maximum value of t_r.

Figure 43. Ready/Busy AC waveform

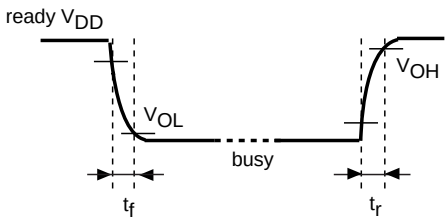


Figure 44. Ready/Busy load circuit

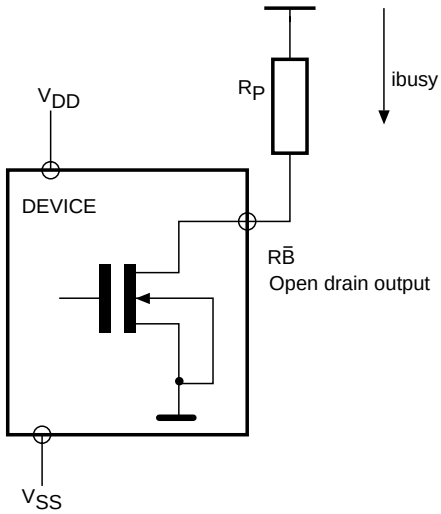
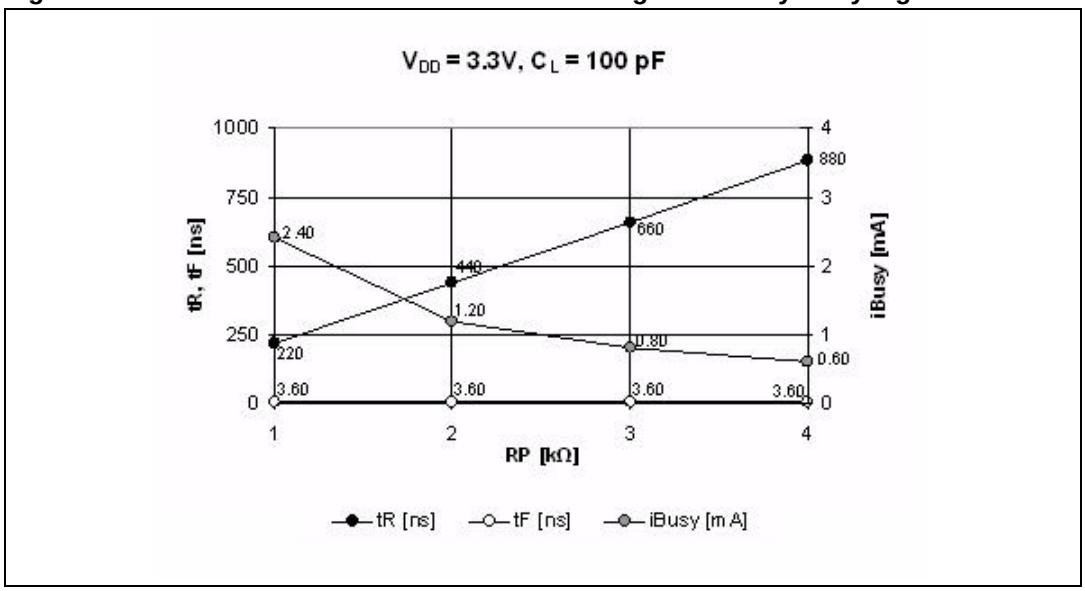


Figure 45. Resistor value versus waveform timings for Ready/Busy signal



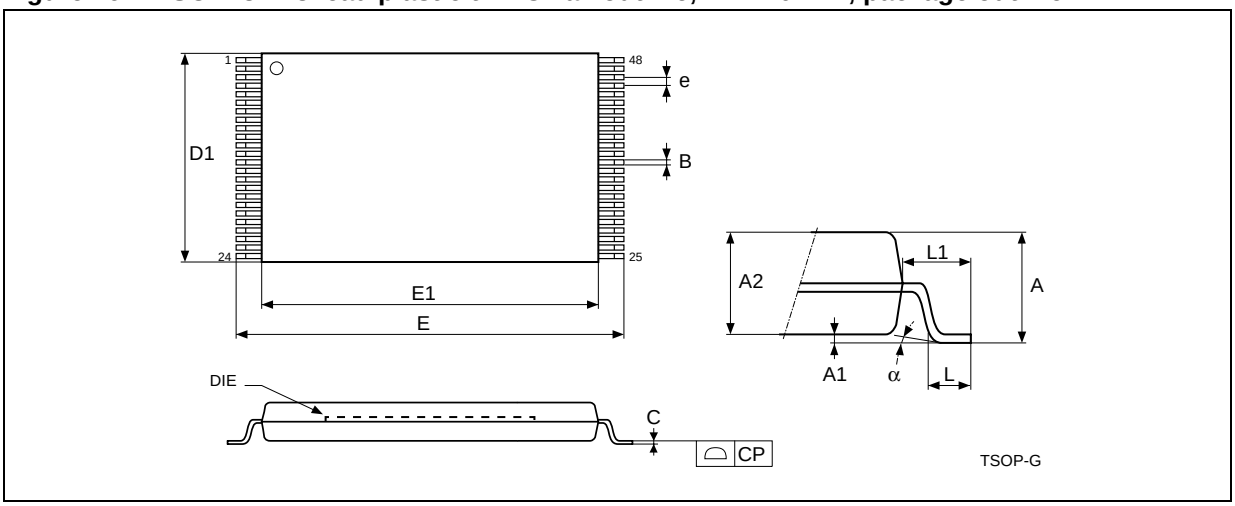
1. T = 25 °C.

13 Package mechanical

To meet environmental requirements, Numonyx offers these devices in RoHS compliant packages, which have a lead-free second-level interconnect. The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

RoHS compliant specifications are available at www.numonyx.com.

Figure 46. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package outline



1. Drawing is not to scale.

Table 22. TSOP48 - 48 lead plastic thin small outline, 12 x 20 mm, package mechanical data

Symbol	Millimeters			Inches		
	Typ	Min	Max	Typ	Min	Max
A			1.20			0.047
A1	0.10	0.05	0.15	0.004	0.002	0.006
A2	1.00	0.95	1.05	0.039	0.037	0.041
B	0.22	0.17	0.27	0.009	0.007	0.011
C		0.10	0.21		0.004	0.008
CP			0.08			0.003
D1	12.00	11.90	12.10	0.472	0.468	0.476
E	20.00	19.80	20.20	0.787	0.779	0.795
E1	18.40	18.30	18.50	0.724	0.720	0.728
e	0.50	–	–	0.020	–	
L	0.60	0.50	0.70	0.024	0.020	0.028
L1	0.80			0.031		
a	3°	0°	5°	3°	0°	5°

14 Ordering information

Table 23. Ordering information scheme

Example: NAND08G W 3 F 2 A N 6 E

Device type

NAND flash memory

Density

08G = 8 Gbits

16G = 16 Gbits

Operating voltage

W = V_{DD} = 2.7 to 3.6 V

Bus width

3 = x8

Family identifier

F = 4 Kbyte-page SLC

Device options

2 = Chip Enable ‘don't care’ enabled

Product version

A = first version

Package

N = TSOP48 12 x 20 mm

Temperature range

6 = –40 to 85 °C

Option

E = RoHS compliant package, standard packing

F = RoHS compliant package, tape and reel packing

Note: Not all combinations are necessarily available. For a list of available devices or for further information on any aspect of these products, please contact your nearest Numonyx sales office.

15 Revision history

Table 24. Document revision history

Date	Revision	Changes
06-Aug-2008	1	Initial release.
30-Oct-2008	2	Document status promoted from target specification to preliminary data. Added information about the OTP area security feature.
24-Sep-2009	3	Added note 1 below *Table 19: DC characteristics*. References to ECOPACK removed and replaced by RoHS compliance. Modified: random access value on the cover page and in *Table 1: Device summary*, *Figure 43: Ready/Busy AC waveform* and *Figure 45: Resistor value versus waveform timings for Ready/Busy signal*. Minor text changes.
07-Oct-2009	4	Modified *Section 9.1: Bad block management*.
19-Nov-2009	5	Further modifications to *Section 9.1: Bad block management*. Modified the value of the single and multiplane page program operation time throughout the document.

Please Read Carefully: