Ordering number : ENA1535A

LC87F0A08A

ON Semiconductor®

http://onsemi.com

CMOS LSI

8-bit Microcontroller

8K-byte Flash ROM / 256-byte RAM / 36-pin

Overview

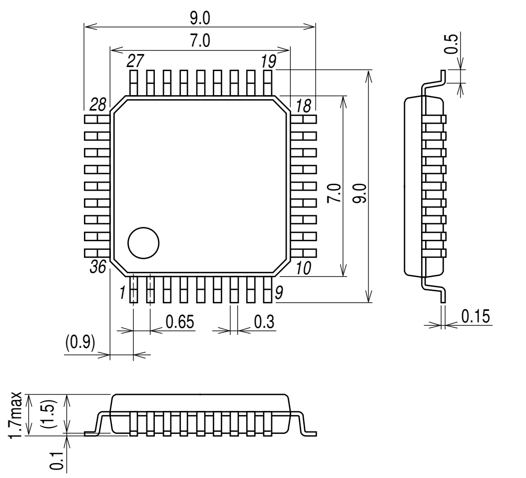
The LC87F0A08A is an 8-bit microcontroller that, centered around a CPU running at a minimum bus cycle time of 12ns, integrates on a single chip a number of hardware features such as 8K-byte flash ROM, 256-byte RAM, an on-chip debugger, a sophisticated 16-bit timer/counter, a 16-bit timer/counter, a 16-bit timer with a prescaler, a base timer serving as a realtime clock, an asynchronous/synchronous SIO interface, a 12-bit 8-channel AD converter with 12-/8-bit resolution selector, a 20× amplifier, constant-voltage detect interrupt, a comparator, a system clock frequency divider, an internal reset circuit, and a 16-source 9-vector interrupt feature.

Features

■Flash ROM
- 8192 × 8 bits
- Capable of on-board programming
  with a wide range of supply voltage 2.7 to 5.5V
- Block-erasable in 128-byte units
- Writes data in 2-byte units

■RAM
- 256 × 9 bits

■Package Form
- QFP36 (7×7): Lead-free and halogen-free type



QFP36(7X7)

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ORDERING INFORMATION

See detailed ordering and shipping information on page 24 of this data sheet.

■Minimum Bus Cycle Time
- 125ns (8MHz at V_{DD}=2.5V to 5.5V)
- 250ns (4MHz at V_{DD}=2.5V to 5.5V)

Note: The bus cycle time here refers to the ROM read speed.

■Minimum Instruction Cycle Time (tCYC)
- 375ns (8MHz V_{DD}=2.5V to 5.5V)
- 750ns (4MHz V_{DD}=2.5V to 5.5V)

■Ports
- Normal withstand voltage I/O ports whose I/O direction specifiable in 1-bit units: 28 (P0n, P1n, P2n, P30 to P32, P70)
- Oscillation/input dedicated ports: 2 (CF1/XT1, CF2/XT2)
- External reset pins: 1 ($\overline{RES}$)
- Power supply pins: 4 (V_{SS}1, AV_{SS}, V_{DD}1, V_{DD}2)
- Reference voltage outputs: 1 (VREF)

■Timers
- Timer 0: 16-bit timer/counter with a capture register.
  - Mode 0: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) × 2 channels
  - Mode 1: 8-bit timer with an 8-bit programmable prescaler (with an 8-bit capture register) + 8-bit counter (with an 8-bit capture register)
  - Mode 2: 16-bit timer with an 8-bit programmable prescaler (with a 16-bit capture register)
  - Mode 3: 16-bit counter (with a 16-bit capture register)
- Timer 1: 16-bit timer/counter that supports PWM/toggle outputs
  - Mode 0: 8-bit timer with an 8-bit prescaler (with toggle outputs) + 8-bit timer/counter with an 8-bit prescaler (with toggle outputs)
  - Mode 1: 8-bit PWM with an 8-bit prescaler × 2 channels
  - Mode 2: 16-bit timer/counter with an 8-bit prescaler (with toggle outputs) (toggle outputs also possible from lower-order 8 bits)
  - Mode 3: 16-bit timer with an 8-bit prescaler (with toggle outputs) (lower-order 8 bits may be used as PWM outputs)
- Timer A: 16-bit timer
  - Mode 0: 8-bit timer with an 8-bit programmable prescaler × 2 channels
  - Mode 1: 16-bit timer with an 8-bit programmable prescaler
- Base timer
  1) The input clock is selectable from the subclock (32.768kHz crystal oscillation), low-speed RC oscillator clock, system clock, and timer 0 prescaler output.
     (Release of the X'tal HOLD mode is enabled when the subclock or low-speed RC oscillator clock is selected.)
  2) Provided with an 8-bit programmable prescaler.
  3) Interrupts programmable in 5 different time schemes.

■SIO
- SIO1: 8-bit asynchronous/synchronous serial interface
  - Mode 0: Synchronous 8-bit serial I/O (2- or 3-wire configuration, 2 to 512 tCYC transfer clocks)
  - Mode 1: Asynchronous serial I/O (half-duplex, 8 data bits, 1 stop bit, 8 to 2048 tCYC baudrates)
  - Mode 2: Bus mode 1 (start bit, 8 data bits, 2 to 512 tCYC transfer clocks)
  - Mode 3: Bus mode 2 (start detect, 8 data bits, stop detect)

■AD Converter
- AD converter input port with a 20× operational amplifier (1 channel)
- AD converter input ports (8 channels)

  12/8 bits AD converter resolution selectable

■Constant Voltage Detection Interrupt (CVD) Function
1) Detects V_{DD} voltage fluctuations and generates an interrupt request.
2) The CVD detection level can be selected from 12 levels (2.6V, 2.8V, 3.0V, 3.2V, 3.4V, 3.6V, 3.8V, 4.0V, 4.2V, 4.4V, 4.6V, and 4.8V) through a register.

■Comparator
Comparator input pin (1 channel)
Comparator output pin (1 channel)
Comparator output set high when (comparator input level) < 1.22V
Comparator output set low when (comparator input level) > 1.22V

■Clock Output Function
- Generates clocks with a clock rate of 1/1, 1/2, 1/4, 1/8, 1/16, 1/32, or 1/64 of the source oscillation clock that is selected as the system clock.

■Watchdog Timer
- Generates an internal reset on an overflow occurring in the timer running on the low-speed RC oscillator clock (approx. 30kHz) or subclock.
- Operating mode at standby is selectable from 3 modes
  (continue counting/suspend operation/suspend counting with the count value retained)

■Interrupts
- 16 sources, 9 vectors
  1) Provides three levels (low (L), high (H), and highest (X)) of multiplex interrupt control. Any interrupt requests of the level equal to or lower than the current interrupt are not accepted.
  2) When interrupt requests to two or more vector addresses occur at the same time, the interrupt of the highest level takes precedence over the other interrupts. For interrupts of the same level, the interrupt into the smallest vector address is given priority.

No.	Vector Address	Level	Interrupt Source
1	00003H	X or L	INT0/CVD
2	0000BH	X or L	INT1
3	00013H	H or L	INT2/T0L/INT4/TAL
4	0001BH	H or L	INT3/BT
5	00023H	H or L	T0H/TAH
6	0002BH	H or L	T1L/T1H
7	00033H	H or L	
8	0003BH	H or L	SIO1
9	00043H	H or L	ADC
10	0004BH	H or L	P0

- Priority levels X > H > L
- When interrupts of the same level occur at the same time, an interrupt with a smaller vector address is given priority.

■Subroutine Stack Levels: Up to 128levels (the stack is allocated in RAM.)

■High-speed Multiplication/Division Instructions
- 16 bits × 8 bits (5 tCYC execution time)
- 24 bits × 16 bits (12 tCYC execution time)
- 16 bits ÷ 8 bits (8 tCYC execution time)
- 24 bits ÷ 16 bits (12 tCYC execution time)

■Oscillation Circuits
- Internal oscillation circuits
  1) Low-speed RC oscillation circuit: For system clock (approx.30kHz)
  2) Medium-speed RC oscillation circuit: For system clock (1MHz)
  3) Hi-speed RC oscillation circuit: For system clock (8MHz)

■System Clock Divider Function
- Can run on low consumption current.
- Minimum instruction cycle selectable from 375ns, 750ns, 1.5µs, 3.0µs, 6.0µs, 12.0µs, 24.0µs, 48.0µs, and 96.0µs (at 8MHz main clock)

■Internal Reset Circuit

- Power-on reset (POR) function
  1) POR reset is generated only at power-on time.
  2) The POR release level can be selected from 8 levels (1.67V, 1.97V, 2.07V, 2.37V, 2.57V, 2.87V, 3.86V, and 4.35V) through option configuration.
- Low-voltage detection reset (LVD) function
  1) LVD and POR functions are combined to generate resets when power is turned on and when power voltage falls below a certain level.
  2) The use/disuse of the LVD function and the low voltage threshold level can be selected from 7 levels (1.91V, 2.01V, 2.31V, 2.51V, 2.81V, 3.79V and 4.28V). through option configuration.

■Standby Function

- HALT mode: Halts instruction execution while allowing the peripheral circuits to continue operation.
  1) Oscillation is not halted automatically.
  2) There are three ways of resetting the HALT mode.
     (1) Setting the reset pin to the low level
     (2) Having the watchdog timer or LVD function generate a reset
     (3) Having an interrupt generated
- HOLD mode: Suspends instruction execution and the operation of the peripheral circuits.
  1) The CF, RC and crystal oscillators automatically stop operation.
     Note: The low-speed RC oscillator is controlled directly by the watchdog timer; its oscillation in the standby mode is also controlled by the watchdog timer.
  2) There are five ways of resetting the HOLD mode:
     (1) Setting the reset pin to the lower level
     (2) Having the watchdog timer or LVD function generate a reset
     (3) Having an interrupt source established at one of the INT0, INT1, INT2 and INT4 pins
         * INT0 and INT1 can be used in the level sense mode only.
     (4) Having an interrupt source established at port 0.
     (5) Having an interrupt source established in the CVD circuit
- X'tal HOLD mode: Suspends instruction execution and the operation of the peripheral circuits except the base timer. (when X’tal oscillation or low-speed RC oscillation is selected).
  1) The CF, low-speed, and medium-speed RC oscillators automatically stop operation.
     Note: The low-speed RC oscillator is controlled directly by the watchdog timer; its oscillation in the standby mode is also controlled by the watchdog timer.
     Note: If the base timer is run with low-speed RC oscillation selected as the base timer input clock source and the X’tal HOLD mode is entered, the low-speed RC oscillator retains the state that is established when the X’tal HOLD mode is entered.
  2) The state of crystal oscillation established when the X'tal HOLD mode is entered is retained.
  3) There are six ways of resetting the X'tal HOLD mode.
     (1) Setting the reset pin to the low level
     (2) Having the watchdog timer or LVD function generate a reset
     (3) Having an interrupt source established at one of the INT0, INT1, INT2, and INT4 pins
         * INT0 and INT1 can be used in the level sense mode only.
     (4) Having an interrupt source established at port 0
     (5) Having an interrupt source established in the base timer circuit
     (6) Having an interrupt source established in the CVD circuit

■On-chip Debugger Function

- Supports software debugging with the IC mounted on the target board.
- Provides 1 channel of on-chip debugger pin.
  DBGP0 (P0)

■Data Security Function

- Protects the program data stored in flash memory from unauthorized read or copy.
  Note: This data security function does not necessarily provide absolute data security.

■Development Tools

- On-chip debugger: TCB87 type B + LC87F0A08A or TCB87 Type C (3-wire interface cable) + LC87F0A08A

■Programming Board

Package	Programming board
QFP36(7×7)	W87F0AQ

■Flash ROM Programmer

Vendor		Model	Supported version	Device
Flash Support Group, Inc. (FSG)	Single	AF9709/AF9709B/AF9709C (Including Ando Electric Co., Ltd. models)	Rev .02. xx or later	LC87F0A08A
	Gang	AF9723/AF9723B(Main body) (Including Ando Electric Co., Ltd. models)	-	-
		AF9833(Unit) (Including Ando Electric Co., Ltd. models)	-	-
Flash Support Group, Inc. + Our company (Note 1)	Onboard Single/Gang	AF9101/AF9103(Main body) (FSG)	(Note 2)	LC87F0A08A
		SIB87(Interface Driver) (Our company model)		
Our company	Single/Gang	SKK/SKK Type B (SANYO FWS)	Application Version 1.16 or later Chip Data Version 2.13 or later	LC87F0A08A
	Onboard Single/Gang	SKK-DBG Type B (SANYO FWS)		

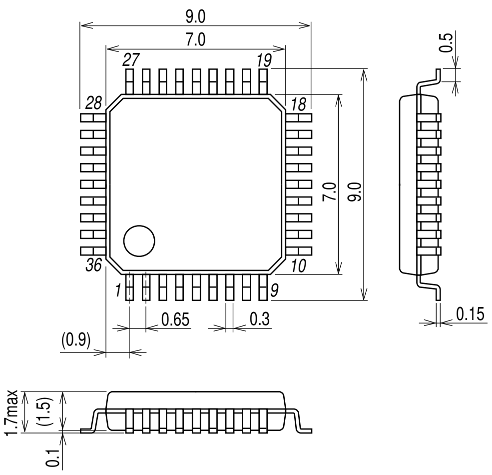
Note1: PC-less standalone onboard programming is possible using the FSG onboard programmer (AF9101/AF9103) and the serial interface driver (SIB87) provided by Our company in pair.

Note2: Dedicated programming device and program are required depending on the programming conditions. Contact Our company or FSG if you have any questions or difficulties regarding this matter.

Package Dimensions

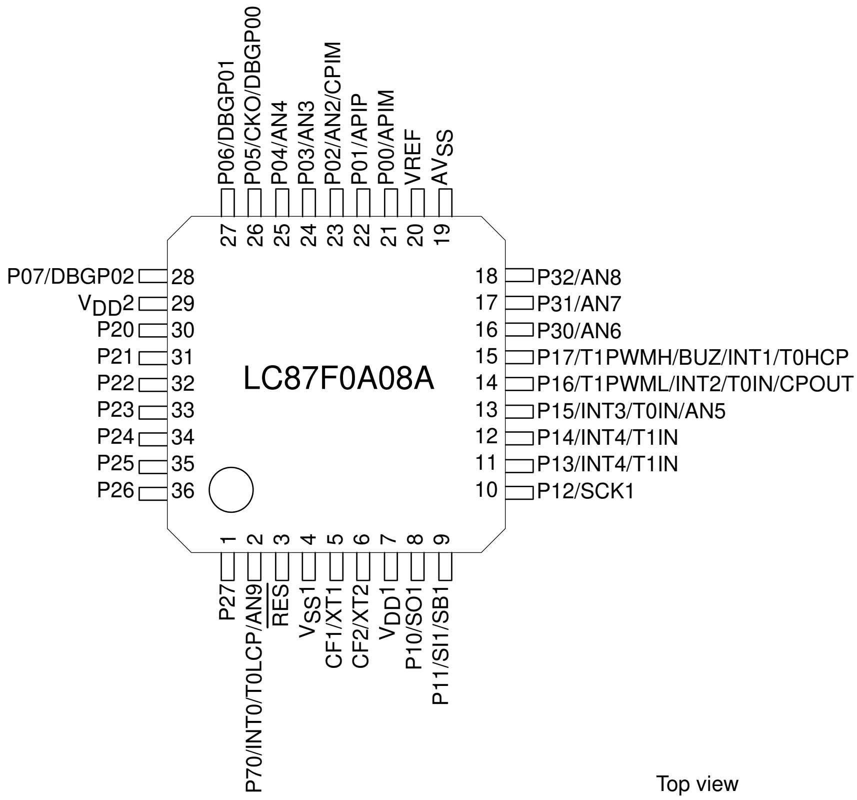
unit : mm (typ)

3162C



QFP36(7X7)

Pin Assignment

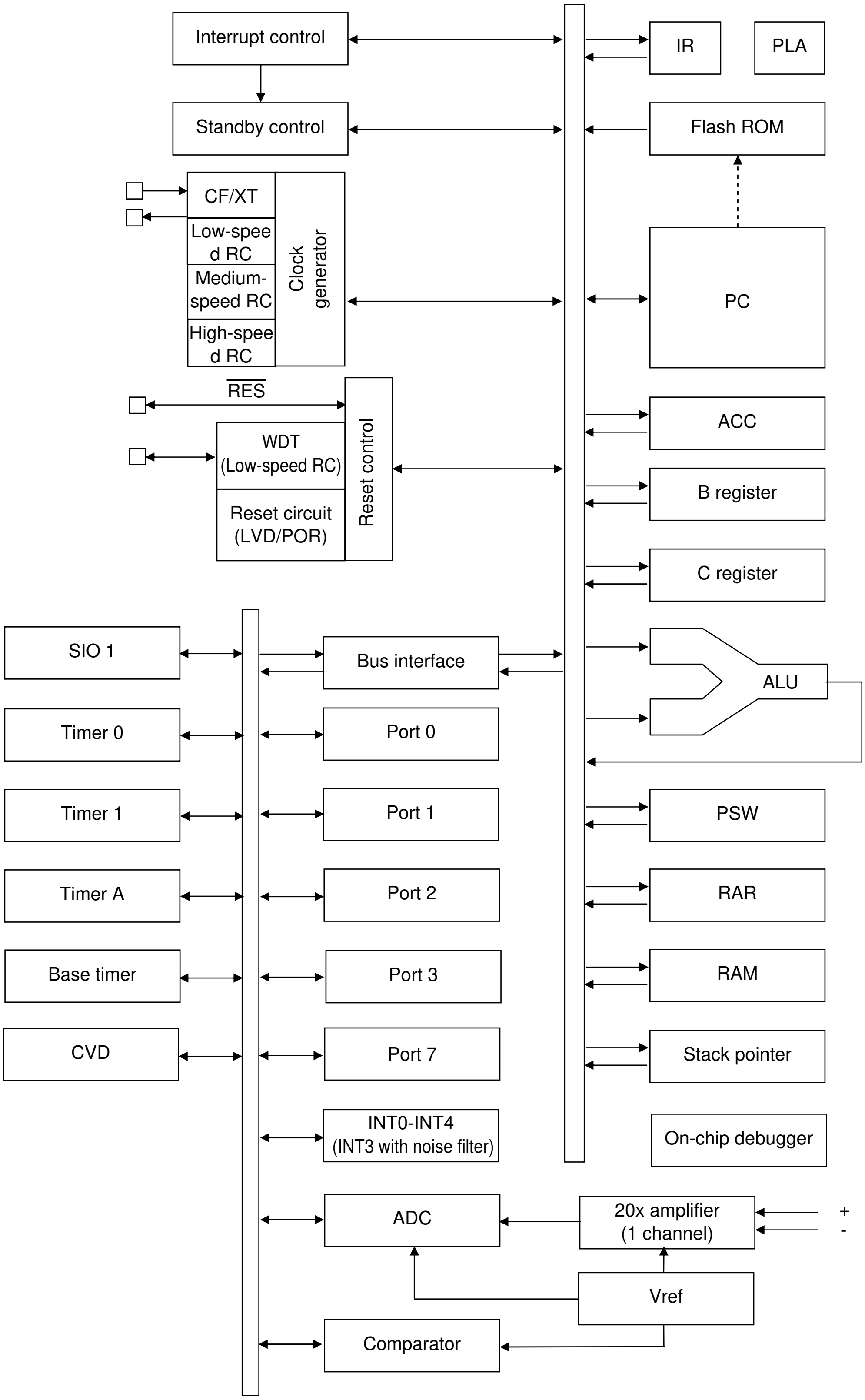


QFP36 (7×7) “Lead-free and halogen-free Type”

QFP36	NAME
1	P27
2	P70/INT0/T0LCP
3	$\overline{RES}$
4	$V_{SS}1$
5	CF1/XT1
6	CF2/XT2
7	$V_{DD}1$
8	P10/SO1
9	P11/SI1/SB1
10	P12/SCK1
11	P13/INT4/T1IN
12	P14/INT4/T1IN
13	P15/INT3/T0IN/AN5
14	P16/T1PWML/INT2/T0IN/CPOUT
15	P17/T1PWMH/BUZ/INT1/T0HCP
16	P30/AN6
17	P31/AN7
18	P32/AN8

QFP36	NAME
19	AV_{SS}
20	VREF
21	P00/AN0
22	P01/AN1
23	P02/AN2/CPIM
24	P03/AN3
25	P04/AN4
26	P05/CKO/DBGP00
27	P06/DBGP01
28	P07/DBGP02
29	$V_{DD}2$
30	P20
31	P21
32	P22
33	P23
34	P24
35	P25
36	P26

System Block Diagram



Pin Description

<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>$V_{SS}1$</td><td>-</td><td>- power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}1$</td><td>-</td><td>+ power supply pin</td><td>No</td></tr>
<tr><td>$V_{DD}2$</td><td>-</td><td>+ power supply pin</td><td>No</td></tr>
<tr><td>AV_{SS}</td><td>-</td><td>- power supply pin</td><td>No</td></tr>
<tr><td>VREF</td><td>O</td><td>Reference voltage output</td><td>No</td></tr>
<tr><td>Port 0
P00 to P07</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units.
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P00 (AN0), P01 (AN1): AD converter input port with 20x operational amplifier
P02: AD converter input port (AN2)/comparator input (CPIM)
P03: AD converter input port (AN3)
P04: AD converter input port (AN4)
P05: System clock output/on-chip debugger pin (DBGP00)
P06: On-chip debugger pin (DBGP01)
P07: On-chip debugger pin (DBGP02)</td><td>Yes</td></tr>
<tr><td>Port 1
P10 to P17</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units.
• Pull-up resistors can be turned on and off in 1-bit units.
• Current controllable in 1-bit units.
5mA (default), 10mA, 15mA, no current control
• Pin functions
P10: SIO1 data output
P11: SIO1 data input/bus input/output
P12: SIO1 clock input/output
P13, P14: INT4 input/HOLD release input/timer 1 event input/timer 0L capture input/
timer 0H capture input
P15: INT3 input(with noise filter)/timer 0 event input/timer 0H capture input/
AD converter input port (AN5)
P16: Timer 1 PWML output/INT2 input/HOLD release input/timer 0 event input/
timer 0L capture input/comparator output (CPOUT)
P17: Timer 1 PWMH output/beeper output/INT1 input/HOLD release input/timer 0H capture input
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT1</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
<tr><td>INT2</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT3</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
<tr><td>INT4</td><td>enable</td><td>enable</td><td>enable</td><td>disable</td><td>disable</td></tr>
</table></td><td>P10, P11 options not available

P12 to P17 options available</td></tr>
<tr><td>Port 2</td><td>I/O</td><td>• 8-bit I/O port
• I/O specifiable in 1-bit units.
• Pull-up resistors can be turned on and off in 1-bit units.
• Current controllable in 1-bit units.
5mA (default), 10mA, 15mA, no current control</td><td>Yes</td></tr>
<tr><td>Port 3</td><td>I/O</td><td>• 3-bit I/O port
• I/O specifiable in 1-bit units.
• Pull-up resistors can be turned on and off in 1-bit units.
• Pin functions
P30: AD converter input port (AN6)
P31: AD converter input port (AN7)
P32: AD converter input port (AN8)</td><td>Yes</td></tr>
</table>

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<table>
<tr><th>Pin Name</th><th>I/O</th><th>Description</th><th>Option</th></tr>
<tr><td>Port 7
P70</td><td>I/O</td><td>• 1-bit I/O port
• I/O specifiable
• Pull-up resistors can be turned on and off.
• Pin functions
P70 : INT0 input/HOLD release input/timer 0L capture input/AD converter input port (AN9)
Interrupt acknowledge type
<table>
<tr><th></th><th>Rising</th><th>Falling</th><th>Rising & Falling</th><th>H level</th><th>L level</th></tr>
<tr><td>INT0</td><td>enable</td><td>enable</td><td>disable</td><td>enable</td><td>enable</td></tr>
</table>
</td><td>No</td></tr>
<tr><td>$\overline{\text{RES}}$</td><td>I/O</td><td>External reset input/internal reset output pin</td><td>No</td></tr>
<tr><td>CF1/XT1</td><td>I</td><td>• Ceramic oscillator/32.768kHz crystal oscillator input pin
• Pin functions
General-purpose input port</td><td>No</td></tr>
<tr><td>CF2/XT2</td><td>I/O</td><td>• Ceramic oscillator/32.768kHz crystal oscillator output pin
• Pin functions
General-purpose input port</td><td>No</td></tr>
</table>

Port Output Types

The table below lists the types of port outputs and the presence/absence of a pull-up resistor.
Data can be read into any input port even if it is in the output mode.

Port Name	Option selected in units of	Option type	Output type	Pull-up resistor
P00 to P07	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P10 to P11	-	No	CMOS	Programmable
P12 to P177	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P20 to P27	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P30 to P32	1 bit	1	CMOS	Programmable
		2	Nch-open drain	Programmable
P70	-	No	Nch-open drain	Programmable

Absolute Maximum Ratings at Ta = 25°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter		Symbol	Pin/Remarks	Conditions	Specification				
					V_{DD}[V]	min	typ	max	unit
Maximum supply voltage		V_{DD} max	$V_{DD}1=V_{DD}2$			-0.3		+6.5	V
Input voltage		V_I	CF1, CF2			-0.3		V_{DD}+0.3	
Input/output voltage		V_{IO}	Ports 0, 1, 2 Ports 3, 7			-0.3		V_{DD}+0.3	
High level output current	Peak output current	IOPH(1)	Ports 0, 3	CMOS output type selected Per 1 applicable pin		-10			mA
		IOPH(2)	Ports 1, 2	CMOS output type selected Per 1 applicable pin		-20			
	Average output current (Note 1-1)	IOMH(1)	Ports 0, 3	CMOS output type selected Per 1 applicable pin		-7.5			
		IOMH(2)	Ports 1, 2	CMOS output type selected Per 1 applicable pin		-15			
	Total output current	ΣIOAH(1)	Ports 0, 1, 3	Total current of all applicable pins		-30			
		ΣIOAH(2)	Port 2	Total current of all applicable pins		-30			
		ΣIOAH(3)	Ports 0, 1, 2, 3	Total current of all applicable pins		-50			
Low level output current	Peak output current	IOPL(1)	Ports 0, 3	Per 1 applicable pin				20	
		IOPL(2)	Ports 1, 2	Per 1 applicable pin				20	
		IOPL(3)	Port 7	Per 1 applicable pin				10	
	Average output current (Note 1-1)	IOML(1)	Ports 0, 3	Per 1 applicable pin				15	
		IOML(2)	Ports 1, 2	Per 1 applicable pin				15	
		IOML(3)	Port 7	Per 1 applicable pin				7.5	
	Total output current	ΣIOAL(1)	Ports 0, 1, 2, 3, 7	Total current of all applicable pins				80	
Allowable power dissipation		Pd max (1)	QFP36	Ta=-40 to +85°C Package alone					mW
		Pd max (2)		Ta=-40 to +85°C Mounted on thermal resistance test board (Note 1-2)					
Operating ambient temperature		Topr				-40		+85	°C
Storage ambient temperature		Tstg				-55		+125	

Note 1-1: The average output current is an average of current values measured over 100ms intervals.

Note 1-2: Thermal resistance test board used conforms to SEMI (size: 76.1×114.3×1.6tmm, glass epoxy board).

Allowable Operating Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Specification				
				V_{DD}[V]	min	typ	max	unit
Operating supply voltage (Note 2-1)	$V_{DD}(1)$	$V_{DD}1=V_{DD}2$	0.367µs ≤ tCYC ≤ 200µs		2.5		5.5	V
	$V_{DD}(2)$		0.735µs ≤ tCYC ≤ 200µs		2.5		5.5	
Memory sustaining supply voltage	VHD	$V_{DD}1=V_{DD}2$	RAM and register contents sustained in HOLD mode		2.0			
High level input voltage	$V_{IH}(1)$	Ports 0, 1, 2, 3 P70		2.5 to 5.5	$0.3V_{DD}$ +0.7		V_{DD}	
	$V_{IH}(4)$	CF1, $\overline{RES}$		2.5 to 5.5	$0.75V_{DD}$		V_{DD}	
Low level input voltage	$V_{IL}(1)$	Ports 1, 2, 3 P70		4.0 to 5.5	V_{SS}		$0.1V_{DD}$ +0.4	
				2.5 to 4.0	V_{SS}		$0.2V_{DD}$	
	$V_{IL}(4)$	CF1, $\overline{RES}$		2.5 to 5.5	V_{SS}		$0.25V_{DD}$	
Instruction cycle time (Note 2-1)	tCYC (Note 2-2)			2.7 to 5.5	0.245		200	µs
				2.5 to 5.5	0.367		200	
				2.5 to 5.5	0.735		200	
External system clock frequency	FEXCF	CF1	• CF2 pin open • System clock frequency division ratio=1/1 • External system clock duty=50±5%	2.7 to 5.5	0.1		12	MHz
				2.5 to 5.5	0.1		8	
Oscillation frequency range (Note 2-3)	FmCF(1)	CF1, CF2	8MHz ceramic oscillation See Fig. 1.	2.5 to 5.5		8		MHz
	FmCF(2)	CF1, CF2	4MHz ceramic oscillation See Fig. 1.	2.5 to 5.5		4		
	FmMRC		1/2 of high-speed RC oscillation frequency (RCCTD=0) (Note 2-4)	2.5 to 5.5	7.44	8.0	8.56	
	FmRC		Internal medium-speed RC oscillation	2.5 to 5.5	0.5	1.0	2.0	
	FmSRC		Internal low-speed RC oscillation	2.5 to 5.5	15	30	60	kHz
	FsX'tal	XT1, XT2	32.768kHz crystal oscillation See Fig. 2.	2.5 to 5.5		32.768		

Note 2-1: V_{DD} must be held greater than or equal to 2.7V in the flash ROM onboard programming mode.

Note 2-2: Relationship between tCYC and oscillation frequency is 3/FmCF at a division ratio of 1/1 and 6/FmCF at a division ratio of 1/2.

Note 2-3: See Tables 1 and 2 for the oscillation constants.

Note 2-4: An oscillation stabilization time of 100µs or longer must be provided before switching the system clock source after the state of the high-speed RC oscillation circuit is switched from “oscillation stopped” to “oscillation enabled” .

Electrical Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
High level input current	$I_{IH}(1)$	Ports 0, 1, 2, 3 Port 7, $\overline{RES}$	Output disabled Pull-up resistor off $V_{IN}=V_{DD}$ (including output TR's off leakage current)	2.5 to 5.5			1	μA
	$I_{IH}(2)$	CF1	$V_{IN}=V_{DD}$	2.5 to 5.5			15	μA
Low level input current	$I_{IL}(1)$	Ports 0, 1, 2, 3 Port 7, $\overline{RES}$	Output disabled Pull-up resistor off $V_{IN}=V_{SS}$ (including output TR's off leakage current)	2.5 to 5.5	-1			μA
	$I_{IL}(2)$	CF1	$V_{IN}=V_{SS}$	2.5 to 5.5	-15			μA
High level output voltage	$V_{OH}(1)$	Ports 0, 3	I_{OH}=-1mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(2)$		I_{OH}=-0.2mA	2.5 to 5.5	V_{DD}-0.4			V
	$V_{OH}(3)$	Ports 1, 2	I_{OH}=-6mA	4.5 to 5.5	V_{DD}-1			V
	$V_{OH}(4)$		I_{OH}=-1.0mA	2.5 to 5.5	V_{DD}-0.4			V
Low level output voltage	$V_{OL}(1)$	Ports 0, 1, 2, 3	I_{OL}=10mA	4.5 to 5.5			1.5	V
	$V_{OL}(2)$		I_{OL}=1.0mA	2.5 to 5.5			0.4	V
	$V_{OL}(3)$	P70	I_{OL}=8mA	4.5 to 5.5			1.5	V
	$V_{OL}(4)$		I_{OL}=1.0mA	2.5 to 5.5			0.4	V
Constant current operation enabled pin voltage	VOCC	Ports 1, 2		2.5 to 5.5	1		V_{DD} -1.0	V
Constant current port current (5mA setting)	ILED(1)	Ports 1, 2	Per 1 applicable pin only ON time V_O=1.0 to (V_{DD}-1.0)	2.7 to 5.5	4	5	6	mA
	ILED(2)			2.5 to 2.7	3	5	6	mA
Constant current port current (10mA setting)	ILED(3)			2.7 to 5.5	8	10	12	mA
	ILED(4)			2.5 to 2.7	6	10	12	mA
Constant current port current (15mA setting)	ILED(5)			2.7 to 5.5	LED(1)+LED(3)			mA
	ILED(6)			2.5 to 2.7	LED(2)+LED(4)			mA
Pull-up resistance	Rpu(1)	Ports 0, 1, 2, 3 Port 7	$V_{OH}=0.9V_{DD}$	4.5 to 5.5	15	35	80	kΩ
	Rpu(2)			2.5 to 4.5	18	50	230	kΩ
Hysteresis voltage	VHYS(1)	Ports 0, 1, 2, 3 P70 $\overline{RES}$		2.5 to 5.5		$0.1V_{DD}$		V
Pin capacitance	CP	All pins	For pins other than that under test $V_{IN}=V_{SS}$ f=1MHz Ta=25°C	2.5 to 5.5		10		pF

SIO1 Serial I/O Characteristics (Note 4-1)

Parameter			Symbol	Pin/Remarks	Conditions	V_{DD}[V]	min	typ	max	unit
Serial clock	Input clock	Frequency	tSCK(1)	SCK1(P12)	• See Fig. 5.	2.5 to 5.5	2			tCYC
		Low level pulse width	tSCKL(1)				1			
		High level pulse width	tSCKH(1)				1			
	Output clock	Frequency	tSCK(2)	SCK1(P12)	• CMOS output type selected • See Fig. 5.	2.5 to 5.5	2			
		Low level pulse width	tSCKL(2)					1/2		tSCK
		High level pulse width	tSCKH(2)					1/2		
Serial input	Data setup time		tsDI(1)	SI1(P11), SB1(P11)	• Specified with respect to rising edge of SIOCLK. • See Fig. 5.	2.5 to 5.5	0.05			µs
	Data hold time		thDI(1)				0.05			
Serial output	Output delay time		tdDO(1)	SO1(P10), SB1(P11)	• Specified with respect to falling edge of SIOCLK • Specified as the time up to the beginning of output change in open drain output mode. • See Fig. 5.	2.5 to 5.5			(1/3)tCYC +0.08	

Note 4-1: These specifications are theoretical values. Margins must be allowed according to the actual operating conditions.

Pulse Input Conditions at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	min	typ	max	unit
High/low level pulse width	tPIH(1) tPIL(1)	INT0(P70), INT1(P71), INT2(P16), INT4(P13, P14)	• Interrupt source flag can be set. • Event inputs for timer 0 or 1 are enabled.	2.5 to 5.5	1			tCYC
	tPIH(2) tPIL(2)	INT3(P15) when noise filter time constant is 1/1	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 5.5	2			tCYC
	tPIH(3) tPIL(3)	INT3(P15) when noise filter time constant is 1/32	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 5.5	64			tCYC
	tPIH(4) tPIL(4)	INT3(P15) when noise filter time constant is 1/128	• Interrupt source flag can be set. • Event inputs for timer 0 are enabled.	2.5 to 5.5	256			tCYC
	tPIL(5)	$\overline{RES}$	• Resetting is enabled.	2.5 to 5.5	200			µs

AD Converter Characteristics at $V_{SS}1 = AV_{SS} = 0V$

<12bits AD Converter Mode/Ta = -40°C to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN2(P02) AN3(P03) AN4(P04) AN5(P15) AN6(P30) AN7(P31) AN8(P32) AN9(P70) (Note 6-3)		3.0 to 5.5		12		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±16	LSB
Conversion time	TCAD		• See conversion time calculation method. (Note 6-2)	4.0 to 5.5	32		115	μs
				3.0 to 5.5	64		115	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		VREF	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	μA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

<8bits AD Converter Mode/Ta = -40°C to +85°C >

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				V_{DD}[V]	min	typ	max	unit
Resolution	N	AN2(P02) AN3(P03) AN4(P04) AN5(P15) AN6(P30) AN7(P31) AN8(P32) AN9(P70) (Note 6-3)		3.0 to 5.5		8		bit
Absolute accuracy	ET		(Note 6-1)	3.0 to 5.5			±1.5	LSB
Conversion time	TCAD		• See “Conversion time calculation method”. (Note 6-2)	4.0 to 5.5	20		90	μs
				3.0 to 5.5	40		90	
Analog input voltage range	VAIN			3.0 to 5.5	V_{SS}		VREF	V
Analog port input current	IAINH		VAIN=V_{DD}	3.0 to 5.5			1	μA
	IAINL		VAIN=V_{SS}	3.0 to 5.5	-1			

<Conversion time calculation method>

12bits AD Converter Mode: TCAD(Conversion time) = ((52/(AD division ratio))+2)×(1/3)×tCYC

8bits AD Converter Mode: TCAD(Conversion time) = ((32/(AD division ratio))+2)× (1/3)×tCYC

<Recommended Operating Conditions>

External oscillation (FmCF)	Operating supply voltage range (V_{DD})	System division ratio (SYSDIV)	Cycle time (tCYC)	AD division ratio (ADDIV)	AD conversion time (TCAD)	
					12bit AD	8bit AD
CF-8MHz	4.0V to 5.5V	1/1	375ns	1/8	52.3μs	32.3μs
	3.0V to 5.5V	1/1	375ns	1/16	104.5μs	64.5μs
CF-4MHz	3.0V to 5.5V	1/1	750ns	1/8	104.5μs	64.5μs

Note 6-1: The quantization error (±1/2LSB) is excluded from the absolute accuracy. The absolute accuracy is measured when no change occurs in the I/O state of the pins that are adjacent to the analog input channel during AD conversion processing.

Note 6-2: The conversion time refers to the interval from the time a conversion starting instruction is issued till the time the complete digital value against the analog input value is loaded in the result register.
The conversion time is twice the normal value when one of the following conditions occurs:
- The first AD conversion executed in the 12-bit AD conversion mode after a system reset
- The first AD conversion executed after the AD conversion mode is switched from 8-bit to 12-bit AD conversion mode

Note 6-3: See section 8, “20× amplifier characteristics”, for analog channel 0 (20× amplifier output).

Reference Voltage Generator Circuit (VREF) Characteristics

at Ta = -40°C to +85°C, $V_{SS}1 = AV_{SS} = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
VREF voltage accuracy	VREFVO	VREF (Note 7-2)	• Ta=-40 to +85°C	2.5 to 4.0	V_{DD}-0.1		V_{DD}	V
				4.0 to 5.5	3.92	4.00	4.08	
			• Ta=-40 to +60°C	4.5 to 5.5	3.96		4.04	
VREF output current	VREFIO		• Ta=-40 to +85°C	2.5 to 5.5	V_{SS}		1	mA
Operation stabilization time (Note 7-1)	tVREFW			2.5 to 5.5			10	µs

Note 7-1: Refers to the interval between the time VRONZ is set to 0 and the time operation gets stabilized.
Note 7-2: An external 4.7µF capacitor must be connected to the VREF pin to stabilize the VREF voltage.

20x Amplifier Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = AV_{SS} = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Amplifier gain	APGAIN See Fig. 7.	P00/APIM P01/APIP	• Ta=-40 to +85°C • VREF=4.0V • P01=0V, P00≤0V or P00=0V, P01≥0V	5.0		20		
Operation stabilization time (Note 8-1)	tAPW						1.0	µs
Amplifier input voltage full scale (Note 8-1)	VAPFUL				0.16		0.19	V
Amplifier input voltage range	VAPIM	P00/APIM	P01/APIP=0V		-VAPFUL		0	
	VAPIP	P01/APIP	P00/APIM=0V		0		VAPFUL	
Amplifier input port input current	IAPINL	P00/APIM	P00/APIM=V_{SS}-0.2V		-1			µA
	IAPINH	P01/APIP	P01/APIP=V_{DD}				1	

Note 8-1: Refers to the interval between the time APON is set to 1 and the time operation gets stabilized.

Comparator Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = AV_{SS} = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	Specification min	typ	max	unit
Comparator threshold voltage (Note 9-1)	VCMVT	P02/CPIM		2.5 to 5.5	1.12	1.22	1.32	V
Common mode input voltage range	VCMIN			2.5 to 5.5	V_{SS}		V_{DD}-1.5	V
Offset voltage	VOFF		• Within common mode input voltage range	2.5 to 5.5		±10	±30	mV
Response time	tRT		• Within common mode input voltage range • Input amplitude=100mV • Overdrive=50mV	2.5 to 5.5		200	600	ns
Operation stabilization time (Note 9-2)	tCMW			2.5 to 5.5			1.0	µs

Note 9-1: Comparator output=High level when (P02/CPIM voltage) < VCMVT
Comparator output=Low level when (P02/CPIM voltage) > (VCMVT +VOFF)
Note 9-2: Refers to the interval between the time CPONZ is set to 0 and the time operation gets stabilized.

Power-on Reset (POR) Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = AV_{SS} = 0V$

Parameter	Symbol	Pin / Remarks	Conditions		Specification			
				Option Selected Voltage	min	typ	max	unit
POR release voltage	PORRL		Option selected (Note 10-1)	1.67V	1.55	1.67	1.79	V
				1.97V	1.85	1.97	2.09	
				2.07V	1.95	2.07	2.19	
				2.37V	2.25	2.37	2.49	
				2.57V	2.45	2.57	2.69	
				2.87V	2.75	2.87	2.99	
				3.86V	3.73	3.86	3.99	
				4.35V	4.21	4.35	4.49	
Detection voltage unpredictable area	POUKS		See Fig. 8. (Note 10-2)			0.7	0.95	
Power supply rise time	PORIS		Power startup time from V_{DD}=0V to 1.6V				100	ms

Note 10-1: The POR release voltage can be selected from 8 levels when the low-voltage detection feature is deselected.
Note 10-2: There is an unpredictable area before the transistor starts to turn on.

Low-voltage Detection (LVD) Reset Characteristics

at Ta = -40°C to +85°C, $V_{SS}1 = AV_{SS} = 0V$

Parameter	Symbol	Pin/Remarks	Conditions		Specification			
				Option Selected Voltage	min	typ	max	unit
LVD reset voltage (Note 11-2)	LVDET		Option selected See Fig. 9. (Note 11-1) (Note 11-3)	1.91V	1.81	1.91	2.01	V
				2.01V	1.91	2.01	2.11	
				2.31V	2.21	2.31	2.41	
				2.51V	2.41	2.51	2.61	
				2.81V	2.71	2.81	2.91	
				3.79V	3.69	3.79	3.89	
				4.28V	4.18	4.28	4.38	
LVD voltage hysteresis	LVHYS			1.91V		55		mV
				2.01V		55		
				2.31V		55		
				2.51V		55		
				2.81V		60		
				3.79V		65		
				4.28V		65		
Detection voltage unpredictable area	LVUKS		See Fig. 9. (Note 11-4)			0.7	0.95	V
Minimum low voltage detection width (response sensitivity)	TLVDW		LVDET-0.5V See Fig. 10.		0.2			ms

Note 11-1: The LVD reset voltage can be selected from 7 levels when the low-voltage detection feature is selected.
Note 11-2: The hysteresis voltage is not included in the LVD reset voltage specification value.
Note 11-3: There are cases when the LVD reset voltage specification value is exceeded when a greater change in the output level or large current is applied to the port.
Note 11-4: There is an unpredictable area before the transistor starts to turn on.

Constant Voltage Detection (CVD) Interrupt Characteristics

at Ta = -40 to +85°C, $V_{SS}1 = AV_{SS} = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	Register Selected Voltage	min	typ	max	unit
CVD detection voltage (Note 12-2)	CVDET		Register selected (Note 12-1) (Note 12-3)	2.6V	2.5	2.6	2.7	V
				2.8V	2.7	2.8	2.9	
				3.0V	2.9	3.0	3.1	
				3.2V	3.1	3.2	3.4	
				3.4V	3.3	3.4	3.6	
				3.6V	3.5	3.6	3.8	
				3.8V	3.7	3.8	4.0	
				4.0V	3.9	4.0	4.2	
				4.2V	4.1	4.2	4.4	
				4.4V	4.3	4.4	4.6	
				4.6V	4.5	4.6	4.8	
				4.8V	4.7	4.8	5.0	
CVD detection voltage hysteresis	CVHYS			2.6V		50		mV
				2.8V		50		
				3.0V		50		
				3.2V		50		
				3.4V		50		
				3.6V		50		
				3.8V		50		
				4.0V		50		
				4.2V		50		
				4.4V		50		
				4.6V		50		
				4.8V		55		
Detection voltage unpredictable area	CVUKS		(Note 12-4)			0.7	0.95	V
Minimum CVD detection width (response sensitivity)	TCVDW		CVDET-0.5V		0.8			ms
Operation stabilization time (Note 12-5)	tCVDON		V_{DD}=2.5 to 5.5V				100	µs

Note 12-1: The CVD detection voltage can be selected from 16 levels.

Note 12-2: The hysteresis voltage is not included in the CVD detection voltage specification value.

Note 12-3: There are cases when the CVD detection voltage specification value is exceeded when a greater change in the output level or large current is applied to the port.

Note 12-4: There is an unpredictable period before the CVD-related transistor starts to turn on.

Note 12-5: Refers to the interval between the time CVDRUN is set to 1 and the time operation gets stabilized.

Consumption Current Characteristics at Ta = -40°C to +85°C, $V_{SS}1 = V_{SS}2 = 0V$

Parameter	Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	min	typ	max	unit
Normal mode consumption current (Note 13-1) (Note 13-2)	IDDOP(1)	$V_{DD}1$ $=V_{DD}2$	• FmCF=8MHz ceramic oscillation mode • System clock set to 8MHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	4.5 to 5.5		5.5	11.3	mA
				2.5 to 4.5		3.4	9.0	
	IDDOP(2)		• FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	4.5 to 5.5		2.8	6.8	
				2.5 to 4.5		2.1	5.4	
	IDDOP(3)		• FsX'tal=32.768kHz crystal oscillation mode • Internal low-speed RC oscillation stopped • System clock set to internal medium-speed RC oscillation mode • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/2	4.5 to 5.5		0.6	1.9	
				2.5 to 4.5		0.3	1.4	
	IDDOP(4)		• FsX'tal=32.768kHz crystal oscillation mode • Internal low-/medium-speed RC oscillation stopped • System clock set to internal high-speed RC oscillation mode • Frequency division ratio set to 1/1	4.5 to 5.5		5.0	9.9	
				2.5 to 4.5		3.5	8.6	
	IDDOP(5)		• External oscillation FsX'tal/FmCF stopped • System clock set to internal low-speed RC oscillation mode • Internal medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	4.5 to 5.5		21.3	89.4	μA
				2.5 to 4.5		13.6	64.8	
	IDDOP(6)		• FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/2	4.5 to 5.5		22.8	101.5	
				2.5 to 4.5		10.9	70.0	
HALT mode consumption current (Note 13-1) (Note 13-2)	IDDHALT(1)	$V_{DD}1$ $=V_{DD}2$	HALT mode • FmCF=8MHz ceramic oscillation mode • System clock set to 8MHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	4.5 to 5.5		2.0	3.2	mA
				2.5 to 4.5		1.0	2.3	
	IDDHALT(2)		HALT mode • FmCF=4MHz ceramic oscillation mode • System clock set to 4MHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	4.5 to 5.5		1.3	2.2	
				2.5 to 4.5		0.6	1.5	
	IDDHALT(3)		HALT mode • FsX'tal=32.768kHz crystal oscillation mode • Internal low-speed RC oscillation stopped • System clock set to internal medium-speed RC oscillation mode • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/2	4.5 to 5.5		0.3	1.2	
				2.5 to 4.5		0.2	0.8	

Note 13-1: The consumption current value includes none of the currents that flow into the output transistors and internal pull-up resistors.

Note 13-2: Unless otherwise specified, the consumption current for the LVD circuit is not included.

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Parameter	Symbol	Pin/ Remarks	Conditions	V_{DD}[V]	min	typ	max	unit
HALT mode consumption current (Note 13-1) (Note 13-2)	IDDHALT(4)	$V_{DD}1$ $=V_{DD}2$	HALT mode • FsX'tal=32.768kHz crystal oscillation mode • Internal low-/medium-speed RC oscillation stopped • System clock set to internal high-speed RC oscillation mode • Frequency division ratio set to 1/1	4.5 to 5.5		1.6	2.2	µA
				2.5 to 4.5		1.1	1.8	
	IDDHALT(5)		HALT mode • External oscillation FsX'tal/FmCF stopped • System clock set to internal low-speed RC oscillation mode • Internal medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/1	4.5 to 5.5		5.6	43	
				2.5 to 4.5		3.3	30.4	
	IDDHALT(6)		HALT mode • FsX'tal=32.768kHz crystal oscillation mode • System clock set to 32.768kHz mode • Internal low-/medium-speed RC oscillation stopped • Internal high-speed RC oscillation stopped • Frequency division ratio set to 1/2	4.5 to 5.5		12.0	69.8	
				2.5 to 4.5		4.4	44.7	
HOLD mode consumption current (Note 13-1) (Note 13-2)	IDDHOLD(1)	$V_{DD}1$ $=V_{DD}2$	HOLD mode	4.5 to 5.5		0.024	41.0	µA
				2.5 to 4.5		0.010	27.2	
	IDDHOLD(2)		HOLD mode • LVD option selected	4.5 to 5.5		2.9	30.2	
				2.5 to 4.5		2.3	22.3	
Timer HOLD mode consumption current (Note 13-1) (Note 13-2)	IDDHOLD(3)	$V_{DD}1$ $=V_{DD}2$	Timer HOLD mode • FsX'tal=32.768kHz crystal oscillation mode	4.5 to 5.5		9.9	63.2	
				2.5 to 4.5		3.2	39.6	
	IDDHOLD(4)		Timer HOLD mode • FmSRC=30kHz internal low-speed RC oscillation mode	4.5 to 5.5		2.1	31.6	
				2.5 to 4.5		1.2	8.4	
	IDDHOLD(5)		Timer HOLD mode • FmSRC=30kHz internal low-speed RC oscillation mode CVD active mode	4.5 to 5.5		29.3	110.2	
				2.5 to 4.5		20.1	86.3	

Note 13-1: The consumption current value includes none of the currents that flow into the output transistors and internal pull-up resistors.

Note 13-2: Unless otherwise specified, the consumption current for the LVD circuit is not included.

F-ROM Programming Characteristics at Ta = +10°C to +55°C, $V_{SS}1 = AV_{SS} = 0V$

Parameter	Symbol	Pin/Remarks	Conditions	V_{DD}[V]	min	typ	max	unit
Onboard programming current	IDDFW(1)	$V_{DD}1$	• Excluding power dissipation in the microcontroller block	2.7 to 5.5		5	10	mA
Programming time	tFW(1)		• Erase mode	2.7 to 5.5		20	30	ms
	tFW(2)		• Programming mode			40	60	µs

Characteristics of a Sample Main System Clock Oscillation Circuit

Given below are the characteristics of a sample main system clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 1 Characteristics of a Sample Main System Clock Oscillator Circuit with a Ceramic Oscillator
■MURATA Manufacturing Co., Ltd.

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [ms]	max [ms]	
4MHz	SMD	CSTCR4M00G53-R0	(10)	(10)	Open	3.3k	2.5 to 5.5	0.03		C1 and C2 integrated type
8MHz	SMD	CSTCE8M00G52-R0	(10)	(10)	Open	1.5k	2.5 to 5.5	0.02		

Characteristics of a Sample Subsystem Clock Oscillation Circuit

Given below are the characteristics of a sample subsystem clock oscillation circuit that are measured using a SANYO-designated oscillation characteristics evaluation board and external components with circuit constant values with which the oscillator vendor confirmed normal and stable oscillation.

Table 2 Characteristics of a Sample Subsystem Clock Oscillator Circuit that Uses a Crystal Oscillator
■EPSON TOYOCOM

Nominal Frequency	Type	Oscillator Name	Circuit Constant				Operating Voltage Range [V]	Oscillation Stabilization Time		Remarks
			C1 [pF]	C2 [pF]	Rf [Ω]	Rd [Ω]		typ [ms]	max [ms]	
32.768kHz	SMD	MC-306	7	7	Open	330k	2.5 to 5.5	0.85		CL value applied: 7pF

The oscillation stabilization time refers to the time interval that is required for the oscillation to get stabilized in the following cases (see Figure 3):

- Till the oscillation gets stabilized after the instruction for starting the subclock oscillation circuit is executed
- Till the oscillation gets stabilized after the HOLD mode is released.

Note: The components that are involved in oscillation should be placed as close to the IC and to one another as possible because they are vulnerable to the influences of the circuit pattern.

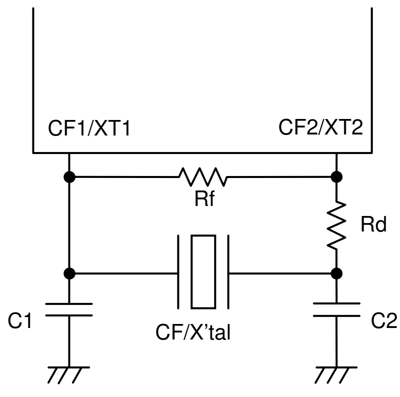


Figure 1 CF/XT Oscillator Circuit

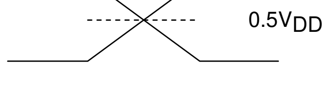
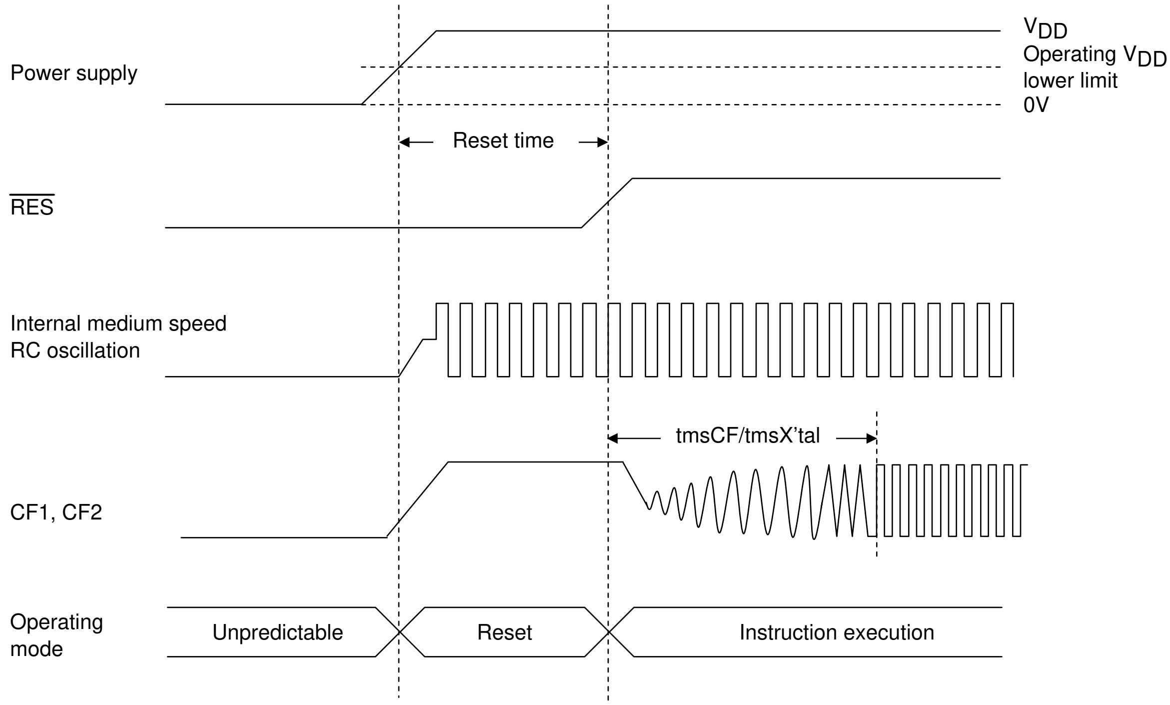
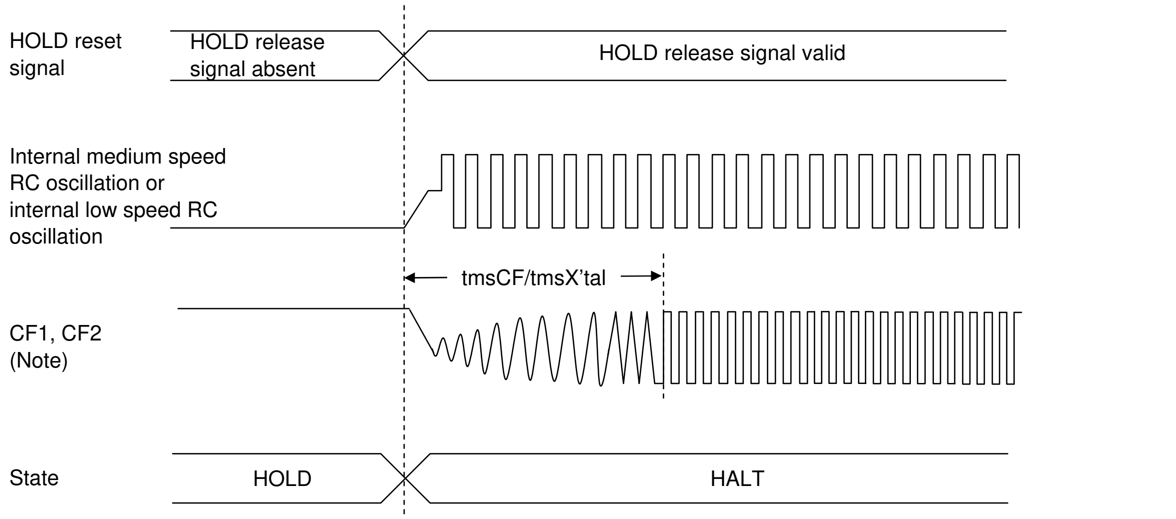


Figure 2 AC Timing Measurement Point



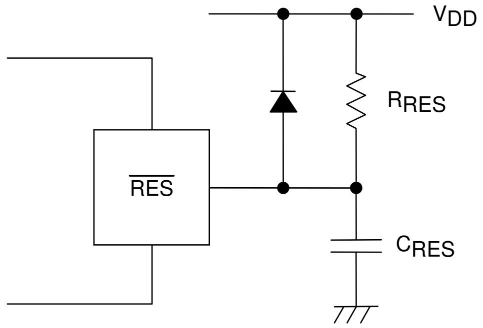
Reset Time and Oscillation Stabilization Time



HOLD Release Signal and Oscillation Stabilization Time

Note: When an external oscillation circuit is selected.

Figure 3 Oscillation Stabilization Time



Note:
The external circuit for reset may vary depending on the usage of POR and LVD. See "Reset Function" in the user's manual.

Figure 4 Sample Reset Circuit

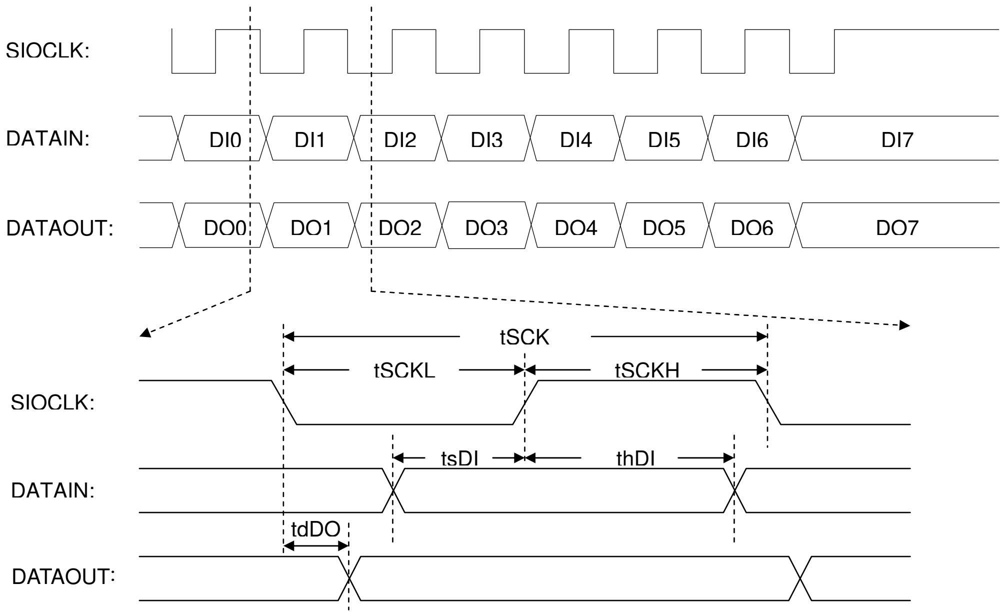


Figure 5 Serial I/O Waveform

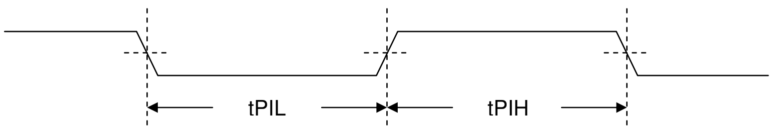


Figure 6 Pulse Input Timing Signal Waveform

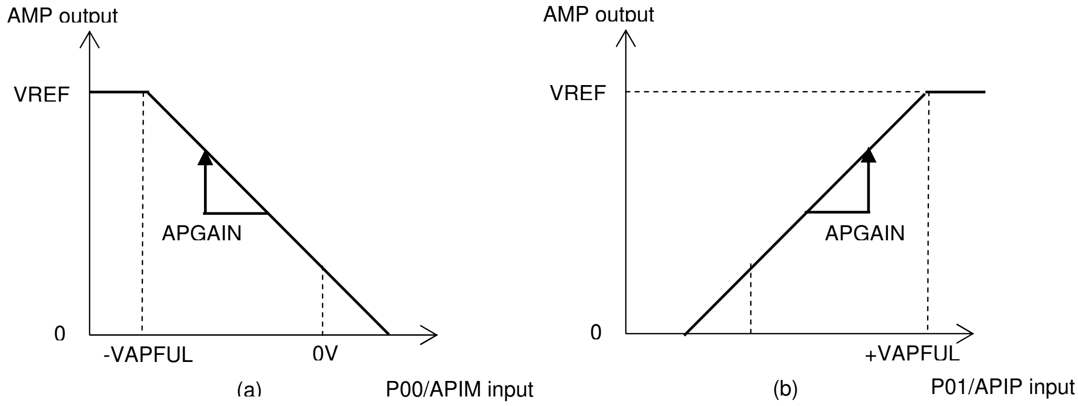


Figure 7 20× Amplifier Characteristics

(a) When P01/APIP is 0V, P00/APIM ≤ 0V.
(b) When P00/APIM is 0V, P01/APIP ≥ 0V.

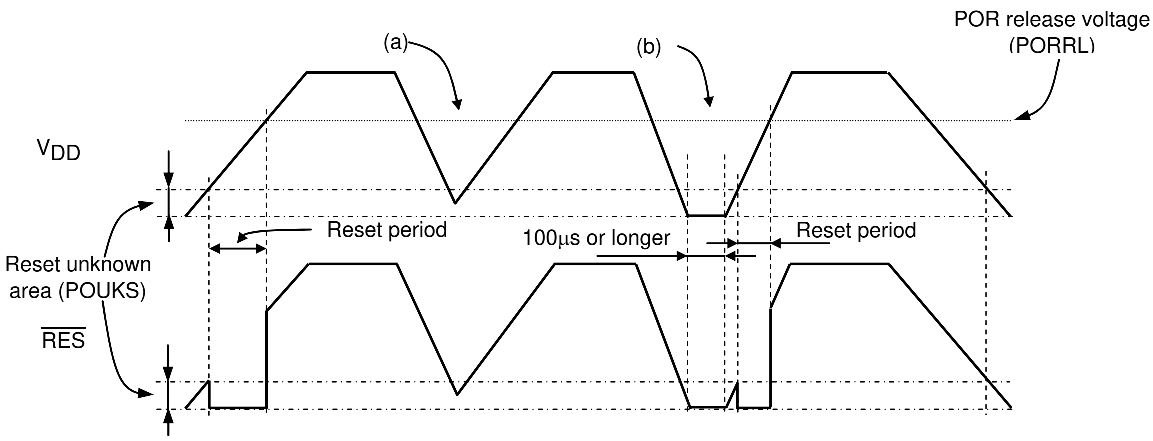


Figure 8 Example of POR Only (LVD Deselected) Mode Waveforms (at Reset Pin with R_{RES} Pull-up Resistor Only)

- The POR function generates a reset only when the power voltage goes up from the V_{SS} level.
- No stable reset will be generated if power is turned on again when the power level does not go down to the V_{SS} level as shown in (a). If such a case is anticipated, use the LVD function together with the POR function or implement an external reset circuit as shown below.
- A reset is generated only when the power level goes down to the V_{SS} level as shown in (b) and power is turned on again after this condition continues for 100µs or longer.

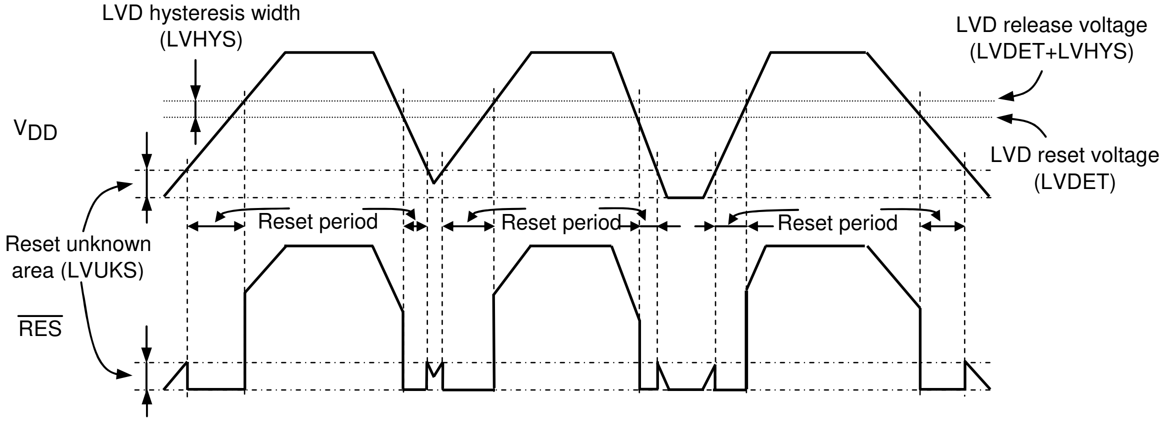


Figure 9 Example of POR + LVD Mode Waveforms (at Reset Pin with R_{RES} Pull-up Resistor Only)

- Resets are generated both when power is turned on and when the power level lowers.
- A hysteresis width (LVHYS) is provided to prevent the repetitions of reset release and entry cycles near the detection level.

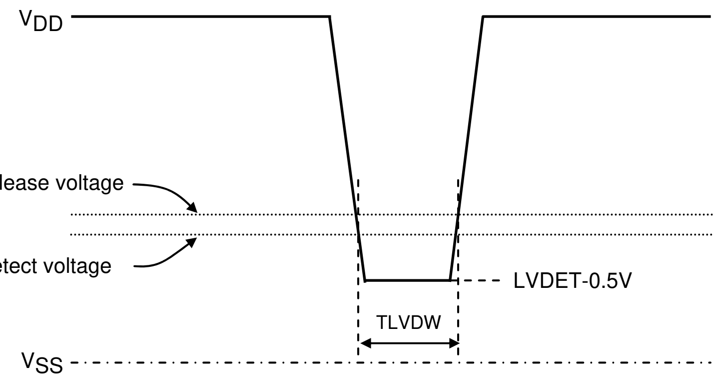


Figure 10 Minimum Low Voltage Detection Width (Example of Voltage Sag/Fluctuation Waveform)

ORDERING INFORMATION

Device	Package	Shipping (Qty / Packing)
LC87F0A08AU-EB-TLM-H	QFP36(7X7) (Pb-Free / Halogen Free)	1000 / Tape & Reel
LC87F0A08AUEB-NH	QFP36(7X7) (Pb-Free / Halogen Free)	1000 / Tape & Reel