National Semiconductor

MICROCIRCUIT DATA SHEET

MN100331-X REV 1B0

Original Creation Date: 10/30/95
Last Update Date: 04/23/04
Last Major Revision Date: 08/21/96

LOW POWER TRIPLE D FLIP-FLOP

General Description

The F100331 contains three D-type, edge-triggered master/slave flip-flops with true and complement outputs, a common clock (CPc), and Master Set (MS) and Master Reset (MR) inputs. Each flip-flop has individual clock (CPn), Direct Set (SDn) and Direct Clear (CDn) Inputs. Data enters a master when both CPn and CPc are LOW and transfers to a slave when CPn or CPc (or both) go HIGH. The Master Set, Master Reset and individual CDn and SDn inputs override the Clock inputs. All inputs have 50k ohm pull-down resistors.

Industry Part Number

100331

Prime Die

F331

Controlling Document

SEE FEATURES SECTION

NS Part Numbers

100331DMQB
100331FMQB
100331J-QMLV
100331W-QMLV
100331WFQMLV

Processing

MIL-STD-883, Method 5004

Quality Conformance Inspection

MIL-STD-883, Method 5005

Subgrp	Description	Temp (^{O}C)
1	Static tests at	+25
2	Static tests at	+125
3	Static tests at	-55
4	Dynamic tests at	+25
5	Dynamic tests at	+125
6	Dynamic tests at	-55
7	Functional tests at	+25
8A	Functional tests at	+125
8B	Functional tests at	-55
9	Switching tests at	+25
10	Switching tests at	+125
11	Switching tests at	-55

Features

- 35% power reduction of the 100131
- 2000V ESD protection
- Pin/Function compatible with 100131
- Voltage compensated operating range= -4.2V to -5.7V
- Available to industrial grade temperature range
- Available to MIL-STD-883

CONTROLLING DOCUMENTS:

100331DMQB	5962-9153601MXA
100331FMQB	5962-9153601MYA
100331J-QMLV	5962-9153601VXA
100331W-QMLV	5962-9153601VYA
100331WFQMLV	5962F9153601VYA

(Absolute Maximum Ratings)
(Note 1)

Storage Temperature (Tstg)	-65C to +150C
Maximum Junction Temperature (Tj)	
Ceramic	+175C
Plastic	+150C
VEE Pin Potential to Ground Pin	-7.0V to +0.5V
Input Voltage (DC)	Vee to +0.5V
Output Current (DC Output HIGH)	-50 mA
ESD (Note 2)	$\geq$2000V

Note 1: Absolute maximum ratings are those values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied.
Note 2: ESD testing conforms to MIL-STD-883, Method 3015.

Recommended Operating Conditions

Case Temperature (Tc)	
Commercial	0 C to +85 C
Industrial	-40 C to +85C
Military	-55C to +125C
Supply Voltage (Vee)	-5.7V to -4.2V

Electrical Characteristics

DC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
DC: Vee Range: -4.2V to -5.7V, VCC=VCCA=GND, Tc=-55C to +125C

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
IIH	Input HIGH Current	VEE=-5.7V, VM=-0.87V	1, 3	INPUTS		240	uA	1, 2
			1, 3	INPUTS		340	uA	3
IIL	Input Low Current	VEE=-4.2V, VM=-1.83V	1, 3	INPUTS		0.5	uA	1, 2, 3
VOH	Output HIGH Voltage	VEE=-4.2V/-5.7V, VIH=-0.87V, VIL=-1.83V, LOADING: 50 ohms to -2.0V	1, 3	OUTPUTS	-1025	-870	mV	1, 2
			1, 3	OUTPUTS	-1085	-870	mV	3
VOL	Output LOW Voltage	Vee=-4.2V/-5.7V, VIH=-0.87V, VIL=-1.83V LOADING:50 Ohms to -2.0V	1, 3	OUTPUTS	-1830	-1620	mV	1, 2
			1, 3	OUTPUTS	-1830	-1555	mV	3
VOHC	Output HIGH Voltage Corner Point High	Vee=-4.2V/-5.7V, VIH=-1.165V, VIL=-1.475V, LOADING: 50 ohms to-2.0V	1, 3	OUTPUTS	-1035		mV	1, 2
			1, 3	OUTPUTS	-1085		mV	3
VOLC	Output LOW Voltage Corner Point High	Vee=-4.2V/-5.7V, VIH=-1.165V, VIL=-1.475V, LOADING: 50 ohms to-2.0V	1, 3	OUTPUTS		-1610	mV	1, 2
			1, 3	OUTPUTS		-1555	mV	3
VIH	Input HIGH Voltage		1, 3, 7	INPUTS	-1165	-870	mV	1, 2, 3
VIL	Input LOW Voltage		1, 3, 7	INPUTS	-1830	-1475	mV	1, 2, 3
IEE	Power Supply Current	VEE=-4.2/-4.8V	1, 3	VEE	-125	-50	mA	1, 2, 3
		VEE=-4.2V/-5.7V	1, 3	VEE	-130		mA	1, 2, 3

AC PARAMETERS

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VEE Range: -4.2 to 5.7V, VCC=VCCA=GND, Loading: 50 ohms to -2.0V

tpLH/tpHL(1)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	CPc to Qn/$\overline{Qn}$	0.6	2.0	ns	9
			2, 4	CPc to Qn/$\overline{Qn}$	0.5	2.4	ns	10
			2, 4	CPc to Qn/$\overline{Qn}$	0.5	2.2	ns	11
tPLH/tPHL(2)	Propagation Delay	VEE=-4.2/-5.7V	2, 4	CPn to Qn/$\overline{Qn}$	0.6	2.0	ns	9
			2, 4	CPn to Qn/$\overline{Qn}$	0.5	2.4	ns	10
			2, 4	CPn to Qn/$\overline{Qn}$	0.5	2.2	ns	11

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VEE Range: -4.2 to 5.7V, VCC=VCCA=GND, Loading: 50 ohms to -2.0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tPLH/tPHL(3)	Propagation Delay	VEE=-4.2/-5.7V CPc, CPn = LOW	2, 4	CDn/SDn to Qn/$\overline{Qn}$	0.6	2.0	ns	9
			2, 4	CDn/SDn to Qn/$\overline{Qn}$	0.5	2.4	ns	10
			2, 4	CDn/SDn to Qn/$\overline{Qn}$	0.5	2.2	ns	11
tPLH/tPHL(4)	Propagation Delay	VEE=-4.2/-5.7V CPc, CPn = HIGH	2, 4	CDn/SDn to Qn/$\overline{Qn}$	0.6	2.1	ns	9
			2, 4	CDn/SDn to Qn/$\overline{Qn}$	0.5	2.5	ns	10
			2, 4	CDn/SDn to Qn/$\overline{Qn}$	0.5	2.4	ns	11
tPLH/tPHL(5)	Propagation Delay	VEE=-4.2/-5.7V CPc, CPn = LOW	2, 4	MS/MR to Qn/$\overline{Qn}$	0.8	2.6	ns	9
			2, 4	MS/MR to Qn/$\overline{Qn}$	0.8	2.9	ns	10
			2, 4	MS/MR to Qn/$\overline{Qn}$	0.7	2.7	ns	11
tPLH/tPHL(6)	Propagation Delay	VEE=-4.2/-5.7V CPc, CPn = HIGH	2, 4	MS/MR to Qn/$\overline{Qn}$	0.8	2.8	ns	9
			2, 4	MS/MR to Qn/$\overline{Qn}$	0.8	3.1	ns	10
			2, 4	MS/MR to Qn/$\overline{Qn}$	0.7	2.9	ns	11
tTLH/tTHL	Transistion Time	VEE=-4.2/-5.7V	6	Qn/$\overline{Qn}$	0.2	1.4	ns	9, 10, 11
tS	Set-up Time	VEE=-4.2/-5.7V	6	Dn to CPc/CPn	0.8		ns	9
			6	Dn to CPc/CPn	0.9		ns	10
			6	Dn to CPc/CPn	1.0		ns	11

Electrical Characteristics

AC PARAMETERS(Continued)

(The following conditions apply to all the following parameters, unless otherwise specified.)
AC: VEE Range: -4.2 to 5.7V, VCC=VCCA=GND, Loading: 50 ohms to -2.0V

SYMBOL	PARAMETER	CONDITIONS	NOTES	PIN-NAME	MIN	MAX	UNIT	SUB-GROUPS
tH	Hold Time	VEE=-4.2/-5.7V	6	Dn to CPc/CPn	1.3		ns	9
			6	Dn to CPc/CPn	1.6		ns	10
			6	Dn to CPc/CPn	1.5		ns	11
tREL	Release Time	VEE=-4.2/-5.7V	6	CDn/SDn	1.3		ns	9
			6	CDn/SDn	1.6		ns	10
			6	CDn/SDn	1.5		ns	11
		VEE= -4.2/-5.7V	6	MS/MR	2.3		ns	9
			6	MS/MR	2.5		ns	10, 11
tPW(H)	Pulse Width High	VEE= -4.2/-5.7V	6	CPc/CPn	2.0		ns	9, 10, 11
tPW(H) 1	Pulse Width High	VEE= -4.2/-5.7V	6	CDn/SDn	2.0		ns	9, 10, 11
tPW(H) 2	Pulse Width High	VEE= -4.2/-5.7V	6	MS/MR	2.0		ns	9, 10, 11
fMAX	Maximum Clock Frequency	VEE= -4.2/-5.7V	6	CPc/CPn	400		MHz	9, 10, 11

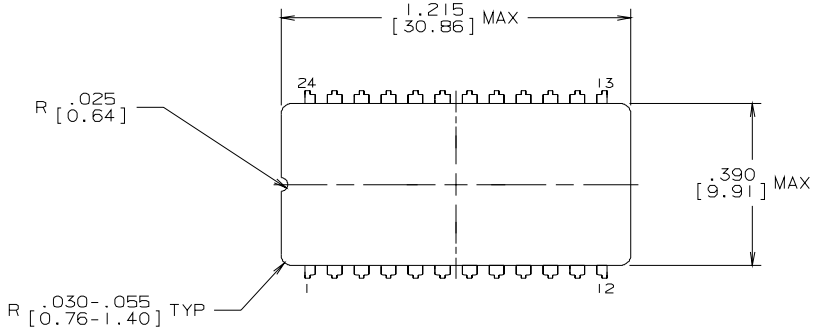
Note 1: Screen tested 100% on each device at -55 C, +25 C and +125 C temp., subgroups 1, 2, 3, 7 & 8.
Note 2: For QB devices, screen tested 100% on each device at +25C temperature only, subgroup A9. For QMLV devices, screen tested 100% on each device at +25C, +125C & -55C temperature, subgroups A9, 10 & 11.
Note 3: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, +125 C & -55 C temp., subgroups A1, 2, 3, 7 & 8.
Note 4: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C, subgroup A9, and at +125 C & -55 C temp., subgroups A10 & 11.
Note 5: Sample tested (Method 5005, Table 1) on each MFG. lot at +25 C temp. only, subgroup A9.
Note 6: Not tested at +25 C, +125 C & -55 C temp. (DESIGN CHARACTERIZATION DATA).
Note 7: Guaranteed by applying specified input condition and testing VOH/VOL.

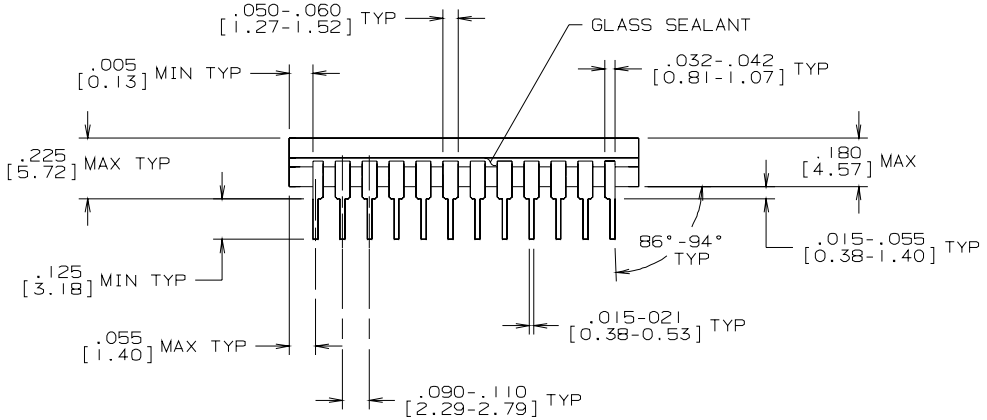
Graphics and Diagrams

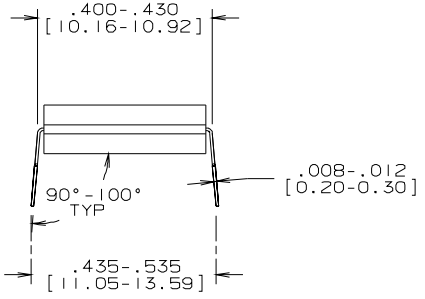
GRAPHICS#	DESCRIPTION
J24ERJ	CERDIP (J), 24LD, .400 CENTERS (P/P DWG)
P000060A	CERDIP (J), 24LD .400 CENTERS (PIN OUT)
P000061A	CERPACK, QUAD, 24 LEAD (PIN OUT)
W24BRE	CERPACK, QUAD, 24 LEAD (P/P DWG)

See attached graphics following this page.

REVISIONS				
LTR	DESCRIPTION	E.C.N.	DATE	BY/APP'D
J	REVISE AND REDRAW	09044	03/05/92	DEG/







NOTES: UNLESS OTHERWISE SPECIFIED

1. LEAD FINISH: SOLDER DIPPED WITH Sn60 OR Sn63 SOLDER CONFORMING TO MIL-M-38510 TO A MINIMUM THICKNESS OF 200 MICROINCHES/5.08 MICROMETERS. SOLDER MAY BE APPLIED OVER LEAD BASIS METAL OR Sn PLATE.
2. LEAD THICKNESS MAY BE INCREASED BY .003 [0.08] MAXIMUM AFTER LEAD FINISH APPLIED.
3. BUMPERS ARE AVAILABLE ON CERTAIN PRODUCTS. BUMPERS WILL ADD .040 [1.02] MAX TO THE LENGTH OF THE PACKAGE.
4. NO JEDEC REGISTRATION AS OF 2/17/92.

MIL/AERO CONFIGURATION CONTROL

MIL-M-38510 CONFIGURATION CONTROL

CONTROLLING DIMENSION: INCH

APPROVALS	DATE
DRAWN D.E.GRADY	03/05/92
DFTG. CHK.	
ENGR. CHK.	
APPROVAL	

PROJECTION INCH MM

NATIONAL SEMICONDUCTOR CORPORATION
2900 Semiconductor Drive, Santa Clara, CA 95052-8090

CERDIP (J), 24 LEAD, .400 CENTERS

SCALE	SIZE	DRAWING NUMBER	REV
N/A	C	MKT-J24E	J

FORMERLY: N/A

SHEET 1 OF 1

Revision History

Rev	ECN #	Rel Date	Originator	Changes
1B0	M0004381	04/23/04	Rose Malone	Updated MDS: MN100331-X, Rev. 1A0 to Rev. 1B0. Added NSID to Main Table and Features Section.