



Features

- ESD protected for 8 high speed I/O channels
- Provide ESD protection for each channel to IEC 61000-4-2 (ESD) $\pm 15\text{kV}$ (air) / $\pm 8\text{kV}$ (contact)
- For low operating voltage of 3.3V and below
- Ultra low capacitance: 0.10pF typical
- Fast turn-on and low clamping voltage
- Array of ESD rated diodes with internal equivalent TVS (Transient Voltage Suppression) diode
- Low leakage current
- Solid-state silicon-avalanche and active circuit triggering technology
- Simplified layout for high speed differential signaling channels
- **Green part**

Applications

- V-by-One
- LVDS Interface
- Thunderbolt
- USB 3.0 and USB 3.1
- DisplayPort Interface
- HDMI 1.3, 1.4 and 2.0 version

Description

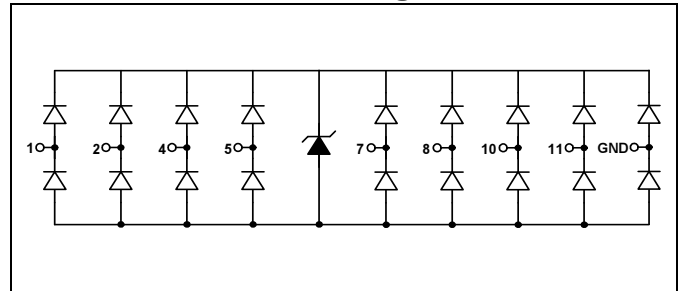
AZ1083-08F is a design which includes ESD rated diode arrays to protect high speed data interfaces in an electronic systems. The AZ1083-08F has been specifically designed to protect sensitive components which are connected to data and transmission lines from over-voltage damage and latch-up caused by Electrostatic Discharging (ESD).

AZ1083-08F is a unique design which includes low capacitance steering diodes and a unique design of clamping cell which is an equivalent TVS diode in a single package. During transient conditions, the steering diodes direct the

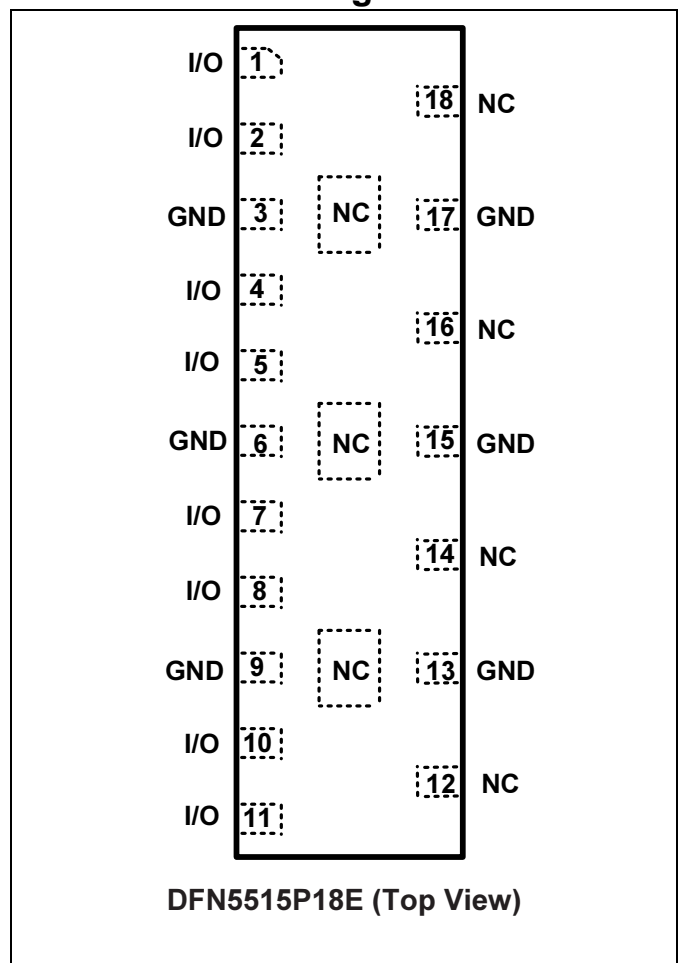
transient to the ground line, protecting any downstream components.

AZ1083-08F may be used to meet the ESD immunity requirements of IEC 61000-4-2, Level 4 ($\pm 15\text{kV}$ air, $\pm 8\text{kV}$ contact discharge).

Circuit Diagram



Pin Configuration





SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS			
PARAMETER	SYMBOL	RATING	UNITS
Peak Pulse Current (tp =8/20μs)	I _{PP}	3	A
Operating Voltage (I/O pin-GND)	V _{DC}	±3.6	V
ESD per IEC 61000-4-2 (Air)	V _{ESD}	±15	kV
ESD per IEC 61000-4-2 (Contact)		±8	
Lead Soldering Temperature	T _{SOL}	260 (10 sec.)	°C
Operating Temperature	T _{OP}	-55 to +85	°C
Storage Temperature	T _{STO}	-55 to +150	°C

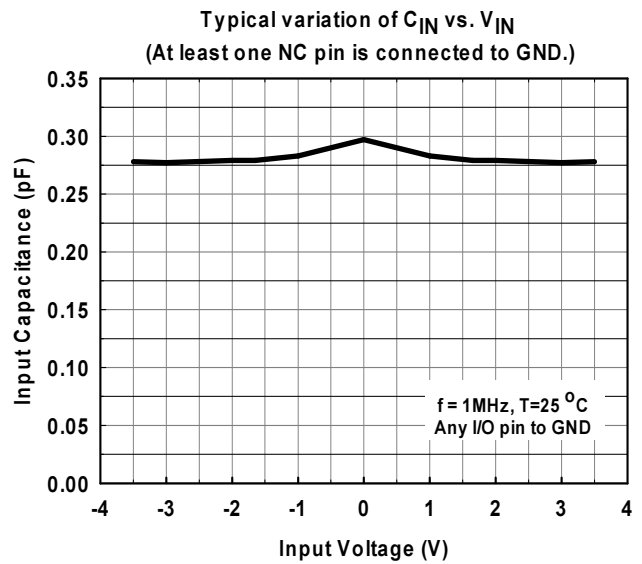
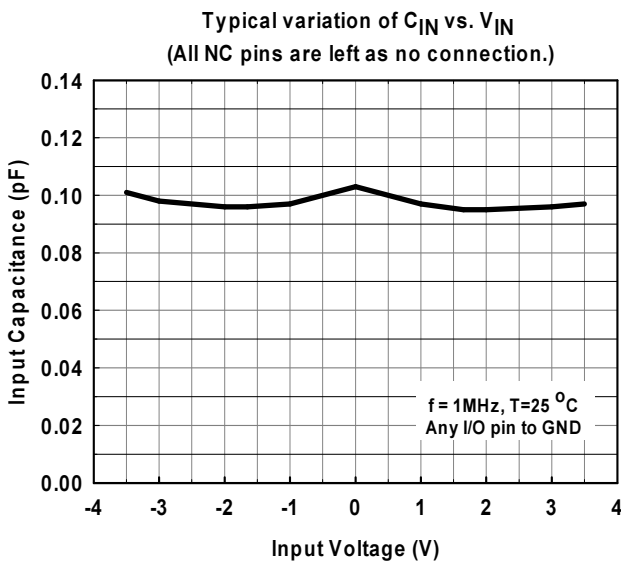
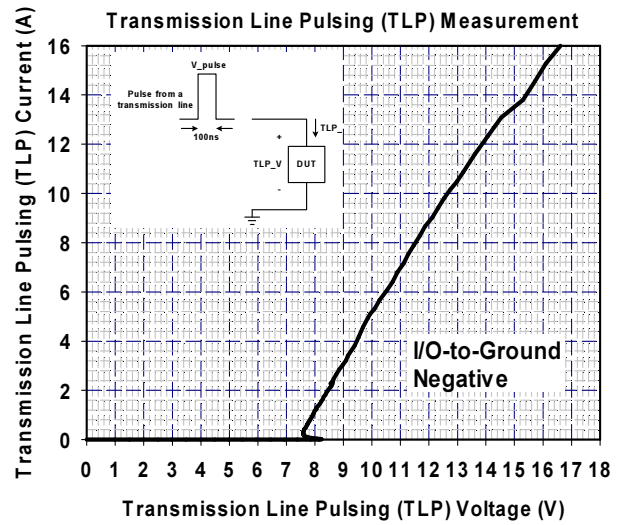
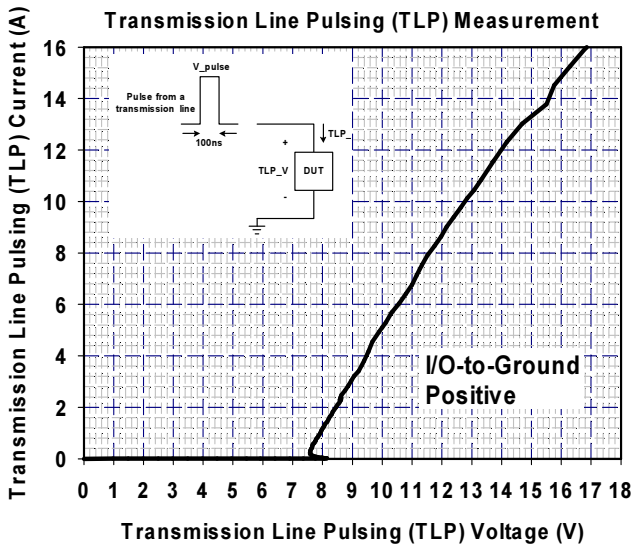
ELECTRICAL CHARACTERISTICS						
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Reverse Stand-Off Voltage	V _{RWM}	Any I/O Pin to GND, T=25 °C.			3.3	V
Channel Leakage Current	I _{Leak}	V _{RWM} = 3.3V, T=25 °C, Any I/O Pin to GND			0.5	μA
Reverse Breakdown Voltage	V _{BV}	I _{BV} = 1mA, T=25 °C, Any I/O Pin to GND	4.5	7.0		V
ESD Clamping Voltage (Note 1)	V _{clamp}	IEC 61000-4-2 +8kV (I _{TLP} = 16A), T=25 °C, Contact mode, Any Channel pin to Ground		16.5		V
Channel Input Capacitance	C _{IN}	V _R = 1.65V, f = 1MHz, T=25 °C. All NC pins are No Connection (Note 2), Any I/O Pin to GND		0.10	0.13	pF
		V _R = 1.65V, f = 1MHz, T=25 °C. At least one of NC pin is connected to GND (Note 3), Any I/O Pin to GND		0.28	0.35	pF

Note 1: ESD Clamping Voltage was measured by Transmission Line Pulsing (TLP) System.

TLP conditions: Z₀= 50Ω, t_p= 100ns, t_r= 1ns.

Note 2: Please refer to Fig. 1 in page 4.

Note 3: Please refer to Fig. 2 in page 5.



Applications

A. Device Connection

The AZ1083-08F is designed to protect 8 high speed data lines from transient over-voltage (such as ESD stress pulse). The typical device connection of AZ1083-08F is shown in the Fig. 1. In Fig. 1, the 8 protected high speed data lines are connected to the ESD protection pins (pin1, pin2, pin4, pin5, pin7, pin8, pin10, and pin11) of AZ1083-08F. The AZ1083-08F is designed for allowing the traces to run straight through the device to simplify the PCB layout. The ground pins (pin3, pin6, pin9, pin13, pin15, and pin17) of AZ1083-08F are negative reference pins. **All of these pins should be directly connected to the GND rail**

of PCB. To get minimum parasitic inductance, the path length should keep as short as possible. The NC pins (pin12, pin14, pin16, pin18, and center-taps) of AZ1083-08F are left as no connection to minimize the parasitic capacitance.

The center-taps of AZ1083-08F can be connected to GND rail of PCB to minimize crosstalk between signals but with higher parasitic capacitance, which is shown in Fig. 2.

AZ1083-08F can provide ESD protection for 8 I/O signal lines simultaneously. If the number of I/O signal lines is less than 8, the unused I/O pins can be left as NC pins.

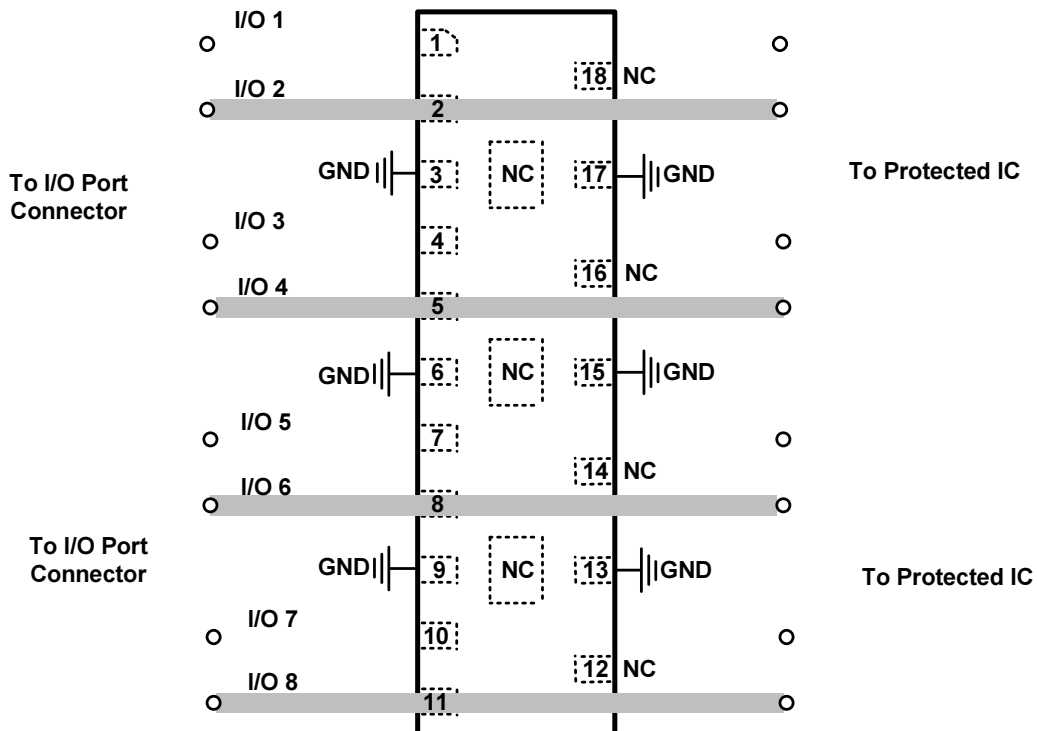


Fig. 1 Data lines connection of AZ1083-08F. All of the NC pins are left as no connection.

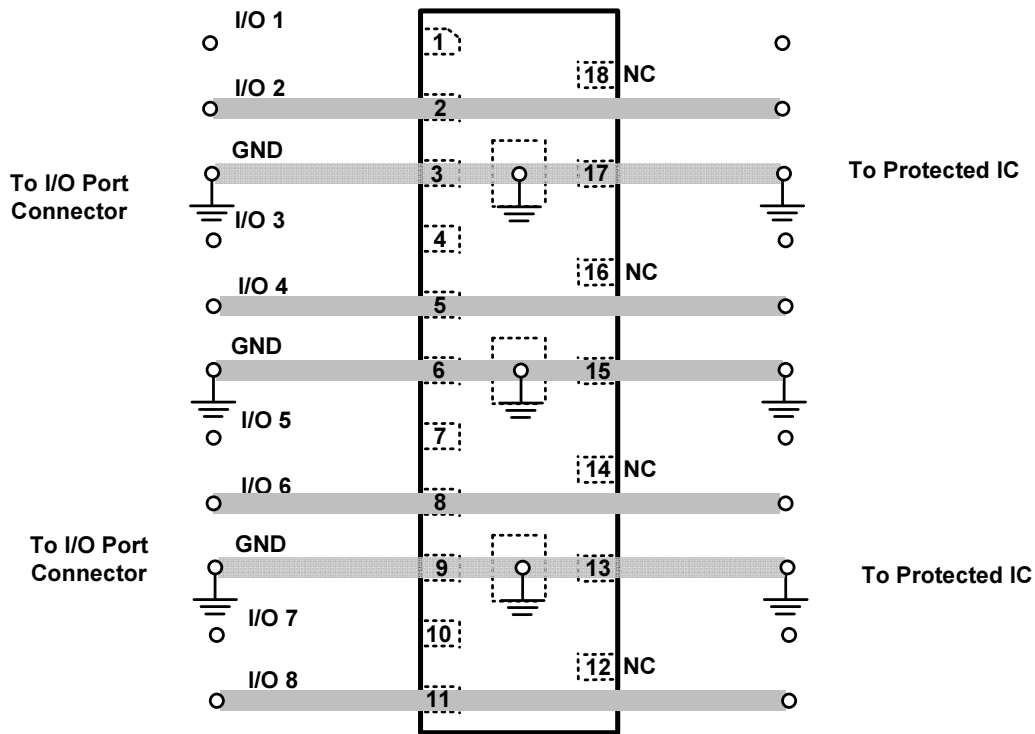


Fig. 2 Data lines connection of AZ1083-08F. The center-taps are connected to GND.



B. V-by-One Application

Fig. 3 shows how to implement the AZ1083-08F in a V-by-One application. The AZ1083-08F is designed for allowing the traces to run straight through the device to simplify the PCB layout. As shown in Fig. 3, the best way to design the PCB trace is using the flow through layout. The gray lines represent the PCB traces. The ground pins (pin3, pin6, pin9, pin13, pin15, and pin17) of AZ1083-08F are negative

reference pins. **All of these pins should be directly connected to the GND rail of PCB.** To get minimum parasitic inductance, the path length should keep as short as possible. The NC pins (pin12, pin14, pin16, pin18, and center-taps) of AZ1083-08F are left as no connection to minimize the parasitic capacitance.

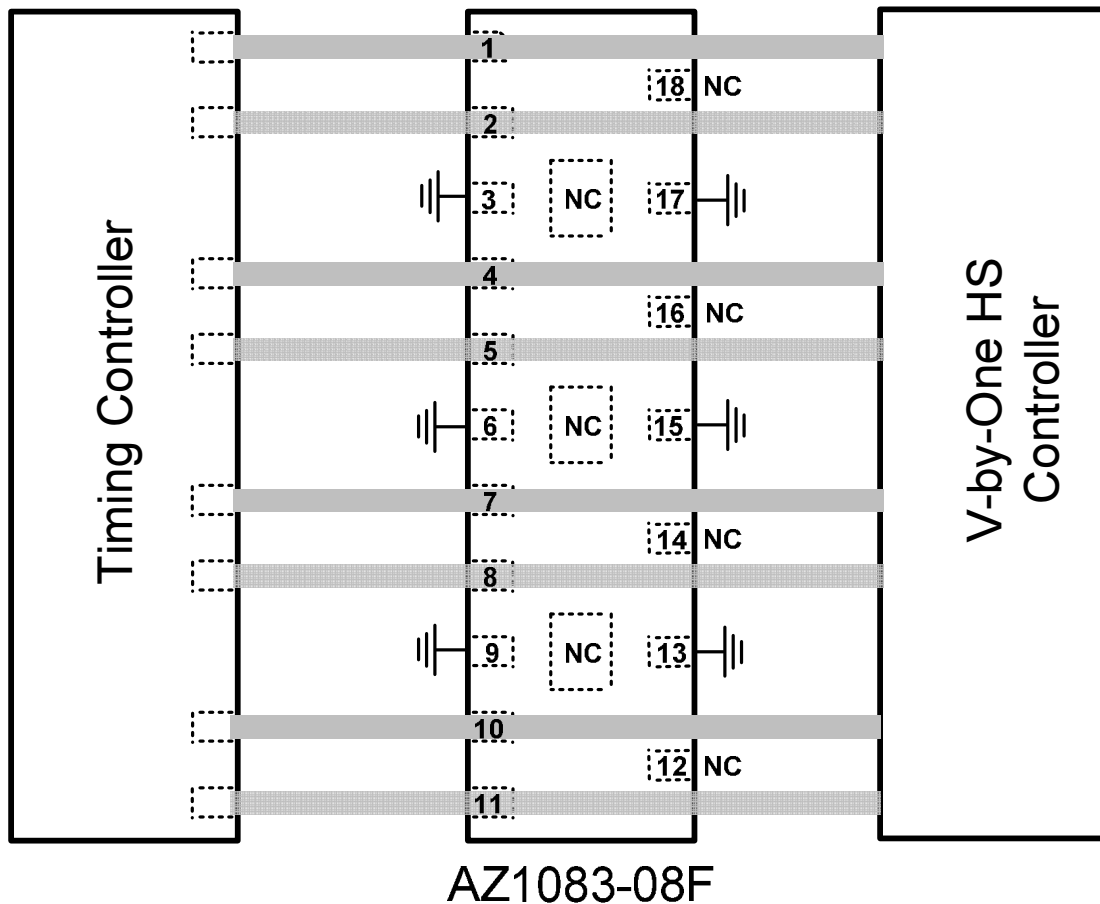


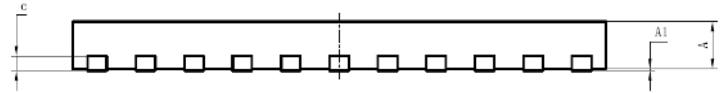
Fig. 3 V-by-One HS layout diagram (for LCD panel).

Mechanical Details

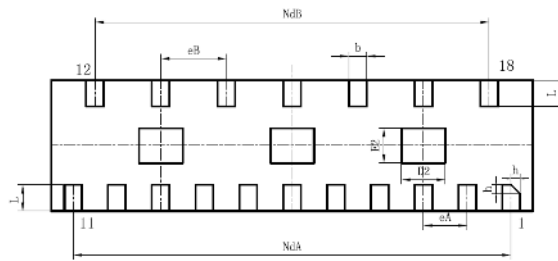
DFN5515P18E PACKAGE DIAGRAMS



Top View



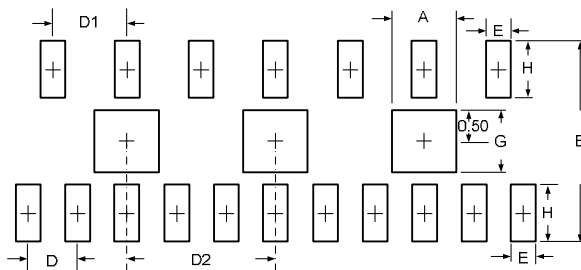
Side View



Bottom View

Symbol	Millimeters		
	min	nom	max
A	0.45	0.50	0.55
A1	0.00	0.02	0.05
b	0.15	0.20	0.25
c	0.10	0.15	0.20
D	5.45	5.50	5.55
E	1.45	1.50	1.55
NdA	5.00BSC		
eA	0.50BSC		
eB	0.75BSC		
NdB	4.50BSC		
D2	0.45	0.50	0.55
E2	0.35	0.40	0.45
L	0.20	0.30	0.40
h	0.05	0.10	0.15

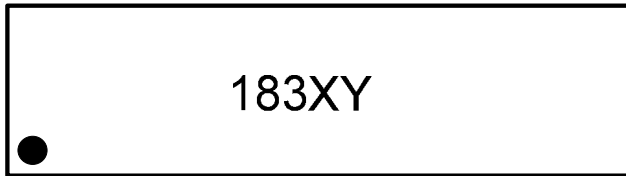
Land Layout



DIMENSIONS	
DIM	MILLIMETERS
A	0.60
B	1.80
D	0.50
D1	0.75
D2	1.50
E	0.30
G	0.50
H	0.50



MARKING CODE



183 = Device Code
X = Date Code
Y = Control Code

Part Number	Marking Code
AZ1083-08F (Green Part)	183XY

Note : Green means Pb-free, RoHS, and Halogen free compliant.

Ordering Information

PN#	Material	Type	Reel size	MOQ	MOQ/internal box	MOQ/carton
AZ1083-08F.R7G	Green	T/R	7 inch	3,000/reel	3 reel= 9,000/box	6 box =54,000/carton

Revision History

Revision	Modification Description
Revision 2014/06/16	Preliminary Release.
Revision 2015/01/30	1. Add "Peak Pulse Current". 2. Add ordering information.
Revision 2015/11/20	Formal Release.
Revision 2016/01/14	Update the marking code.