



# Automotive N-Channel 300 V (D-S) 175 °C MOSFET

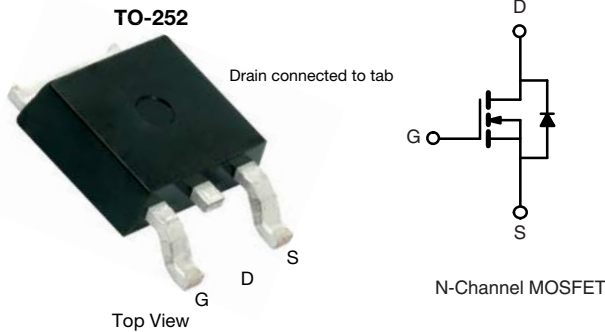


RoHS COMPLIANT HALOGEN FREE

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	300
R <sub>DS(on)</sub> (Ω) at V <sub>GS</sub> = 10 V	0.330
I <sub>D</sub> (A)	10
Configuration	Single

## FEATURES

- TrenchFET® power MOSFET
- Package with low thermal resistance
- AEC-Q101 qualified <sup>d</sup>
- 100 % R<sub>g</sub> tested
- Material categorization: for definitions of compliance please see [www.vishay.com/doc?99912](http://www.vishay.com/doc?99912)



ORDERING INFORMATION	
Package	TO-252
Lead (Pb)-free and Halogen-free	SQD10N30-330H-GE3

ABSOLUTE MAXIMUM RATINGS (T <sub>C</sub> = 25 °C, unless otherwise noted)				
PARAMETER		SYMBOL	LIMIT	UNIT
Drain-Source Voltage		V <sub>DS</sub>	300	V
Gate-Source Voltage		V <sub>GS</sub>	± 30	
Continuous Drain Current	T <sub>C</sub> = 25 °C	I <sub>D</sub>	10	A
	T <sub>C</sub> = 125 °C		5	
Continuous Source Current (Diode Conduction) <sup>a</sup>		I <sub>S</sub>	50	
Pulsed Drain Current <sup>b</sup>		I <sub>DM</sub>	16	
Single Pulse Avalanche Current <sup>e</sup>	L = 0.05 mH	I <sub>AS</sub>	12.65	
Single Pulse Avalanche Energy <sup>e</sup>		E <sub>AS</sub>	4	
Maximum Power Dissipation <sup>b</sup>	T <sub>C</sub> = 25 °C	P <sub>D</sub>	107	W
	T <sub>C</sub> = 125 °C		35	
Operating Junction and Storage Temperature Range		T <sub>J</sub> , T <sub>stg</sub>	-55 to +175	°C

THERMAL RESISTANCE RATINGS				
PARAMETER		SYMBOL	LIMIT	UNIT
Junction-to-Ambient	PCB Mount <sup>c</sup>	R <sub>thJA</sub>	50	°C/W
Junction-to-Case (Drain)		R <sub>thJC</sub>	1.4	

### Notes

- Package limited.
- Pulse test; pulse width ≤ 300 μs, duty cycle ≤ 2 %.
- When mounted on 1" square PCB (FR4 material).
- Parametric verification ongoing.
- 1.5 kΩ resistance in series with the gate.



SPECIFICATIONS ( $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted)							
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT	
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	300	-	-	V	
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	3.4	3.8	4.4		
Gate-Source Leakage	$I_{GSS}$	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 30\text{ V}$	-	-	$\pm 100$	nA	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 300\text{ V}$	-	-	1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$	$V_{DS} = 300\text{ V}$ , $T_J = 125\text{ }^\circ\text{C}$	-	-	50	
		$V_{GS} = 0\text{ V}$	$V_{DS} = 300\text{ V}$ , $T_J = 175\text{ }^\circ\text{C}$	-	-	250	
On-State Drain Current <sup>a</sup>	$I_{D(on)}$	$V_{GS} = 10\text{ V}$	$V_{DS} \geq 5\text{ V}$	10	-	-	A
Drain-Source On-State Resistance <sup>a</sup>	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 14\text{ A}$	-	0.275	0.330	$\Omega$
		$V_{GS} = 10\text{ V}$	$I_D = 14\text{ A}$ , $T_J = 125\text{ }^\circ\text{C}$	-	-	0.733	
		$V_{GS} = 10\text{ V}$	$I_D = 14\text{ A}$ , $T_J = 175\text{ }^\circ\text{C}$	-	-	1.000	
Forward Transconductance <sup>b</sup>	$g_{fs}$	$V_{DS} = 15\text{ V}$ , $I_D = 14\text{ A}$		-	26	-	S
<b>Dynamic <sup>b</sup></b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$	-	1749	2190	$\mu\text{F}$
Output Capacitance	$C_{oss}$			-	112	140	
Reverse Transfer Capacitance	$C_{rss}$			-	44	55	
Total Gate Charge <sup>c</sup>	$Q_g$	$V_{GS} = 10\text{ V}$	$V_{DS} = 150\text{ V}$ , $I_D = 7\text{ A}$	-	31	47	nC
Gate-Source Charge <sup>c</sup>	$Q_{gs}$			-	8	-	
Gate-Drain Charge <sup>c</sup>	$Q_{gd}$			-	9.6	-	
Gate Resistance	$R_g$	$f = 1\text{ MHz}$		0.4	0.8	3	$\Omega$
Turn-On Delay Time <sup>c</sup>	$t_{d(on)}$	$V_{DD} = 150\text{ V}$ , $R_L = 21\text{ }\Omega$ $I_D \cong 7\text{ A}$ , $V_{GEN} = 10\text{ V}$ , $R_g = 1\text{ }\Omega$		-	10	15	ns
Rise Time <sup>c</sup>	$t_r$			-	18	28	
Turn-Off Delay Time <sup>c</sup>	$t_{d(off)}$			-	20	30	
Fall Time <sup>c</sup>	$t_f$			-	8	12	
<b>Source-Drain Diode Ratings and Characteristics <sup>b</sup></b>							
Pulsed Current <sup>a</sup>	$I_{SM}$			-	-	16	A
Forward Voltage	$V_{SD}$	$I_F = 25\text{ A}$ , $V_{GS} = 0\text{ V}$		-	0.9	1.5	V

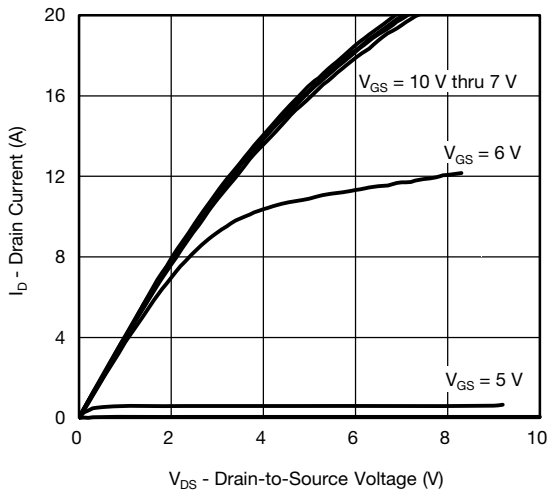
**Notes**

- a. Pulse test; pulse width  $\leq 300\text{ }\mu\text{s}$ , duty cycle  $\leq 2\%$ .  
b. Guaranteed by design, not subject to production testing.  
c. Independent of operating temperature.

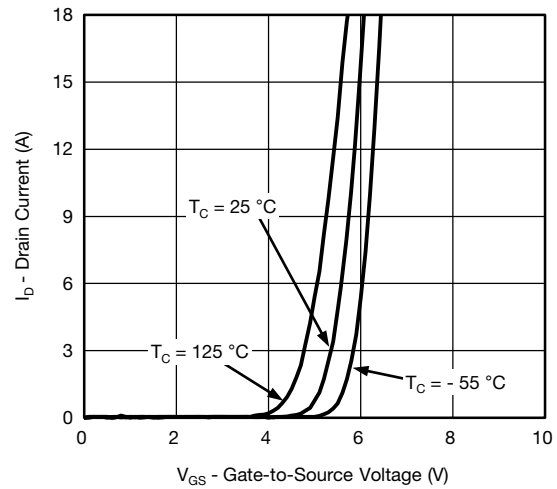
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



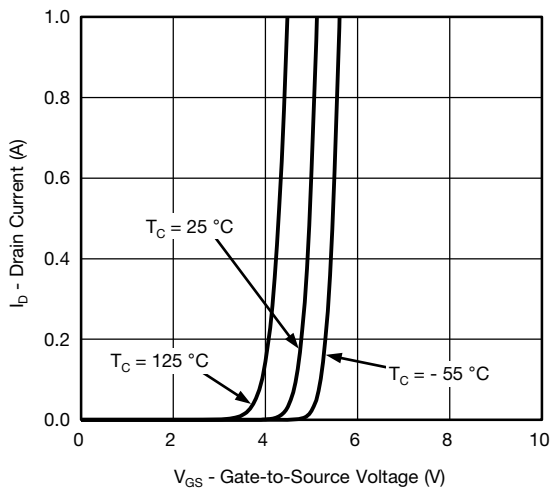
### TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



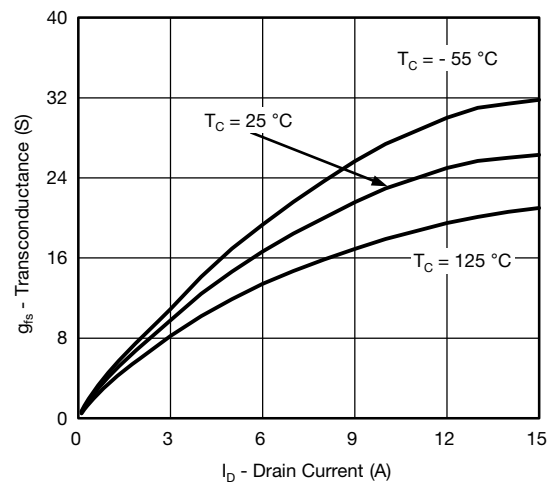
**Output Characteristics**



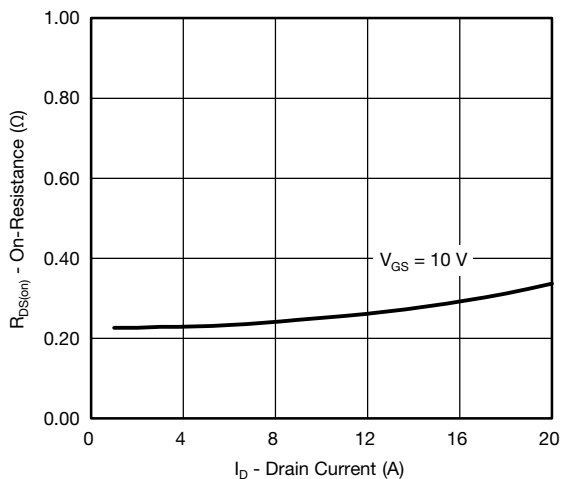
**Transfer Characteristics**



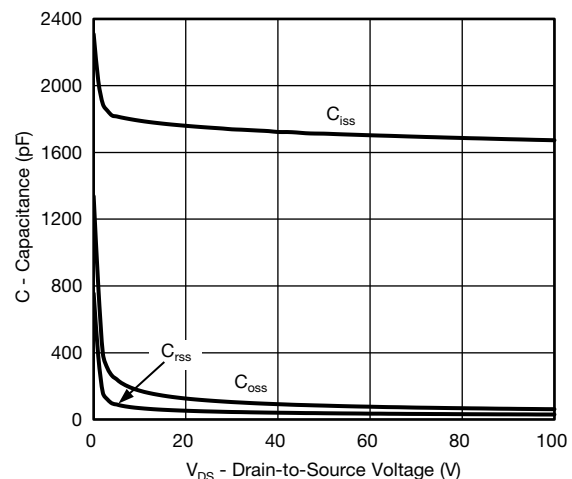
**Transfer Characteristics**



**Transconductance**



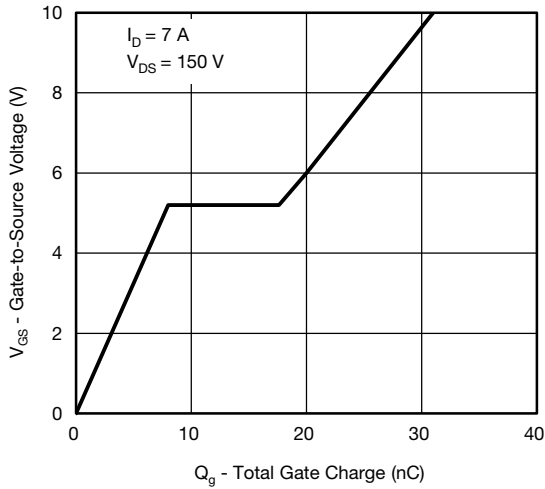
**On-Resistance vs. Drain Current**



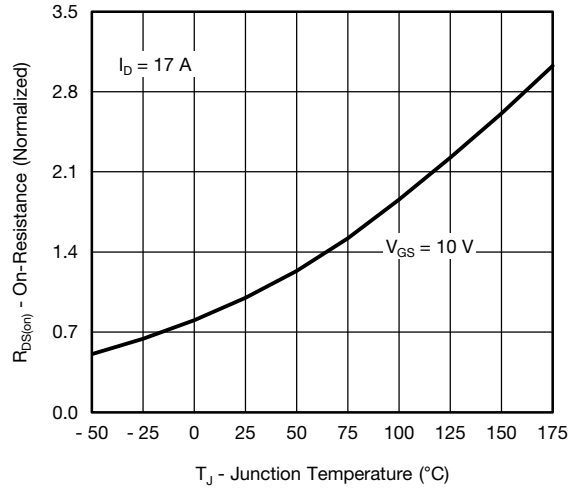
**Capacitance**



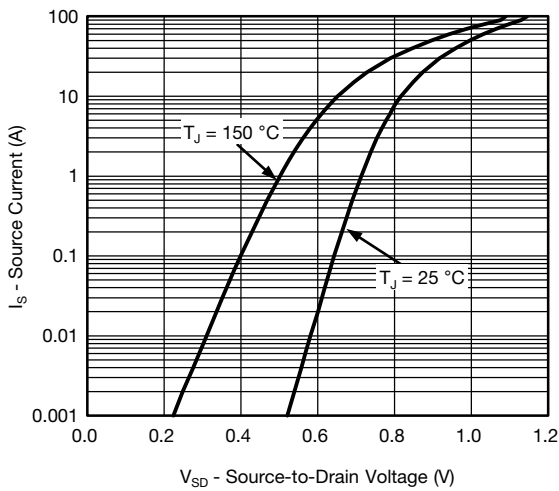
TYPICAL CHARACTERISTICS (T<sub>A</sub> = 25 °C, unless otherwise noted)



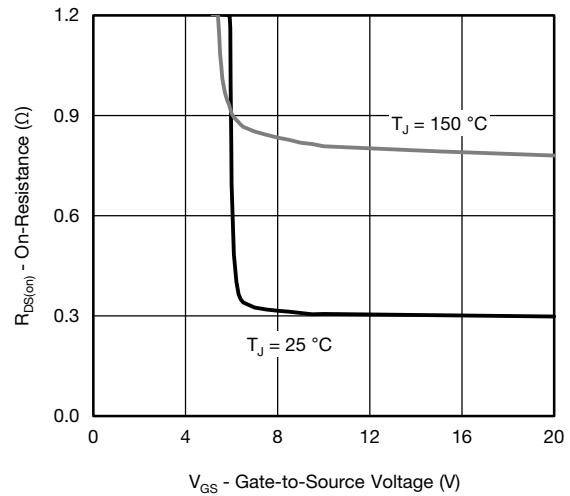
Gate Charge



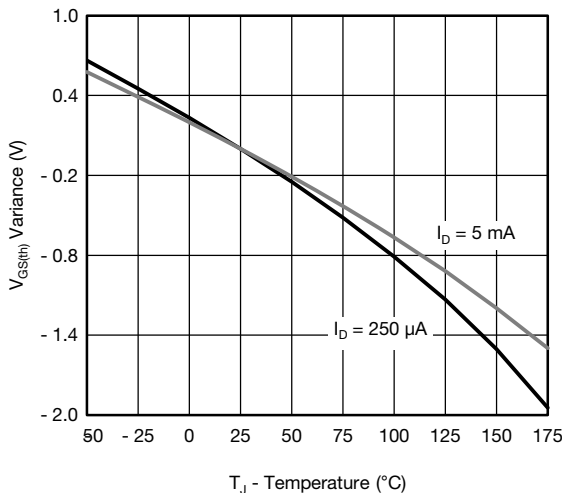
On-Resistance vs. Junction Temperature



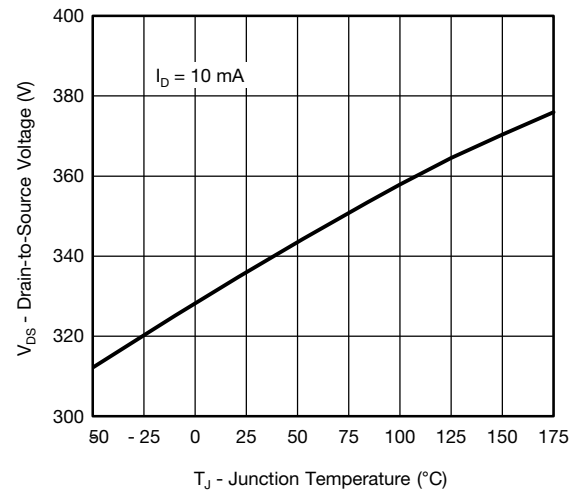
Source Drain Diode Forward Voltage



On-Resistance vs. Gate-to-Source Voltage



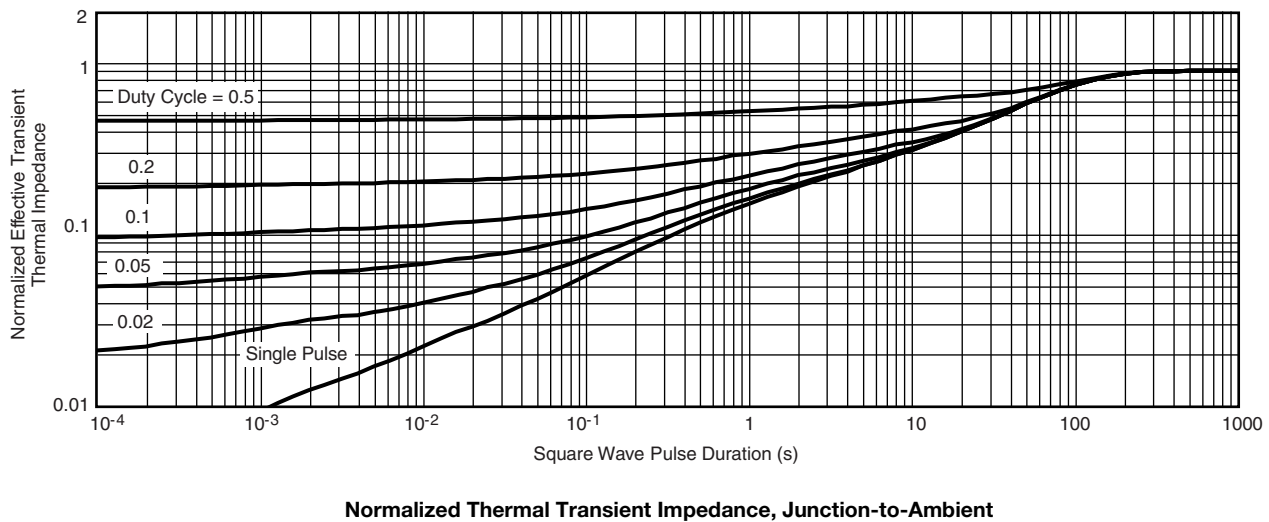
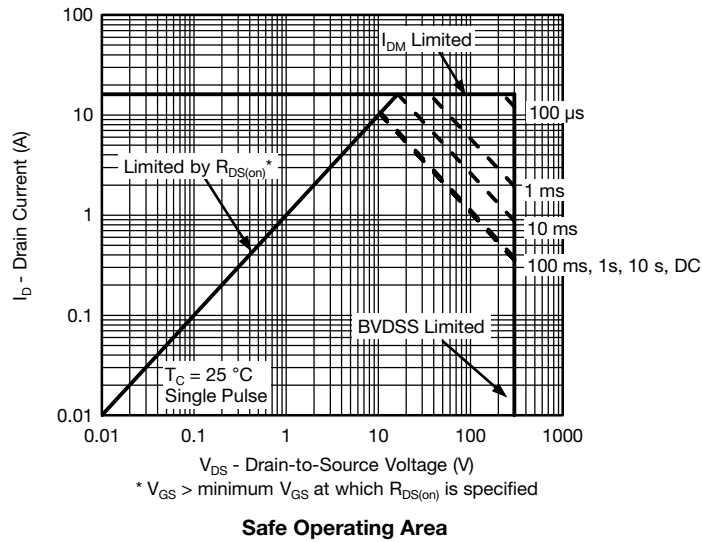
Threshold Voltage



Drain Source Breakdown vs. Junction Temperature

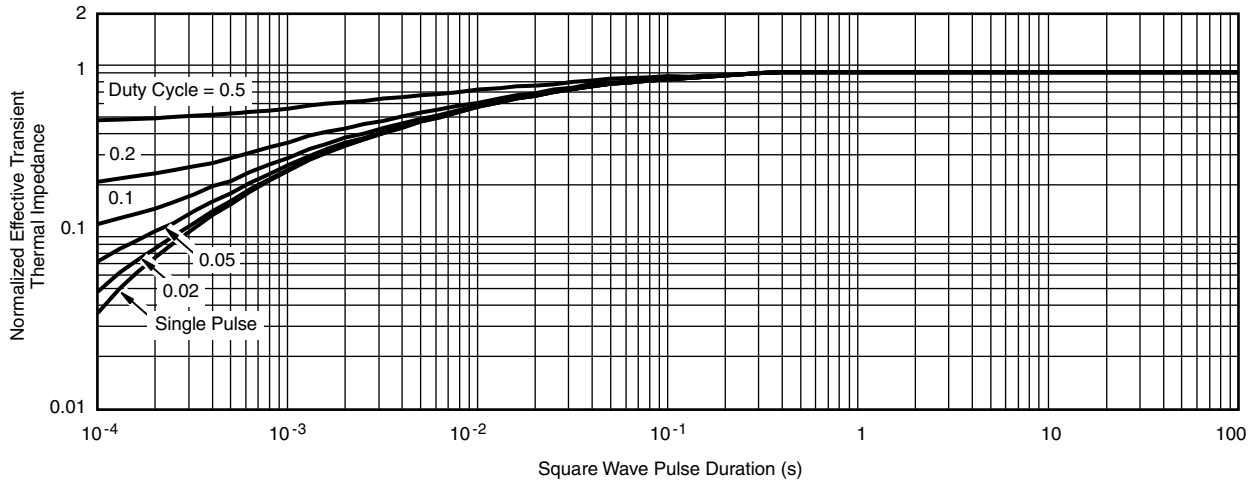


**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)





**THERMAL RATINGS** ( $T_A = 25\text{ }^\circ\text{C}$ , unless otherwise noted)



**Normalized Thermal Transient Impedance, Junction-to-Case**

**Note**

- The characteristics shown in the two graphs
    - Normalized Transient Thermal Impedance Junction-to-Ambient (25 °C)
    - Normalized Transient Thermal Impedance Junction-to-Case (25 °C)
- are given for general guidelines only to enable the user to get a “ball park” indication of part capabilities. The data are extracted from single pulse transient thermal impedance characteristics which are developed from empirical measurements. The latter is valid for the part mounted on printed circuit board - FR4, size 1" x 1" x 0.062", double sided with 2 oz. copper, 100 % on both sides. The part capabilities can widely vary depending on actual application parameters and operating conditions.

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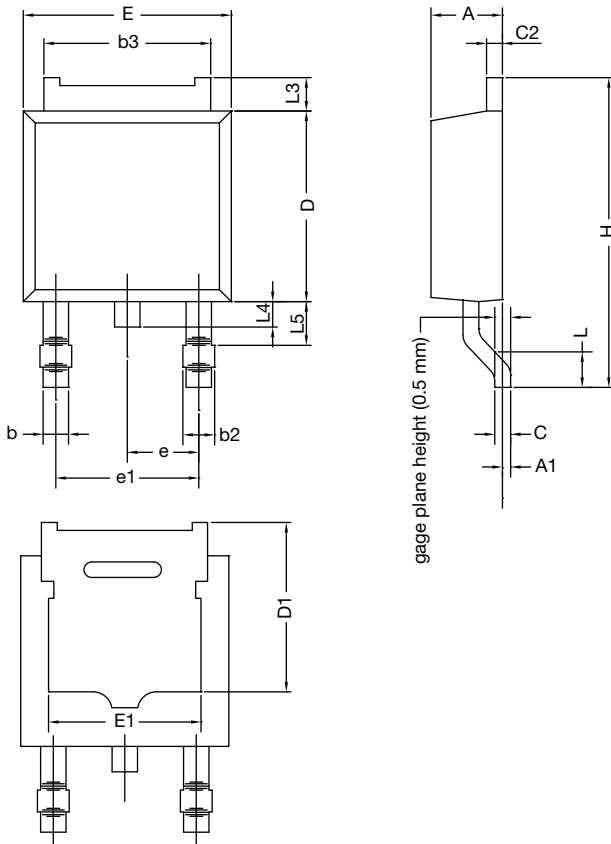
REVISION HISTORY <sup>a</sup>		
REVISION	DATE	DESCRIPTION OF CHANGE
B	26-Feb-2015	• UIS changed
C	04-May-2015	• $R_g$ , $C_{iss}$ and $t_r$ updated

**Note**

a. As of April 2014



### TO-252AA Case Outline



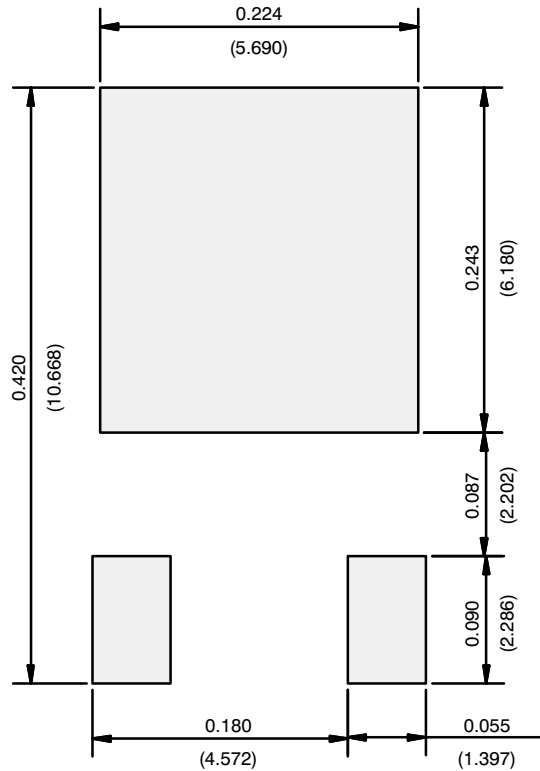
DIM.	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	2.18	2.38	0.086	0.094
A1	-	0.127	-	0.005
b	0.64	0.88	0.025	0.035
b2	0.76	1.14	0.030	0.045
b3	4.95	5.46	0.195	0.215
C	0.46	0.61	0.018	0.024
C2	0.46	0.89	0.018	0.035
D	5.97	6.22	0.235	0.245
D1	4.10	-	0.161	-
E	6.35	6.73	0.250	0.265
E1	4.32	-	0.170	-
H	9.40	10.41	0.370	0.410
e	2.28 BSC		0.090 BSC	
e1	4.56 BSC		0.180 BSC	
L	1.40	1.78	0.055	0.070
L3	0.89	1.27	0.035	0.050
L4	-	1.02	-	0.040
L5	1.01	1.52	0.040	0.060
ECN: T13-0592-Rev. A, 02-Sep-13 DWG: 6019				

**Note**

- Dimension L3 is for reference only.



## RECOMMENDED MINIMUM PADS FOR DPAK (TO-252)



Recommended Minimum Pads  
Dimensions in Inches/(mm)

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