Programmable Transimpedance, Current to Bits Receiver μModule

Data Sheet

ADA4355

FEATURES

- High performance, current input, data acquisition μModule that includes a TIA, analog filter, ADC driver, and ADC
  - 3 selectable T_Z settings: 2 kΩ, 20 kΩ, and 200 kΩ
  - Internal 1.8 V LDO for the ADC
  - All passive components including supply decoupling
- Small form factor: 12.00 mm × 6.00 mm CSP_BGA
- Operation from a single 3.3 V supply
- Full-scale input current to 800 μA (T_Z = 2 kΩ)
- Fast input overload recovery
- High analog input current to 40 mA
- Analog filter for noise reduction and antialias filtering
  - Selectable 1.0 MHz and 100 MHz LPF bandwidth
- Low input referred current noise: 16 pA rms
  - T_Z = 200 kΩ, 65,536 averages, 1 MHz analog filter
- Supports input pulse widths down to 10 ns
- 14-bit ADC with sample rate up to 125 MSPS
  - Serial LVDS data output
  - SPI control interface
- Quiescent power: 546 mW, LDO enabled
- Temperature range: −40°C to +85°C

APPLICATIONS

- Current to voltage conversion
- Chemical analyzers
- Mass spectroscopy
- Time of Flight
- Fiber optic sensing
- OTDR
  - Optical amplifiers
  - Reconfigurable optical add and drop multiplexers (ROADM)

GENERAL DESCRIPTION

The ADA4355 is a complete, high performance, current input μModule®. For space savings, the ADA4355 includes all the required active and passive components to realize a complete current to bits data acquisition solution, supporting a small form factor, optical modules as well as multichannel systems.

The high speed transimpedance amplifier (TIA) of the device supports 10 ns pulse widths, allowing high spatial resolution for Time of Flight (ToF) measurements. Additionally, the ADA4355 includes three TIA gain (T_Z) settings to maximize dynamic range. An internal, selectable, analog low-pass filter (LPF) can limit the device bandwidth with a corner frequency of 100 MHz to minimize broadband noise while also serving as an antialiasing filter for the 125 MSPS ADC. For lower bandwidth signals, or wider signal pulses (for example, 20 μs or wider), the filter can be set to a corner frequency of 1.0 MHz to provide additional noise reduction.

The 14-bit ADC converts the amplified voltage signal at a rate of up to 125 MSPS and outputs the digitized signals through two serial, low voltage differential signaling (LVDS) data lanes, operating at rates of up to 1 Gbps per lane. The data clock output (DCO) operates at frequencies of up to 500 MHz and supports double data rate (DDR) operation.

The ADA4355 exhibits fast overdrive recovery from a large input current signal and is available in a 12.00 mm × 6.00 mm CSP_BGA package with a −40°C to +85°C operating temperature range.

FUNCTIONAL BLOCK DIAGRAM

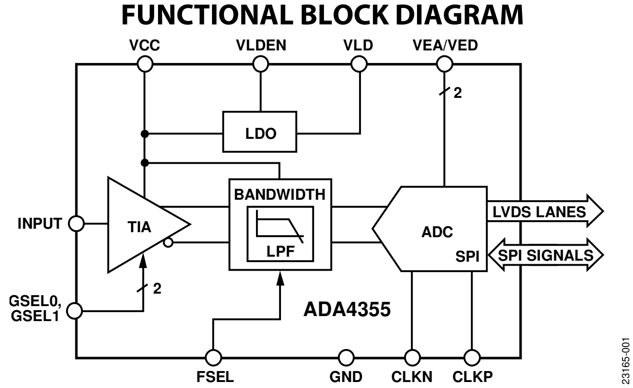

Figure 1.

Rev. A Document Feedback

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REVISION HISTORY

10/2020—Revision A: Initial Version

SPECIFICATIONS

PERFORMANCE SPECIFICATIONS

T_A = 25°C, VCC = 3.3 V, LDO enabled (see the power connection scheme shown in Figure 3), FSEL = 0, and the source capacitance (C_S) = 0.5 pF, unless otherwise noted.

Table 1.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
INPUT					
Input Referred Current Noise, I_N	T_Z = 2 kΩ		159		nA rms
	T_Z = 20 kΩ		32		nA rms
	T_Z = 200 kΩ, FSEL = 1		4		nA rms
	T_Z = 2 kΩ, 65,536 averages		621		pA rms
	T_Z = 20 kΩ, 65,536 averages		125		pA rms
	T_Z = 200 kΩ, 65,536 averages, FSEL = 1		16		pA rms
Input Voltage, V_{IN}	See Figure 2		1.65		V
Input Bias Current, I_B			±1		nA
Linear Input Current Range, I_{IN}	T_Z = 2 kΩ		−80 to +800		μA
	T_Z = 20 kΩ		−8.0 to +80		μA
	T_Z = 200 kΩ		−0.8 to +8.0		μA
T_Z Gain Accuracy	All gains		±1	±5	%
Input Capacitance			2.0		pF
ADC Input Bias Voltage	All gains, see Figure 2, I_{IN} = 0 μA		825		mV
AC PERFORMANCE					
Input Referred Supply Sensitivity	All gains		0.5		nA/mV
TIA Bandwidth	T_Z = 2 kΩ		43		MHz
	T_Z = 20 kΩ		18		MHz
	T_Z = 200 kΩ		1.6		MHz
LPF Bandwidth	FSEL = 0		100		MHz
	FSEL = 1		1.0		MHz
ADC PERFORMANCE					
ADC Internal Reference Voltage (VREF)		0.98	1	1.02	V
Resolution		14			Bits
Sampling Rate		20		125	MSPS
No Missing Codes			Guaranteed		
DIGITAL OUTPUTS, ANSI-644					
Logic Compliance			LVDS		
Differential Output Voltage, V_{OD}		290	345	400	mV
Output Offset Voltage, V_{OS}		1.15	1.25	1.35	V
Output Coding (Default)			Twos complement		
OPERATION TEMPERATURE RANGE		−40		+85	°C

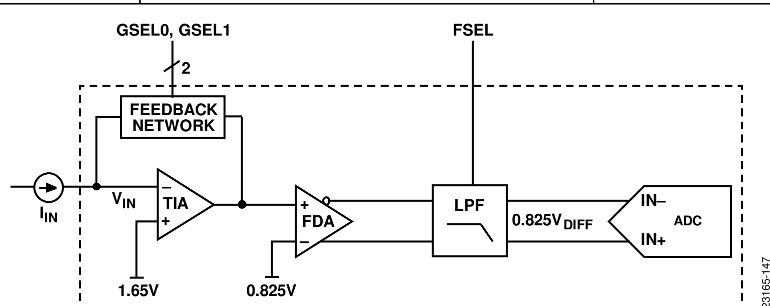


Figure 2. Internal Bias Voltages (FDA Is a Fully Differential Amplifier.)

POWER SPECIFICATIONS

T_A = 25°C and VCC = 3.3 V, unless otherwise noted. VEA and VED are the internal ADC 1.8 V supply rails, and VLD is the 1.8 V on-board LDO output.

Table 2.

Parameter	Symbol	Test Conditions/Comments	Min	Typ	Max	Unit
POWER SUPPLIES	VCC		3.1	3.3	3.6	V
VCC Current	I_{VCC}	See Figure 3, LDO enabled		165		mA
		See Figure 4, LDO disabled		72		mA
ADC Digital Circuit Supply	VED	See Figure 4, LDO disabled		1.8 ± 5%		V
VED Current	I_{VED}			47		mA
ADC Analog Circuit Supply	VEA	See Figure 4, LDO disabled		1.8 ± 5%		V
VEA Current	I_{VEA}			47		mA
On-Chip LDO Output	VLD	See Figure 3, LDO enabled		1.8		V
Quiescent Power	P_Q	See Figure 3, LDO enabled		546		mW
		See Figure 4, LDO disabled		406		mW
		ADC power-down mode		238		mW
		ADC standby mode		322		mW

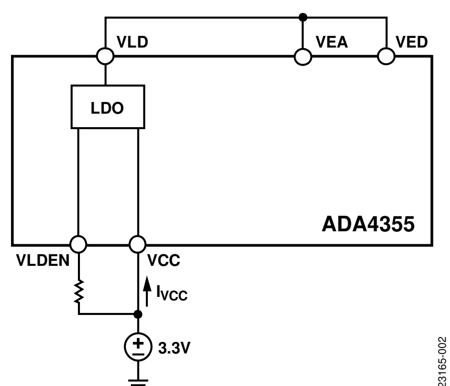


Figure 3. On-Chip LDO Enabled

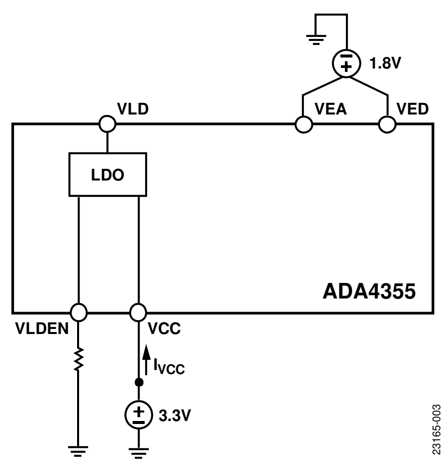


Figure 4. On-Chip LDO Disabled

CLK, SPI, AND CONTROL SPECIFICATIONS

T_A = 25°C, VCC = 3.3 V, and LDO enabled (see the power scheme shown in Figure 3), unless otherwise noted.

Table 3.

Parameter	Test Conditions/Comments	Min	Typ	Max	Unit
CLOCK INPUTS (CLKP AND CLKN)					
External Clock Frequency		10		1000	MHz
Conversion Rate		10		125	MSPS
Logic Compliance			CMOS/LVDS/LVPECL		
Differential Input Voltage	For LVDS and LVPECL	0.2		3.6	V p-p
Input Voltage Range		GND − 0.2		VEA + 0.2	V
Input Common-Mode Voltage			0.9		V
Input Resistance (Differential)			15		kΩ
Input Capacitance, C_{IN}			4		pF
SERIAL PORT INTERFACE (SPI) CLOCK					
SCLK Frequency				25	MHz
SPI INPUTS (SCLK, $\overline{CS}$, AND SDIO)					
Input High Voltage, V_{INH}		1.2		VEA + 0.2	V
Input Low Voltage, V_{INL}		0		0.8	V
SCLK					
Input Resistance, R_{IN}			30		kΩ
C_{IN}			2		pF
$\overline{CS}$					
R_{IN}			26		kΩ
C_{IN}			2		pF
SDIO					
R_{IN}			26		kΩ
C_{IN}			5		pF
SPI OUTPUT (SDIO)					
Logic 1 Output Voltage	High output current (I_{OH}) = 800 µA		1.79		V
Logic 0 Output Voltage	Low output current (I_{OL}) = 50 µA			0.05	V
OTHER CONTROL INPUTS (GSEL0, GSEL1, FSEL, AND VLDEN)					
V_{INH}		2		VCC	V
V_{INL}		0		0.4	V
Input Low or High Current, I_{INL} or I_{INH}	Input voltage (V_{IN}) = V_{INL} or V_{INH}		40		nA
C_{IN}			2		pF

ADC SPI TIMING SPECIFICATIONS

Table 4.

Parameter	Description	Min	Typ	Max	Unit
SPI TIMING REQUIREMENTS	See Figure 5, unless otherwise noted				
t_{DS}	Setup time between the data and the rising edge of SCLK	2			ns
t_{DH}	Hold time between the data and the rising edge of SCLK	2			ns
t_{CLK}	Period of the SCLK	40			ns
t_S	Setup time between $\overline{CS}$ and SCLK	2			ns
t_H	Hold time between $\overline{CS}$ and SCLK	2			ns
t_{HIGH}	SCLK pulse width high	10			ns
t_{LOW}	SCLK pulse width low	10			ns
t_{EN_SDIO}[1]	Time required for SDIO to switch from an input to an output relative to the SCLK falling edge	10			ns
t_{DIS_SDIO}[1]	Time required for SDIO to switch from an output to an input relative to the SCLK rising edge	10			ns

[1] This parameter is not shown in Figure 5.

ADC SPI Timing Diagram

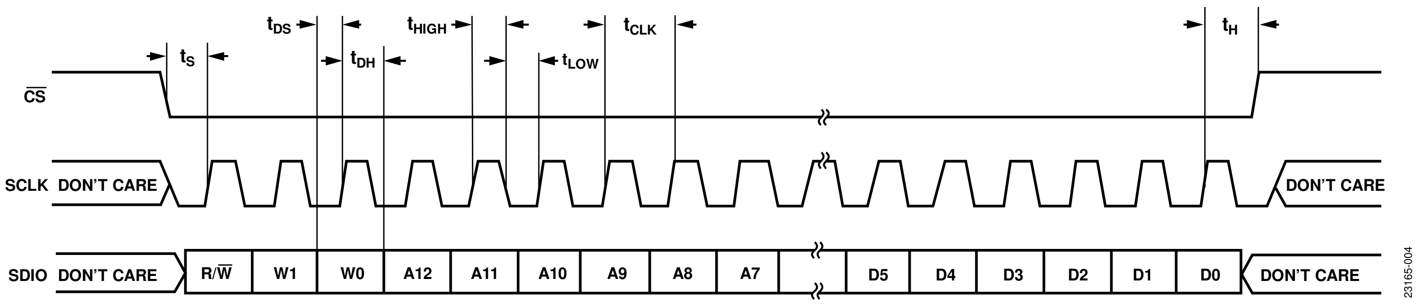


Figure 5. Serial Port Interface Timing Diagram

ADC LVDS OUTPUT SPECIFICATIONS

Table 5.

Parameter[1, 2]	Temperature	Min	Typ	Max	Unit
CLOCK[3]					
Input Rate	Full	10		1000	MHz
Conversion Rate[4]	Full	10		125	MSPS
Pulse Width					
High (t_{EH})	Full		6.25 to 4.00		ns
Low (t_{EL})	Full		6.25 to 4.00		ns
OUTPUT PARAMETERS[3]					
Propagation Delay, t_{PD}	Full	1.5	2.3	3.1	ns
Rise Time, t_R (20% to 80%)[5]	Full		300		ps
Fall Time, t_F (20% to 80%)[5]	Full		300		ps
Frame Clock Output (FCO) Propagation Delay, t_{FCO}	Full	1.5	2.3	3.1	ns
DCO Propagation Delay, t_{CPD}[6]	Full		t_{FCO} + (t_{SAMPLE}/16)		ns
DCO to Data Delay, t_{DATA}[6]	Full	(t_{SAMPLE}/16) − 300	t_{SAMPLE}/16	(t_{SAMPLE}/16) + 300	ps
DCO to FCO Delay, t_{FRAME}[6]	Full	(t_{SAMPLE}/16) − 300	t_{SAMPLE}/16	(t_{SAMPLE}/16) + 300	ps
Lane Delay, t_{LD}	Full		90		ps
Data to Data Skew, $t_{DATA\text{-}MAX} - t_{DATA\text{-}MIN}$[5]	Full		±50	±200	ps
Wake-Up Time (Standby)	25°C		250		ns
Wake-Up Time (Power-Down)	25°C		375		µs
Pipeline Latency	Full		16		Clock cycles
APERTURE					
Aperture Delay, t_A	25°C		1		ns
Aperture Uncertainty (Jitter, t_J)[5]	25°C		174		fs rms
Out-of-Range Recovery Time	25°C		1		Clock cycles

[1] See the AN-835 Application Note, *Understanding High Speed ADC Testing and Evaluation*, for definitions and for details on how these tests were completed.
[2] These parameters were measured on standard FR4 materials.
[3] The clock can be adjusted via the SPI.
[4] The conversion rate is the clock rate after the divider. Valid for 2-lane operation.
[5] This parameter is not shown in Figure 6 through Figure 11.
[6] t_{SAMPLE}/16 is based on the number of bits in two LVDS data lanes. t_{SAMPLE} = 1/f.

ADC LVDS Output Timing Diagram

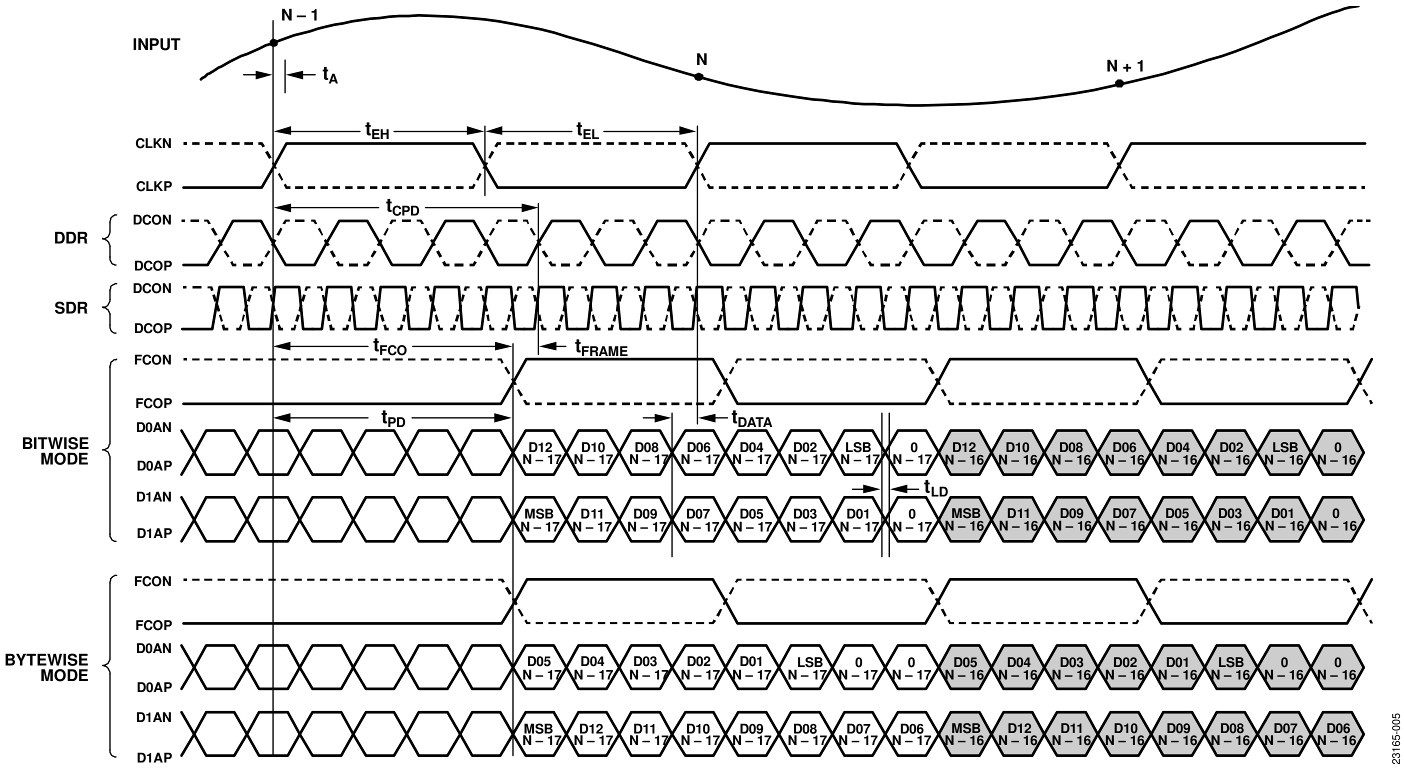


Figure 6. 16-Bit DDR/Single Data Rate (SDR), Two-Lane, 1× Frame Mode (Default)

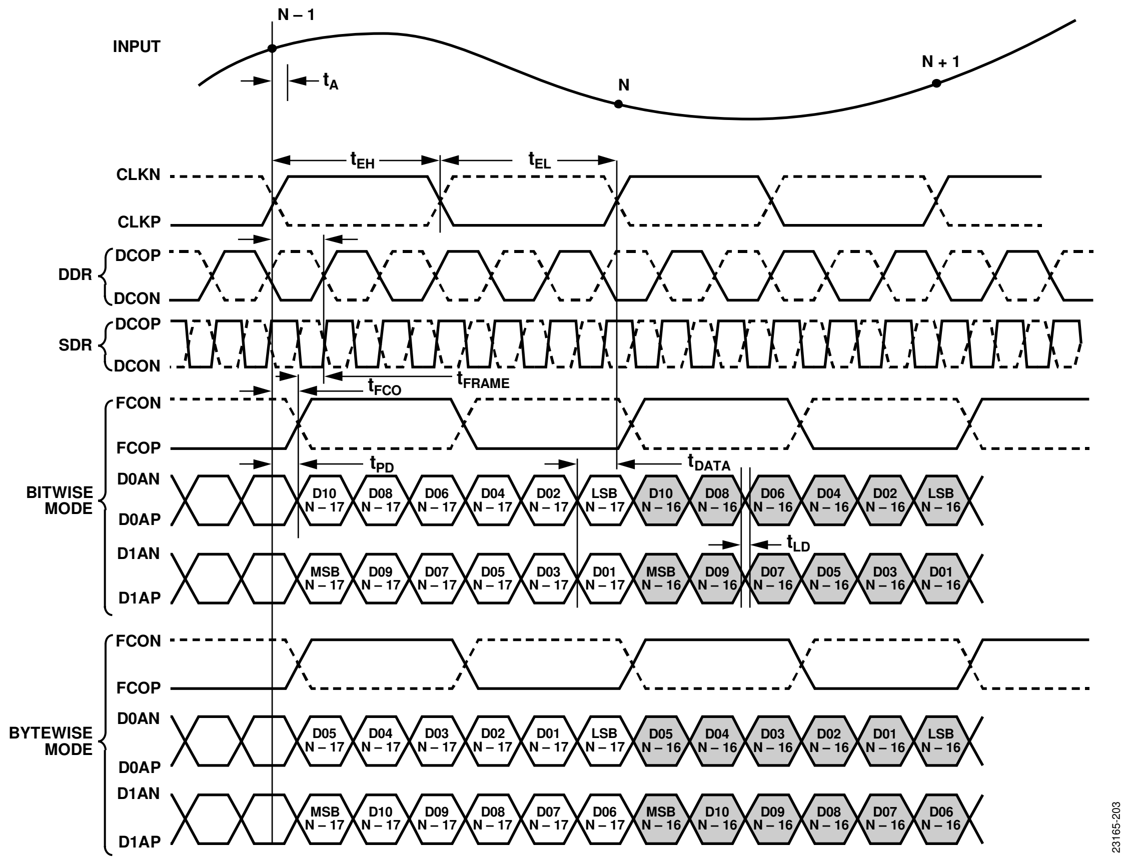


Figure 7. 12-Bit DDR/SDR, Two-Lane, 1× Frame Mode

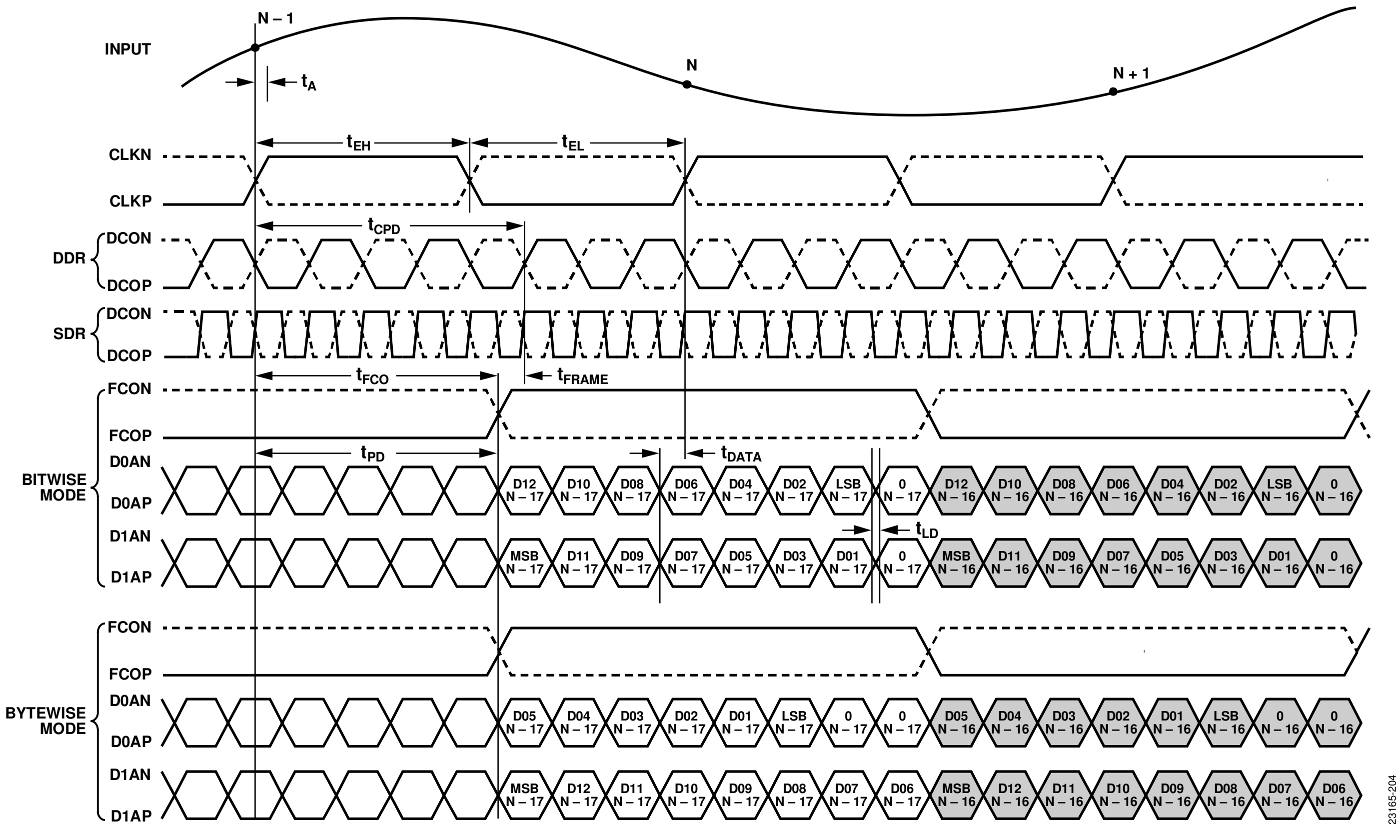


Figure 8. 16-Bit DDR/SDR, Two-Lane, 2× Frame Mode

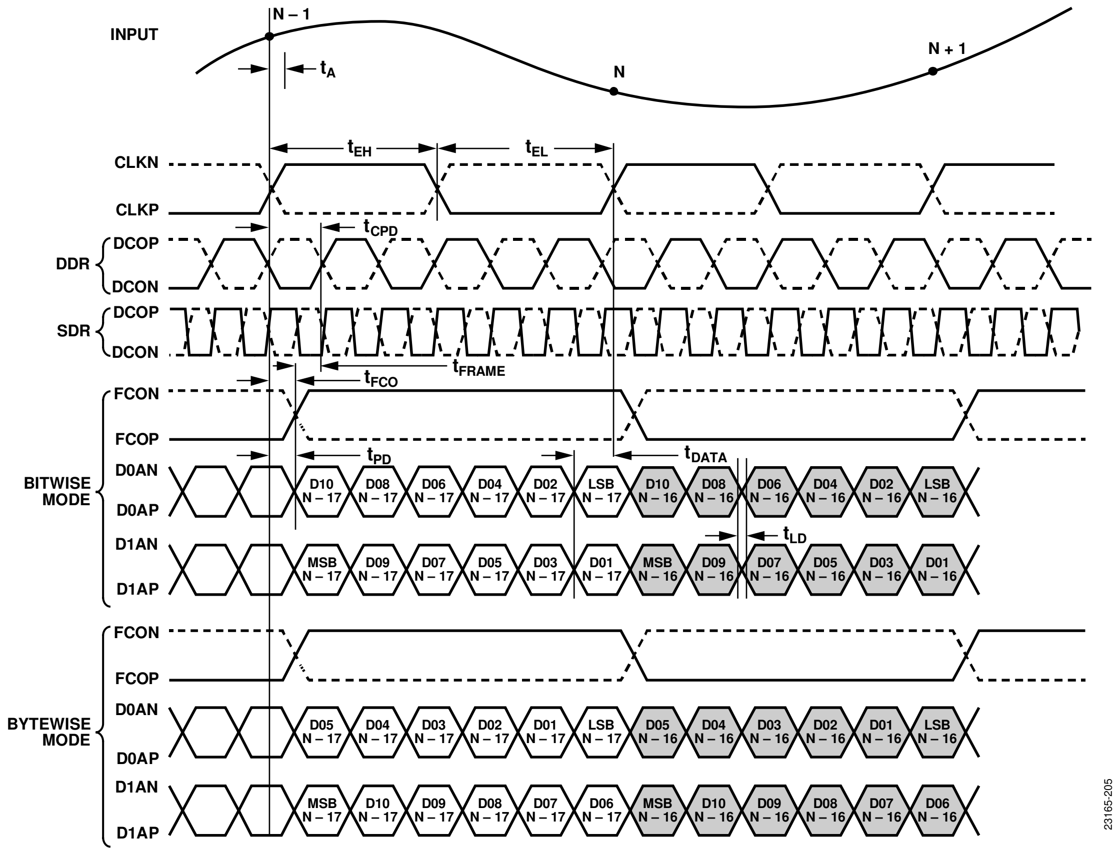


Figure 9. 12-Bit DDR/SDR, Two-Lane, 2× Frame Mode

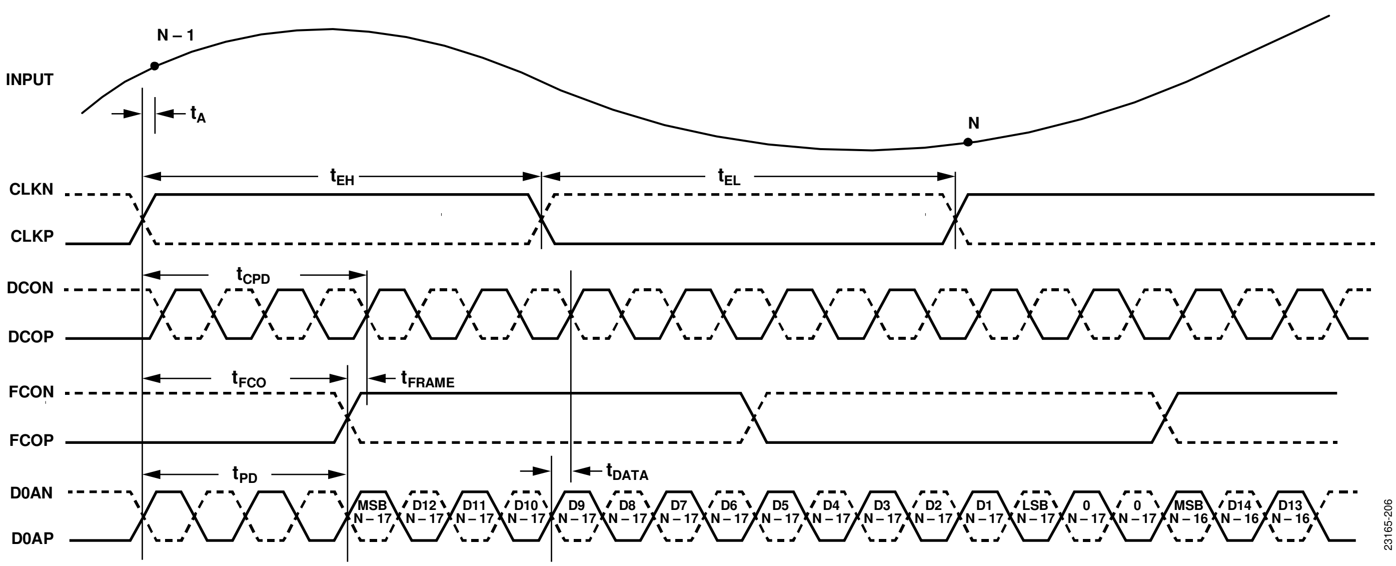


Figure 10. Wordwise DDR, One-Lane, 1× Frame, 16-Bit Output Mode

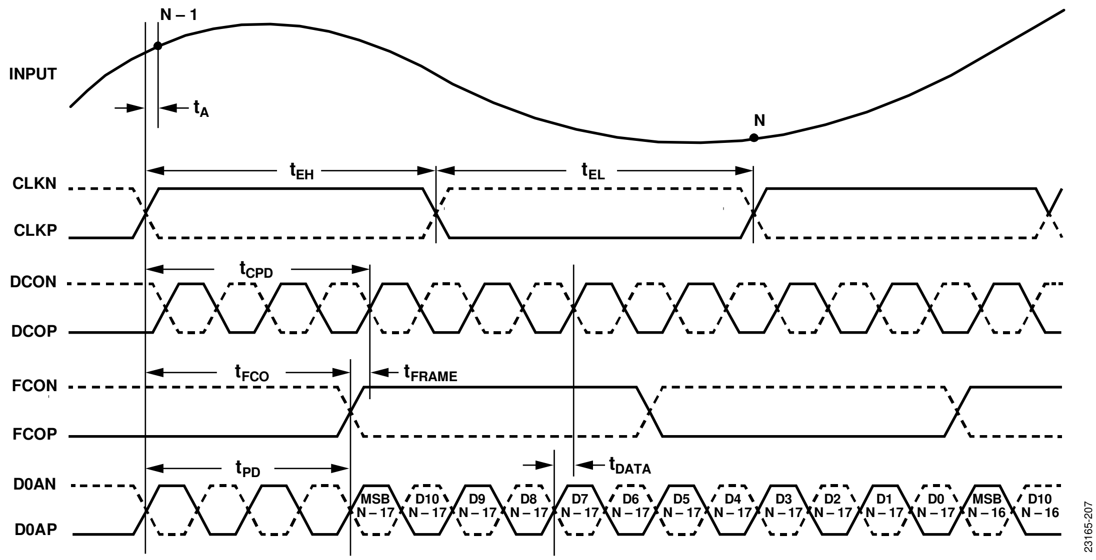


Figure 11. Wordwise DDR, One-Lane, 1× Frame, 12-Bit Output Mode

ABSOLUTE MAXIMUM RATINGS

Table 6.

Parameter	Rating
Electrical	
VCC to GND	−0.3 V to +4.0 V
VEA, VED to GND	−0.3 V to +2.0 V
VLD to GND	−0.3 V to VCC
CLKP, CLKN, SPI[1] to GND	−0.3 V to +2.0 V
INPUT to GND	−0.2 V to VCC + 0.2 V
Analog Input Current	40 mA
Control[2] to GND	−0.3 V to VCC + 0.3 V or 1 mA, whichever occurs first
Digital Output[3] to GND	−0.3 V to +2.0 V
Environmental Temperature	
Storage Range (Ambient)	−65°C to +125°C
Maximum Junction	125°C
Electrostatic Discharge (ESD)	
Human Body Model	
INPUT (Ball E1) and DNC (Ball F1) Balls	500 V
All Other Balls	3000 V
Field Induced Charge Device Model (FICDM)	1250 V
Assemble (Soldering, 10 sec)	300°C

[1] Includes SCLK, SDIO, and $\overline{\text{CS}}$.
[2] Includes FSEL, GSEL1, GSEL0, and VLDEN.
[3] Includes D0AP, D0AN, D1AP, D1AN, DCOP, DCON, FCOP, and FCON.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

THERMAL RESISTANCE

Thermal performance is directly linked to printed circuit board (PCB) design and operating environment. Close attention to PCB thermal design is required.

Thermal resistance values specified in Table 7 are calculated based on standard JEDEC specifications.

Table 7. Thermal Resistance

Package Type	θ_{JA}	$\theta_{JC\,TOP}$	Ψ_{JT}	Unit
BC-84-4	52.6	22.0	17.7	°C/W

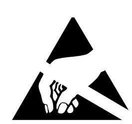
Only use θ_{JA} and $\theta_{JC\,TOP}$ to compare thermal performance of the package of the device with other semiconductor packages when all test conditions listed are similar. One common mistake is to use θ_{JA} and θ_{JC} to estimate the junction temperature in the system environment. Instead, using Ψ_{JT} is a more appropriate way to estimate the worst case junction temperature of the device in the system environment. First, take an accurate thermal measurement of the top center of the device (on the mold compound in this case) while the device operates in the system environment. This measurement is known in the following equation as T_{TOP}.

Then, use this equation to solve for the worst case T_J in that given environment as follows:

$$T_J = \Psi_{JT} \times P + T_{TOP}$$

where:
Ψ_{JT} is the junction to top thermal characterization number as specified in the data sheet.
P refers to the total power dissipation in the chip (W).
T_{TOP} refers to the package top temperature (°C) and is measured at the top center of the package in that given environment.

ESD CAUTION



ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

ADA4355
TOP VIEW
(BALL SIDE DOWN)

	1	2	3	4	5	6	7	8	9	10	11	12	13	14
A	GND	DNC	VCC	GSEL0	GSEL1	FSEL	DNC	GND	DNC	$\overline{CS}$	SCLK	GND	D0AN	D0AP
B	GND	GND	GND	GND	GND	GND	DNC	DNC	GND	GND	SDIO	GND	D1AN	D1AP
C	GND	GND	VCC	VCC	VCC	GND	GND	GND	GND	GND	GND	GND	FCON	FCOP
D	GND	DNC	VCC	VCC	VCC	GND	DNC	DNC	DNC	GND	GND	GND	DCON	DCOP
E	INPUT	GND	GND	DNC	DNC	GND	GND	DNC	GND	VEA	CLKN	VED	DNC	DNC
F	DNC	DNC	VCC	VCC	VCC	VCC	VLDEN	VCC	GND	DNC	CLKP	VLD	DNC	DNC

NOTES
1. DO NOT CONNECT. THESE BALLS ARE RESERVED.

23165-006

Figure 12. Ball Configuration

Table 8. Ball Configuration and Function Descriptions

Ball No.	Mnemonic	Type[1]	Description
A1, A8, A12, B1 to B6, B9, B10, B12, C1, C2, C6 to C12, D1, D6, D10 to D12, E2, E3, E6, E7, E9, F9	GND	P	Ground.
A3, C3 to C5, D3 to D5, F3 to F6, F8	VCC	P	3.3 V Power Supply.
E10	VEA	P	1.8 V Analog Power Supply to ADC.
E12	VED	P	1.8 V Digital Power Supply to ADC.
F12	VLD	PO	1.8 V LDO Output. Connect VLD to VEA and VED to power the ADC from the internal LDO or leave VLD floating if the ADC is powered from the external source. Do not connect VLD to the external circuitry.
F7	VLDEN	DI	VLD Output Enable. Set VLDEN = 1 to enable the VLD output.
A6	FSEL	DI	LPF Bandwidth Select. FSEL selects the 100 MHz (FSEL = 0) or 1.0 MHz (FSEL = 1) LPF bandwidth.
A10	$\overline{CS}$	DI	Chip Select. Set $\overline{CS}$ = 0 to enable SPI mode. $\overline{CS}$ has an internal 15 kΩ pull-up resistor.
B11	SDIO	DIO	Serial Data Input/Output. In SPI mode, SDIO is a bidirectional SPI data input/output with a 31 kΩ internal pull-down resistor.
A11	SCLK	DI	SPI Clock Input in SPI Mode. SCLK has a 30 kΩ internal pull-down resistor.
D13, D14	DCON, DCOP	DO	Data Clock Outputs, Differential.
C13, C14	FCON, FCOP	DO	Frame Clock Outputs, Differential.
B13, B14	D1AN, D1AP	DO	Lane 1 Digital Outputs, Differential.
A13, A14	D0AN, D0AP	DO	Lane 0 Digital Outputs, Differential.
F11, E11	CLKP, CLKN	DI	ADC Sampling Clock Inputs, Differential.
A4, A5	GSEL0, GSEL1	DI	TIA Gain Selection. See Table 9 for the truth table.
E1	INPUT	AI	Analog Input. Connect INPUT to a reversed biased photodiode anode.
A2, A7, A9, B7, B8, D2, D7 to D9, E4, E5, E8, E13, E14 ,F1, F2, F10, F13, F14	DNC	N/A	Do Not Connect. These balls are reserved.

[1] P means power, PO means power output, DI means data input, DIO means data input/output, DO means data output, AI means analog input, and N/A means not applicable.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, VCC = 3.3 V, no averaging, and LDO enabled (see the power scheme shown in Figure 3), unless otherwise noted.

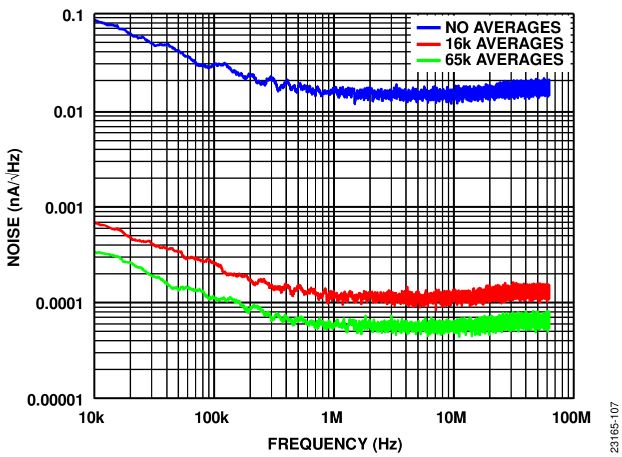


Figure 13. Noise Spectral Density, T_Z = 2 kΩ, LPF = 100 MHz

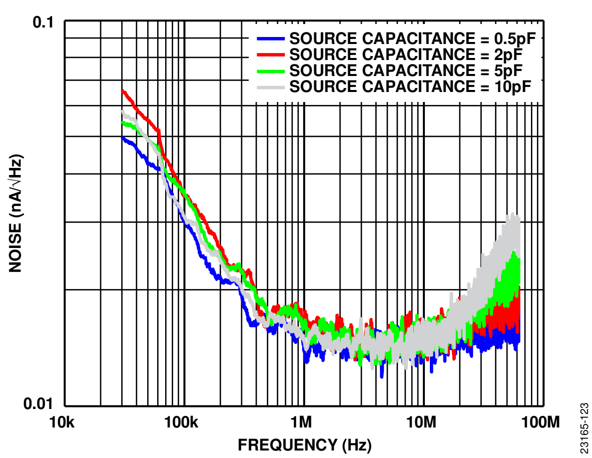


Figure 14. Noise Spectral Density for Various Source Capacitances, T_Z = 2 kΩ, LPF = 100 MHz

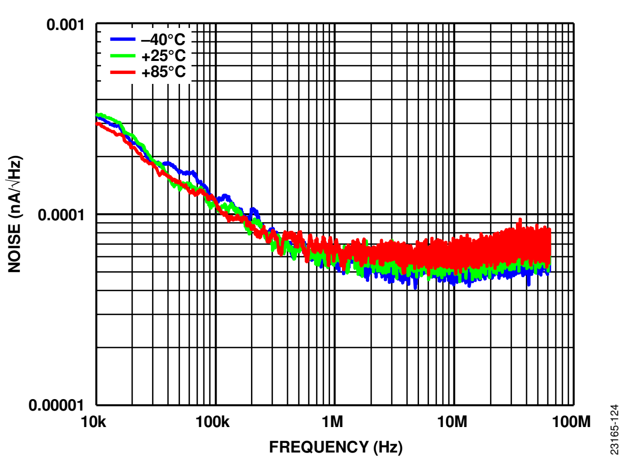


Figure 15. Noise Spectral Density for Various Temperatures, T_Z = 2 kΩ, LPF = 100 MHz

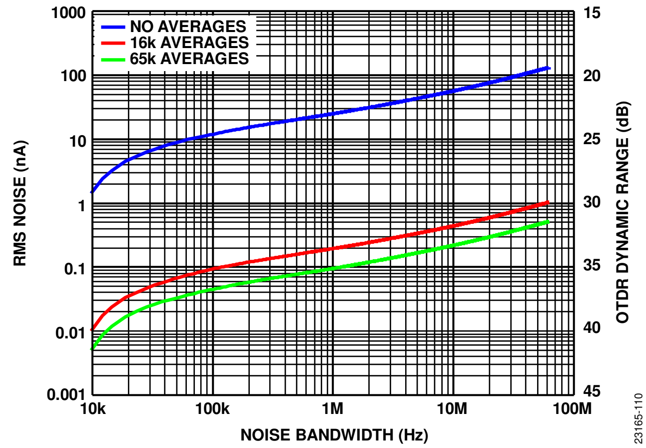


Figure 16. RMS Noise and Optical Time Domain Reflectometry (OTDR) Dynamic Range vs. Noise Bandwidth, T_Z = 2 kΩ, LPF = 100 MHz

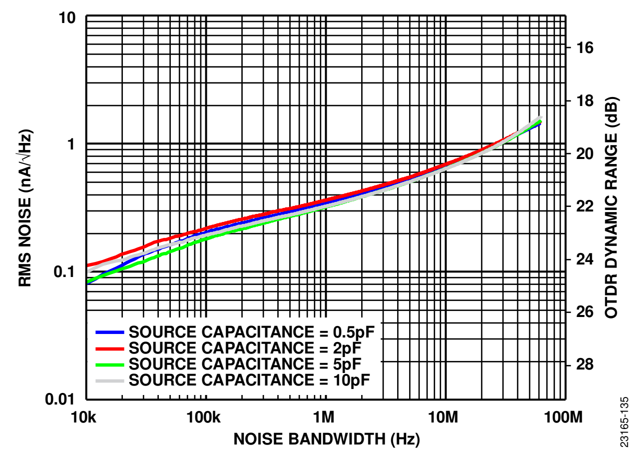


Figure 17. RMS Noise and OTDR Dynamic Range vs. Noise Bandwidth for Various Source Capacitances, T_Z = 2 kΩ, LPF = 100 MHz

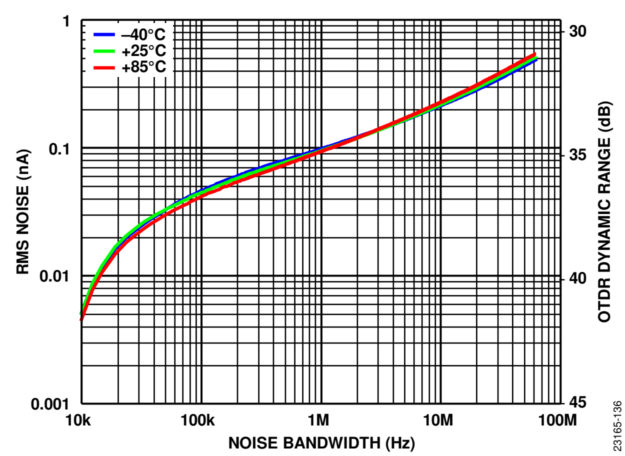


Figure 18. RMS Noise and OTDR Dynamic Range vs. Noise Bandwidth for Various Temperatures, T_Z = 2 kΩ, LPF = 100 MHz

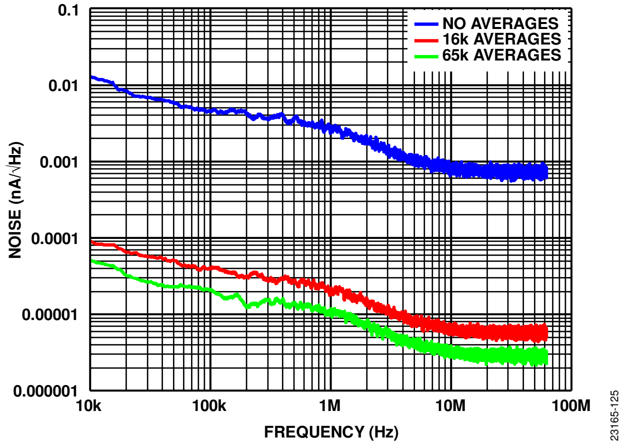


Figure 19. Noise Spectral Density, T_Z = 20 kΩ, LPF = 1 MHz

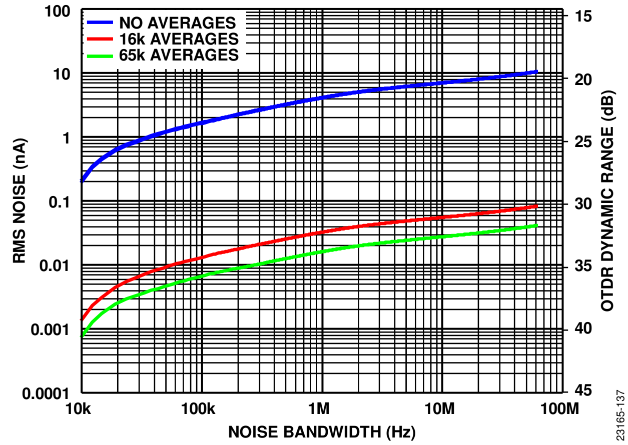


Figure 22. RMS Noise and OTDR Dynamic Range vs. Noise Bandwidth, T_Z = 20 kΩ, LPF = 1 MHz

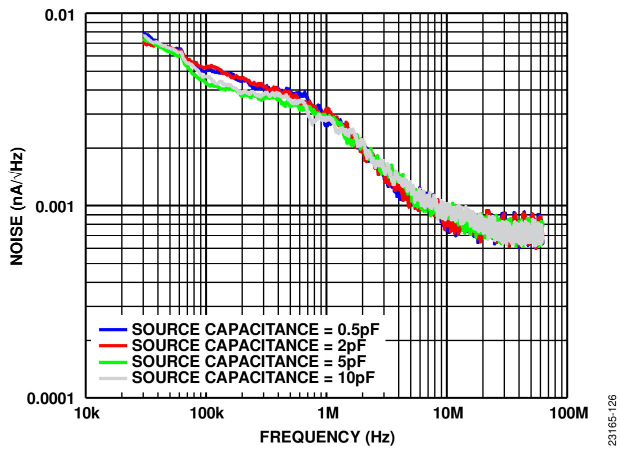


Figure 20. Noise Spectral Density for Various Source Capacitances, T_Z = 20 kΩ, LPF = 1 MHz

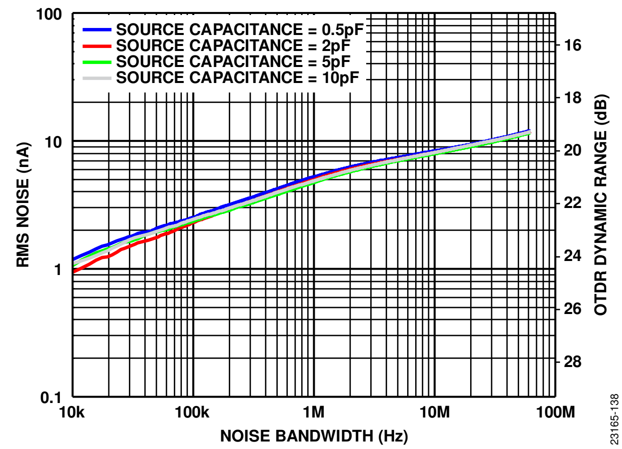


Figure 23. RMS Noise and OTDR Dynamic Range vs. Noise Bandwidth for Various Source Capacitances, T_Z = 20 kΩ, LPF = 1 MHz

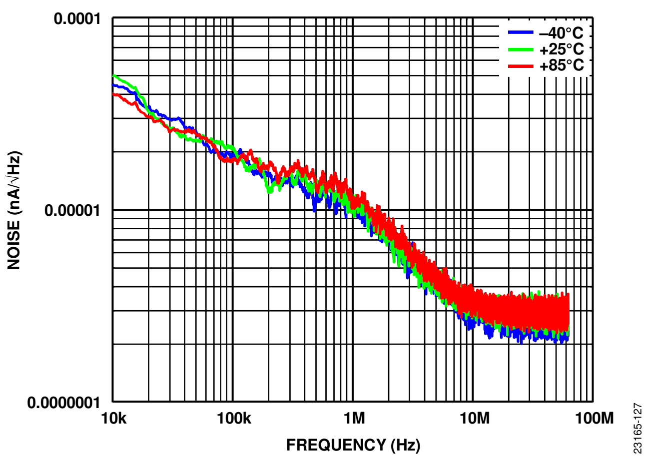


Figure 21. Noise Spectral Density for Various Temperatures, T_Z = 20 kΩ, LPF = 1 MHz

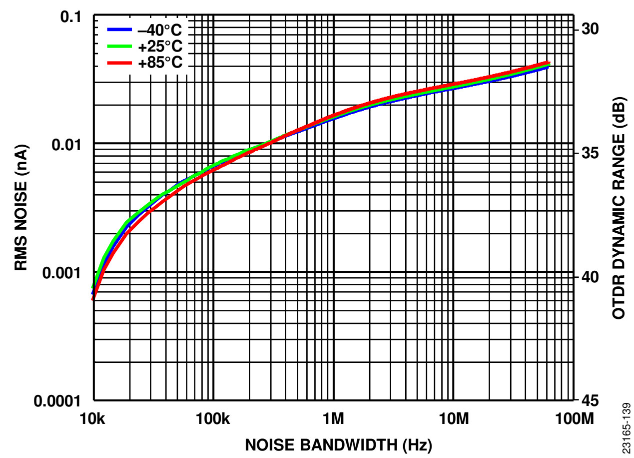


Figure 24. RMS Noise and OTDR Dynamic Range vs. Noise Bandwidth for Various Temperatures, T_Z = 20 kΩ, LPF = 1 MHz

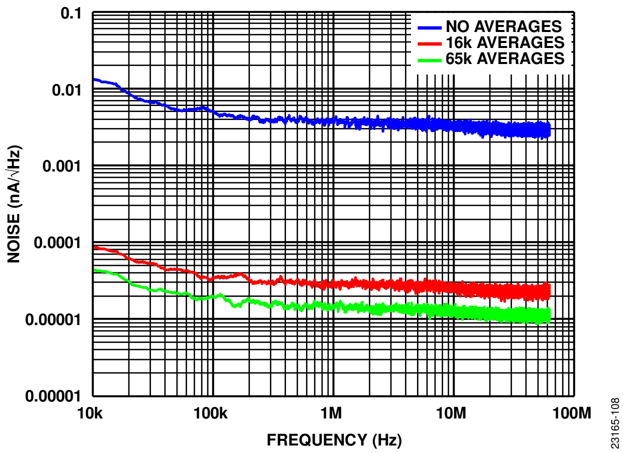


Figure 25. Noise Spectral Density, T_Z = 20 kΩ, LPF = 100 MHz

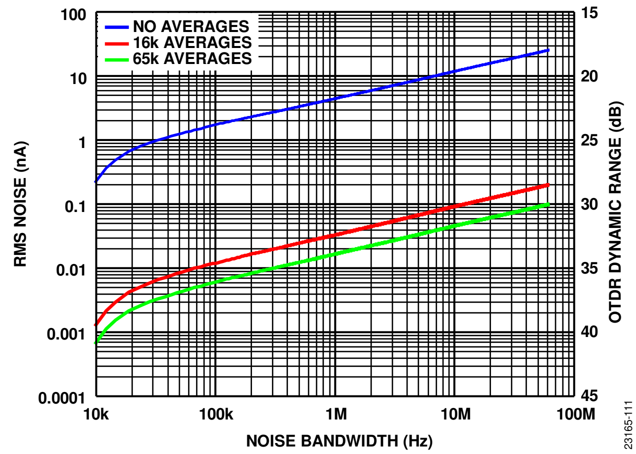


Figure 28. RMS Noise and OTDR Dynamic Range vs. Noise Bandwidth, T_Z = 20 kΩ, LPF = 100 MHz

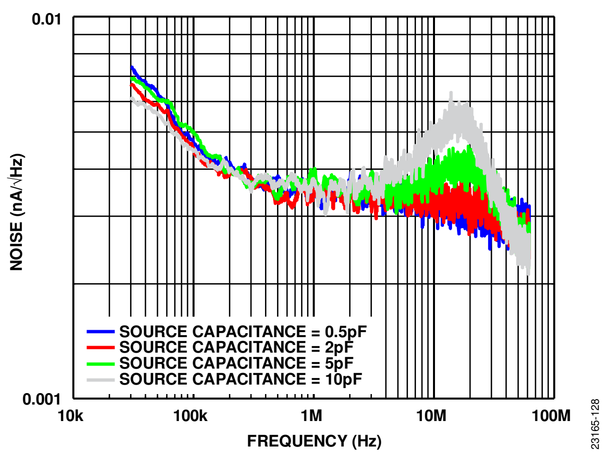


Figure 26. Noise Spectral Density for Various Source Capacitances, T_Z = 20 kΩ, LPF = 100 MHz

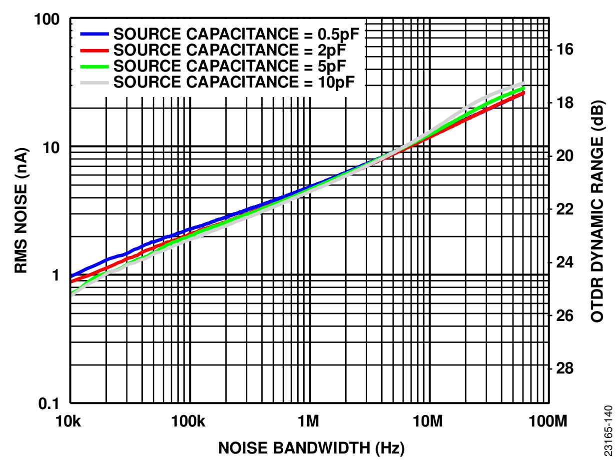


Figure 29. RMS Noise and OTDR Dynamic Range vs. Noise Bandwidth for Various Source Capacitances, T_Z = 20 kΩ, LPF = 100 MHz

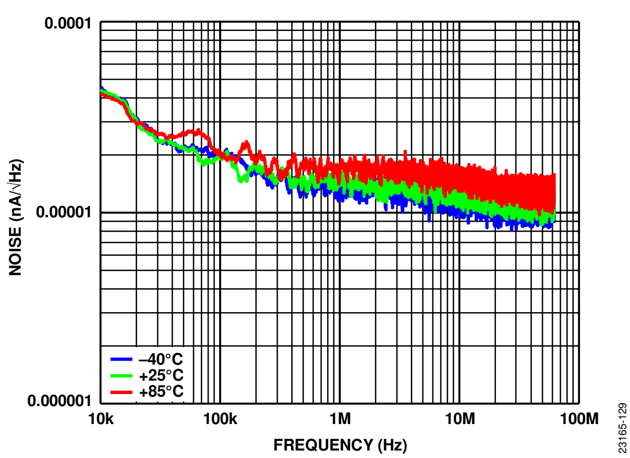


Figure 27. Noise Spectral Density for Various Temperatures, T_Z = 20 kΩ, LPF = 100 MHz

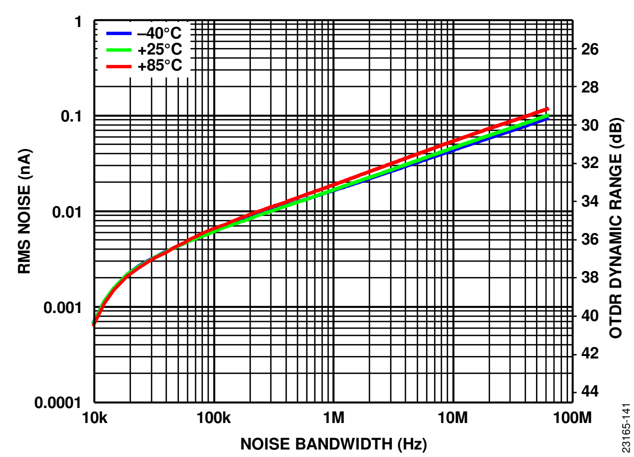


Figure 30. RMS Noise and OTDR Dynamic Range vs. Noise Bandwidth for Various Temperatures, T_Z = 20 kΩ, LPF = 100 MHz

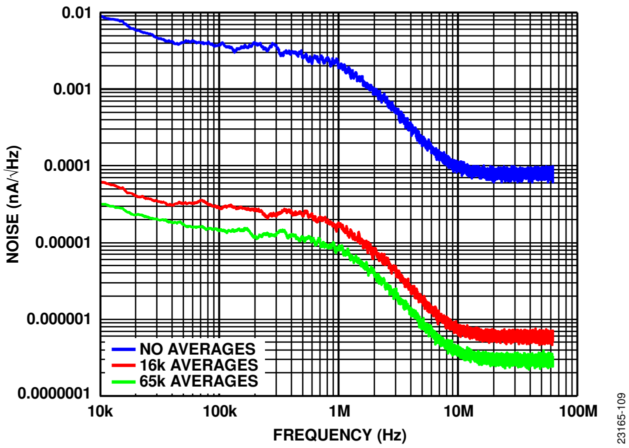


Figure 31. Noise Spectral Density, T_Z = 200 kΩ, LPF = 1 MHz

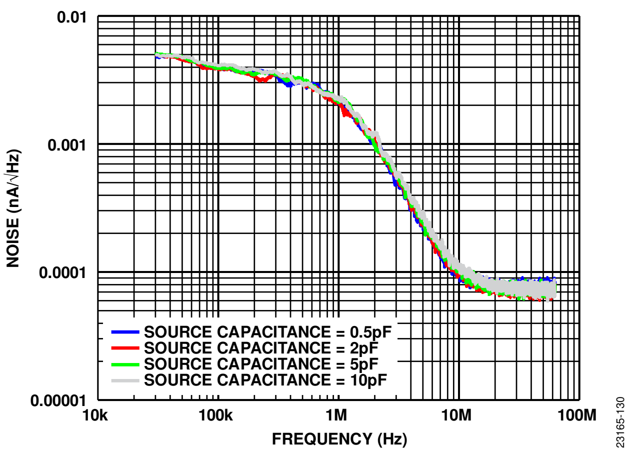


Figure 32. Noise Spectral Density for Various Source Capacitances, T_Z = 200 kΩ, LPF = 1 MHz

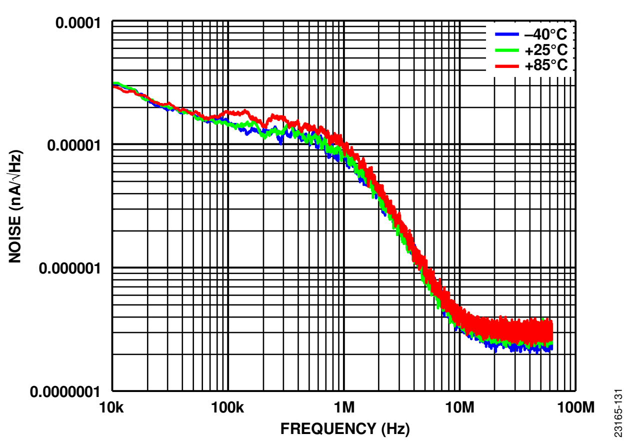


Figure 33. Noise Spectral Density for Various Temperatures, T_Z = 200 kΩ, LPF = 1 MHz

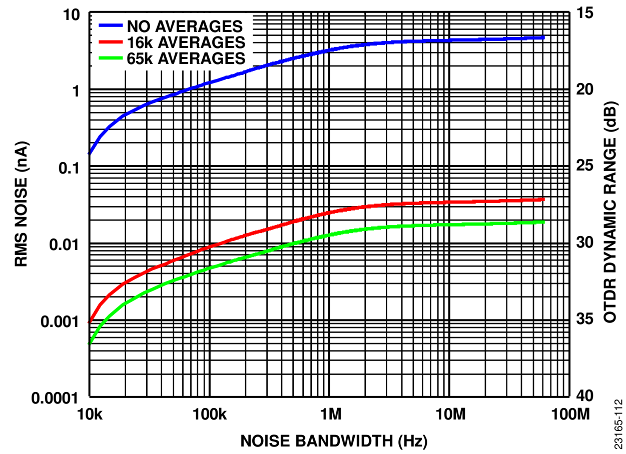


Figure 34. RMS Noise and OTDR Dynamic Range vs. Noise Bandwidth, T_Z = 200 kΩ, LPF = 1 MHz

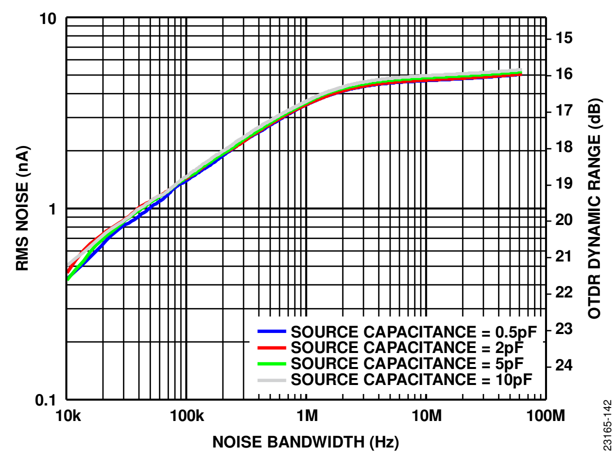


Figure 35. RMS Noise and OTDR Dynamic Range vs. Noise Bandwidth for Various Source Capacitances, T_Z = 200 kΩ, LPF = 1 MHz

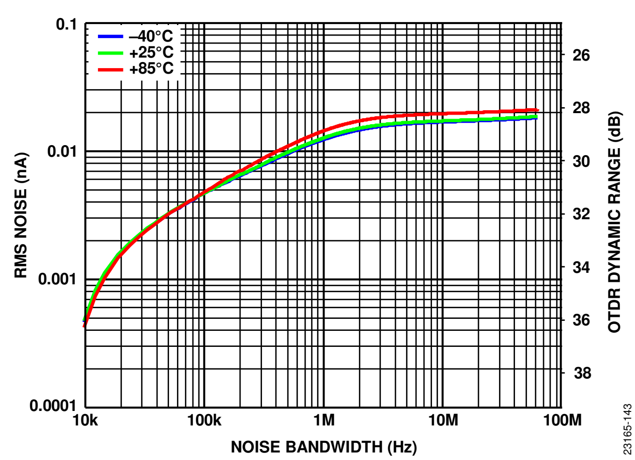


Figure 36. RMS Noise and OTDR Dynamic Range vs. Noise Bandwidth for Various Temperatures, T_Z = 200 kΩ, LPF = 1 MHz

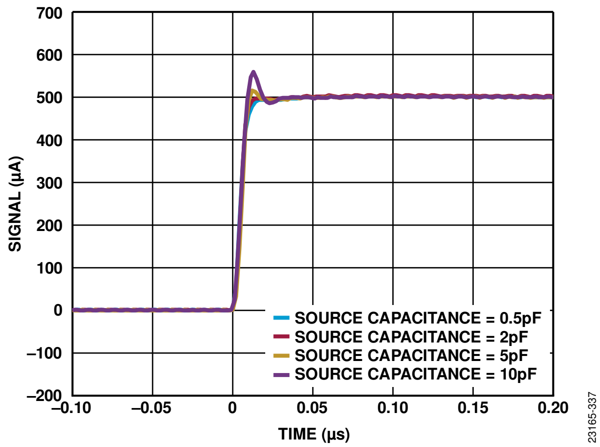


Figure 37. Pulse Response Rising Edge for Various Source Capacitances, T_Z = 2 kΩ, LPF = 100 MHz

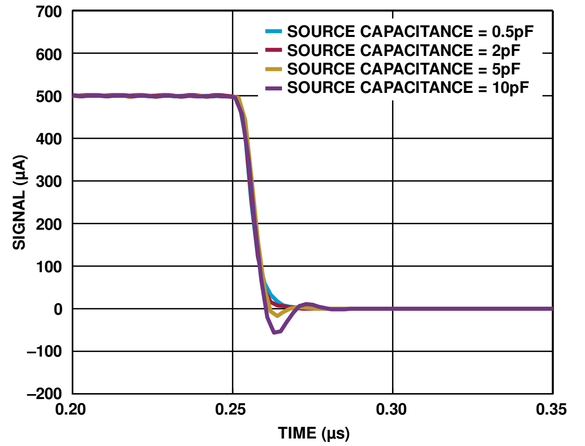


Figure 40. Pulse Response Falling Edge for Various Source Capacitances, T_Z = 2 kΩ, LPF = 100 MHz

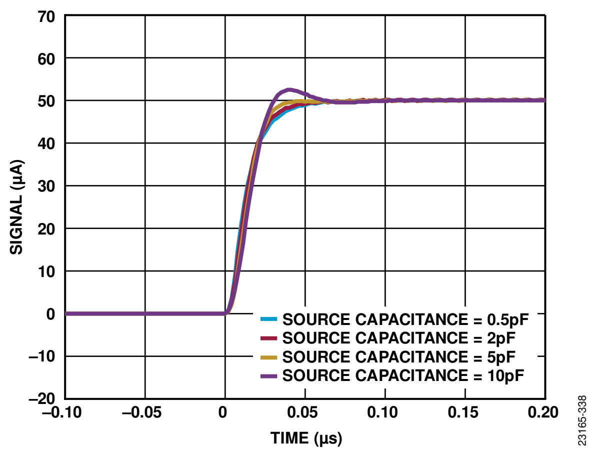


Figure 38. Pulse Response Rising Edge for Various Source Capacitances, T_Z = 20 kΩ, LPF = 100 MHz

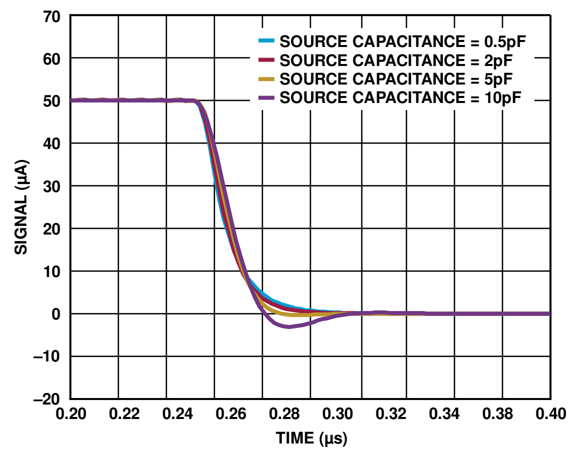


Figure 41. Pulse Response Falling Edge for Various Source Capacitances, T_Z = 20 kΩ, LPF = 100 MHz

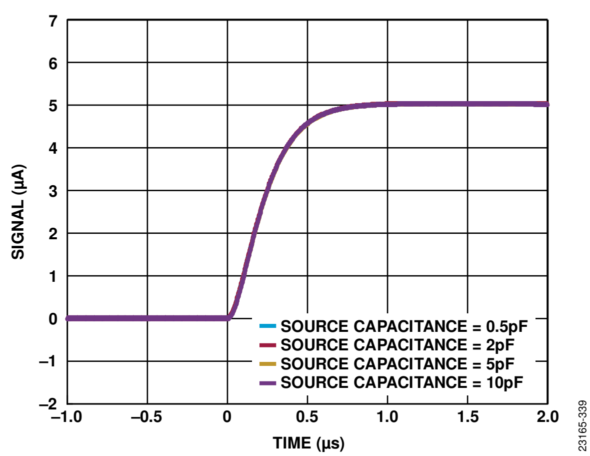


Figure 39. Pulse Response Rising Edge for Various Source Capacitances, T_Z = 200 kΩ, LPF = 1 MHz

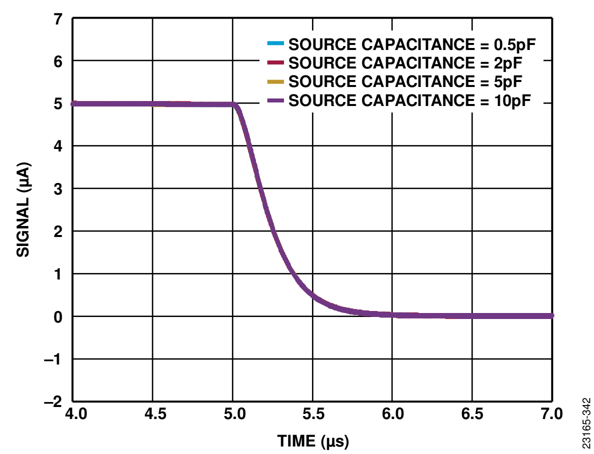


Figure 42. Pulse Response Falling Edge for Various Source Capacitances, T_Z = 200 kΩ, LPF = 1 MHz

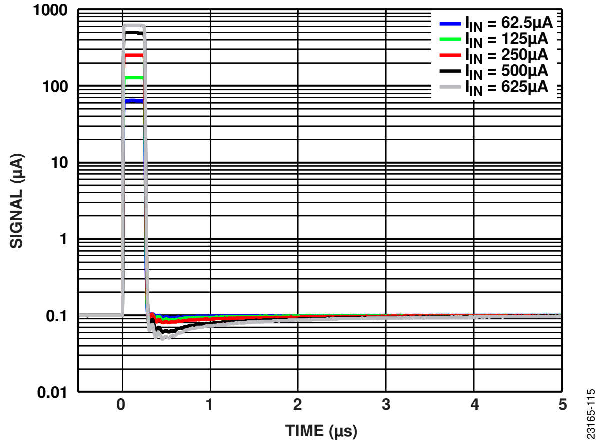


Figure 43. Settling Time for Various Input Currents, T_Z = 2 kΩ, 250 ns Pulse Width, LPF = 100 MHz

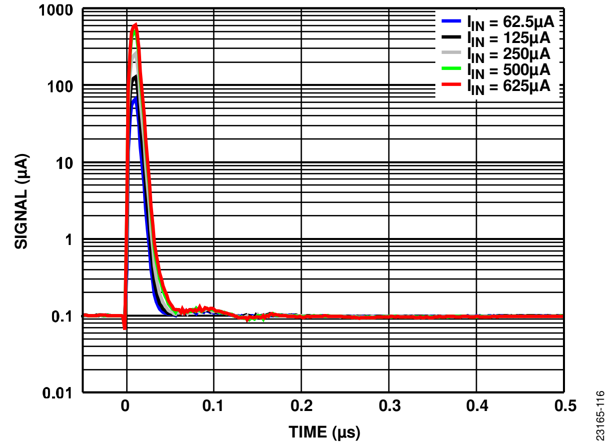


Figure 46. Settling Time for Various Input Currents, T_Z = 2 kΩ, 10 ns Pulse Width, LPF = 100 MHz

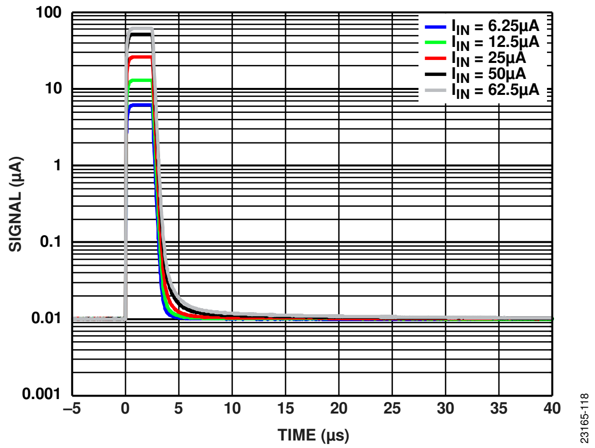


Figure 44. Settling Time for Various Input Currents, T_Z = 20 kΩ, 2.5 µs Pulse Width, LPF = 1 MHz

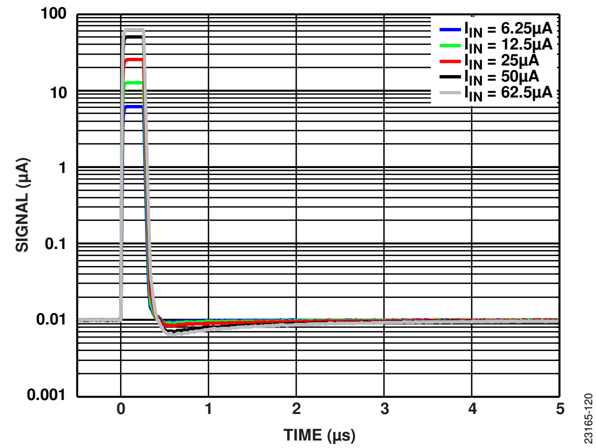


Figure 47. Settling Time for Various Input Currents, T_Z = 20 kΩ, 250 ns Pulse Width, LPF = 100 MHz

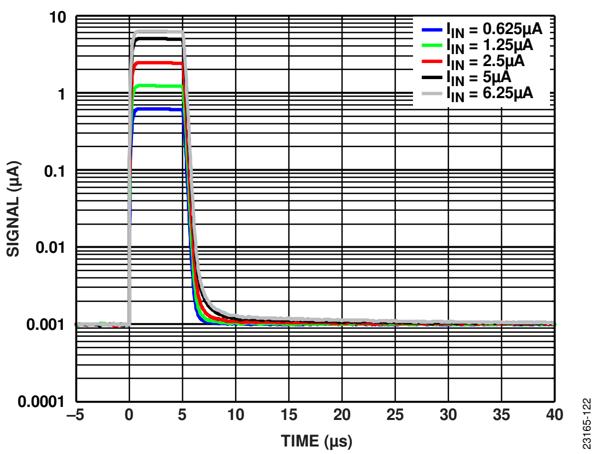


Figure 45. Settling Time for Various Input Currents, T_Z = 200 kΩ, 5 µs Pulse Width, LPF = 1 MHz

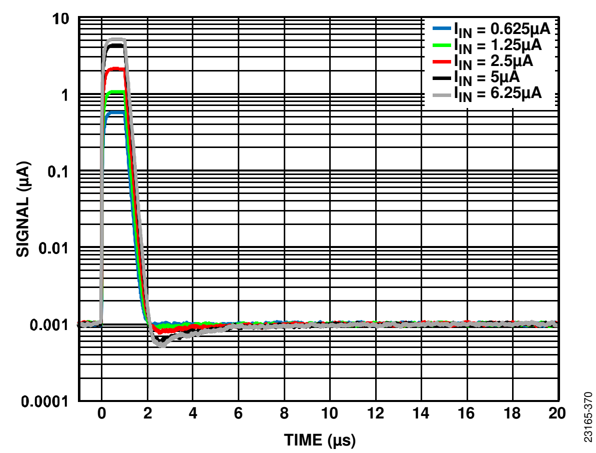


Figure 48. Settling Time for Various Input Currents, T_Z = 200 kΩ, 1 µs Pulse Width, LPF = 100 MHz

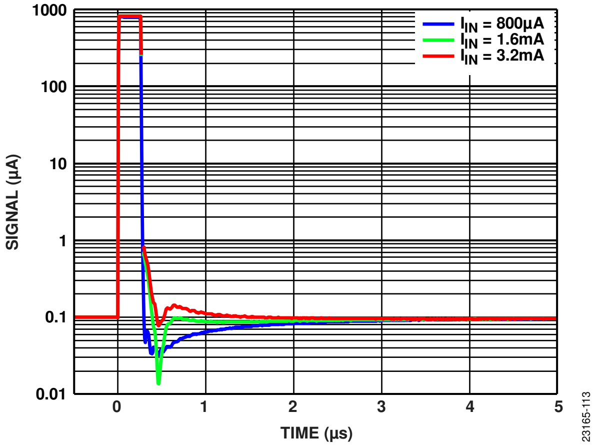


Figure 49. Overload Recovery, T_Z = 2 kΩ, 250 ns Pulse Width, LPF = 100 MHz

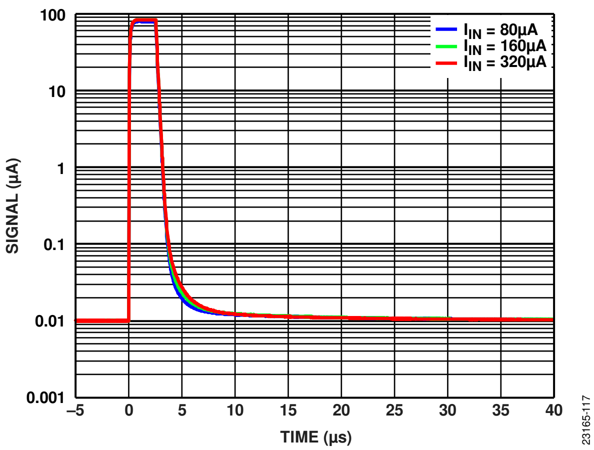


Figure 50. Overload Recovery, T_Z = 20 kΩ, 2.5 µs Pulse Width, LPF = 1 MHz

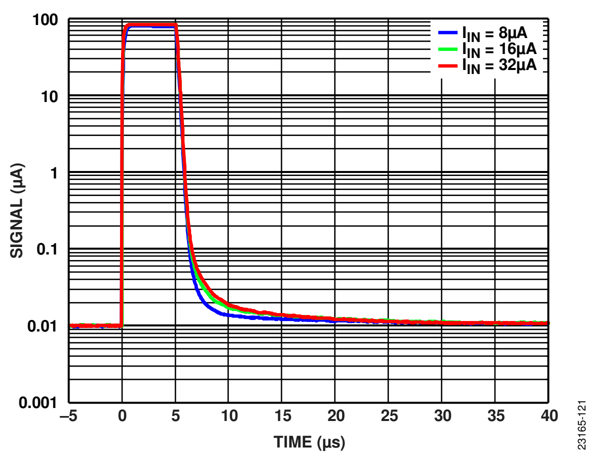


Figure 51. Overload Recovery, T_Z = 200 kΩ, 5 µs Pulse Width, LPF = 1 MHz

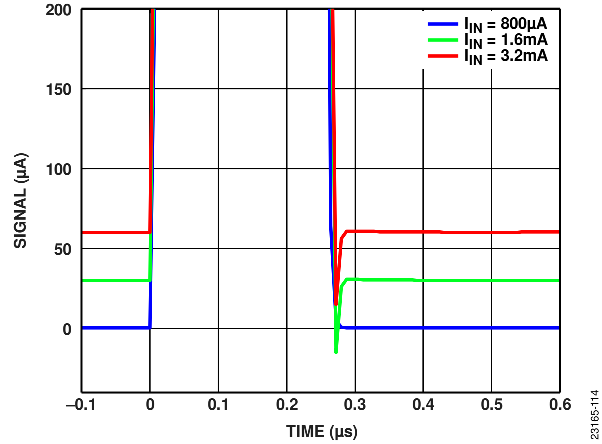


Figure 52. Overload Recovery (Zoomed In), T_Z = 2 kΩ, 250 ns Pulse Width, LPF = 100 MHz (Traces Offset Vertically for Readability)

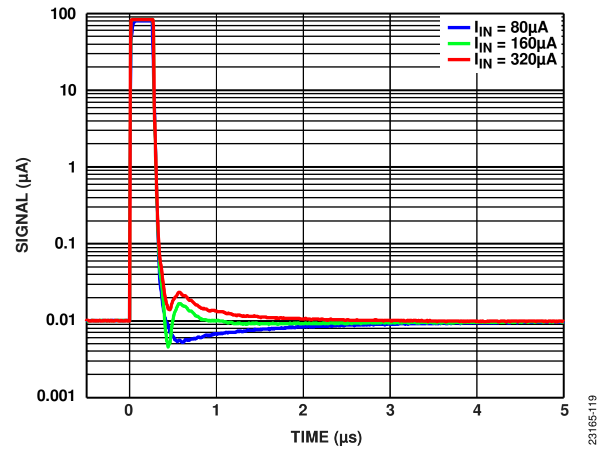


Figure 53. Overload Recovery, T_Z = 20 kΩ, 250 ns Pulse Width, LPF = 100 MHz

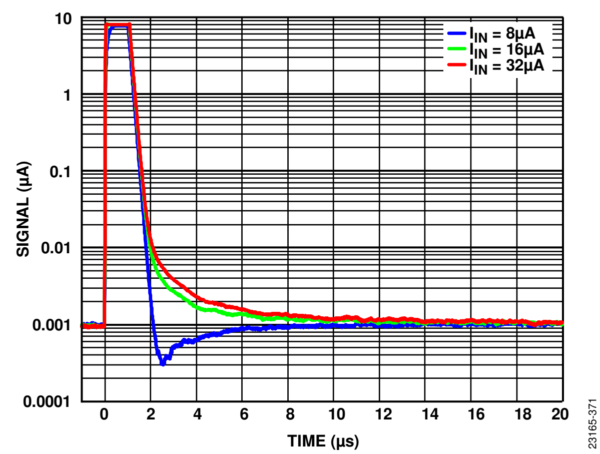


Figure 54. Overload Recovery, T_Z = 200 kΩ, 1 µs Pulse Width, LPF = 100 MHz

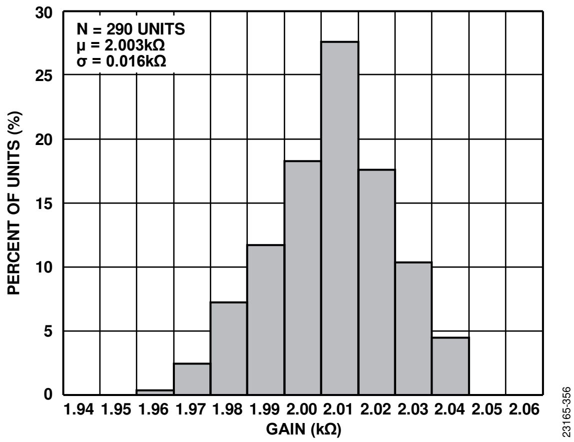


Figure 55. TIA Gain Distribution, $T_Z = 2\ k\Omega$

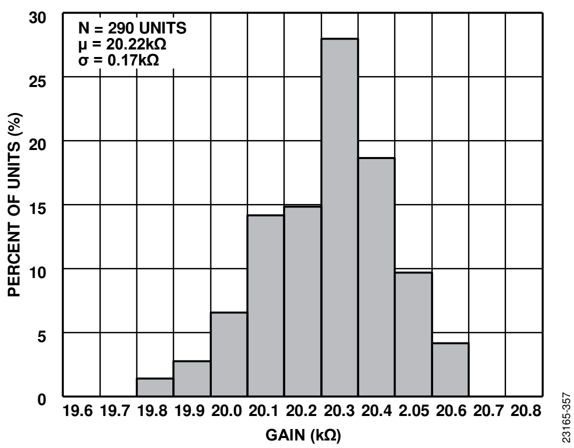


Figure 56. TIA Gain Distribution, $T_Z = 20\ k\Omega$

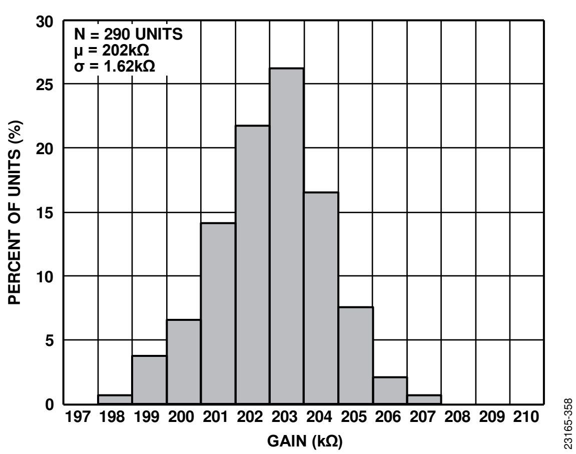


Figure 57. TIA Gain Distribution, $T_Z = 200\ k\Omega$

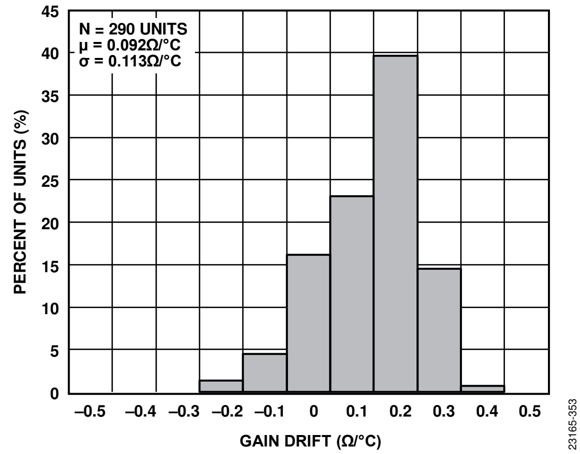


Figure 58. TIA Gain Drift Distribution, $T_Z = 2\ k\Omega$

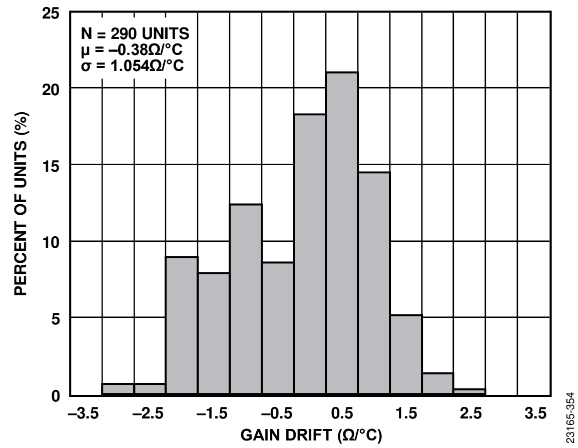


Figure 59. TIA Gain Drift Distribution, $T_Z = 20\ k\Omega$

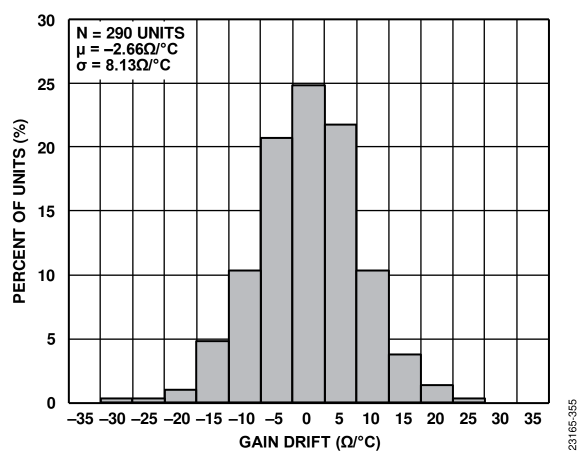


Figure 60. TIA Gain Drift Distribution, $T_Z = 200\ k\Omega$

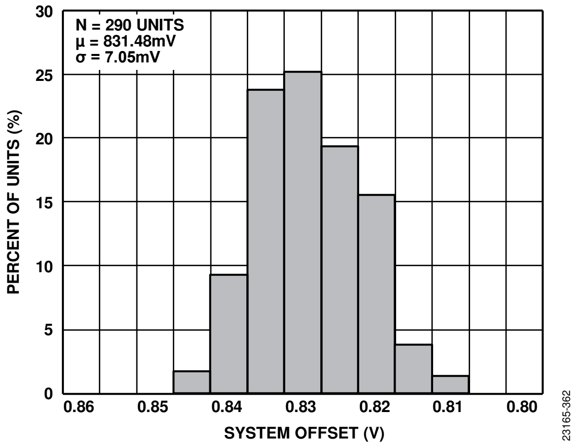


Figure 61. System Offset Distribution, T_Z = 2 kΩ, LPF = 100 MHz

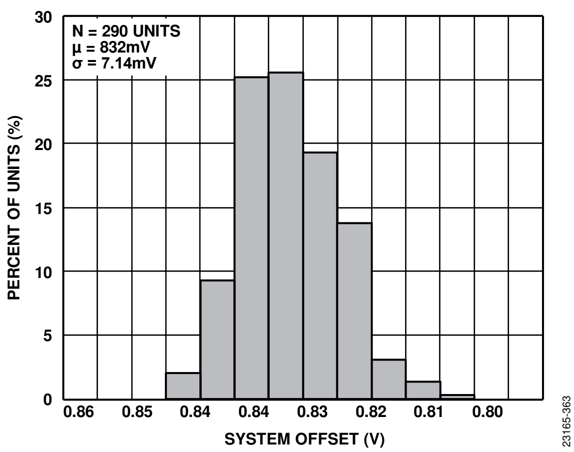


Figure 62. System Offset Distribution, T_Z = 20 kΩ, LPF = 100 MHz

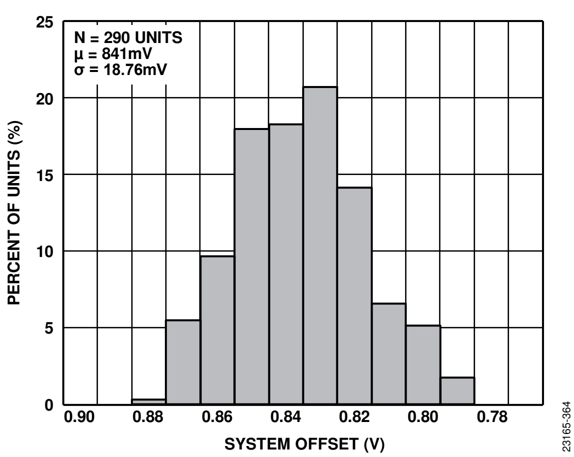


Figure 63. System Offset Distribution, T_Z = 200 kΩ, LPF = 1 MHz

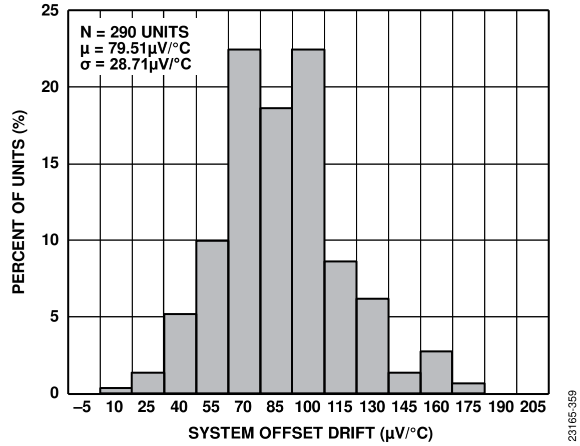


Figure 64. System Offset Drift Distribution, T_Z = 2 kΩ, LPF = 100 MHz

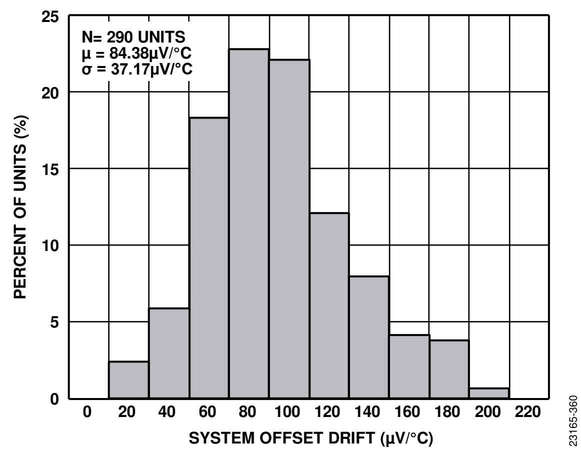


Figure 65. System Offset Drift Distribution, T_Z = 20 kΩ, LPF = 100 MHz

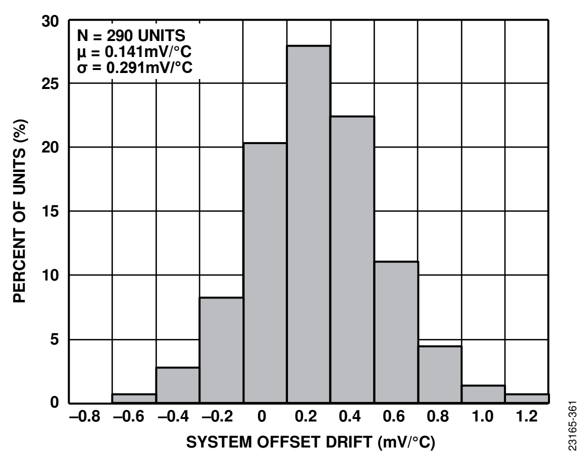


Figure 66. System Offset Drift Distribution, T_Z = 200 kΩ, LPF = 1 MHz

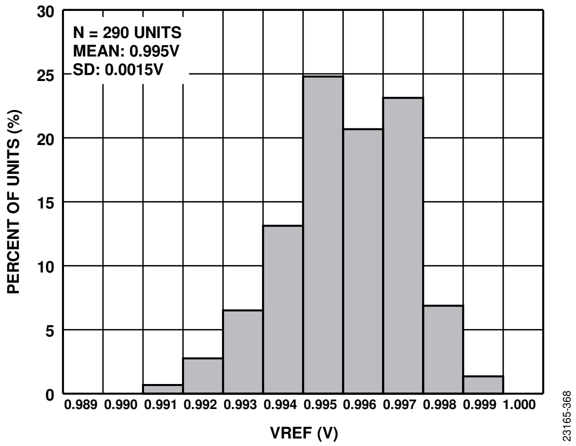


Figure 67. ADC Internal Reference Voltage (VREF) Distribution

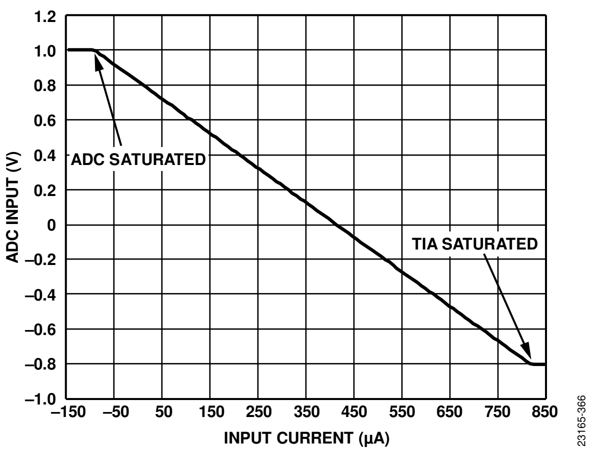


Figure 68. ADC Input Voltage vs. Input Current, T_Z = 2 kΩ

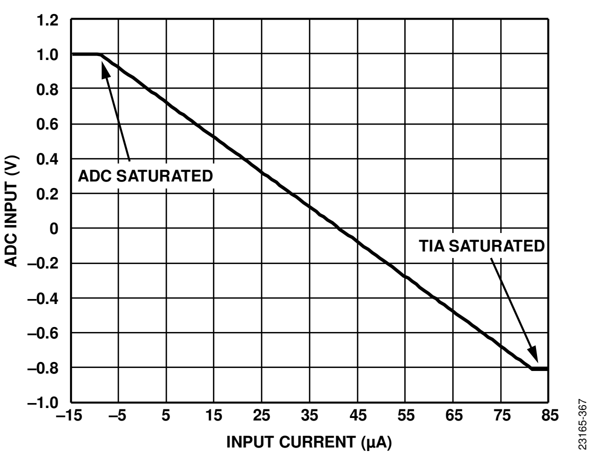


Figure 69. ADC Input Voltage vs. Input Current, T_Z = 20 kΩ

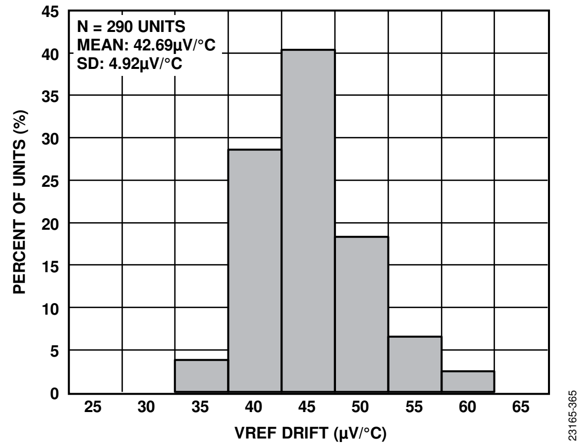


Figure 70. ADC Internal VREF Drift Distribution

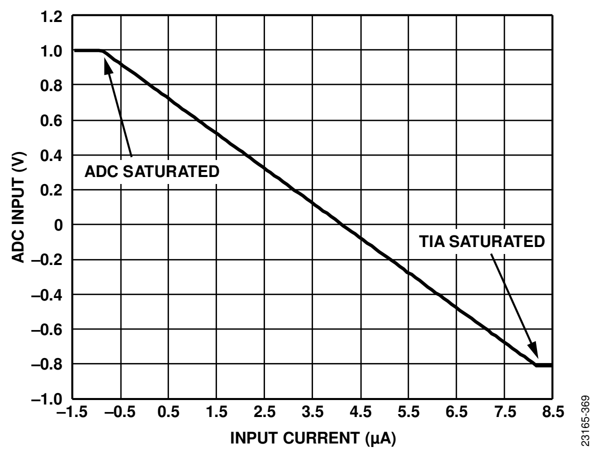


Figure 71. ADC Input Voltage vs. Input Current, T_Z = 200 kΩ

EQUIVALENT CIRCUITS

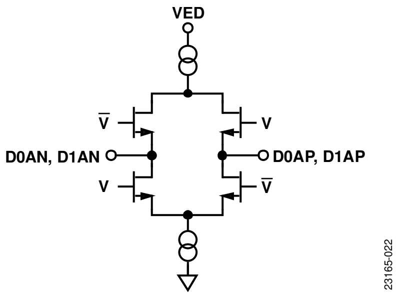


Figure 72. Equivalent Digital Output Circuit

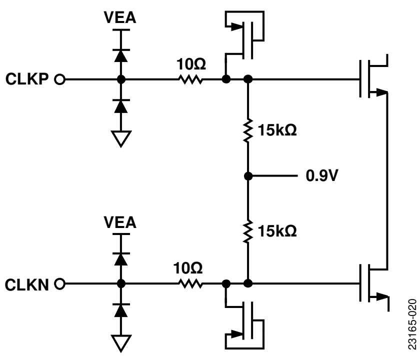


Figure 73. Equivalent Clock Input Circuit

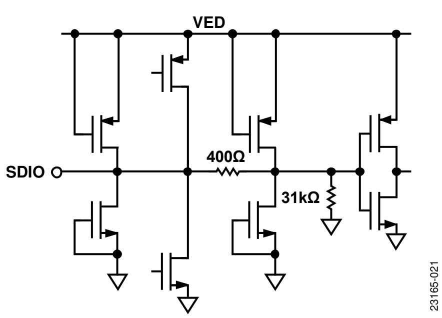


Figure 74. Equivalent SDIO Input Circuit

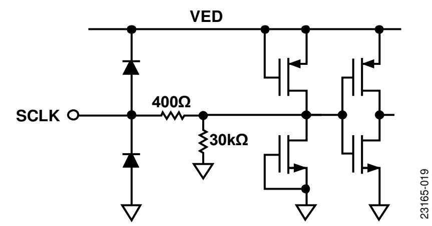


Figure 75. Equivalent SCLK Input Circuit

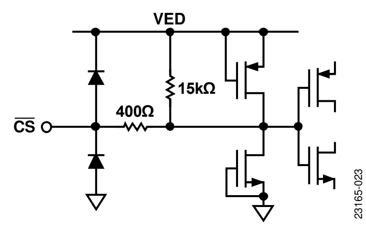


Figure 76. Equivalent $\overline{CS}$ Input Circuit

THEORY OF OPERATION

The ADA4355 integrates a field effect transistor (FET), input TIA with three switchable gains (2 kΩ, 20 kΩ, and 200 kΩ). The gain switches are designed to minimize error sources that result in slow settling time and slow overload recovery. The internal overload current protection allows the input current to exceed the full-scale current while still providing fast overload recovery. Additionally, the overload current protection enables analog input current levels up to 40 mA to be sustained with no damage to the TIA. The positive node of the TIA is biased to 1.65 V as shown in Figure 2.

Figure 77 shows the overall system transfer function. Because the photodetector provides current in only one direction (sink or source), the overall transfer function has 0.825 V offset to maximize the input range of the ADC. When the input current is 0 µA, the ADC differential input is 0.825 V. As the input current increases, the TIA output decreases toward GND. When the input current reaches 1.65 V/T_Z, the TIA output is at GND, limiting the ADC differential input voltage to −0.825 V. The positive full-scale input current is 1.65 V/T_Z, and there is room to measure negative input current down to −0.175 V/T_Z.

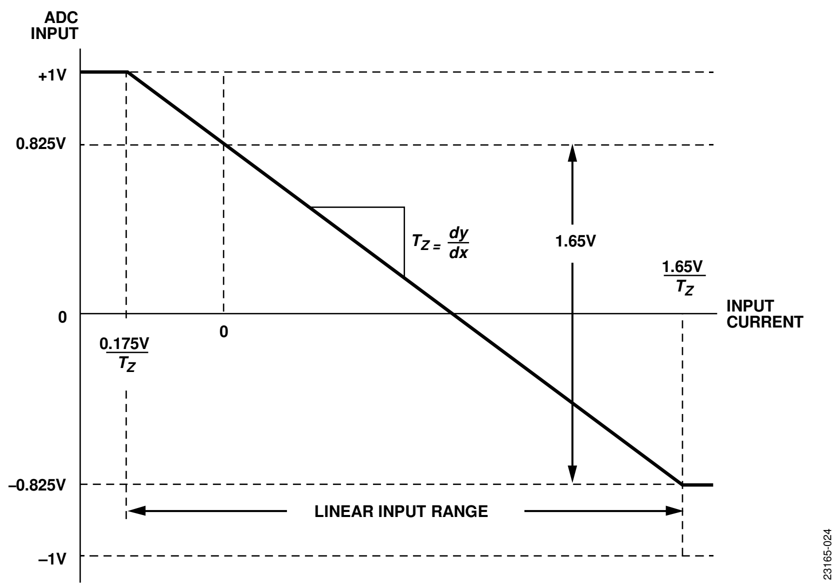


Figure 77. Overall Transfer Function

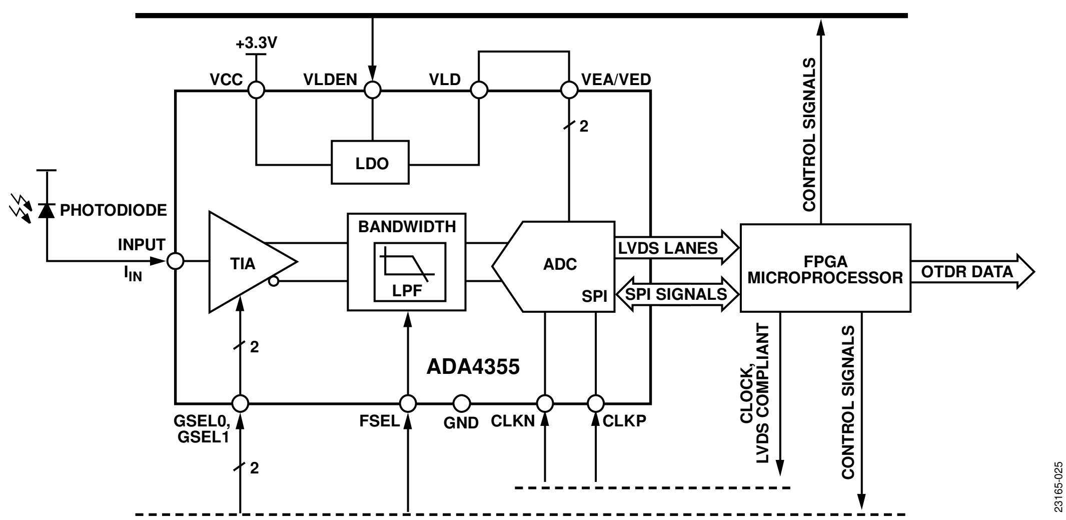


Figure 78. Typical Application Block Diagram with a Single V_{CC} Supply, FPGA Control, and Data Process

APPLICATIONS INFORMATION

POWER AND POWER CONTROL

The 12 mm × 6 mm CSP_BGA has multiple balls designated to support the ADA4355 power requirements, with 12 balls assigned to VCC, and one ball each to VEA, VED, and VLD.

Connect VCC to a clean 3.3 V supply to provide power to the ADA4355 analog core and on-chip LDO. It is important to connect all VCC balls to the 3.3 V supply. VLD is the on-chip 1.8 V LDO output, and VEA and VED are the ADC supply balls.

To power the ADC via the on-chip LDO, connect VLD to VEA and VED, and pull VLDEN high (see Figure 3).

If external 1.8 V supplies are desired, disable the on-chip LDO by pulling VLDEN low and connect VEA and VED to an external 1.8 V supply (see Figure 4).

Ground

The ADA4355 has multiple balls assigned as GND. There is no connection between the GND balls inside the package. Therefore, connect all GND balls to a low impedance GND plane on the PCB.

CLOCKS

For optimum performance, drive the ADC sample clock inputs, CLKP and CLKN, with a differential signal. The clock signal is typically ac-coupled into the CLKP and CLKN balls via a transformer or capacitors. These balls are biased internally (see Figure 73) and require no external bias.

Clock Input Options

The ADA4355 has a flexible clock input structure. The clock input can be a CMOS, LVDS, low voltage, positive emitter coupled logic (LVPECL), or sine wave signal. Regardless of the type of signal used, clock source jitter is an important consideration, as described in the Jitter Considerations section.

Figure 79 and Figure 80 show two preferred methods for clocking the ADA4355 (at clock rates up to 1 GHz prior to the internal clock divider). A low jitter clock source is converted from a single-ended signal to a differential signal using either an RF transformer or an RF balun.

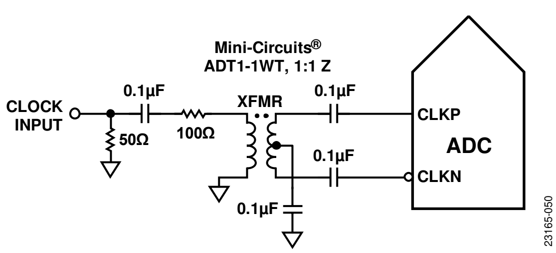


Figure 79. Transformer-Coupled Differential Clock (Up to 200 MHz)

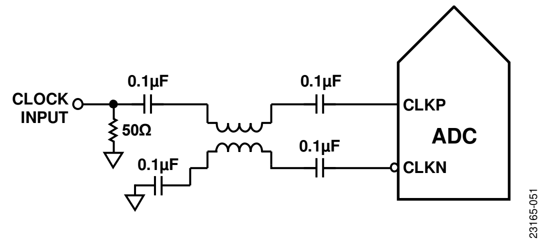


Figure 80. Balun-Coupled Differential Clock (up to 1 GHz)

The RF balun configuration is recommended for clock frequencies between 125 MHz and 1 GHz, and the RF transformer configuration is recommended for clock frequencies from 10 MHz to 200 MHz.

If a low jitter clock source is not available, another option is to ac couple a differential PECL signal to the sample clock input balls, as shown in Figure 81. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-0/AD9516-1/AD9516-2/AD9516-3/AD9516-4/AD9516-5/AD9517-0/AD9517-1/AD9517-2/AD9517-3/AD9517-4 PECL drivers offer excellent jitter performance.

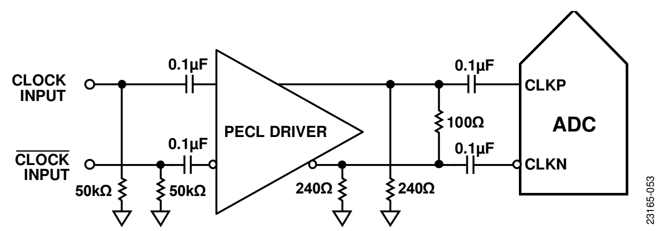


Figure 81. Differential PECL Sample Clock (up to 1 GHz)

A third option is to ac couple a differential LVDS signal to the sample clock input balls, as shown in Figure 82. The AD9510/AD9511/AD9512/AD9513/AD9514/AD9515/AD9516-0/AD9516-1/AD9516-2/AD9516-3/AD9516-4/AD9516-5/AD9517-0/AD9517-1/AD9517-2/AD9517-3/AD9517-4 LVDS drivers offer excellent jitter performance.

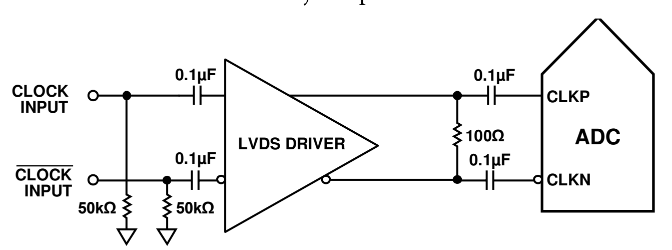


Figure 82. Differential LVDS Sample Clock (up to 1 GHz)

In some applications, it may be acceptable to drive the sample clock inputs with a single-ended 1.8 V CMOS signal. In such applications, drive the CLKP ball directly from a CMOS gate, and bypass the CLKN ball to ground with a 0.1 µF capacitor (see Figure 83).

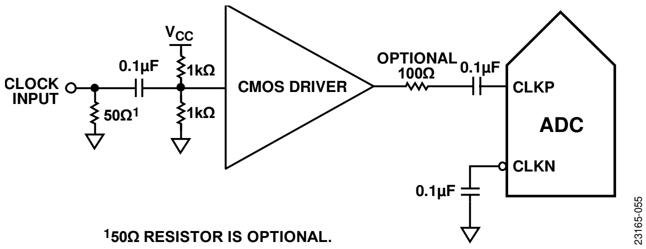


Figure 83. Single-Ended 1.8 V CMOS Input Clock (up to 200 MHz)

Input Clock Divider

The ADA4355 contains an input clock divider that can divide the input clock by integer values from 1 to 8. The power-on default, clock divider ratio is always 1. If a different clock divide ratio is required, change SPI Register 0x0B. To achieve a given sample rate, multiply the frequency of the externally applied clock by the divide value. The increased rate of the external clock normally results in lower clock jitter, which is beneficial for intermediate frequency (IF) undersampling applications.

Clock Duty Cycle

The ADC uses both clock edges to generate a variety of internal timing signals and, as a result, can be sensitive to the clock duty cycle. Commonly, a ±5% tolerance is required on the clock duty cycle to maintain dynamic performance characteristics.

The ADA4355 offers a duty cycle stabilizer (DCS) that retimes the nonsampling (falling) edge, providing an internal clock signal with a nominal 50% duty cycle. The DCS allows the user to provide a wide range of clock input duty cycles without affecting the performance of the ADA4355. Noise and distortion performance are nearly unchanged for a wide range of duty cycles with the DCS on. To bypass DCS, the user can change SPI Register 0x09.

Jitter in the rising edge of the clock is still a concern and is not easily reduced by the internal stabilization circuit. The duty cycle control loop does not function for clock rates <20 MHz, nominally. The loop has a time constant associated with it that must be considered in applications where the clock rate can change dynamically. A wait time of 5 µs is required after a dynamic clock frequency increase or decrease before the DCS loop relocks to the input signal.

Jitter Considerations

High speed, high resolution ADCs are sensitive to the quality of the clock input. The following equation shows how signal-to-noise ratio (SNR) degrades at a given input frequency (f_A) due only to aperture jitter (t_J):

$$SNR\ Degradation = 20\log_{10}\left(\frac{1}{2\pi \times f_A \times t_J}\right)$$

In this equation, the rms aperture jitter represents the rms of all jitter sources, including the clock input, analog input signal, and ADC aperture jitter specifications. IF undersampling applications are particularly sensitive to jitter. The effect of jitter alone on SNR, with no other noise contributors, is shown in Figure 84.

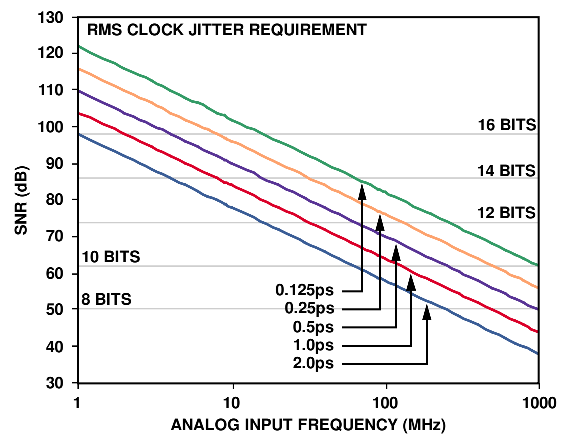


Figure 84. Ideal SNR vs. Analog Input Frequency and Jitter

Treat the clock input as an analog signal when aperture jitter can affect the dynamic range of the ADA4355. Separate clock driver power supplies from the ADC output driver supplies to avoid modulating the clock signal with digital noise. Low jitter, crystal oscillators are the best clock sources. If the clock is generated from another type of source (by gating, dividing, or other methods), it is recommended to retime the clock by the original clock as the last step.

See the AN-501 Application Note and the AN-756 Application Note for more information about jitter performance as it relates to the internal ADC of the ADA4355.

CLOCK STABILITY CONSIDERATIONS

Immediately after power-on, the ADA4355 enters an initialization phase during which an internal state machine sets up the biases and the registers for proper operation. During the initialization process, the ADA4355 needs a stable clock. If the clock source to the ADC is not present or not stable during ADC power-up, it disrupts the state machine and causes the ADC to start up in an unknown state. To correct this, invoke a digital reset via Register 0x08 after the clock source is stable. Clock instability during normal operation may also necessitate a digital reset to restore proper operation.

The pseudo code sequence for a digital reset is as follows:

1. Write Register 0x08 = 0x03 for a digital reset.
2. Write Register 0x08 = 0x00 for normal operation.

CONTROLS

The ADA4355 uses four balls to control various functions of the analog front end. Use the GSEL1 and GSEL0 balls to select T_Z (see Table 9), use the VLDEN ball to enable or disable the on-chip LDO, and use FSEL to select the filter bandwidth for the internal LPF. These control balls must be driven as these balls have no internal pull-up or pull-down resistors.

Transimpedance Gain and Performance Controls

Each T_Z determines its relevant saturation current (I_{SAT}) and input referred rms current noise (I_N). The GSEL0 and GSEL1 balls work together as shown in Table 9.

Table 9. Truth Table for GSEL1 and GEL0

GSEL1 (Ball A5)	GSEL0 (Ball A4)	Transimpedance (T_Z)
0	1	T_Z = 2 kΩ
1	0	T_Z = 20 kΩ
0	0	T_Z = 200 kΩ
1	1	Reserved

LDO Enable Controls

The on-chip 1.8 V LDO is controlled via the VLDEN ball. The control signal vs. LDO output are shown in Table 10.

Table 10. LDO Control Signal Truth Table

VLDEN (Ball F7)	VLD (Ball F12)
0	No output
1	1.8 V

LPF Bandwidth Selection

The ADA4355 uses an internal analog LPF to optimize settling time and noise performance. The LPF is controlled via the FSEL ball as shown in Table 11. Input signal pulse width should be considered when choosing the LPF bandwidth.

Table 11. LPF Truth Table

FSEL (Ball A6)	LPF Bandwidth (MHz)
0	100
1	1

DIGITAL OUTPUT AND TIMING

The ADA4355 supports high speed, digital serial outputs. These serial differential outputs are LVDS-compatible data and clock lanes. These output lanes include the D0AP, D0AN, D1AP, D1AN, DCOP, DCON, FCOP, and FCON balls.

At power-on default, the ADA4355 differential outputs conform to the ANSI-644 LVDS standard. Each of the LVDS output driver currents sets a nominal 3.5 mA. A 100 Ω differential termination resistor placed at the LVDS receiver inputs results in a nominal 350 mV swing (or 700 mV p-p differential) at the receiver.

The ADA4355 differential outputs also support a low power, reduced signal range option (similar to the IEEE 1596.3 standard) via the SPI programming. When operating in reduced range mode, the LVDS output driver current reduces to 2 mA. This reduction results in a 200 mV swing (or 400 mV p-p differential) across a 100 Ω termination at the receiver.

The LVDS outputs facilitate interfacing with LVDS receivers in custom application specific ICs (ASICs) and FPGAs for improved switching performance in noisy environments. To reduce the environmental noise impact, the PCB trace design recommends single point-to-point net topologies with a 100 Ω termination resistor placed as close as possible to the receiver. Timing errors may result if there is no far end receiver termination, or if there is poor differential trace routing. To avoid such timing errors, minimize trace lengths and keep the differential output traces close together and at equal lengths.

Figure 85 shows an example of the FCO and data stream with proper trace length and position. In Figure 85 and Figure 86, D0 is the differential signal, D0AP – D0AN, and D1 is the differential signal, D1AP – D1AN.

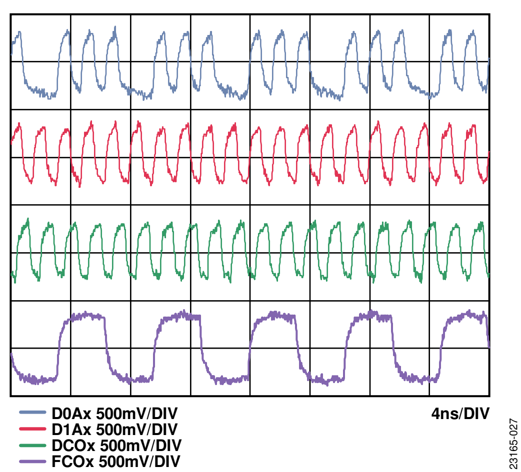


Figure 85. LVDS Output Timing Example in ANSI-644 Mode (Default)

Figure 86 shows the LVDS output timing example in reduced range mode.

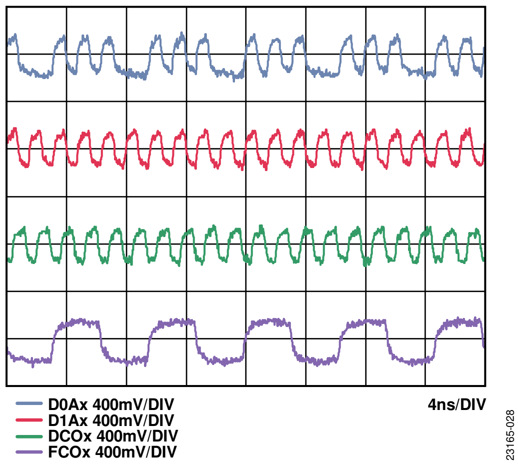


Figure 86. LVDS Output Timing Example in Reduced Range Mode

Figure 87 shows an example of the LVDS output data eye using the ANSI-644 standard (default) with trace lengths of less than 24 inches on standard FR-4 material.

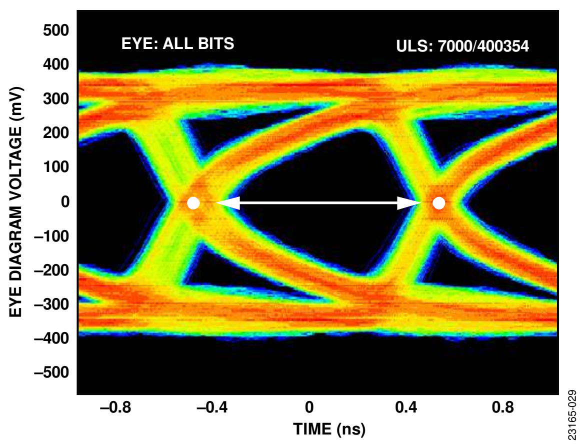


Figure 87. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths of Less Than 24 Inches (Approximate 6 Inch Trace Length Result Shown) on Standard FR-4 Material, External 100 Ω Far End Termination Only

Figure 88 shows a time interval error (TIE) jitter histogram with trace lengths of less than 24 inches on standard FR-4 material.

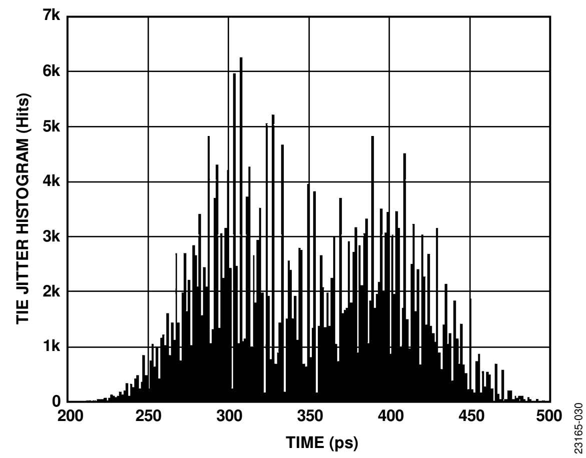


Figure 88. TIE Jitter Histogram for Trace Lengths Less Than 24 Inches (Approximate 6 Inch Trace Length Result Shown) on Standard FR-4 Material

The TIE jitter histogram reflects the decrease of the data eye opening because the edge deviates from the ideal position. It is the responsibility of the user to determine if the waveforms meet the timing budget of the design.

The format of the output data is twos complement by default. An example of the output coding format can be found in Table 12. To change the output data format to offset binary, see the Memory Map section.

Immediately after power-on, the ADA4355 output serial stream sets as double data rate (DDR), two-lane, byte wise, MSB first, 1× frame, and 16-bit mode. In this default setting, the ADA4355 data rate for each serial stream is equal to (16 bits × the sample clock rate)/2 lanes, with a maximum of 1 Gbps per lane ((16 bits × 125 MSPS)/2 lanes = 1 Gbps per lane).

Figure 89 shows an example of the LVDS output data eye using the ANSI-644 standard (default) with trace lengths greater than 24 inches on standard FR-4 material.

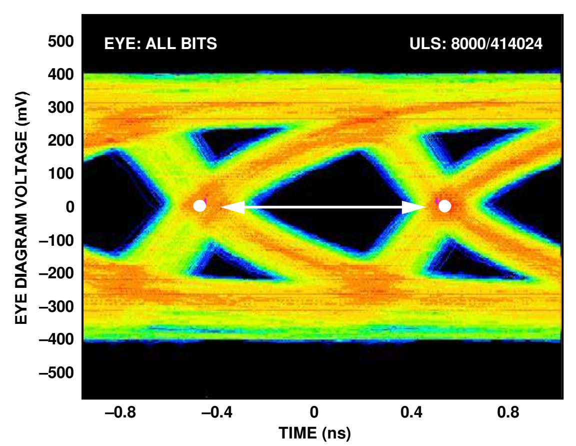


Figure 89. Data Eye for LVDS Outputs in ANSI-644 Mode with Trace Lengths Greater Than 24 Inches (Approximate 36 Inch Trace Length Result Shown) on Standard FR-4 Material, External 100 Ω Far End Termination Only

Figure 90 shows a TIE jitter histogram with trace lengths greater than 24 inches on standard FR-4 material.

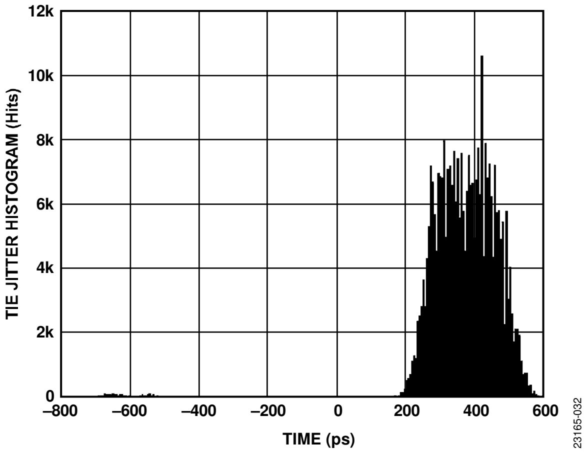


Figure 90. TIE Jitter Histogram for Trace Lengths Greater Than 24 Inches (Approximate 36 Inch Trace Length Result Shown) on Standard FR-4 Material

Two output clocks assist in capturing data from the ADA4355. The DCO clocks the output data and is equal to 4× the sample clock (CLK) rate for the default mode of operation. Data is clocked out of the ADA4355 and must be captured on the rising and falling edges of the DCO that supports DDR capturing. The FCO signals the start of a new output byte and is equal to the sample clock rate in 1× frame mode. See Figure 6 for more information.

When the SPI is used, the DCO phase can be adjusted in approximately 60° increments relative to one data cycle (30° relative to one DCO cycle). This adjustment allows the user to refine system time margins, if required. The example DCOP and DCON timing, as shown in Figure 6, is 180° relative to one data cycle (90° relative to one DCO cycle).

In power-on default mode, as shown in Figure 6, the MSB is first in the data output serial stream. This configuration can be inverted by programming the SPI so that the LSB is first in the data output serial stream.

Digital Output Coding

There are 12 digital output test pattern options available that can be initiated through the SPI. This feature is useful when validating receiver capture and timing. Refer to Table 13 for the output bit sequencing options available. Some test patterns have two serial sequential words and can be alternated in various ways depending on the test pattern chosen.

Note that some patterns do not adhere to the data format select option. In addition, custom, user defined test patterns can be assigned in the following register addresses: Register 0x19, Register 0x1A, Register 0x1B, and Register 0x1C.

Table 12. Digital Output Coding

Input (V)[1]	Condition	Offset Binary Output Mode	Twos Complement Mode
VIN+ – VIN–	<−1 V − 0.5 LSB	0000 0000 0000 0000	1000 0000 0000 0000
VIN+ – VIN–	−1 V	0000 0000 0000 0000	1000 0000 0000 0000
VIN+ – VIN–	0 V	1000 0000 0000 0000	0000 0000 0000 0000
VIN+ – VIN–	+1 V − 1.0 LSB	1111 1111 1111 1100	0111 1111 1111 1100
VIN+ – VIN–	>+1 V − 0.5 LSB	1111 1111 1111 1100	0111 1111 1111 1100

[1] VIN+ and VIN− are the positive and negative input voltages.

Table 13. Flexible Output Test Modes

Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1	Digital Output Word 2	Subject to Data Format Select	Notes
0000	Off (default)	Not applicable (N/A)	Not applicable	Not applicable	Not applicable
0001	Midscale short	1000 0000 0000 (12-bit) 1000 0000 0000 0000 (16-bit)	Not applicable	Yes	Offset binary code shown
0010	+Full-scale short	1111 1111 1111 (12-bit) 1111 1111 1111 1100 (16-bit)	Not applicable	Yes	Offset binary code shown
0011	−Full-scale short	0000 0000 0000 (12-bit) 0000 0000 0000 0000 (16-bit)	Not applicable	Yes	Offset binary code shown
0100	Checkerboard	1010 1010 1010 (12-bit) 1010 1010 1010 1000 (16-bit)	0101 0101 0101 (12-bit) 0101 0101 0101 0100 (16-bit)	No	Not applicable

Output Test Mode Bit Sequence	Pattern Name	Digital Output Word 1	Digital Output Word 2	Subject to Data Format Select	Notes
0101	PN sequence long[1]	Not applicable	Not applicable	Yes	PN23 ITU 0.150 $X^{23} + X^{18} + 1$
0110	PN sequence short[1]	Not applicable	Not applicable	Yes	PN9 ITU 0.150 $X^{9} + X^{5} + 1$
0111	One-/zero-word toggle	1111 1111 1111 (12-bit) 111 1111 1111 1100 (16-bit)	0000 0000 0000 (12-bit) 0000 0000 0000 0000 (16-bit)	No	Not applicable
1000	User input	Register 0x19 and Register 0x1A	Register 0x1B and Register 0x1C	No	Not applicable
1001	1-/0-bit toggle	1010 1010 1010 (12-bit) 1010 1010 1010 1000 (16-bit)	Not applicable	No	Not applicable
1010	1× sync	0000 0011 1111 (12-bit) 0000 0001 1111 1100 (16-bit)	Not applicable	No	Not applicable
1011	One bit high	1000 0000 0000 (12-bit) 1000 0000 0000 0000 (16-bit)	Not applicable	No	Pattern associated with the external ball
1100	Mixed frequency	1010 0011 0011 (12-bit) 1010 0001 1001 1100 (16-bit)	Not applicable	No	Not applicable

[1] All test mode options except pseudorandom number (PN) sequence short and PN sequence long can support 12-bit to 16-bit word lengths to verify data capture to the receiver.

OTDR PERFORMANCE

The adjustable transimpedance gain and LPF bandwidth of the ADA4355 enable the device to deliver excellent performance over a wide range of OTDR applications. The combination of a 200 kΩ transimpedance gain and a 1 MHz LPF cutoff frequency enables the ADA4355 to reach the low noise levels needed to achieve the dynamic range required for long haul OTDR applications. Conversely, the combination of a 2 kΩ gain and a 100 MHz LPF cutoff frequency provides the higher bandwidth needed for the narrow pulse widths that are required for the closely spaced event detection necessary for data center applications.

In addition, an extension in dynamic range can be realized by combining multiple gain measurements into a single result. This technique is discussed in the Dynamic Range Extension section.

High Dynamic Range

Figure 92 shows the OTDR test setup used to measure 160 km of optical fiber. The transimpedance gain was set to 200 kΩ, and the LPF was set to 1 MHz. The laser pulse width was 20 µs with a peak pulsed power of 15 dBm and an avalanche photodiode (APD) current gain of 3. The measurement time was limited to 3 minutes, allowing for 65,000 averages, which lowered the noise level to approximately 14 pA rms. Using the SNR = 1 calculation, the OTDR dynamic range achieved is 28 dB. Additional digital filtering can be used to further lower the noise for improved dynamic range. Applying a simple moving average filter with a window size of 1000 samples improves the dynamic range to 31 dB. Figure 91 shows a comparison of the OTDR results for before digital filtering and after digital filtering.

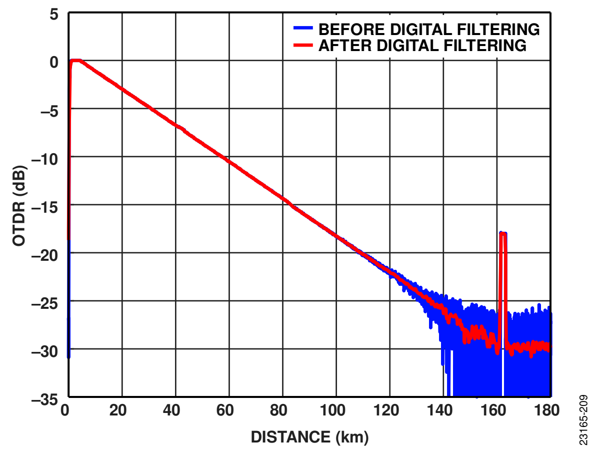


Figure 91. OTDR Measurement on 160 km Optical Fiber

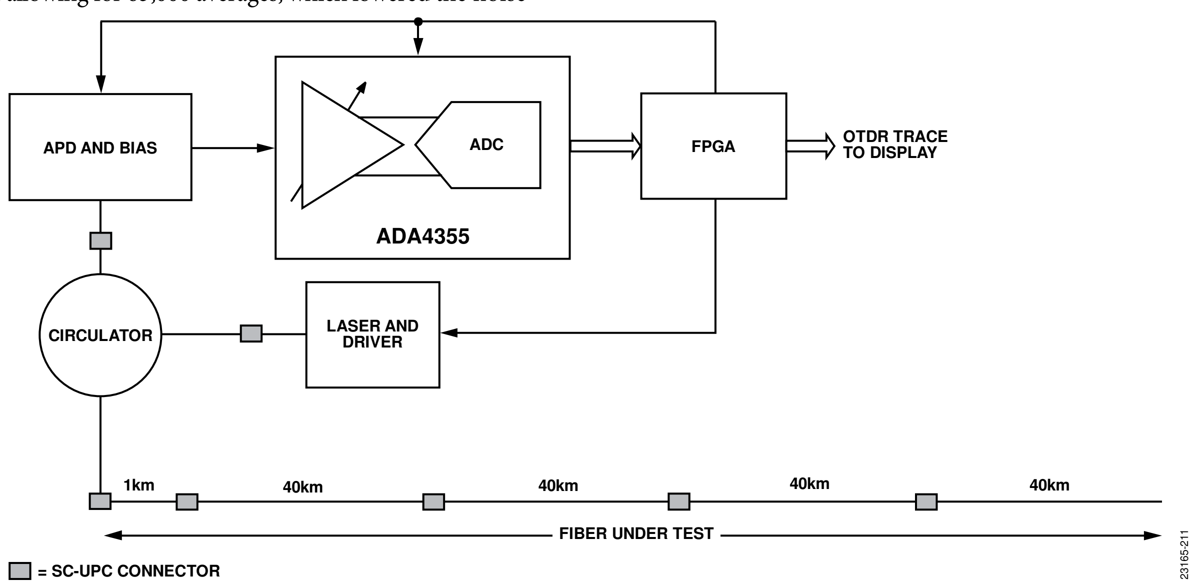


Figure 92. OTDR Test Set-Up

Dynamic Range Extension

One of the primary benefits of selectable gains on the ADA4355 is the ability to extend the dynamic range of the OTDR measurement. A length of optical fiber approximately 160 km long, with 0.2 dB/km of attenuation, was once again tested. The ADA4355 transimpedance gain was maintained at 200 kΩ, as was the laser launch power and pulse width at 15 dBm and 20 µs, respectively. Averaging was held to 3 minutes, or 65,000 averages, and a moving average filter was used. For this case, the APD bias voltage was increased, thereby raising the APD current gain to approximately 30×.

The measurement result is shown in Figure 93 and reveals that the system becomes saturated at an 8 µA input current. Because of this saturation, the first 20 km of fiber cannot be analyzed.

Note that the y-axis of Figure 93 is expressed in terms of current so that the 8 µA saturation current can easily be seen.

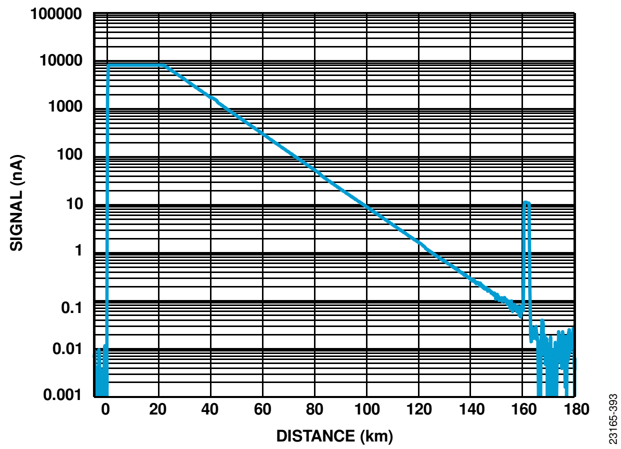


Figure 93.OTDR Measurement with 200 kΩ Gain

Switching the ADA4355 gain from 200 kΩ to 20 kΩ allows a maximum signal level that is 10× larger than when using 200 kΩ, which means the saturation current is now 80 µA and that much of the region below 20 km can now be analyzed.

Figure 94 shows the results from a single frame taken with 20 kΩ gain and using all the same settings as the 200 kΩ measurement. The single frame measurement takes 2 ms to complete only and only the first 20 km are of interest.

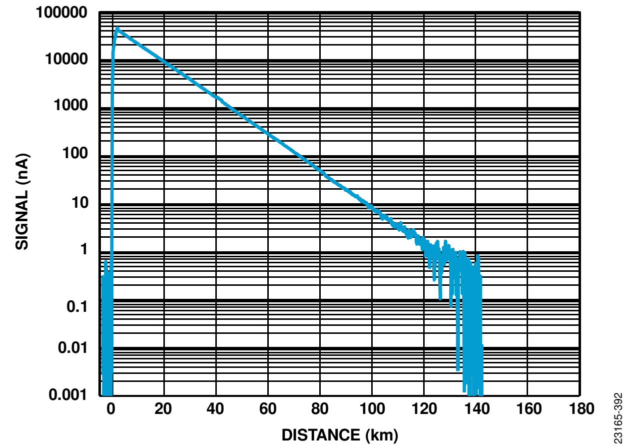


Figure 94. OTDR Measurement with 20 kΩ Gain

Combining the measurements from Figure 93 and Figure 94 yield the results shown in Figure 95. The portion >20 km comes from Figure 93, and the portion ≤20 km comes from Figure 94. The combined dynamic range is 34.5 dB, which is an extension of almost 4 dB at a time cost of only 2 ms.

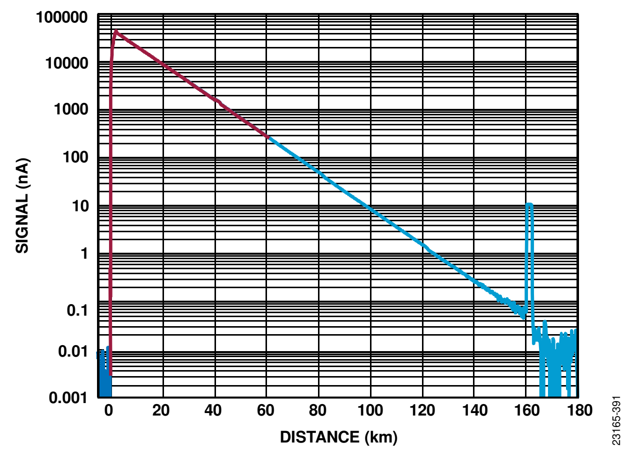


Figure 95. OTDR Combined Measurement, 200 kΩ Gain and 20 kΩ Gain

If additional dynamic range is required, the process can be repeated by using 2 kΩ gain, which raises the saturation current to 800 µA, and then stitching all three individual results together.

High Spatial Resolution

The ADA4355 has a maximum sampling rate of 125 MSPS, which translates to an 8 ns sampling period and a best case theoretical spatial resolution of approximately 0.8 m. This resolution is marginally acceptable for pulse widths of approximately 10 ns or greater. Although, with only one sample per pulse, closely spaced events can be difficult to detect. However, while using a fixed sampling rate, spatial resolution can be increased by using a phase shift to advance or delay the laser pulse and/or the rising and falling edge of the sampling clock.

Figure 96 shows the sampling period of the ADA4355 and the placement of the laser driving pulses. In this example, four phase shifts were applied (0 ns, 2 ns, 4 ns, and 6 ns). This phase shifting effectively improves the spatial resolution from approximately 0.8 m to 0.2 m, thereby enabling the use of shorter pulse widths and positive detection of more closely spaced events.

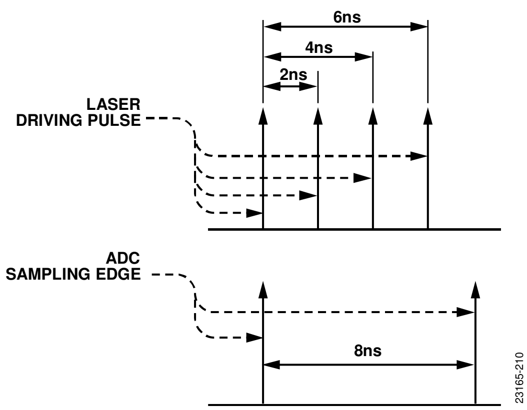


Figure 96. Phase Shifting the Laser Pulses

Figure 97 clearly shows the benefit of phase shifting for the detection of closely spaced events. A 4 ns pulse was used to detect two events 1 m apart. Figure 97 shows two distinct events are detected in the phase shifted case, while the two events blend together and appear as a single event in the nonphase shifted case.

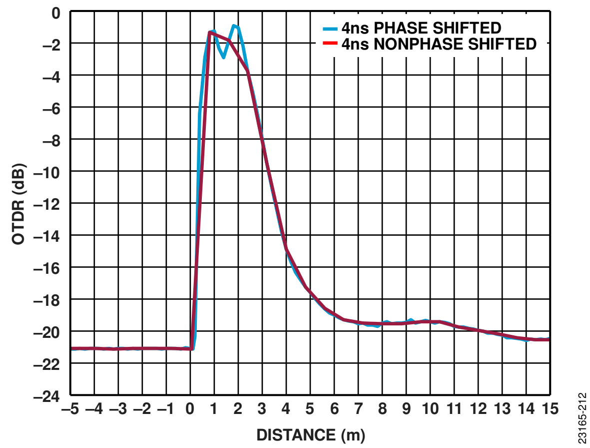


Figure 97. Comparison of Closely Spaced Event Detection with and Without Phase Shifting, 4 ns Pulse Width, 1 m Event Separation

Figure 98 illustrates the method used to build the phase shifted curve from Figure 97. The nonphase shifted measurement was repeated four times, but each time it was shifted an additional 2 ns to the right. The phase shifted curve from Figure 97 was then assembled by taking the points from the four individual measurements and combining these points as shown in Figure 98. The end result takes four times longer to complete. However, the end result has four times as many data points (2 ns apart), resulting in much improved horizontal resolutions.

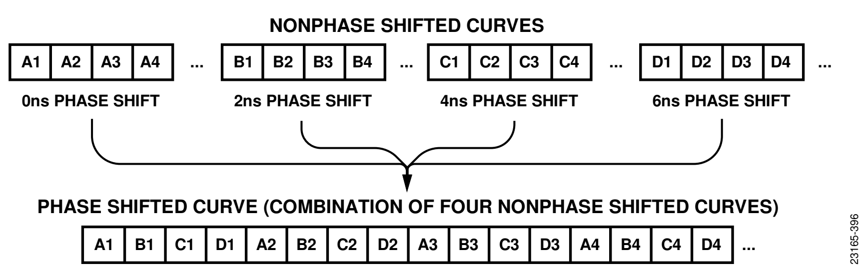


Figure 98. Method Used to Assemble Phase Shifted Curve From Figure 97

PCB DESIGN TIPS

Signal Integrity Recommendations

Place the photodiode signal source as close as possible to the ADA4355 input to minimize trace length and associated parasitic capacitance. Clear away all ground layers directly underneath the input trace to reduce parasitics even further. Additionally, match all LVDS line (DCON, DCOP, FCON, FCOP, D0AN, D0AP, D1AN, and D1AP) lengths to eliminate potential timing issues.

Thermal Design Recommendations

The ADA4355 uses multiple VCC and GND balls to facilitate the internal power and grounding requirements. All of these balls must be connected for proper electrical connectivity within the module. Additionally, the PCB connection of the multiple VCC and GND balls is an integral part of the thermal design. All of the ADA4355 VCC and GND balls must be connected to a PCB copper plane with the lowest thermal resistance possible. To achieve the best thermal performance, these planes must have as many thermal vias as practical to provide the lowest possible thermally resistive path for heat dissipation to flow through the bottom of the PCB. Solder fill or plug these vias.

Surface-Mount Design

Table 14 is provided as an aid to PCB design to accommodate CSP_BGA style surface-mount packages. For industry-standard design recommendations, refer to IPC-7351, *Generic Requirements for Surface Mount Design and Land Pattern Standard*.

Table 14. CSP_BGA Data for Use with Surface-Mount Design

Package	Ball Attach Type	Solder Mask Opening	Ball Pad Size
84-Ball CSP_BGA (BC-84-4)	Solder mask defined	0.35 mm diameter	0.40 mm diameter

SPI

The ADA4355 SPI allows users to configure the internal ADC for specific functions or operations through a structured register space. Registers are accessible via the SPI port. Register contents can be modified by writing to the port. Bytes that can be further divided into fields constitute register memory, which is documented in the Memory Map section. Information specified in this data sheet takes precedence over the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*, which provides general information.

CONFIGURATION USING THE SPI

The ADA4355 uses a 3-wire SPI configuration, SCLK, SDIO, and $\overline{CS}$. See Table 15 for the functionality for each ball.

Table 15. Serial Port Interface Balls

Mnemonic	Function
SCLK	Serial clock when $\overline{CS}$ is low. The serial shift clock input, which synchronizes serial interface reads and writes.
SDIO	Serial data input/output when $\overline{CS}$ is low. Serves as an input or output, depending on the instruction sent and the relative position in the timing frame.
$\overline{CS}$	Chip select. An active low control that enables the SPI mode read and write cycles.

The falling edge of $\overline{CS}$, in conjunction with the rising edge of SCLK, determines the start of the framing. An example of the serial timing is shown in Figure 5. See Table 4 for definitions of the timing parameters.

In an ADA4355 application, $\overline{CS}$ must be held low at power-up to enable SPI mode, and then kept low, which is called streaming. $\overline{CS}$ can stall high between bytes to allow additional external timing.

During the instruction phase of an SPI operation, a 16-bit instruction is transmitted. Data follows the instruction phase, and the length of this data is determined by the W0 and W1 bits (see Figure 5).

In addition to word length, the instruction phase determines whether the serial frame is a read or write operation, allowing the serial port to both program the chip and to read the contents of the on-chip memory. The first bit of the first byte in a multibyte serial data transfer frame indicates whether a read command or a write command is issued. If the instruction is a readback operation, performing a readback causes the SDIO ball to change direction from an input to an output at the appropriate point in the serial frame.

All data is composed of 8-bit words. Data can be sent in MSB first mode or in LSB first mode. MSB first mode is the default on power-up and can be changed via the SPI port configuration register. For more information about this and other features, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

ADC SPI START-UP SEQUENCE

To ensure proper device operation and power dissipation, the following SPI sequence must be written after the ADA4355 is powered on and anytime a power cycle occurs:

```
//SPI_WRITE(Memory Map Register,
  Register Value)
SPI_WRITE(0x00, 0x00);
SPI_WRITE(0x05, 0x02);
SPI_WRITE(0x22, 0x03);
SPI_WRITE(0x05, 0x31);
```

HARDWARE INTERFACE

The balls described in Table 15 comprise the physical interface between the user-programming device and the serial port of the ADA4355. The SCLK ball and the $\overline{CS}$ ball function as inputs when using the SPI interface. The SDIO ball is bidirectional, functioning as an input during write phases and as an output during readback.

The SPI interface is flexible enough to be controlled by either FPGAs or microcontrollers. One method for SPI configuration is described in detail in the AN-812 Application Note, *Microcontroller-Based Serial Port Interface (SPI) Boot Circuit*.

It is recommended that the SPI port not be active during periods when the full dynamic performance of the converter is required. Because the signals on SCLK, $\overline{CS}$, and SDIO are typically asynchronous to the ADC clock, noise from these signals can degrade converter performance. If the on-board SPI bus is used for other devices, it may be necessary to provide buffers between this bus and the ADA4355 to prevent these signals from transitioning at the converter inputs during critical sampling periods.

SPI ACCESSIBLE FEATURES

Table 16 provides a brief description of the general features accessible via the SPI. These features are described in general in the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. ADA4355 device-specific features are described in Table 17, the memory map register table.

Table 16. Features Accessible Using the SPI

Feature Name	Description
Power Mode	Allows the user to set either power-down mode or standby mode
Clock	Allows the user to access the DCS, set the clock divider, and set the clock divider phase
Offset	Allows the user to digitally adjust the converter offset

MEMORY MAP

OVERVIEW

The memory map register table (see Table 17) describes the ADA4355 registers. These registers configure and control the ADC only.

The memory map is divided into three sections: the chip configuration registers, the device index register, and the global ADC function registers, including setup and control.

Each register has eight bit locations. The column with the Bit 7 (MSB) heading contains the most significant bit of the default hexadecimal value given. For example, Register 0x05, the device index register, has a hexadecimal default value of 0x33, which means that in Register 0x05, Bits[7:6] = 00, Bits[5:4] = 11, Bits[3:2] = 00, and Bits [1:0] = 11 (in binary).

For more information on this SPI port function, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*. This application note documents the functions controlled by Register 0x00 to Register 0xFF.

Open Locations

In the Table 17, the register bit open locations are reserved to the ADA4355. These bits must be set to 0 at all times.

Default Values

The default values are available in Table 17.

After power-on, all registers have loaded their default values. To soft reset the ADA4355, use Register 0x00. All registers, except the read only register (Register 0x02), are loaded with default values.

Logic Levels

An explanation of logic level terminology follows:

- “Bit is set” is synonymous with “bit is set to Logic 1” or “writing Logic 1 for the bit.”
- “Clear a bit” is synonymous with “bit is set to Logic 0” or “writing Logic 0 for the bit.”

MEMORY MAP REGISTER TABLE

The ADA4355 uses a 3-wire interface and 16-bit addressing. Therefore, Bit 0 and Bit 7 in Register 0x00 are set to 0, and Bit 3 and Bit 4 are set to 1.

When Bit 5 in Register 0x00 is set high, the SPI enters a soft reset, where all of the user registers revert to their default values, and Bit 2 is automatically cleared.

Table 17. Memory Map Register

Reg. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments
Chip Configuration Registers											
0x00	SPI port configuration	0 = SDO active	LSB first	Soft reset	1 = 16-bit address	1 = 16-bit address	Soft reset	LSB first	0 = SDO active	0x18	Nibbles are mirrored to allow a given register value to perform the same function for either MSB-first or LSB-first mode.
0x01	Chip ID (global)	8-bit chip ID, Bits[7:0], ADA4355								0x8B	Unique chip ID used to differentiate devices; read only.
Device Index and Transfer Registers											
0x05	Device index	Open	Open	Clock channel DCO	Clock channel FCO	Open	Open	01 = data channel enabled, 00 = data channel disabled, Bit 1 only used after start up or power cycle, see ADC SPI Start-Up Sequence		0x33	Bits are set to determine which channels will receive the next write command. Bit 1 is only used after start-up or power cycle.
0xFF	Transfer	Open	Open	Open	Open	Open	Open	Open	Initiate override	0x00	Set resolution/ sample rate override.
Global ADC Function Registers											
0x08	ADC power modes (global)	Open	Open	Open	Open	Open	Open	Power mode: 00 = chip run, 01 = full power-down, 10 = standby, 11 = reset		0x00	Determines various generic modes of chip operation.
0x09	Clock (global)	Open	Open	Open	Open	Open	Open	Open	DCS: 0 = off, 1 = on	0x00	Turns DCS on or off.
0x0B	Clock divide (global)	Open	Open	Open	Open	Open	Clock divide ratio[2:0]: 000 = divide by 1 001 = divide by 2 010 = divide by 3 011 = divide by 4 100 = divide by 5 101 = divide by 6 110 = divide by 7 111 = divide by 8			0x00	Not applicable.

Reg. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments
0x0D	Test mode (local except for PN sequence resets)	User input test mode: 00 = single, 01 = alternate, 10 = single once, 11 = alternate once (affects user input test mode only, Bits[3:0] = 1000)		Reset PN long gen	Reset PN short gen	Output test mode, Bits[3:0] (local): 0000 = off (default), 0001 = midscale short, 0010 = positive full-scale, 0011 = negative full-scale, 0100 = alternating checkerboard, 0101 = PN23 sequence, 0110 = PN9 sequence, 0111 = one-/zero-word toggle, 1000 = user input, 1001 = 1-/0-bit toggle, 1010 = 1× sync, 1011 = one bit high, 1100 = mixed bit frequency				0x00	When set, the test data is placed on the output balls in place of normal data.
0x14	Output mode	Open	LVDS-ANSI/ LVDS-IEEE option: 0 = LVDS-ANSI, 1 = LVDS-IEEE reduced range link (global), see Table 18	Open	Open	Open	Output invert (local)	Open	Output format: 0 = offset binary, 1 = twos complement (global)	0x01	Configures the outputs and format of the data.
0x15	Output adjust	Open	Open	Output driver termination, Bits[1:0]: 00 = none, 01 = 200 Ω, 10 = 100 Ω, 11 = 100 Ω		Open	Open	Open	Output drive: 0 = 1× drive, 1 = 2× drive	0x00	Determines LVDS or other output properties.
0x16	Output phase	Open	Input clock phase adjust, Bits[6:4] (value is the number of input clock cycles of phase delay), see Table 19			Output clock phase adjust, Bits[3:0] (0000 through 1011), see Table 20				0x03	On devices using global clock divide, Register 0x16 determines which phase of the divider output is used to supply the output clock. Internal latching is unaffected.
0x19	USER_PATT1_ LSB (global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User Defined Pattern 1 LSB.
0x1A	USER_PATT1_ MSB (global)	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User Defined Pattern 1 MSB.
0x1B	USER_PATT2_ LSB (global)	B7	B6	B5	B4	B3	B2	B1	B0	0x00	User Defined Pattern 2 LSB.
0x1C	USER_PATT2_ MSB (global)	B15	B14	B13	B12	B11	B10	B9	B8	0x00	User Defined Pattern 2 MSB.
0x21	Serial output data control (global)	LVDS output: 0 = MSB first (default), 1 = LSB first	SDR/DDR one-lane/two-lane, bitwise/bytewise, Bits[6:4]: 000 = SDR two-lane, bitwise, 001 = SDR two-lane, bytewise, 010 = DDR two-lane, bitwise, 011 = DDR two-lane, bytewise (default) , 100 = DDR one-lane, wordwise			Encode mode : 0 = normal encode rate mode (default), 1 = low encode mode for sample rate of <20 MSPS	0 = 1× frame (default), 1 = 2× frame	Serial output number of bits: 00 = 16 bits (default), 10 = 12 bits		0x30	Serial stream control. Sample rate of <20 MSPS requires that Bits[6:4] = 100 (DDR one-lane) and Bit 3 = 1 (low encode mode).

Reg. (Hex)	Register Name	Bit 7 (MSB)	Bit 6	Bit 5	Bit 4	Bit 3	Bit 2	Bit 1	Bit 0 (LSB)	Default Value (Hex)	Comments
0x22	Serial channel status (local)	Open	Open	Open	Open	Open	Open	Channel output reset	Channel power-down	0x00	Used to power down individual sections of a converter.
0x100	Resolution/ sample rate override	Open	Resolution/ sample rate override enable	Resolution: 01 = 14 bits, 10 = 12 bits		Open	Sample rate: 000 = 20 MSPS, 001 = 40 MSPS, 010 = 50 MSPS, 011 = 65 MSPS, 100 = 80 MSPS, 101 = 105 MSPS, 110 = 125 MSPS			0x00	Resolution/ sample rate override (requires writing to the transfer register, 0xFF).
0x101	User input/ output control	Open	Open	Open	Open	Open	Open	Open	SDIO pull-down	0x00	Disables SDIO pull-down.

MEMORY MAP REGISTER DESCRIPTIONS

For information on registers not described herein, and for general information about the functions controlled in Register 0x00 to Register 0xFF, see the AN-877 Application Note, *Interfacing to High Speed ADCs via SPI*.

Chip ID (Register 0x01)

The power-on default value of this register is 0x8B.

Register 0x01 is a read-only register that is used for chip identification and for SPI authentication.

Device Index (Register 0x05)

The power-on default value of this register is 0x33.

Bits[7:6]—Open

Bit 5—Clock Channel DCO

Bit 5 is used to select the output DCO clock channel.

Bit 4—Clock Channel FCO

Bit 4 is used to select the output FCO clock channel.

Bits[3:2]—Open

Bits[1:0]—Data Channel

Setting Bit 1 enables the data channel to receive SPI write commands. To ensure Bit 0 is configured correctly, perform the SPI write commands in the ADC SPI Start-Up Sequence section immediately after start-up or reset.

ADC Power Modes (Register 0x08)

The power-on default value of this register is 0x00.

Bits[7:2]—Open

Bits[1:0]—Power Mode

In normal operation (Bits[1:0] = 00), ADC is active.

In power-down mode (Bits[1:0] = 01), the digital datapath clocks are disabled, while the digital datapath is reset. Outputs are disabled.

In standby mode (Bits[1:0] = 10), the digital datapath clocks, and the outputs are disabled.

During a digital reset (Bits[1:0] = 11), all digital clocks and outputs (where applicable) on the chip are reset, except the SPI port. The SPI port is always left under control of the user, that is, the port is never automatically disabled or in reset, except by power-on reset.

Clock (Register 0x09)

The power-on default value of this register is 0x00

Bits[7:1]—Open

Bit 0—DCS

This bit turns the DCS on and off.

Clock Divide (Register 0x0B)

The power-on default value of this register is 0x00

Bits[7:3]—Open

Bits[2:0]—Clock Divide Ratio

Bits [2:0] are used to set the clock divide ratio.

Output Mode (Register 0x14)

The power-on default value of this register is 0x01.

Bit 7—Open

Bit 6—LVDS-ANSI/LVDS-IEEE Option

Setting this bit selects the LVDS-IEEE (reduced range) option.

The default setting for this bit is LVDS-ANSI. When LVDS-ANSI or the LVDS-IEEE reduced range link is selected, the driver current is automatically selected to give the proper output swing.

Table 18. LVDS-ANSI/LVDS-IEEE Options

Bit 6	Output Mode	Output Driver Current
0	LVDS-ANSI (default)	Automatically selected to give proper swing
1	LVDS-IEEE reduced range link	Automatically selected to give proper swing

Bits[5:3]—Open

Bit 2—Output Invert

Setting this bit inverts the output bit stream.

Bit 1—Open

Bit 0—Output Format

By default, this bit is set to send the data output in twos complement format. Clearing this bit to 0 changes the output mode to offset binary.

Output Adjust (Register 0x15)

The power-on default value of this register is 0x00.

Bits[7:6]—Open

Bits[5:4]—Output Driver Termination

These bits allow the user to select the internal termination resistor.

Bits[3:1]—Open

Bit 0—Output Driver

Bit 0 of the output adjust register controls the drive strength on the LVDS driver of the FCO and DCO outputs only. The default value sets the drive to 1×, or the drive can increase to 2× by setting the appropriate channel bit in Register 0x05 and then setting Bit 0, Register 0x15. These features cannot be used with the output driver termination select. The termination selection takes precedence over the 2× driver strength on FCO and DCO when both the output driver termination and output driver are selected.

Output Phase (Register 0x16)

The power-on default value of this register is 0x03.

Bit 7—Open

Bits[6:4]—Input Clock Phase Adjust

When the clock divider (Register 0x0B) is used, the applied clock is at a higher frequency than the internal sampling clock. Bits[6:4] of Register 0x16 determine at which phase the external clock sampling occurs. The input clock phase adjust is only applicable when the clock divider is used. Selecting a value for Bits[6:4] greater than Register 0x0B, Bits[2:0] is prohibited. See Table 19.

Bits[3:0]—Output Clock Phase Adjust

See Table 20 for details.

Table 19. Input Clock Phase Adjust Options

Input Clock Phase Adjust, Register 0x16, Bits[6:4]	Number of Input Clock Cycles of Phase Delay
000 (Default)	0
001	1
010	2
011	3
100	4
101	5
110	6
111	7

Table 20. Output Clock Phase Adjust Options

Output Clock (DCO), Phase Adjust, Register 0x16, Bits[3:0]	DCO Phase Adjustment (Approximate Degrees Relative to the DxAP/DxAN Edge)
0000	0
0001	60
0010	120
0011 (Default)	180
0100	240
0101	300
0110	360
0111	420
1000	480
1001	540
1010	600
1011 through 1111	660

Serial Output Data Control (Register 0x21)

The power-on default value of this register is 0x30.

The serial output data control register programs the ADA4355 in various output data modes, depending on the data capture solution. Table 21 describes the various serialization options available in the ADA4355. Note that, in single data rate (SDR) mode, the DCO frequency is double that of the frequency in DDR mode for a given sample rate. In SDR mode, to stay within the capability of the DCO LVDS driver, reduce the ADC sample rate to ≤62.5 MSPS to keep the DCO frequency at ≤500 MHz.

User Input/Output Control 2 (Register 0x101)

The power-on default value of this register is 0x00.

Bits[7:1]—Open

Bit 0—Disable SDIO Pull-Down

Bit 0 can be set to disable the internal 31 kΩ pull-down resistor on the SDIO ball, which limits the loading when many devices are connected to the SPI bus.

Table 21. Register 0x21 Options

	Serialization Options Selected				
Register 0x21 Contents	**Serial Output Number of Bits (SONB)**	**Frame Mode**	**Serial Data Mode**	**DCO Multiplier**	**Timing Diagram**
0x30	16-bit	1×	DDR two-lane bytewise	$4 \times f_S$	See Figure 6 (default setting)
0x20	16-bit	1×	DDR two-lane bitwise	$4 \times f_S$	See Figure 6
0x10	16-bit	1×	SDR two-lane bytewise	$8 \times f_S$	See Figure 6
0x00	16-bit	1×	SDR two-lane bitwise	$8 \times f_S$	See Figure 6
0x34	16-bit	2×	DDR two-lane bytewise	$4 \times f_S$	See Figure 8
0x24	16-bit	2×	DDR two-lane bitwise	$4 \times f_S$	See Figure 8
0x14	16-bit	2×	SDR two-lane bytewise	$8 \times f_S$	See Figure 8
0x04	16-bit	2×	SDR two-lane bitwise	$8 \times f_S$	See Figure 8
0x40	16-bit	1×	DDR one-lane wordwise	$8 \times f_S$	See Figure 10
0x32	12-bit	1×	DDR two-lane bytewise	$3 \times f_S$	See Figure 7
0x22	12-bit	1×	DDR two-lane bitwise	$3 \times f_S$	See Figure 7
0x12	12-bit	1×	SDR two-lane bytewise	$6 \times f_S$	See Figure 7
0x02	12-bit	1×	SDR two-lane bitwise	$6 \times f_S$	See Figure 7
0x36	12-bit	2×	DDR two-lane bytewise	$3 \times f_S$	See Figure 9
0x26	12-bit	2×	DDR two-lane bitwise	$3 \times f_S$	See Figure 9
0x16	12-bit	2×	SDR two-lane bytewise	$6 \times f_S$	See Figure 9
0x06	12-bit	2×	SDR two-lane bitwise	$6 \times f_S$	See Figure 9
0x42	12-bit	1×	DDR one-lane wordwise	$6 \times f_S$	See Figure 11

OUTLINE DIMENSIONS

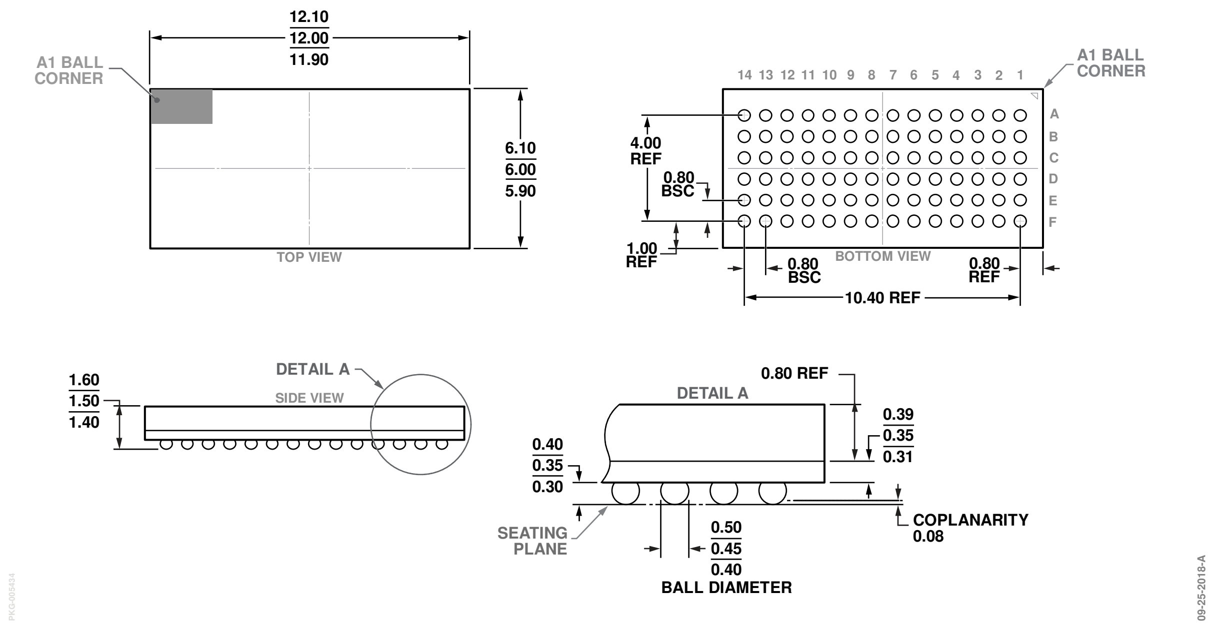


Figure 99. 84-Ball Chip Scale Package Ball Grid Array [CSP_BGA]
(BC-84-4)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADA4355ABCZ	−40°C to +85°C	84-Ball Chip Scale Package Ball Grid Array [CSP_BGA]	BC-84-4
EVAL-ADA4355EBZ		Evaluation Board	

[1] Z = RoHS Compliant Part