KAF-16803

4096 (H) x 4096 (V) Full Frame CCD Image Sensor

ON Semiconductor®

www.onsemi.com

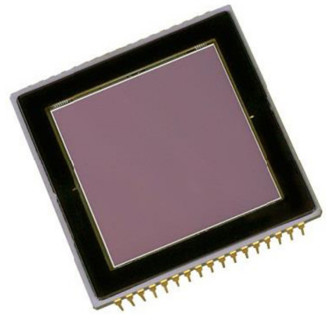


Figure 1. KAF−16803 CCD Image Sensor

Description

The KAF−16803 image sensor is a redesigned version of the popular KAF−16801 image sensor (4096 (H) × 4096 (V) pixel resolution), with enhancements that specifically target the needs of high performance digital radiography applications. Improvements include enhanced quantum efficiency for improved DQE at higher spatial frequencies, lower noise for improved contrast in areas of high density, and anti-blooming protection to prevent image bleed from over exposure in regions outside the patient.

The sensor utilizes the TRUESENSE Transparent Gate Electrode to improve sensitivity compared to the use of a standard front side illuminated polysilicon electrode, as well as microlenses to maximize light sensitivity. When combined with large imaging area and small pixel size, the KAF−16803 provides the sensitivity, resolution and contrast necessary for high quality digital radiographs.

To simplify device integration, the KAF−16803 image sensor uses the same pin-out and package as the KAF−16801 image sensor.

Table 1. GENERAL SPECIFICATIONS

Parameter	Typical Value
Architecture	Full Frame CCD, Square Pixels
Total Number of Pixels	4145 (H) × 4128 (V) = 17.1 Mp
Number of Effective Pixels	4127 (H) × 4128 (V) = 17.0 Mp
Number of Active Pixels	4096 (H) × 4096 (V) = 16.8 Mp
Pixel Size	9.0 μm (H) × 9.0 μm (V)
Active Image Size	36.8 mm (H) × 36.8 mm (V) 52.1 mm Diagonal 645 1.3x Optical Format
Aspect Ratio	1:1
Horizontal Outputs	1
Saturation Signal	100,000 electrons
Output Sensitivity	22 μV/e−
Quantum Efficiency (550 nm)	60%
Responsivity (550 nm)	28.7 V/μJ/cm^2
Read Noise (f = 4 MHz)	9 e−
Dark Signal	3 e−/pix/sec
Dark Current Doubling Temperature	6.3°C
Linear Dynamic Range (f = 4 MHz)	80 dB
Blooming Protection (4 ms Exposure Time)	> 100 X Saturation Exposure
Maximum Date Rate	10 MHz
Package	CERDIP (Sidebrazed, CuW)
Cover Glass	AR Coated, 2 Sides and Taped Clear

NOTE: Parameters above are specified at T = 25°C unless otherwise noted.

Features

- TRUESENSE Transparent Gate Electrode for High Sensitivity
- High Resolution
- Large Image Area
- High Quantum Efficiency
- Low Noise Architecture
- Board Dynamic Range

Application

- Medical
- Scientific

ORDERING INFORMATION

See detailed ordering and shipping information on page 2 of this data sheet.

ORDERING INFORMATION

Table 2. ORDERING INFORMATION − KAF−16803 IMAGE SENSOR

Part Number	Description	Marking Code
KAF−16803−ABA−DD−BA	Monochrome, Microlens, CERDIP Package (Sidebrazed, CuW), AR Coated 2 Sides, Standard Grade	KAF−16803−ABA Serial Number
KAF−16803−ABA−DD−AE	Monochrome, Microlens, CERDIP Package (Sidebrazed, CuW), AR Coated 2 Sides, Engineering Sample	
KAF−16803−ABA−DP−BA	Monochrome, Microlens, CERDIP Package (Sidebrazed, CuW), Taped Clear Cover Glass, Standard Grade	
KAF−16803−ABA−DP−AE	Monochrome, Microlens, CERDIP Package (Sidebrazed, CuW), Taped Clear Cover Glass, Engineering Sample	

See the ON Semiconductor *Device Nomenclature* document (TND310/D) for a full description of the naming convention used for image sensors. For reference documentation, including information on evaluation kits, please visit our web site at www.onsemi.com.

DEVICE DESCRIPTION

Architecture

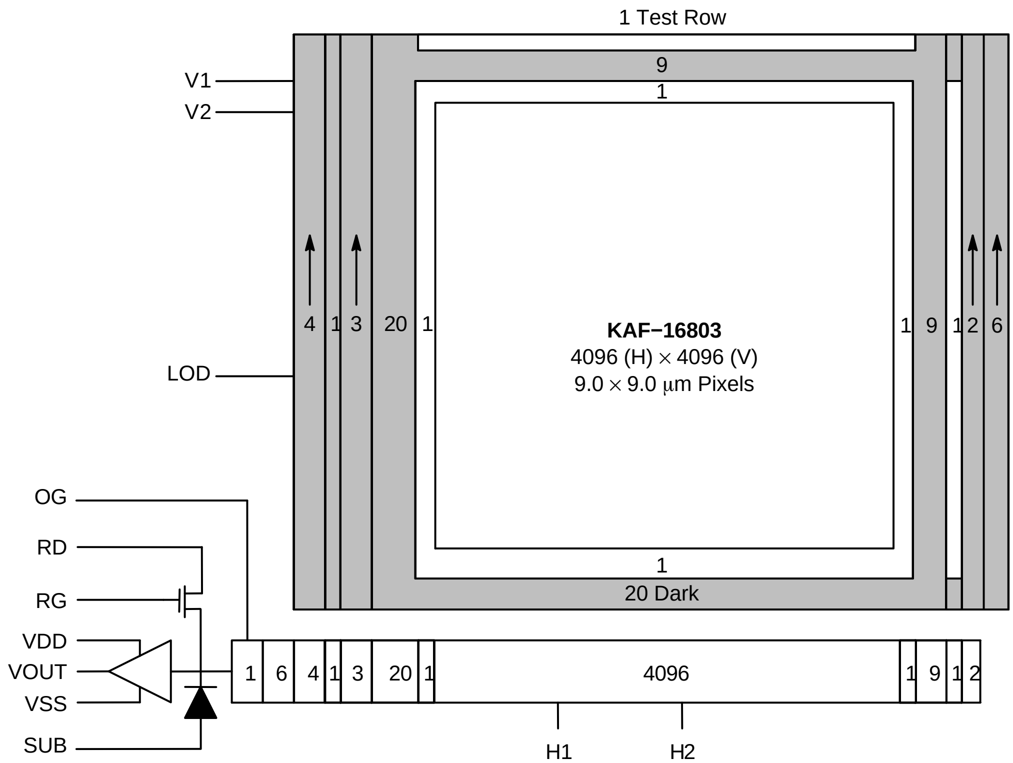


Figure 2. Block Diagram

Each line is composed of dummy pixels, internal test pixels, active buffer pixels, and valid photoactive pixels.

Dummy Pixels

Within each horizontal shift register the first pixels are 11 dummy pixels and should not be used to determine a dark reference level.

Internal Test

The next 4 pixels are introduced into the design to facilitate production testing. These behave differently than the buffer and dark pixels and should not be used to establish a dark reference. The last three pixels in each line are also internal test pixels and should not be used to establish a dark reference.

Dark Reference Pixels

Surrounding the periphery of the device is a border of light shielded pixels creating a dark region. Within this dark region, exist light shielded pixels that include 20 leading dark pixels on every line. There are also 20 full dark lines at the start and 9 full dark lines at the end of every frame. Under normal circumstances, these pixels do not respond to light and may be used as a dark reference.

Active Buffer Pixels

There is 1 photoactive buffer row and column adjacent to the valid photoactive pixels. These may have signals levels different from those in the imaging array and are not counted in the active pixel count.

Image Acquisition

An electronic representation of an image is formed when incident photons falling on the sensor plane create electron-hole pairs within the device. These photon-induced electrons are collected locally by the formation of potential wells at each pixel site. The number of electrons collected is linearly dependent on light level and exposure time and non-linearly dependent on wavelength. When the pixel's capacity is reached, excess electrons are discharged into the lateral overflow drain to prevent crosstalk or 'blooming'. During the integration period, the V1 and V2 register clocks are held at a constant (low) level.

Charge Transport

The integrated charge from each pixel is transported to the output using a two-step process. Each line (row) of charge is first transported from the vertical CCDs to a horizontal CCD register using the V1 and V2 register clocks. The horizontal CCD is presented a new line on the falling edge of V2 while H1 is held high. The horizontal CCDs then transport each line, pixel by pixel, to the output structure by alternately clocking the H1 and H2 pins in a complementary fashion.

Horizontal Register

Output Structure

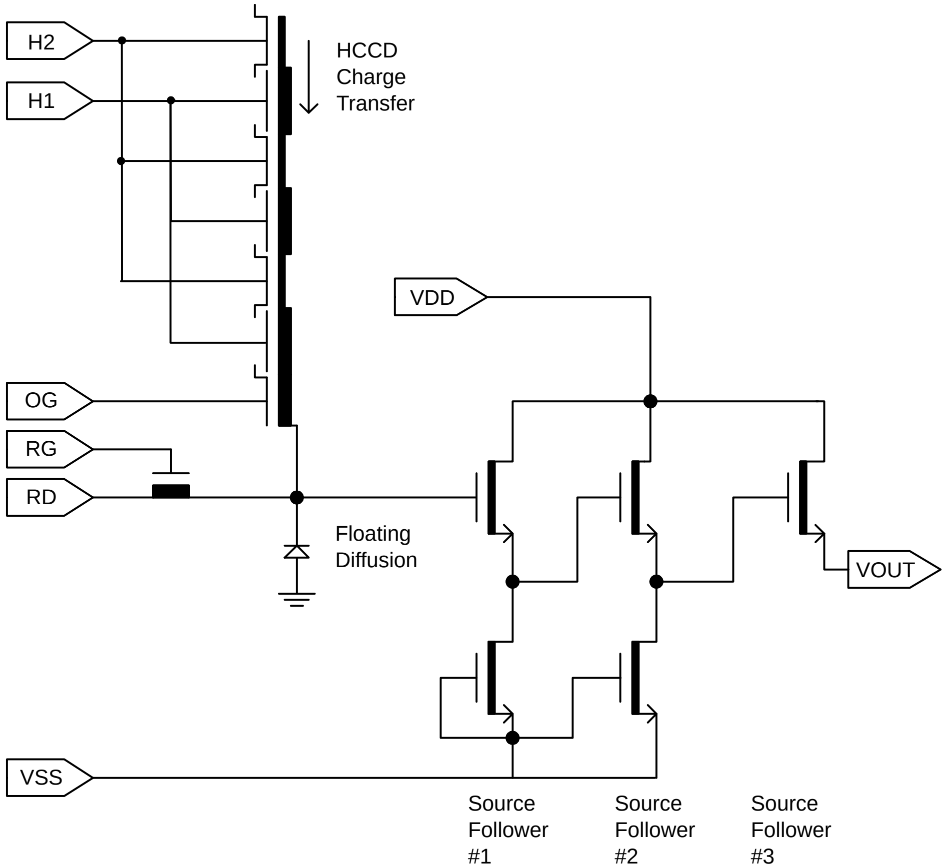
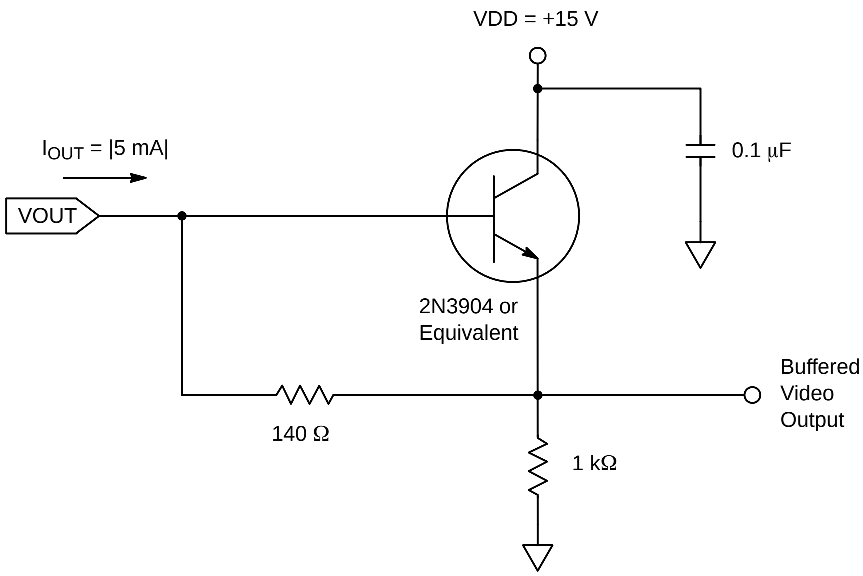


Figure 3. Output Architecture

The output consists of a floating diffusion capacitance connected to a three-stage source follower. Charge presented to the floating diffusion (FD) is converted into a voltage and is current amplified in order to drive off-chip loads. The resulting voltage change seen at the output is linearly related to the amount of charge placed on the FD. Once the signal has been sampled by the system electronics, the reset gate (RG) is clocked to remove the signal and FD is reset to the potential applied by reset drain (RD). Increased signal at the floating diffusion reduces the voltage seen at the output pin. To activate the output structure, an off-chip current source must be added to the VOUT pin of the device. See Figure 4.

Output Load

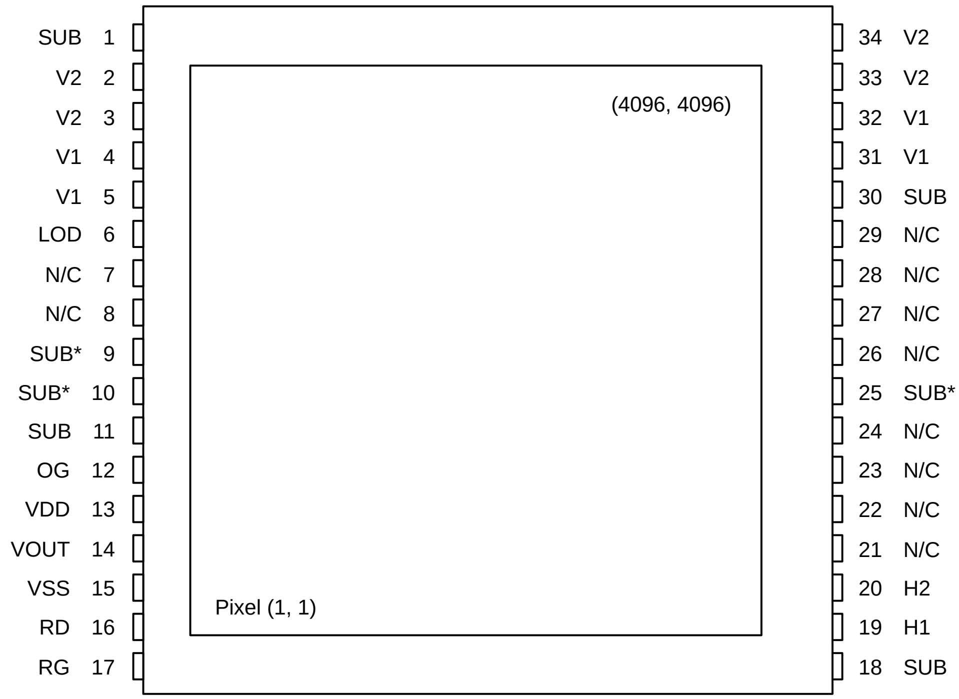


NOTE: Component values may be revised based on operating conditions and other design considerations.

Figure 4. Recommended Output Structure Load Diagram

Physical Description

Pin Description and Device Orientation



Notes:
1. Pins with the same name are to be tied together on the circuit board and have the same timing.
2. Unlike the KAF−16801, pins 9, 10, and, 25 are internally connected to SUB. They may be connected to SUB on the printed circuit board or otherwise must be left floating.

Figure 5. Device Orientation and Pinout

Table 3. PIN DESCRIPTION

Pin	Name	Description
1	SUB	Substrate
2	V2	Vertical CCD Clock − Phase 2
3	V2	Vertical CCD Clock − Phase 2
4	V1	Vertical CCD Clock − Phase 1
5	V1	Vertical CCD Clock − Phase 1
6	LOD	Anti Blooming Drain
7	N/C	No Connection
8	N/C	No Connection
9	SUB*	Substrate or No Connection
10	SUB*	Substrate or No Connection
11	SUB	Substrate
12	OG	Output Gate
13	VDD	Output Amplifier Supply
14	VOUT	Video Output
15	VSS	Amplifier Supply Returen
16	RD	Reset Drain
17	RG	Reset Gate

Pin	Name	Description
18	SUB	Substrate
19	H1	Horizontal CCD Clock − Phase 1
20	H2	Horizontal CCD Clock − Phase 2
21	N/C	No Connection
22	N/C	No Connection
23	N/C	No Connection
24	N/C	No Connection
25	SUB*	Substrate or No Connection
26	N/C	No Connection
27	N/C	No Connection
28	N/C	No Connection
29	N/C	No Connection
30	SUB	Substrate
31	V1	Vertical CCD Clock − Phase 1
32	V1	Vertical CCD Clock − Phase 1
33	V2	Vertical CCD Clock − Phase 2
34	V2	Vertical CCD Clock − Phase 2

*Unlike the KAF−16801, pins 9, 10, and, 25 are internally connected to SUB. They may be connected to SUB on the printed circuit board or must be left floating

IMAGING PERFORMANCE

Table 4. TYPICAL OPERATIONAL CONDITIONS

Description	Condition − Unless Otherwise Noted	Notes
Integration Time (t_{INT})	Variable	
Horizontal Clock Frequency	4 MHz	
Temperature	25°C	Room Temperature
Mode	Integrate − Readout Cycle	
Operation	Nominal Operating Voltages and Timing with Min. Vertical Pulse Width t_{VW} = 20 μs	

Table 5. SPECIFICATIONS

Description	Symbol	Min.	Nom.	Max.	Units	Notes	Verification Plan
Saturation Signal	V_{SAT} N_{e^-SAT}	1,900 85,000	2,200 100,000	− −	mV e^-	1	Die[11]
Quantum Efficiency (550 nm)	$QE_{(MAX)}$	−	60	−	%	1	Design[12]
Responsivity (550)	$R_{(MAX)}$	−	28.7	−	V/μJ/cm^2		Design[12]
Photoresponse Non-Linearity	PRNL	−	1	−	%	2	Design[12]
Photoresponse Non-Uniformity	PRNU	−	1	−	%	3	Design[12]
Integration Dark Signal	$V_{DARK,INT}$	− −	3 0.6	15 3	e^-/pix/sec pA/cm^2	4	Die[11]
Readout Dark Signal	$V_{DARK,READ}$	−	45	225	electrons	10	Die[11]
Dark Signal Non-Uniformity	DSNU	−	3	15	e^-/pix/sec	5	Die[11]
Dark Signal Doubling Temperature	ΔT	−	6.3	−	°C		Design[12]
Read Noise	N_R	−	9	15	e^- rms	6	Design[12]
Linear Dynamic Range	DR	−	80	−	dB	7	Design[12]
Blooming Protection	X_{AB}	100	−	−	V_{SAT}	8	Design[12]
Output Amplifier Sensitivity	V_{OUT}/N_{e^-}	20	22	−	μV/e^-		Design[12]
DC Offset, Output Amplifier	V_{ODC}	−	V_{RD} − 3.0	V_{RD} − 2.0	V	9	Die[11]
Output Amplifier Bandwidth	f_{-3dB}	−	100	−	MHz		Design[12]
Output Impedance, Amplifier	R_{OUT}	−	160	200	Ω		Die[11]

1. Increasing output load currents to improve bandwidth will decrease these values.
2. Worst case deviation from straight line fit, between 1% and 90% of V_{SATmin}.
3. One sigma deviation of a 128 × 128 sample when CCD illuminated uniformly.
4. Average of all pixels with no illumination at 25°C.
5. Average dark signal of any of 32 × 32 blocks within the sensor (Each block is 128 × 128 pixels).
6. Output amplifier noise at 25°C, operating at pixel frequency up to 4 MHz, bandwidth < 10 MHz, t_{INT} = 0, and no dark current shot noise.
7. 20log (V_{SAT} / V_N) − see Note 6 and Note 1.
   $V_N = N_R \cdot Q / V$.
8. X_{AB} is the number of times above the V_{SAT} illumination level that the sensor will bloom by spot size doubling. The spot size is 10% of the imager height. X_{AB} is measured at 4 ms.
9. Video level offset with respect to ground.
10. Readout dark current per pixel measured at 25°C and vertical CCD clock width = 20 ms.
11. A parameter that is measured on every sensor during production testing.
12. A parameter that is quantified during the design verification activity.

TYPICAL PERFORMANCE CURVES

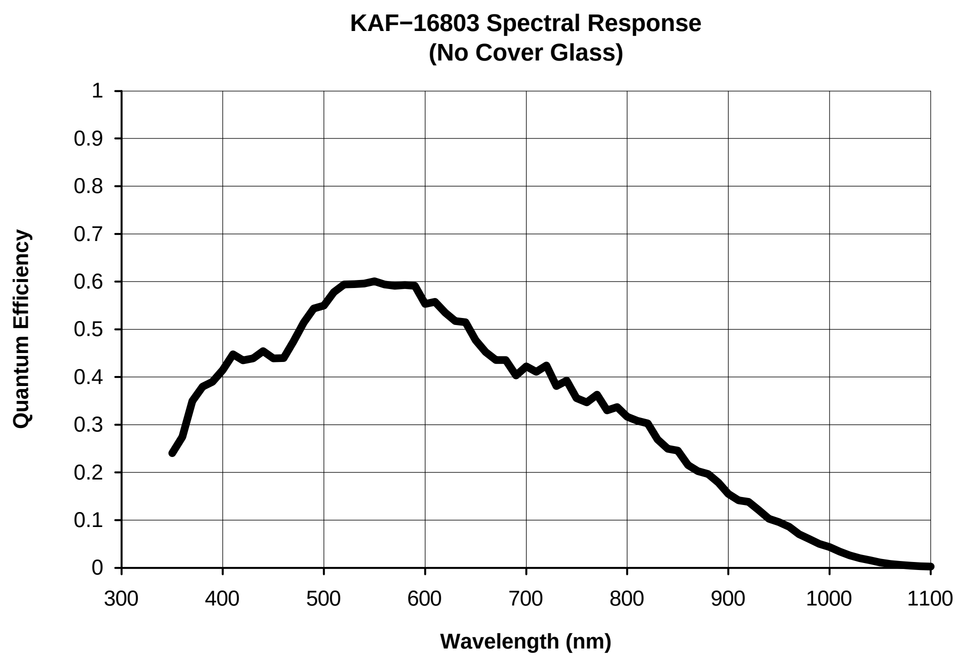


Figure 6. Typical Spectral Response

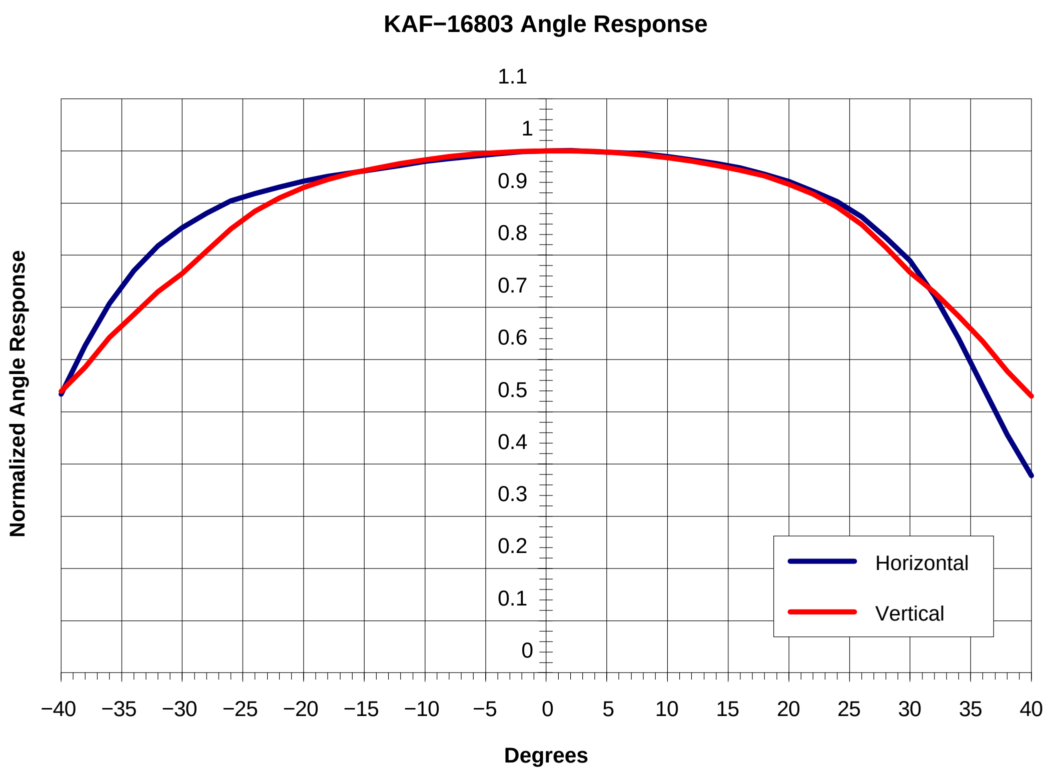


Figure 7. Typical Angle Response

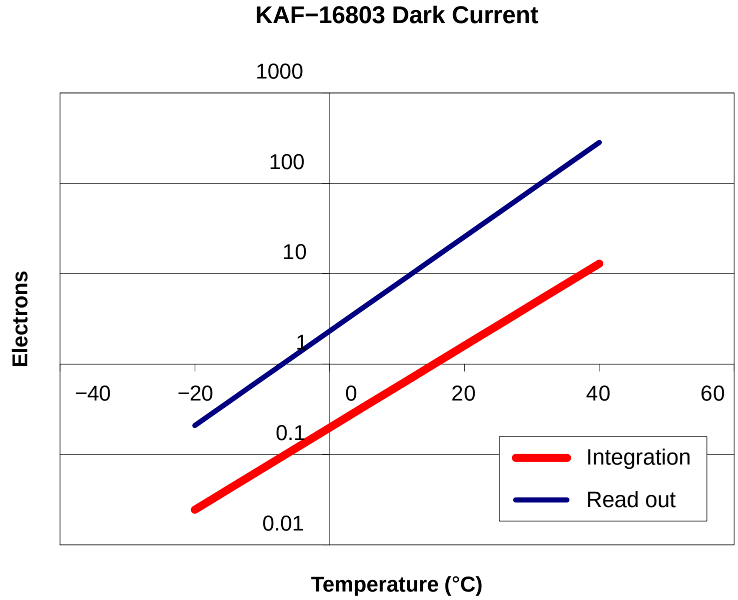


Figure 8. Dark Current

Noise Floor

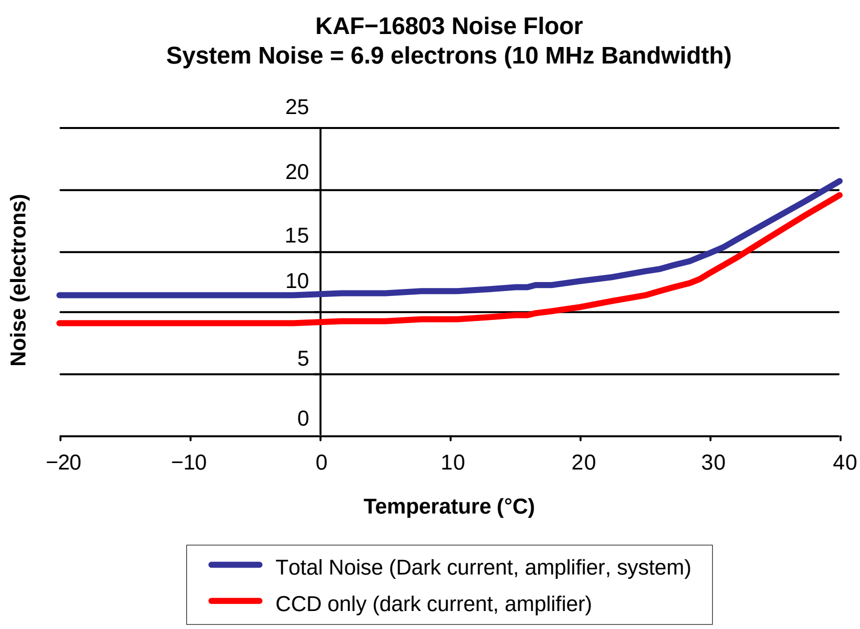


Figure 9. Noise Floor

DEFECT DEFINITIONS

Table 6. SPECIFICATIONS (All defect tests performed at T = 25°C)

Classification	Point	Cluster	Column
Standard Grade	< 200	< 20	< 10

Point Defects

Dark: A pixel which deviates by more than 6% from neighboring pixels when illuminated to 70% of saturation.

Bright: A pixel with a dark current > 3,000 e^-/pixel/sec at 25°C.

Cluster Defect

A grouping of not more than 10 adjacent point defects.

Cluster defects are separated by no less than 4 good pixels in any direction.

Column Defect

A grouping of more than 10 point defects along a single column.

A column containing a pixel with dark current > 15,000 e^-/pixel/sec (Bright column).

A column that does not meet the CTE specification for all exposures less than the specified maximum saturation signal level and greater than 2 ke^-.

A column that contains a pixel which loses more than 250 e^- under 2 ke^- illumination (Trap defect).

Column defects are separated by no less than 4 good columns. No multiple column defects (double or more) will be permitted.

Column and cluster defects are separated by at least 4 good columns in the x direction.

OPERATION

Table 7. ABSOLUTE MAXIMUM RATINGS

Description	Symbol	Minimum	Maximum	Units	Notes
Diode Pin Voltages	V_{DIODE}	−0.5	20	V	1, 2
Gate Pin Voltages	V_{GATE1}	−16	16	V	1, 3
Adjacent Gate Voltages	V_{1-2}	−16	16	V	4
Output Bias Current	I_{OUT}	−	−30	mA	5
LOD Diode Voltage	V_{LOD}	−0.5	13.0	V	1
Operating Temperature	T_{OP}	−60	60	°C	7

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

1. Referenced to pin SUB.
2. Includes pins: RD, VDD, VSS, VOUT.
3. Includes pins: V1, V2, H1, H2, RG, VOG.
4. Voltage difference between adjacent gates. Includes: V1 to V2; H1 to H2; H1 to VOG; and V2 to H1.
5. Avoid shorting output pins to ground or any low impedance source during operation. Amplifier bandwidth increases at higher currents and lower load capacitance at the expense of reduced gain (sensitivity).
6. Absolute maximum rating is defined as a level or condition that should not be exceeded at any time per the description. If the level or condition is exceeded, the device will be degraded and may be damaged.
7. Noise performance will degrade at higher temperatures.

Power-Up Sequence

The sequence chosen to perform an initial power-up is not critical for device reliability. A coordinated sequence may minimize noise and the following sequence is recommended:

1. Connect the ground pins (SUB).
2. Supply the appropriate biases and clocks to the remaining pins.

Table 8. DC BIAS OPERATING CONDITIONS

Description	Symbol	Minimum	Nominal	Maximum	Units	Maximum DC Current (mA)	Notes
Reset Drain	V_{RD}	12.75	13	13.625	V	I_{RD} = 0.01	
Output Amplifier Supply	V_{SS}	1.75	2.0	2.25	V	I_{SS} = 3.0	
Output Amplifier Return	V_{DD}	14.75	15.0	17.0	V	I_{OUT} + I_{SS}	
Substrate	V_{SUB}	0	0	0	V	0.01	
Output Gate	V_{OG}	1.0	2.0	2.5	V	0.01	
Lateral Overflow Drain	V_{LOD}	7.75	8.0	8.25	V	0.01	
Video Output Current	I_{OUT}	−3	−5	−7	mA		1

1. An output load sink must be applied to VOUT to activate output amplifier – see Figure 4.

AC Operating Conditions

Table 9. CLOCK LEVELS

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Notes
V1 Low Level	V1L	Low	−9.2	−9.0	−8.8	V	1
V1 High Level	V1H	High	2.3	2.5	2.7	V	1
V2 Low Level	V2L	Low	−9.2	−9.0	−8.8	V	1
V2 High Level	V2H	High	2.3	2.5	2.7	V	1
H1 Low Level	H1L	Low	−3.2	−3.0	−2.8	V	1
H1 High Level	H1H	High	6.8	7.0	7.2	V	1

1. All pins draw less than 10 μA DC current. Capacitance values relative to SUB (substrate).

Table 9. CLOCK LEVELS (continued)

Description	Symbol	Level	Minimum	Nominal	Maximum	Units	Notes
H2 Low Level	H2L	Low	−3.2	−3.0	−2.8	V	1
H2 High Level	H2H	High	6.8	7.0	7.2	V	1
RG Low Level	RGL	Low	5.8	6.0	6.2	V	1
RG High Level	RGH	High	10.8	11.0	11.2	V	1

1. All pins draw less than 10 μA DC current. Capacitance values relative to SUB (substrate).

Capacitance Equivalent Circuit

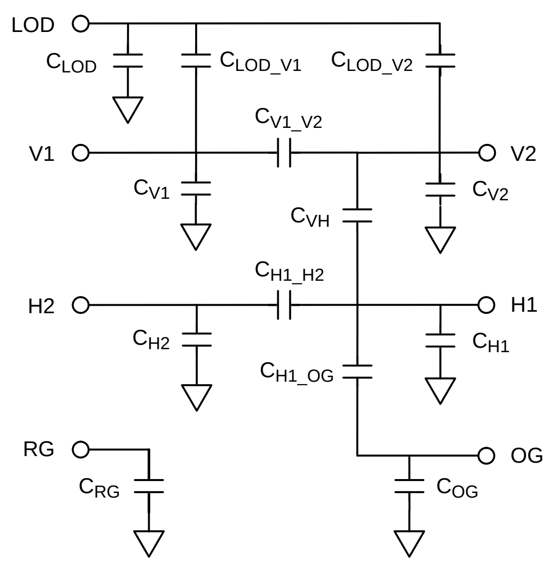


Figure 10. Equivalent Circuit Model

Table 10.

Description	Label	Value	Unit
LOD−Sub Capacitance	C_{LOD}	6.5	nF
LOD−V1 Capacitance	C_{LOD_V1}	36	nF
LOD−V2 Capacitance	C_{LOD_V2}	36	nF
V1−V2 Capacitance	C_{V1_V2}	80	nF
V1−Sub Capacitance	C_{V1_SUB}	250	nF
V2−Sub Capacitance	C_{V2_SUB}	250	nF
V2−H1 Capacitance	C_{VH}	36	pF
H1−H2 Capacitance	C_{H1_H2}	75	pF
H1−Sub Capacitance	C_{H1_Sub}	500	pF
H2−Sub Capacitance	C_{H2_Sub}	300	pF
OG−Sub Capacitance	C_{OG_Sub}	5	pF
RG−Sub Capacitance	C_{RG_Sub}	13	pF

TIMING

Table 11. REQUIREMENTS AND CHARACTERISTICS

Description	Symbol	Minimum	Nominal	Maximum	Units	Notes
H1, H2 Clock Frequency	f_H	−	4	10	MHz	1
H1, H2 Rise, Fall Times	t_{H1r}, t_{H1f}	5	−	−	%	3
V1, V2 Rise, Fall Times	t_{V1r}, t_{V1f}	5	−	−	%	3
V1 − V2 Cross-Over	V_{VCR}	−1	0	1	V	
H1 − H2 Cross-Over	V_{HCR}	1	2	5	V	
H1, H2 Setup Time	t_{HS}	5	10	−	μs	
RG Clock Pulse Width	t_{RGw}	5	10	−	ns	4
V1, V2 Clock Pulse Width	t_{Vw}	20	20	−	μs	
Pixel Period (1 Count)	t_e	100	250	−	ns	2
Integration Time	t_{INT}	−	−	−		5
Line Time	t_{LINE}	0.460	1.08	−	ms	6
Readout Time	$t_{READOUT}$	1,897	4,450	−	ms	7

1. 50% duty cycle values.
2. CTE will degrade above the maximum frequency.
3. Relative to the pulse width (based on 50% of high/low levels).
4. RG should be clocked continuously.
5. Integration time is user specified.
6. $(4145 \cdot t_e) + t_{HS} + (2 \cdot t_{Vw}) = 1.08$ ms
7. $t_{READOUT} = t_{LINE} \cdot 4128$ lines

Edge Alignment

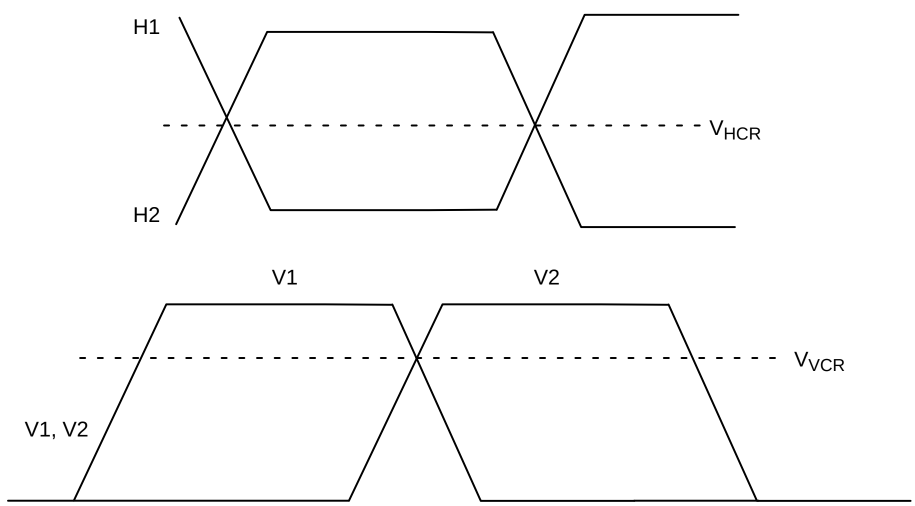


Figure 11. Edge Alignment

Frame Timing

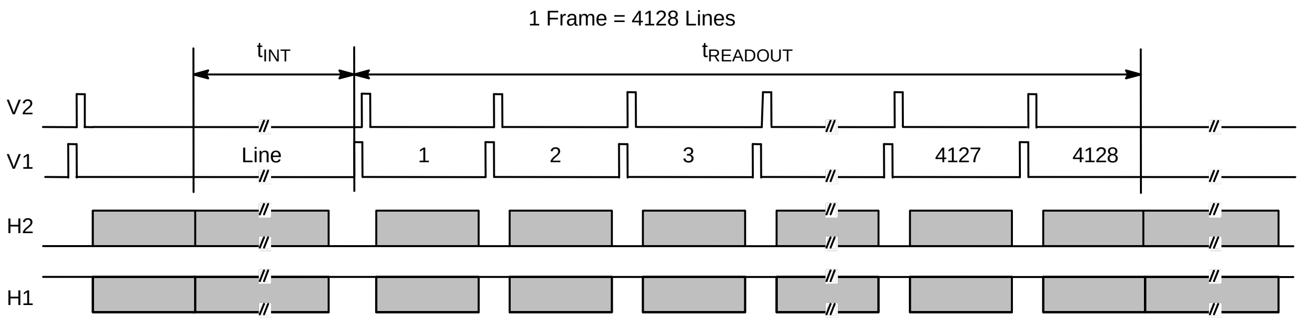


Figure 12. Frame Timing

Frame Timing Detail

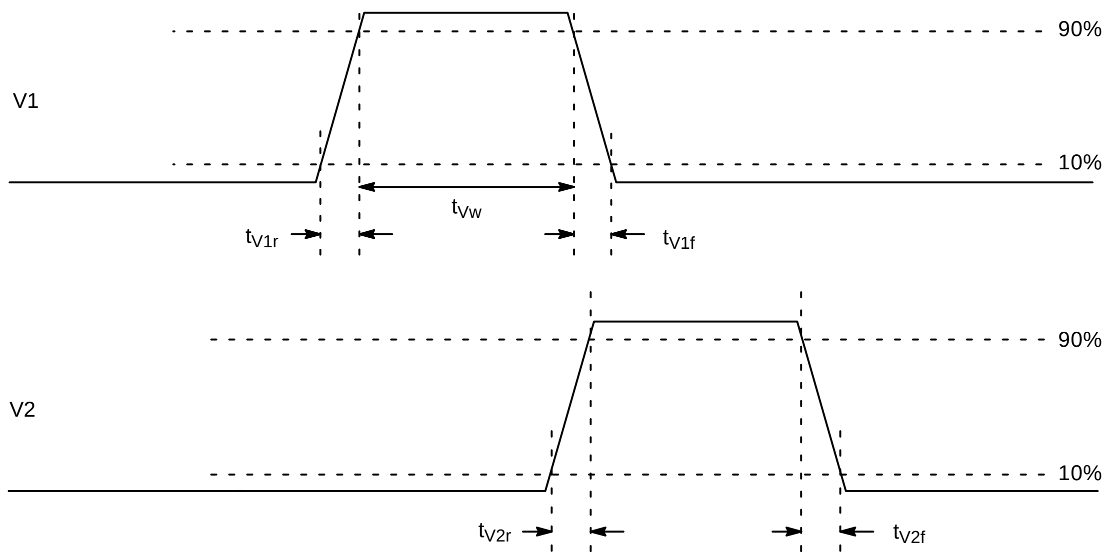


Figure 13. Frame Timing Detail

Line Timing (Each Output)

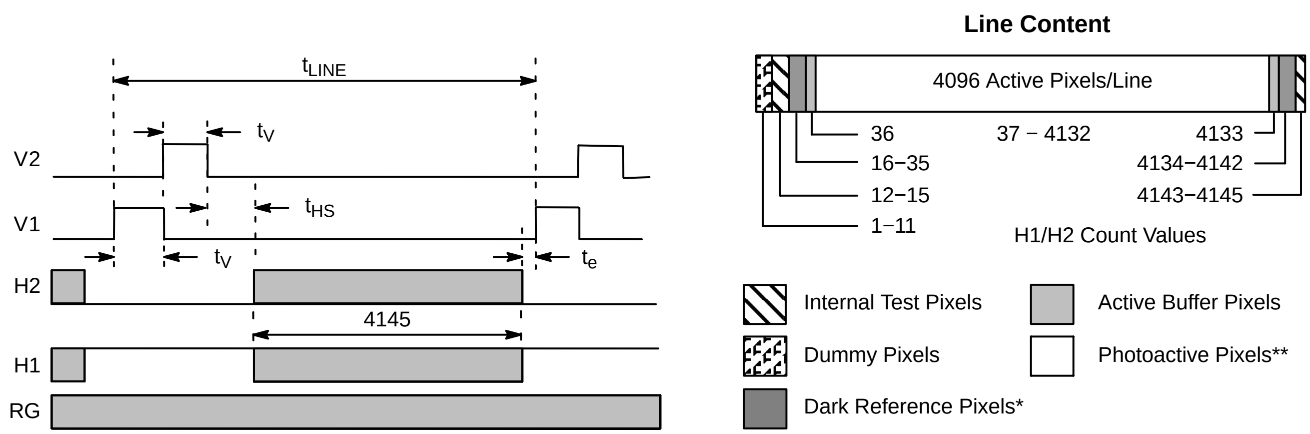


Figure 14. Line Timing

Pixel Timing

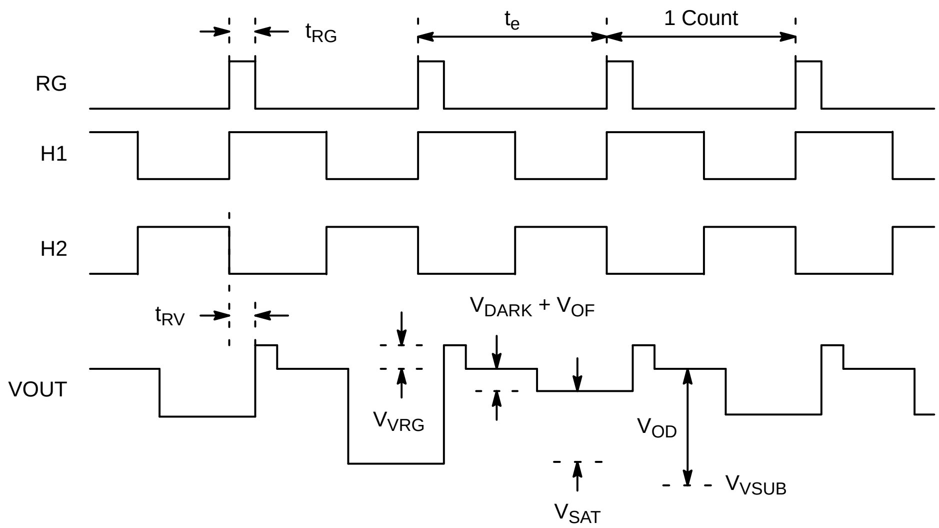


Figure 15. Pixel Timing

Pixel Timing Detail

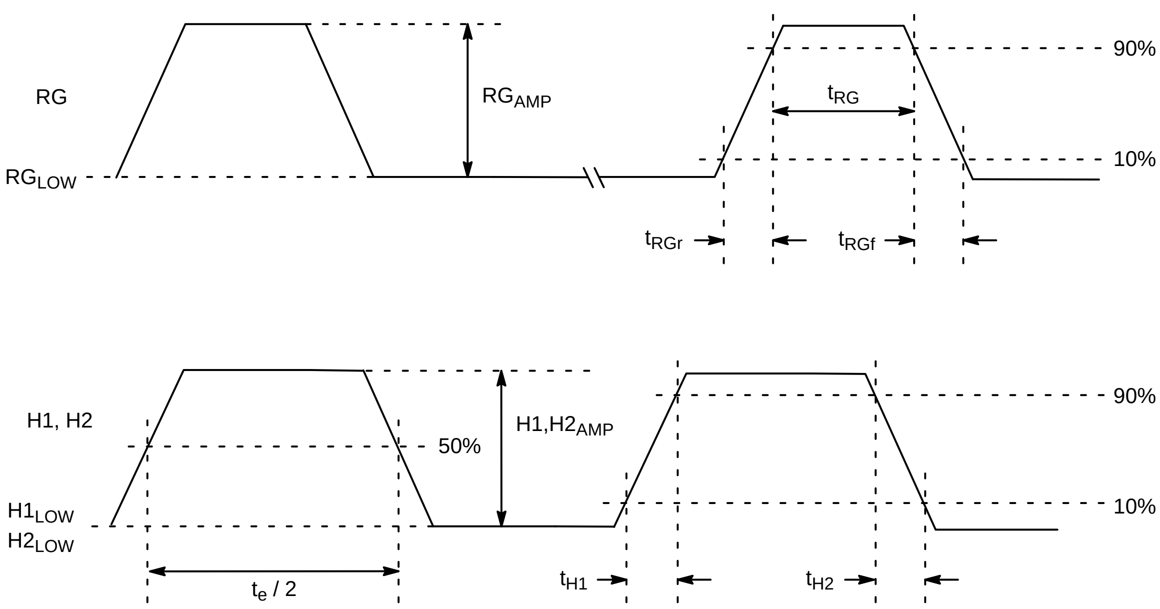


Figure 16. Pixel Timing Detail

Example Waveforms

Video Waveform Horizontal CCD Clocks

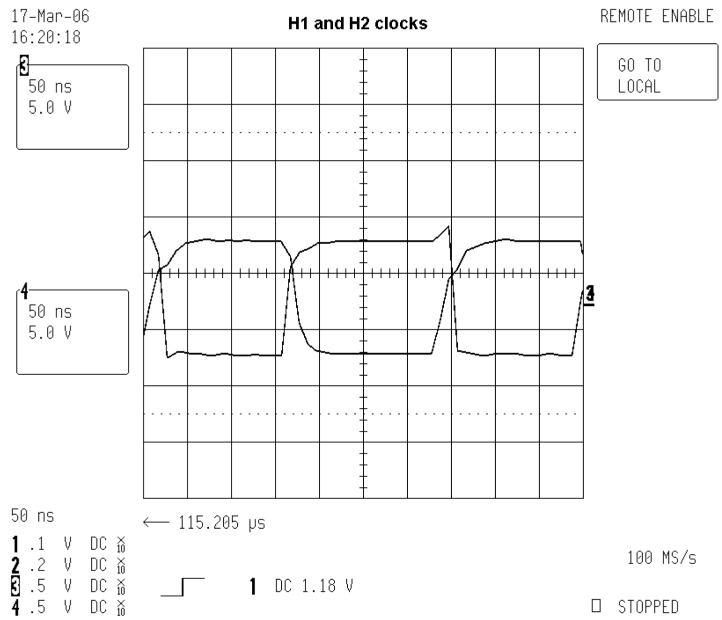


Figure 17. Horizontal Clock Waveform

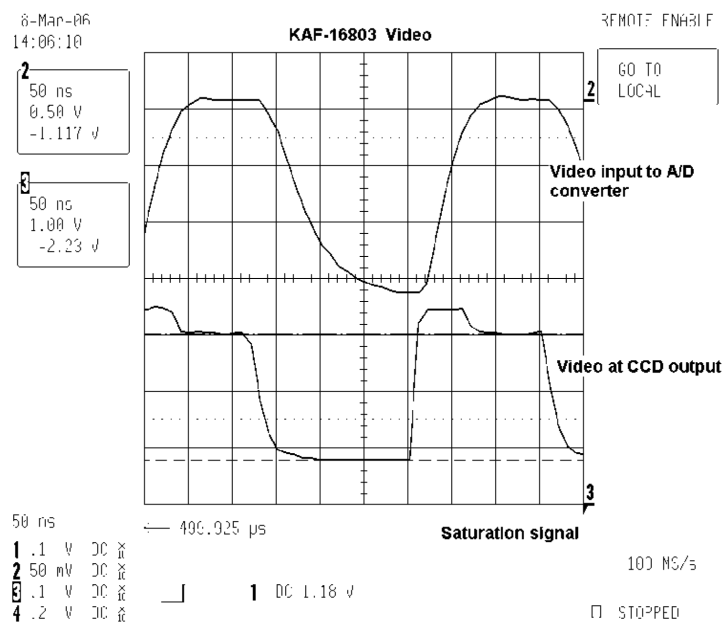


Figure 18. Video Waveform

NOTE: Video Waveform – The bottom curve was taken at the CCD output. The top curve is bandwidth limited and was measured at the analog to digital converter.

Video Waveform and Clamp Clock

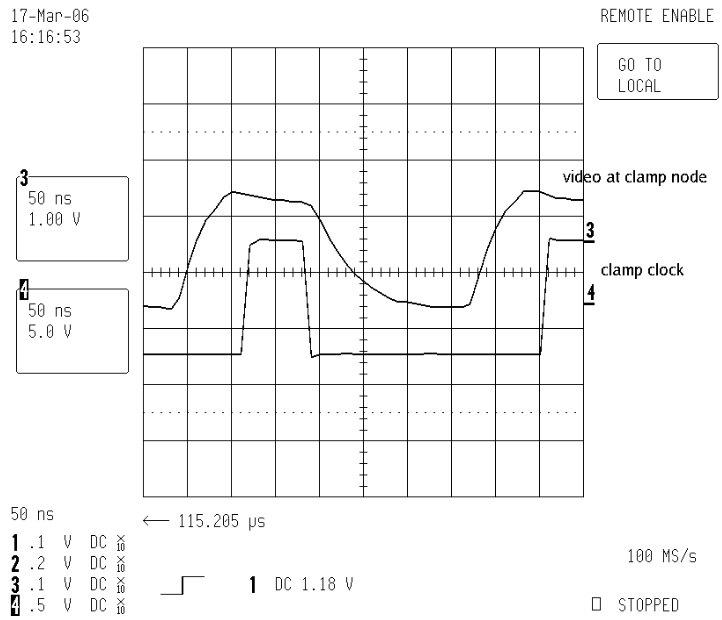


Figure 19. Video and Clamp

Video Waveform and Sample Clock

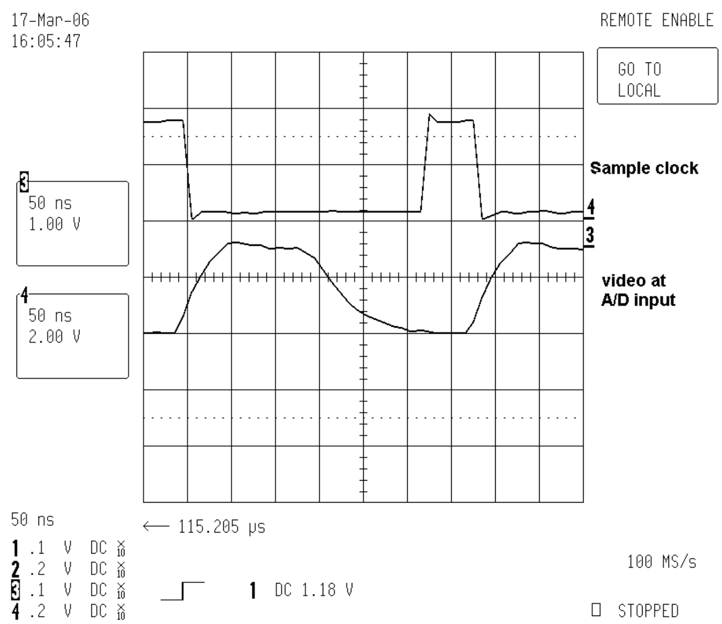


Figure 20. Video and Sample Clock

STORAGE AND HANDLING

Table 12. STORAGE CONDITIONS

Description	Symbol	Minimum	Maximum	Units	Notes
Storage Temperature	T_{ST}	−20	70	°C	1

1. Long-term storage toward the maximum temperature will accelerate color filter degradation (This condition applies to color parts only).
2. T = 25°C. Excessive humidity will degrade MTTF.

For information on ESD and cover glass care and cleanliness, please download the *Image Sensor Handling and Best Practices* Application Note (AN52561/D) from www.onsemi.com.

For information on soldering recommendations, please download the Soldering and Mounting Techniques Reference Manual (SOLDERRM/D) from www.onsemi.com.

For quality and reliability information, please download the *Quality & Reliability* Handbook (HBD851/D) from www.onsemi.com.

For information on device numbering and ordering codes, please download the *Device Nomenclature* technical note (TND310/D) from www.onsemi.com.

For information on Standard terms and Conditions of Sale, please download Terms and Conditions from www.onsemi.com.

MECHANICAL INFORMATION

Completed Assembly

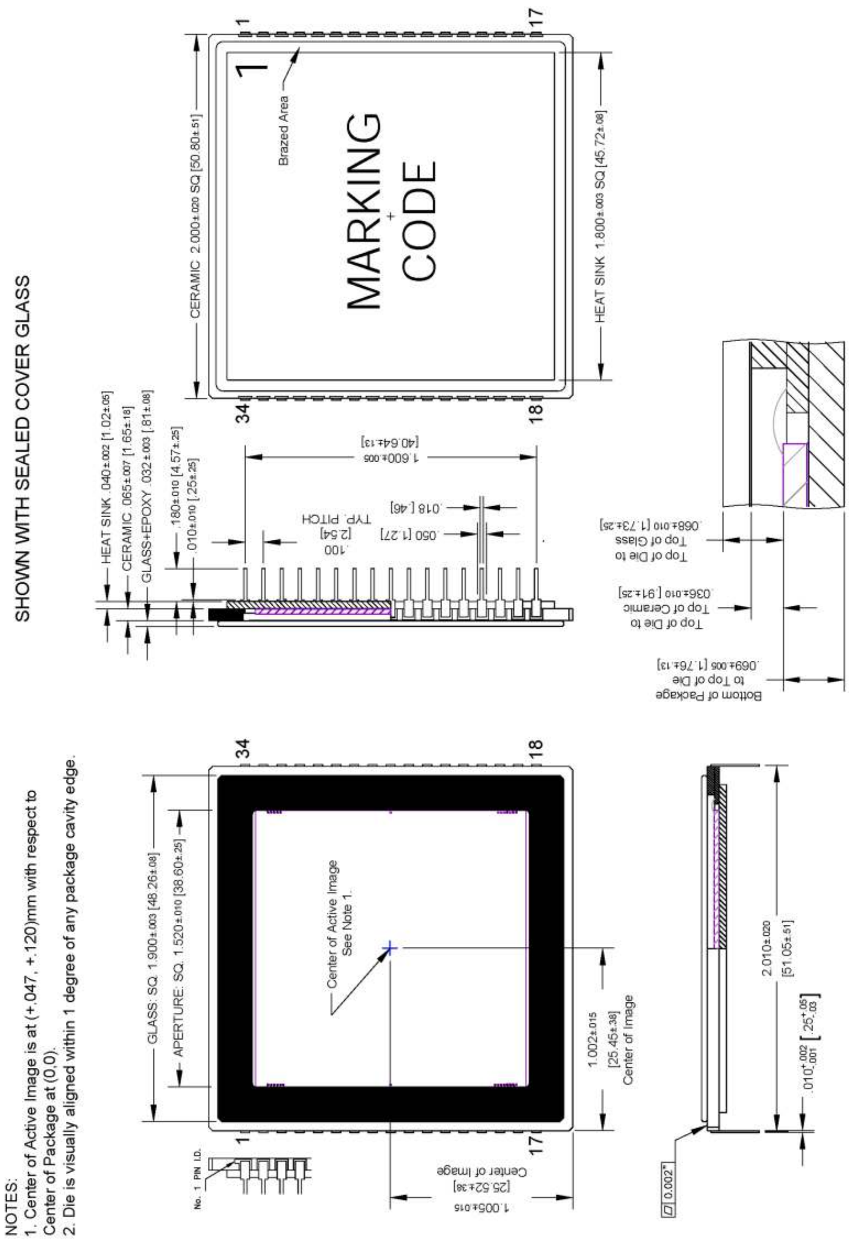


Figure 21. Completed Assembly (1 of 1)

Cover Glass Specification

1. Scratch and dig: 10 micron max
2. Substrate material Schott D263T eco or equivalent
3. Multilayer anti-reflective coating

Table 13.

Wavelength	Total Reflectance
420−450	≤ 2%
450−630	≤ 1%
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