

## SNx4LV86A Quadruple 2-Input Exclusive-OR Gates

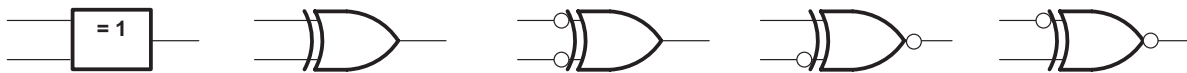
### 1 Features

- 2-V to 5.5-V  $V_{CC}$  Operation
- Max  $t_{pd}$  of 8 ns at 5 V
- Typical  $V_{OLP}$  (Output Ground Bounce)  $<0.8$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Typical  $V_{OHV}$  (Output  $V_{OH}$  Undershoot)  $>2.3$  V at  $V_{CC} = 3.3$  V,  $T_A = 25^\circ\text{C}$
- Support Mixed-Mode Voltage Operation on All Ports
- Latch-Up Performance Exceeds 250 mA per JESD 17
- ESD Protection Exceeds JESD 22
  - 2000-V Human-Body Model (A114-A)
  - 200-V Machine Model (A115-A)
  - 1000-V Charged-Device Model (C101)

### 2 Applications

- EPOS
- Programmable Logic Controller (PLC)
- DCS and PAC: Analog Input Module
- Medical Meters: Portable
- Server Motherboard
- Printer

### 4 Simplified Schematic



- A. These are five equivalent exclusive-OR symbols valid for an 'LV86A gate in positive logic; negation can be shown at any two ports. See [Functional Block Diagram](#) for more information.

### 3 Description

The 'LV86A devices are quadruple 2-input exclusive-OR gates designed for 2-V to 5.5-V  $V_{CC}$  operation.

These devices contain four independent 2-input exclusive-OR gates. They perform the Boolean function  $Y = A \oplus B$  or  $Y = \overline{A}B + A\overline{B}$  in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

#### Device Information<sup>(1)</sup>

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LV86A	VQFN (14)	3.50 mm × 3.50 mm
	SOIC (14)	8.65 mm × 3.91 mm
	SOP (14)	10.30 mm × 5.30 mm
	SSOP (14)	6.20 mm × 5.30 mm
	TSSOP (14)	5.00 mm × 4.40 mm

- (1) For all available packages, see the orderable addendum at the end of the data sheet.



## Table of Contents

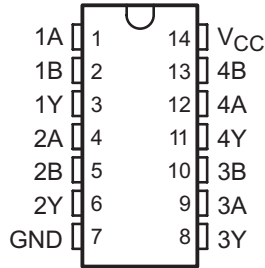
<b>1 Features</b> .....	<b>1</b>	<b>9 Detailed Description</b> .....	<b>9</b>
<b>2 Applications</b> .....	<b>1</b>	9.1 Overview .....	9
<b>3 Description</b> .....	<b>1</b>	9.2 Functional Block Diagram .....	9
<b>4 Simplified Schematic</b> .....	<b>1</b>	9.3 Feature Description .....	9
<b>5 Revision History</b> .....	<b>2</b>	9.4 Device Functional Modes .....	9
<b>6 Pin Configuration and Functions</b> .....	<b>3</b>	<b>10 Application and Implementation</b> .....	<b>10</b>
<b>7 Specifications</b> .....	<b>4</b>	10.1 Application Information .....	10
7.1 Absolute Maximum Ratings .....	4	10.2 Typical Application .....	10
7.2 ESD Ratings .....	4	<b>11 Power Supply Recommendations</b> .....	<b>11</b>
7.3 Recommended Operating Conditions .....	5	<b>12 Layout</b> .....	<b>11</b>
7.4 Thermal Information .....	5	12.1 Layout Guidelines .....	11
7.5 Electrical Characteristics .....	6	12.2 Layout Example .....	11
7.6 Switching Characteristics, $V_{CC} = 2.5\text{ V} \pm 0.2\text{ V}$ .....	6	<b>13 Device and Documentation Support</b> .....	<b>12</b>
7.7 Switching Characteristics, $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ .....	6	13.1 Related Links .....	12
7.8 Switching Characteristics, $V_{CC} = 5\text{ V} \pm 0.5\text{ V}$ .....	6	13.2 Trademarks .....	12
7.9 Noise Characteristics for SN74LV86A .....	7	13.3 Electrostatic Discharge Caution .....	12
7.10 Operating Characteristics .....	7	13.4 Glossary .....	12
7.11 Typical Characteristics .....	7	<b>14 Mechanical, Packaging, and Orderable Information</b> .....	<b>12</b>
<b>8 Parameter Measurement Information</b> .....	<b>8</b>		

## 5 Revision History

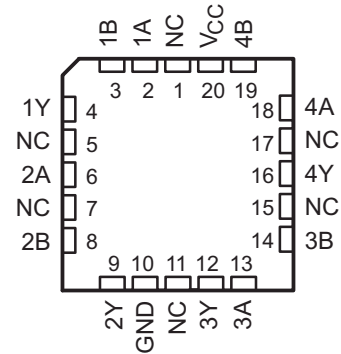
Changes from Revision F (April 2005) to Revision G	Page
• Added <i>ESD Ratings</i> table, <i>Feature Description</i> section, <i>Device Functional Modes</i> , <i>Application and Implementation</i> section, <i>Power Supply Recommendations</i> section, <i>Layout</i> section, <i>Device and Documentation Support</i> section, and <i>Mechanical, Packaging, and Orderable Information</i> section .....	1
• Updated operating free-air temperature maximum from 85°C to 125°C for SN74LV86A .....	5

## 6 Pin Configuration and Functions

SN54LV86A: J or W Package  
SN74LV86A: D, DB, DGV, NS, or PW Package  
(Top View)



SN54LV86A: FK Package  
(Top View)



B. NC – No internal connection

### Pin Functions

PIN	I/O	DESCRIPTION
1	1A	A input 1
2	1B	B input 1
3	1Y	Output 1
4	2A	A input 2
5	2B	B input 2
6	2Y	Output 2
7	GND	ground
8	3Y	Output 3
9	3A	A input 3
10	3B	B input 3
11	4Y	Output 4
12	4A	A input 4
13	4B	B input 4
14	V <sub>CC</sub>	Power pin

## 7 Specifications

### 7.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) <sup>(1)</sup>

		MIN	MAX	UNIT
$V_{CC}$	Supply voltage	-0.5	7	V
$V_I$	Input voltage <sup>(2)</sup>	-0.5	7	V
$V_O$	Voltage applied to any output in the high-impedance or power-off state <sup>(2)</sup>	-0.5	7	V
$V_O$	Output voltage <sup>(2)(3)</sup>	-0.5	$V_{CC} + 0.5$ V	V
$I_{IK}$	Input clamp current, $V_I < 0$		-20	mA
$I_{OK}$	Output clamp current, $V_O < 0$		-50	mA
$I_O$	Continuous output current, $V_O = 0$ to $V_{CC}$	-25	25	mA
	Continuous current through $V_{CC}$ or GND	-50	50	mA
$T_{stg}$	Storage temperature	-65	150	°C

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
- (3) This value is limited to 5.5-V maximum.

### 7.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 <sup>(1)</sup>	2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 <sup>(2)</sup>	1000	

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

### 7.3 Recommended Operating Conditions

 see <sup>(1)</sup>

		MIN	MAX	UNIT
V <sub>CC</sub>	Supply voltage	2	5.5	V
V <sub>IH</sub>	High-level input voltage	V <sub>CC</sub> = 2 V	1.5	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.7	
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.7	
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.7	
V <sub>IL</sub>	Low-level input voltage	V <sub>CC</sub> = 2 V	0.5	V
		V <sub>CC</sub> = 2.3 V to 2.7 V	V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 3 V to 3.6 V	V <sub>CC</sub> × 0.3	
		V <sub>CC</sub> = 4.5 V to 5.5 V	V <sub>CC</sub> × 0.3	
V <sub>I</sub>	Input voltage	0	5.5	V
V <sub>O</sub>	Output voltage	0	V <sub>CC</sub>	V
I <sub>OH</sub>	High-level output current	V <sub>CC</sub> = 2 V	–50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V	–2	
		V <sub>CC</sub> = 3 V to 3.6 V	–6	
		V <sub>CC</sub> = 4.5 V to 5.5 V	–12	
I <sub>OL</sub>	Low-level output current	V <sub>CC</sub> = 2 V	50	μA
		V <sub>CC</sub> = 2.3 V to 2.7 V	2	
		V <sub>CC</sub> = 3 V to 3.6 V	6	
		V <sub>CC</sub> = 4.5 V to 5.5 V	12	
Δt/Δv	Input transition rise or fall rate	V <sub>CC</sub> = 2.3 V to 2.7 V	200	ns/V
		V <sub>CC</sub> = 3 V to 3.6 V	100	
		V <sub>CC</sub> = 4.5 V to 5.5 V	20	
T <sub>A</sub>	Operating free-air temperature	–55	125	°C

(1) All unused inputs of the device must be held at V<sub>CC</sub> or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, [SCBA004](#).

### 7.4 Thermal Information

THERMAL METRIC <sup>(1)</sup>	D	DB	DGV	NS	PW	UNIT
	14 PINS					
R <sub>θJA</sub>	90.6	107.1	129.0	90.7	122.6	°C/W
R <sub>θJC(top)</sub>	50.9	59.6	52.1	48.3	51.4	
R <sub>θJB</sub>	44.8	54.4	62.0	49.4	64.4	
ψ <sub>JT</sub>	14.7	20.5	6.5	14.6	6.7	
ψ <sub>JB</sub>	44.5	53.8	61.3	49.1	63.8	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report, [SPRA953](#).

(2) The package thermal impedance is calculated in accordance with JESD 51-7.

## 7.5 Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

PARAMETER	TEST CONDITIONS	V <sub>CC</sub>	SN54LV86A			SN74LV86A –40°C to 125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
V <sub>OH</sub>	I <sub>OH</sub> = –50 μA	2 to 5.5 V	V <sub>CC</sub> – 0.1			V <sub>CC</sub> – 0.1			V
	I <sub>OH</sub> = –2 mA	2.3 V	2			2			
	I <sub>OH</sub> = –6 mA	3 V	2.48			2.48			
	I <sub>OH</sub> = –12 mA	4.5 V	3.8			3.8			
V <sub>OL</sub>	I <sub>OL</sub> = 50 μA	2 to 5.5 V	0.1			0.1			V
	I <sub>OL</sub> = 2 mA	2.3 V	0.4			0.4			
	I <sub>OL</sub> = 6 mA	3 V	0.44			0.44			
	I <sub>OL</sub> = 12 mA	4.5 V	0.55			0.55			
I <sub>I</sub>	V <sub>I</sub> = 5.5 V or GND	0 to 5.5 V	±1			±1			μA
I <sub>CC</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND, I <sub>O</sub> = 0	5.5 V	20			20			μA
I <sub>off</sub>	V <sub>I</sub> or V <sub>O</sub> = 0 to 5.5 V	0	5			5			μA
C <sub>i</sub>	V <sub>I</sub> = V <sub>CC</sub> or GND	3.3 V	1.4			1.4			pF

## 7.6 Switching Characteristics, V<sub>CC</sub> = 2.5 V ±0.2 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>pd</sub>	A or B	Y	C <sub>L</sub> = 15 pF	7.9 <sup>(1)</sup> 17.6 <sup>(1)</sup>			1 <sup>(2)</sup>	21 <sup>(2)</sup>	ns
			C <sub>L</sub> = 50 pF	10.5 22.6					

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) This note applies to SN54LV86A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 7.7 Switching Characteristics, V<sub>CC</sub> = 3.3 V ±0.3 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>pd</sub>	A or B	Y	C <sub>L</sub> = 15 pF	5.5 <sup>(1)</sup> 11 <sup>(1)</sup>			1 <sup>(2)</sup>	13 <sup>(2)</sup>	ns
			C <sub>L</sub> = 50 pF	7.4 14.5					

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) This note applies to SN54LV86A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.

## 7.8 Switching Characteristics, V<sub>CC</sub> = 5 V ±0.5 V

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 3)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	LOAD CAPACITANCE	T <sub>A</sub> = 25°C			MIN	MAX	UNIT
				MIN	TYP	MAX			
t <sub>pd</sub>	A or B	Y	C <sub>L</sub> = 15 pF	3.7 <sup>(1)</sup> 6.8 <sup>(1)</sup>			1 <sup>(2)</sup>	8 <sup>(2)</sup>	ns
			C <sub>L</sub> = 50 pF	5.3 8.8					

(1) On products compliant to MIL-PRF-38535, this parameter is not production tested.

(2) This note applies to SN54LV86A only: On products compliant to MIL-PRF-38535, this parameter is not production tested.

### 7.9 Noise Characteristics for SN74LV86A

$V_{CC} = 3.3\text{ V}$ ,  $C_L = 50\text{ pF}$ ,  $T_A = 25^\circ\text{C}$  (see <sup>(1)</sup>)

PARAMETER		MIN	TYP	MAX	UNIT
$V_{OL(P)}$	Quiet output, maximum dynamic $V_{OL}$		0.2	0.8	V
$V_{OL(V)}$	Quiet output, minimum dynamic $V_{OL}$		-0.1	-0.8	
$V_{OH(V)}$	Quiet output, minimum dynamic $V_{OH}$		3.1		
$V_{IH(D)}$	High-level dynamic input voltage	2.31			
$V_{IL(D)}$	Low-level dynamic input voltage			0.99	

(1) Characteristics are for surface-mount packages only.

### 7.10 Operating Characteristics

$T_A = 25^\circ\text{C}$

PARAMETER		TEST CONDITIONS	$V_{CC}$	TYP	UNIT
$C_{pd}$	Power dissipation capacitance	$C_L = 50\text{ pF}$ , $f = 10\text{ MHz}$	3.3 V	8.4	pF
			5 V	8.8	

### 7.11 Typical Characteristics

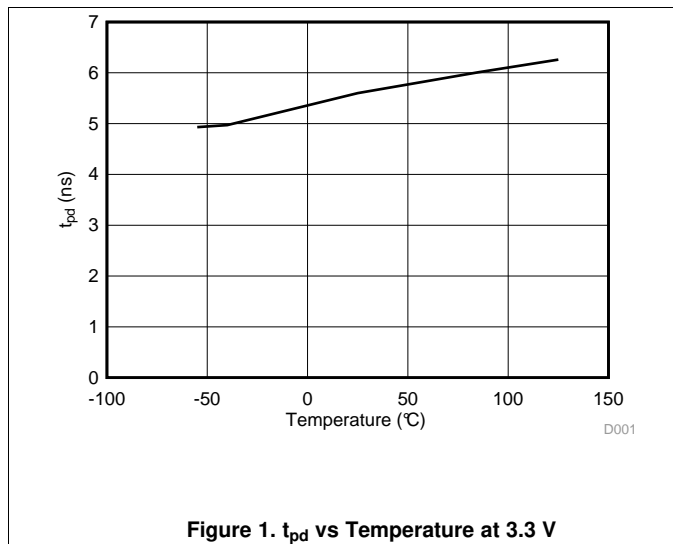


Figure 1.  $t_{pd}$  vs Temperature at 3.3 V

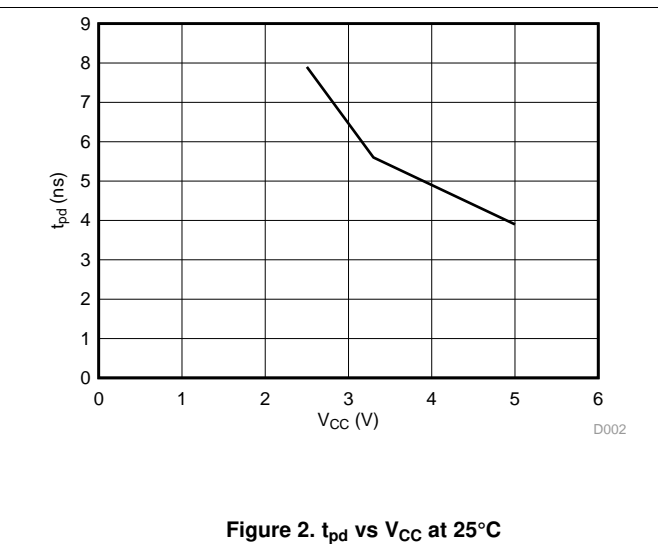
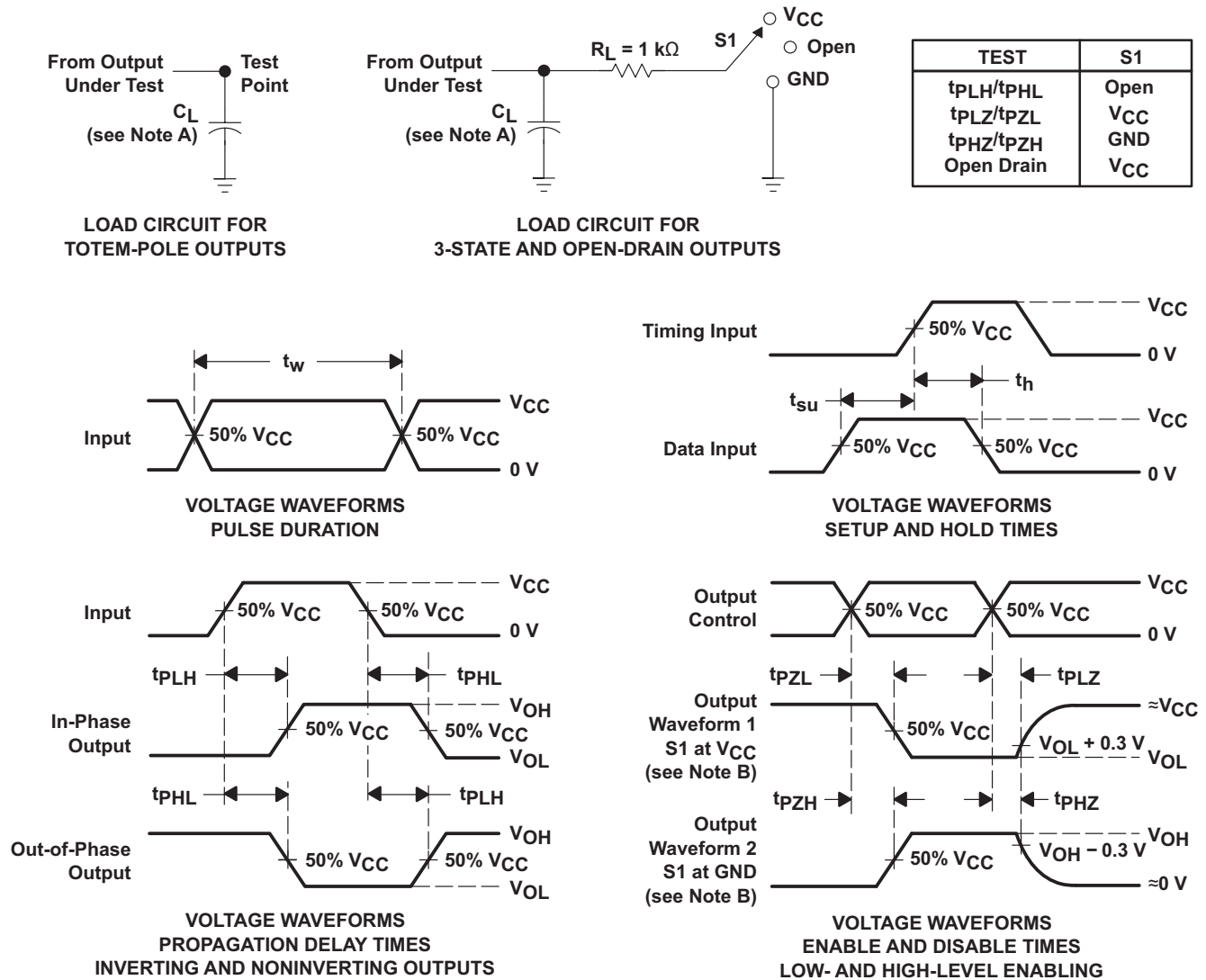


Figure 2.  $t_{pd}$  vs  $V_{CC}$  at 25°C

## 8 Parameter Measurement Information



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 1\text{ MHz}$ ,  $Z_O = 50\ \Omega$ ,  $t_r \leq 3\text{ ns}$ ,  $t_f \leq 3\text{ ns}$ .
- D. The outputs are measured one at a time, with one input transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PHL}$  and  $t_{PLH}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

**Figure 3. Load Circuit and Voltage Waveforms**



## 9 Detailed Description

### 9.1 Overview

The 'LV86A devices are quadruple 2-input exclusive-OR gates designed for 2-V to 5.5-V  $V_{CC}$  operation.

These devices contain four independent 2-input exclusive-OR gates. They perform the Boolean function  $Y = A \oplus B$  or  $Y = \overline{A}B + A\overline{B}$  in positive logic.

A common application is as a true/complement element. If one of the inputs is low, the other input is reproduced in true form at the output. If one of the inputs is high, the signal on the other input is reproduced inverted at the output.

### 9.2 Functional Block Diagram

An exclusive-OR gate has many applications, some of which can be represented better by alternative logic symbols.



A. These are five equivalent exclusive-OR symbols valid for an 'LV86A gate in positive logic; negation can be shown at any two ports.

**Figure 4. Exclusive OR**



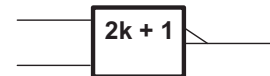
The output is active (low) if all inputs stand at the same logic level (that is,  $A = B$ ).

**Figure 5. Logic-Identity Element**



The output is active (low) if an even number of inputs (that is, 0 or 2) are active.

**Figure 6. Even-Parity Element**



The output is active (high) if an odd number of inputs (that is, only 1 of the 2) are active.

**Figure 7. Odd-Parity Element**

### 9.3 Feature Description

- Wide operating voltage range, operates from 2 to 5.5 V
- Allows down voltage translation, inputs accept voltages to 5.5 V

### 9.4 Device Functional Modes

**Table 1. Function Table (Each Gate)**

INPUTS		OUTPUT Y
A	B	
L	L	L
L	H	H
H	L	H
H	H	L

## 10 Application and Implementation

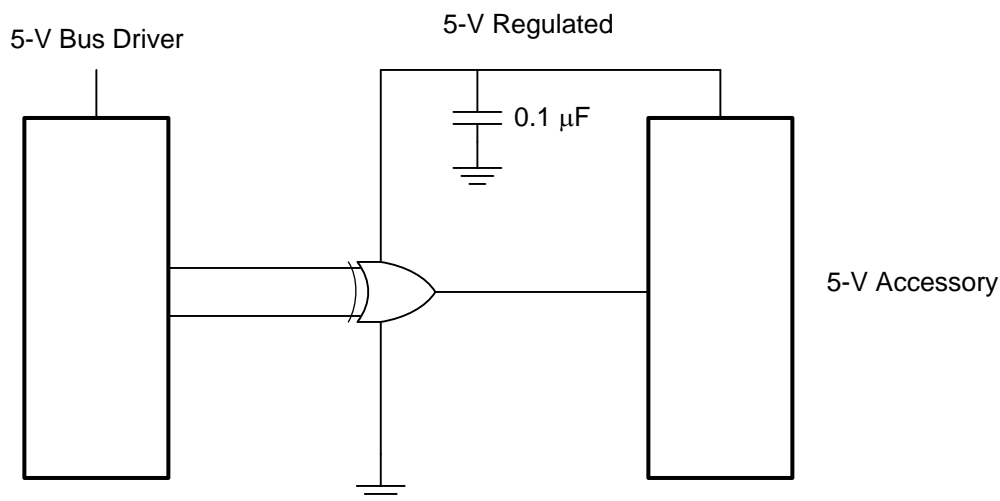
### NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

### 10.1 Application Information

The SN74LV86A is a low drive CMOS device that can be used for a multitude of bus interface type applications where output ringing is a concern. The low drive and slow edge rates will minimize overshoot and undershoot on the outputs. The inputs can accept voltages to 5.5 V at any valid  $V_{CC}$  making it ideal for down translation.

### 10.2 Typical Application



**Figure 8. Typical Application Schematic**

#### 10.2.1 Design Requirements

This device uses CMOS technology and has balanced output drive. Care should be taken to avoid bus contention because it can drive currents that would exceed maximum limits. The high drive will also create fast edges into light loads so routing and load conditions should be considered to prevent ringing.

#### 10.2.2 Detailed Design Procedure

1. Recommended Input conditions
  - Rise time and fall time specs see  $(\Delta t/\Delta V)$  in [Recommended Operating Conditions](#).
  - Specified High and low levels. See  $(V_{IH}$  and  $V_{IL})$  in [Recommended Operating Conditions](#).
2. Recommend output conditions
  - Load currents should not exceed 25 mA per output and 50 mA total for the part
  - Outputs should not be pulled above  $V_{CC}$

## Typical Application (continued)

### 10.2.3 Application Curve

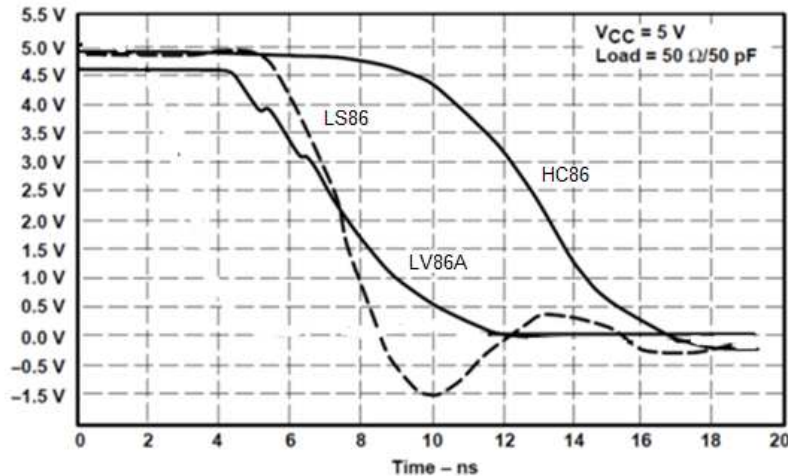


Figure 9. Switching Characteristics Comparison

## 11 Power Supply Recommendations

The power supply can be any voltage between the minimum and maximum supply voltage rating located in [Recommended Operating Conditions](#).

Each  $V_{CC}$  terminal should have a good bypass capacitor to prevent power disturbance. For devices with a single supply, TI recommends 0.1  $\mu\text{F}$  and if there are multiple  $V_{CC}$  terminals then .01 or .022  $\mu\text{F}$  is recommended for each power terminal. It is okay to parallel multiple bypass capacitors to reject different frequencies of noise. A 0.1  $\mu\text{F}$  and 1  $\mu\text{F}$  are commonly used in parallel. The bypass capacitor should be installed as close to the power terminal as possible for best results.

## 12 Layout

### 12.1 Layout Guidelines

When using multiple bit logic devices inputs should not ever float.

In many cases, functions or parts of functions of digital logic devices are unused, for example, when only two inputs of a triple-input AND gate are used or only 3 of the 4 buffer gates are used. Such input pins should not be left unconnected because the undefined voltages at the outside connections result in undefined operational states. Specified below are the rules that must be observed under all circumstances. All unused inputs of digital logic devices must be connected to a high or low bias to prevent them from floating. The logic level that should be applied to any particular unused input depends on the function of the device. Generally they will be tied to GND or  $V_{CC}$  whichever make more sense or is more convenient. It is generally okay to float outputs unless the part is a transceiver. If the transceiver has an output enable pin it will disable the outputs section of the part when asserted. This will not disable the input section of the IOs so they also cannot float when disabled.

### 12.2 Layout Example

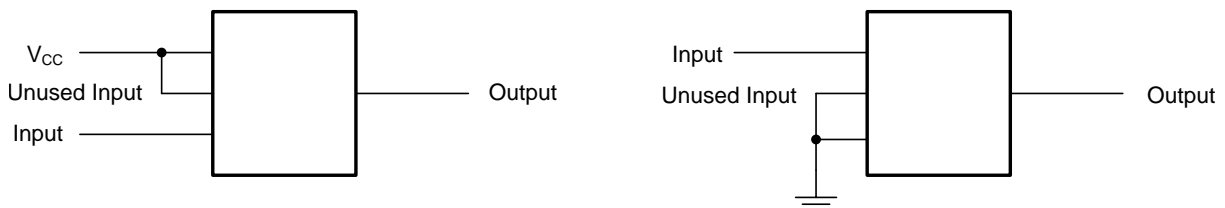


Figure 10. Layout Recommendation

## 13 Device and Documentation Support

### 13.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

**Table 2. Related Links**

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
SN54LV86A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>
SN74LV86A	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>	<a href="#">Click here</a>

### 13.2 Trademarks

All trademarks are the property of their respective owners.

### 13.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

### 13.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

## 14 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

**PACKAGING INFORMATION**

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
SN74LV86ADBR	ACTIVE	SSOP	DB	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV86A	<a href="#">Samples</a>
SN74LV86ADGVR	ACTIVE	TVSOP	DGV	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV86A	<a href="#">Samples</a>
SN74LV86ADR	ACTIVE	SOIC	D	14	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV86A	<a href="#">Samples</a>
SN74LV86ANSR	ACTIVE	SO	NS	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	74LV86A	<a href="#">Samples</a>
SN74LV86APWR	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV86A	<a href="#">Samples</a>
SN74LV86APWRG4	ACTIVE	TSSOP	PW	14	2000	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 125	LV86A	<a href="#">Samples</a>

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

**Important Information and Disclaimer:** The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

**OTHER QUALIFIED VERSIONS OF SN74LV86A :**

- Automotive : [SN74LV86A-Q1](#)
- Enhanced Product : [SN74LV86A-EP](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
SN74LV86ADBR	SSOP	DB	14	2000	330.0	16.4	8.35	6.6	2.4	12.0	16.0	Q1
SN74LV86ADGVR	TVSOP	DGV	14	2000	330.0	12.4	6.8	4.0	1.6	8.0	12.0	Q1
SN74LV86ADR	SOIC	D	14	2500	330.0	16.4	6.5	9.0	2.1	8.0	16.0	Q1
SN74LV86ANSR	SO	NS	14	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
SN74LV86APWR	TSSOP	PW	14	2000	330.0	12.4	6.9	5.6	1.6	8.0	12.0	Q1

**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
SN74LV86ADBR	SSOP	DB	14	2000	356.0	356.0	35.0
SN74LV86ADGVR	TVSOP	DGV	14	2000	356.0	356.0	35.0
SN74LV86ADR	SOIC	D	14	2500	356.0	356.0	35.0
SN74LV86ANSR	SO	NS	14	2000	356.0	356.0	35.0
SN74LV86APWR	TSSOP	PW	14	2000	356.0	356.0	35.0



# MECHANICAL DATA

NS (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE PACKAGE

14-PINS SHOWN

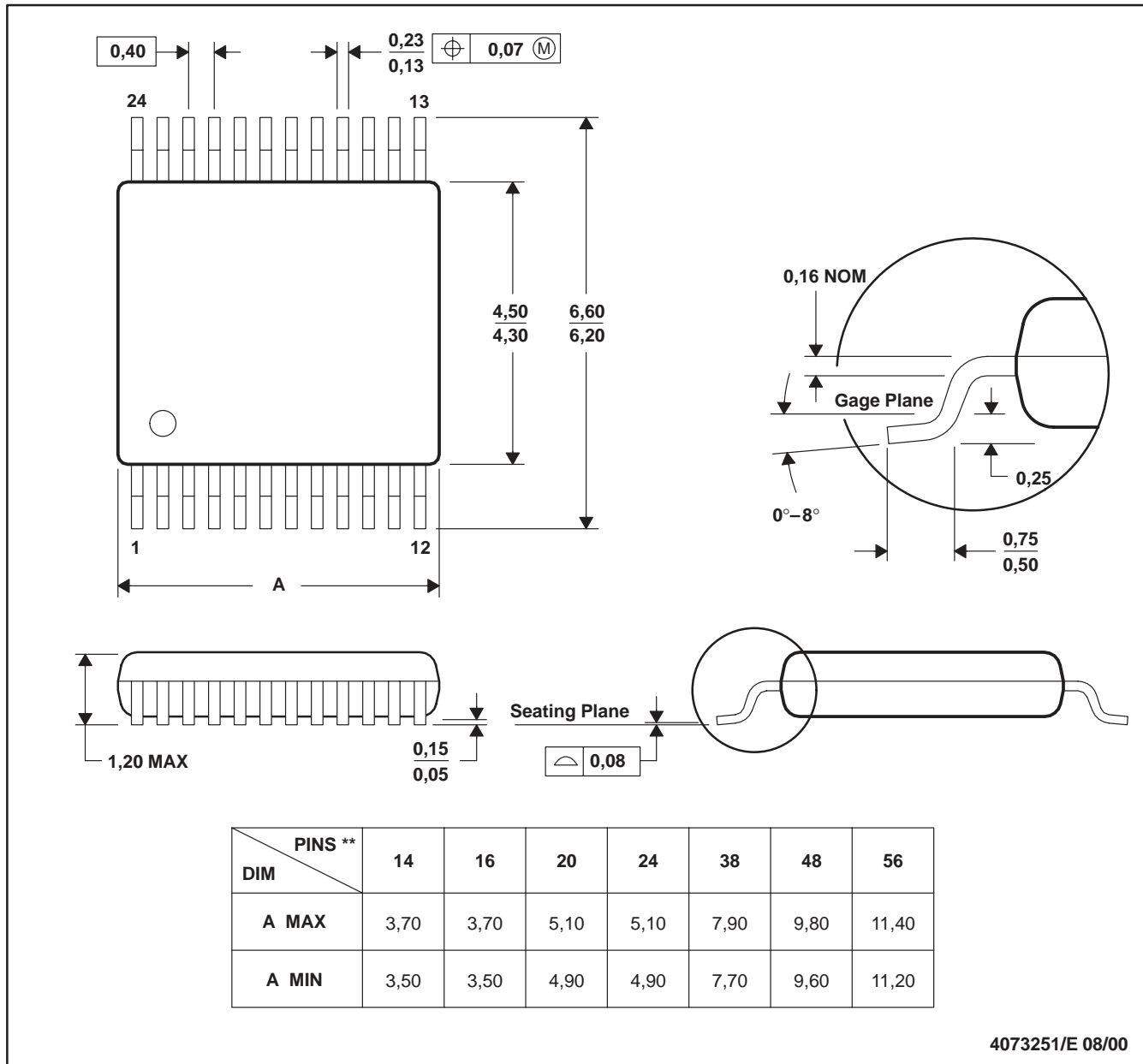


- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15.

DGV (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

24 PINS SHOWN



4073251/E 08/00

- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.  
 D. Falls within JEDEC: 24/48 Pins – MO-153  
 14/16/20/56 Pins – MO-194

D (R-PDSO-G14)

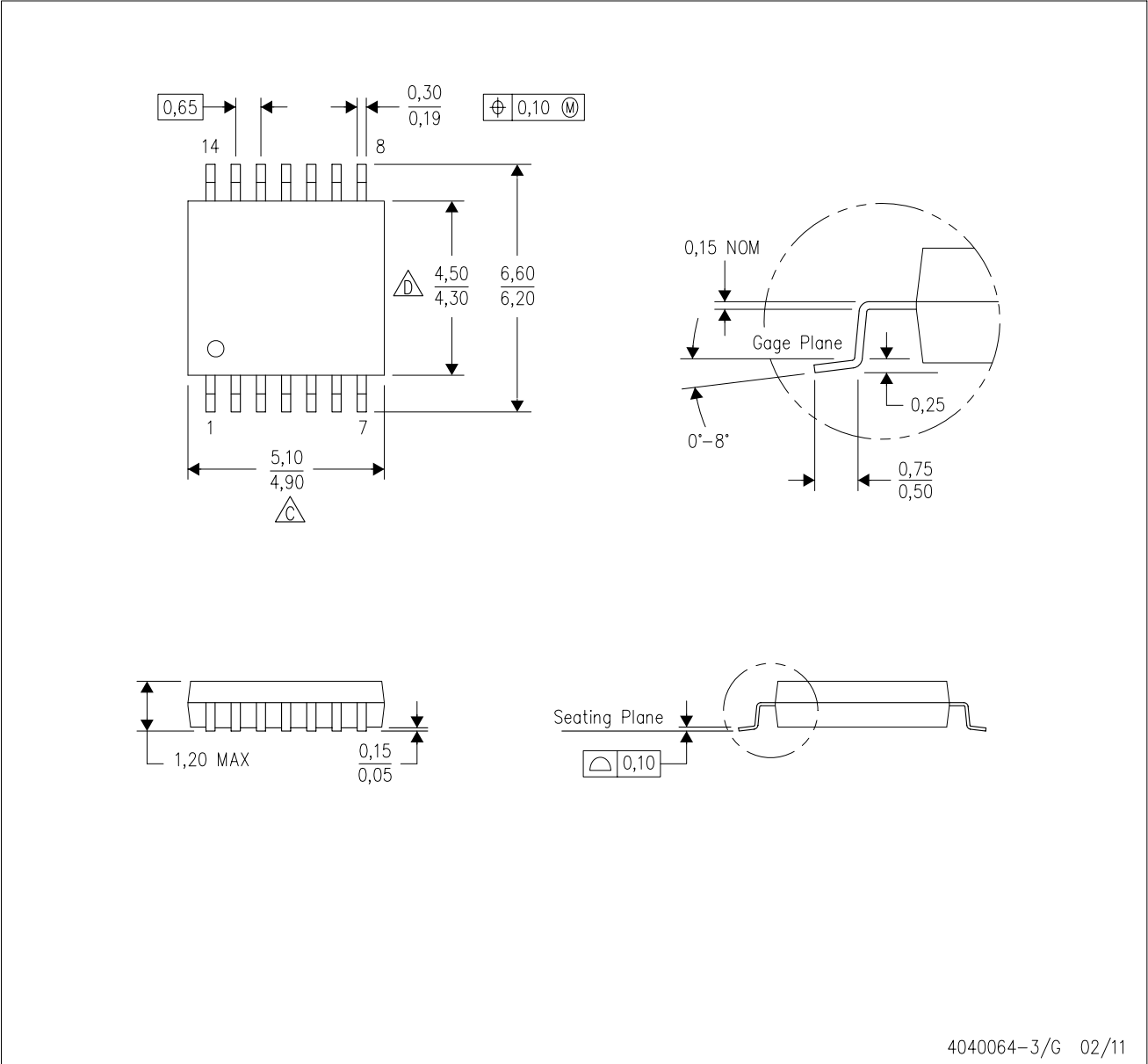
PLASTIC SMALL OUTLINE



- NOTES:
- A. All linear dimensions are in inches (millimeters).
  - B. This drawing is subject to change without notice.
  - Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
  - Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
  - E. Reference JEDEC MS-012 variation AB.

PW (R-PDSO-G14)

PLASTIC SMALL OUTLINE



4040064-3/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
  - B. This drawing is subject to change without notice.
  - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
  - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
  - E. Falls within JEDEC MO-153

DB (R-PDSO-G\*\*)

PLASTIC SMALL-OUTLINE

28 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.  
 B. This drawing is subject to change without notice.  
 C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.  
 D. Falls within JEDEC MO-150

## IMPORTANT NOTICE AND DISCLAIMER

TI PROVIDES TECHNICAL AND RELIABILITY DATA (INCLUDING DATA SHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for skilled developers designing with TI products. You are solely responsible for (1) selecting the appropriate TI products for your application, (2) designing, validating and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, regulatory or other requirements.

These resources are subject to change without notice. TI grants you permission to use these resources only for development of an application that uses the TI products described in the resource. Other reproduction and display of these resources is prohibited. No license is granted to any other TI intellectual property right or to any third party intellectual property right. TI disclaims responsibility for, and you will fully indemnify TI and its representatives against, any claims, damages, costs, losses, and liabilities arising out of your use of these resources.

TI's products are provided subject to [TI's Terms of Sale](#) or other applicable terms available either on [ti.com](https://www.ti.com) or provided in conjunction with such TI products. TI's provision of these resources does not expand or otherwise alter TI's applicable warranties or warranty disclaimers for TI products.

TI objects to and rejects any additional or different terms you may have proposed.

Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265  
Copyright © 2023, Texas Instruments Incorporated