

# ILC6383

## 1-Cell to 3-Cell Boost DC-DC Converter with True Load Disconnect, 3.3V, 5V or Adjustable Output

### Features

- Guaranteed start up in PWM at 0.9V input
- Synchronous rectification requires no external diode
- True load disconnect from battery input in shutdown
- Up to 75mA at 3.3V and 40mA at 5V from 1V input
- Up to 375mA at 3.3V and 300mA at 5V from 3V input
- Peak efficiency > 90%
- 1µA battery input current in shutdown (with  $V_{OUT} = 0V$ )
- Internal Oscillator frequency: 300kHz to  $\pm 15\%$
- ILC6383: Fixed 3.3V or 5V output
- ILC6383-ADJ: Adjustable output to 6V maximum
- Low battery detector with 100ms transient rejection delay
- Powergood output flag when  $V_{OUT}$  is in regulation

### Applications

- Cellular Phones, Pagers
- Palmtops, PDAs and portable electronics
- High efficiency 1V step up converters

### Description

The ILC6383 series of step-up DC-DC converters operate from 1-cell to 3-cell input. They are direct replacement for ILC6382, in applications where SYNC pin is not used. The PFM or PWM operating mode is user selectable through SEL pin connected to ground or left open, respectively. The choice should be dependent upon the current to be delivered to the load: PFM is recommended for input voltage higher than 1.5V and loads below 100mA, while PWM is recommended for more than 50mA load current and in noise sensitive applications. In shutdown mode, the device allows true load disconnect from battery input. Designed for wireless communications applications, the oscillator frequency is set at 300kHz with no harmonics at sub 20kHz audio band or at 455kHz IF band.

Internal synchronous rectification and externally selectable PFM/PWM mode of operation allows the selection of the best efficiency at light or full load. The ILC6383 is capable of delivering 75mA at 3.3V output from a single cell input. The ILC6383-XX offers 3.3V or 5V fixed output voltage while the ILC6383-ADJ allows adjustable output voltage to 6V maximum. Output voltage accuracy is  $\pm 3.5\%$  over full operating temperature range.

Additional features include power good output ( $\overline{POK}$ ) and an internal low battery detector with 100ms transient rejection delay. The device will reject low battery input transients under 100ms in duration. The ILC6383 series is available in a space saving eight lead micro SOP (MSOP-8) package.

### Typical Applications

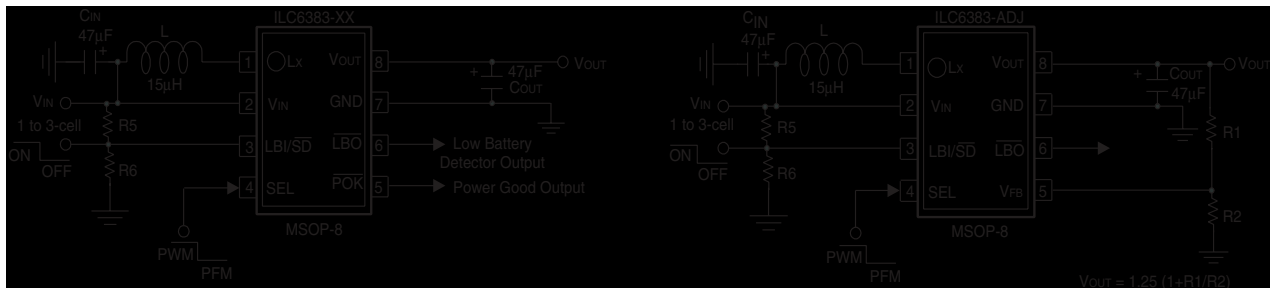
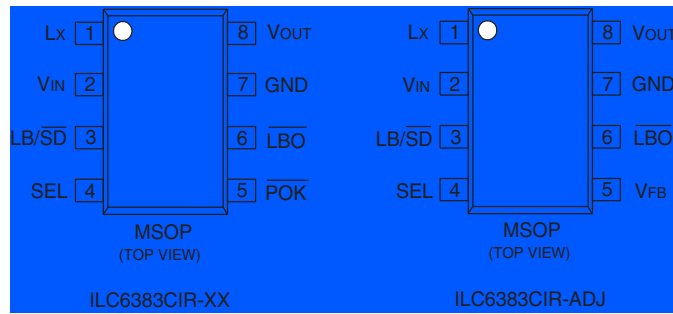


Figure 1. ILC6383CIR-XX

Figure 2. ILC6383CIR-ADJ

## Pin Assignments



## Pin Definitions

Pin Number	Pin Number	Pin Description
1	L <sub>X</sub>	<b>Inductor input.</b> Inductor L connected between this pin and the battery
2	V <sub>IN</sub>	<b>Input Voltage.</b> Connect directly to battery
3	LBI/ $\overline{\text{SD}}$	<b>Low battery detect input and shutdown.</b> Low battery detect threshold is set with this pin using a potential divider. If this pin is pulled to logic low then the device will shutdown.
4	SEL	<b>Select Input.</b> A low logic level signal applied to this pin selects PFM operation mode. If the pin is left open or high logic level is applied, PWM mode is selected.
5	$\overline{\text{POK}}$ (ILC6383CIR-XX)	<b>Power Good Output.</b> This open drain output pin will go high when output voltage is within regulation, $0.92 \cdot V_{\text{OUT(NOM)}} \leq V_{\text{threshold}} \leq 0.98 \cdot V_{\text{OUT(NOM)}}$
	V <sub>FB</sub> (ILC6383CIR-ADJ)	<b>Feedback Input.</b> This pin sets the adjustable output voltage via an external resistor divider network. The formula for choosing the resistors is shown in the “Applications Information” section.
6	$\overline{\text{LBO}}$	This open drain output will go low if the battery voltage is below the low battery threshold set at pin 3
7	GND	<b>Ground of the IC.</b> Connect this pin to the battery and system ground
8	V <sub>OUT</sub>	<b>Regulated output voltage.</b>

## Absolute Maximum Ratings (Note 1)

Parameter	Symbol	Ratings	Units
Voltage on V <sub>OUT</sub> pin	V <sub>OUT</sub>	-0.3 to 7	V
Voltage on LBI, Sync, $\overline{\text{LBO}}$ , $\overline{\text{POK}}$ , V <sub>FB</sub> , L <sub>X</sub> and V <sub>IN</sub> pins	-	-0.3 to 7	V
Peak switch current on L <sub>X</sub> pin	I <sub>LX</sub>	1	A
Current on $\overline{\text{LBO}}$ pin	I <sub>SINK(LBO)</sub>	5	mA
Continuous total power dissipation at 85°C	P <sub>D</sub>	315	mW
Short circuit current	I <sub>SC</sub>	Internally protected (1 sec. duration)	A
Operating ambient temperature	T <sub>A</sub>	-40 to 85	°C
Maximum junction temperature	T <sub>J(MAX)</sub>	150	°C
Storage temperature	T <sub>stg</sub>	-40 to 125	°C
Lead temperature (soldering 10 sec.)		300	°C
Package thermal resistance	θ <sub>JA</sub>	206	°C/W

**Electrical Characteristics ILC6383CIR-33 in PFM Mode** (SEL in LOW State)

Unless otherwise specified, all limits are at  $V_{IN} = V_{LBI} = 2.0V$ ,  $I_{OUT} = 1mA$  and  $T_A = 25^{\circ}C$ , test circuit Figure 1.

**BOLDFACE** type indicates limit that apply over the full operating temperature range. (Note 2)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Voltage	$V_{OUT(nom)}$	$1.5V \leq V_{IN} \leq 2.4V$ , $1.5V \leq V_{IN} \leq 2.4V$	3.217 <b>3.184</b>	3.3	3.382 <b>3.415</b>	V
Maximum Output Current	$I_{OUT}$	$V_{OUT} \geq 0.96V_{OUT(nom)}$ ,		150		mA
Load Regulation	$\frac{\Delta V_{OUT}}{V_{OUT}}$	$1mA \leq I_{OUT} \leq 20mA$		1		%
No Load Battery Input Current	$I_{IN}$ (no load)	$I_{OUT} = 0mA$ , $V_{IN}=V_{LBI}=1.2V$		250		$\mu A$
Efficiency	$\eta$	$I_{OUT} = 20mA$		88		%

**Electrical Characteristics ILC6383CIR-33 in PWM Mode** (SEL Open)

Unless otherwise specified, all limits are at  $V_{IN} = V_{LBI} = 2.0V$ ,  $I_{OUT} = 50mA$  and  $T_A = 25^{\circ}C$ , test circuit Figure 1.

**BOLDFACE** type indicates limit that apply over the full operating temperature range. (Note 2)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Voltage	$V_{OUT}$	$1.5V \leq V_{IN} \leq 2.4V$ , $1.5V \leq V_{IN} \leq 2.4V$	3.217 <b>3.184</b>	3.3	3.382 <b>3.415</b>	V
Maximum Output Current	$I_{OUT}$	$V_{IN} = 1.2V$ , $V_{OUT} \geq 0.96V_{OUT(nom)}$ $V_{IN} = 2.0V$ , $V_{OUT} \geq 0.96V_{OUT(nom)}$ $V_{IN} = 2.4V$ , $V_{OUT} \geq 0.96V_{OUT(nom)}$ $V_{IN} = 3.0V$ , $V_{OUT} \geq 0.96V_{OUT(nom)}$		75 150 200 375		mA
Load Regulation	$\frac{\Delta V_{OUT}}{V_{OUT}}$	$50mA \leq I_{OUT} \leq 100mA$		1		%
Efficiency	$\eta$	$I_{OUT} = 50mA$		90		%

**Electrical Characteristics ILC6383CIR-50 in PFM Mode** (SEL in LOW State)

Unless otherwise specified, all limits are at  $V_{IN} = V_{LBI} = 2.4V$ ,  $I_{OUT} = 1mA$  and  $T_A = 25^{\circ}C$ , test circuit Figure 1.

**BOLDFACE** type indicates limit that apply over the full operating temperature range. (Note 2)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Voltage	$V_{OUT(nom)}$	$1.5V \leq V_{IN} \leq 3V$ , $1.5V \leq V_{IN} \leq 3V$	4.875 <b>4.825</b>	5.0	5.125 <b>5.175</b>	V
Maximum Output Current	$I_{OUT}$	$V_{OUT} \geq 0.96V_{OUT(nom)}$		150		mA
Load Regulation	$\frac{\Delta V_{OUT}}{V_{OUT}}$	$1mA \leq I_{OUT} \leq 20mA$		1		%
No Load Battery Input Current	$I_{IN}$ (no load)	$I_{OUT} = 0mA$ , $V_{IN}=V_{LBI}=1.5V$		550		$\mu A$
Efficiency	$\eta$	$I_{OUT} = 20mA$		90		%

## Electrical Characteristics ILC6383CIR-50 in PWM Mode (SEL Open)

Unless otherwise specified, all limits are at  $V_{IN} = V_{LBI} = 2.4V$ ,  $I_{OUT} = 50mA$  and  $T_A = 25^\circ C$ , test circuit Figure 1.

**BOLDFACE** type indicates limit that apply over the full operating temperature range. (Note 2)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Output Voltage	$V_{OUT}$	$1.5V \leq V_{IN} \leq 3V$ , $1.5V \leq V_{IN} \leq 3V$	4.875 <b>4.825</b>	5.0	5.125 <b>5.175</b>	V
Maximum Output Current	$I_{OUT}$	$V_{IN} = 1.2V$ , $V_{OUT} \geq 0.96V_{OUT(nom)}$ $V_{IN} = 2.0V$ , $V_{OUT} \geq 0.96V_{OUT(nom)}$ $V_{IN} = 2.4V$ , $V_{OUT} \geq 0.96V_{OUT(nom)}$ $V_{IN} = 3.0V$ , $V_{OUT} \geq 0.96V_{OUT(nom)}$		75 150 200 300		mA
Load Regulation	$\frac{\Delta V_{OUT}}{V_{OUT}}$	$1mA \leq I_{OUT} \leq 50mA$		1		%
Efficiency	$\eta$	$I_{OUT} = 50mA$		90		%

## General Electrical Characteristics

Unless otherwise specified, all limits are at  $V_{IN} = V_{LBI} = 2.4V$  and  $T_A = 25^\circ C$ , test circuit figure 1 and figure 2 for.

ILC6383CIR-XX and ILC6383CIR-ADJ respectively. (Note 2)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
$\overline{LBO}$ Output Voltage Low	$V_{LBO(low)}$	$I_{SINK} = 2mA$ , open drain output, $V_{LBI} = 1V$			<b>0.4</b>	V
$\overline{LBO}$ Output Leakage Current	$I_{LBO(hi)}$	$V_{LBO} = 5V$		1	<b>2</b>	$\mu A$
Shutdown Input Voltage Low	$V_{SD(low)}$				<b>0.4</b>	V
Shutdown Input Voltage High	$V_{SD(hi)}$		<b>1</b>		<b>6</b>	V
SEL Input Voltage High	$V_{SEL(hi)}$		<b>1.5</b>			V
SEL Input Voltage Low	$V_{SEL(low)}$				<b>0.4</b>	V
$\overline{POK}$ Output Voltage Low	$V_{POK(low)}$	$I_{SINK} = 2mA$ , open drain output			<b>0.4</b>	V
$\overline{POK}$ Output Voltage High	$V_{POK(hi)}$				<b>6</b>	V
$\overline{POK}$ Output Leakage Current	$I_{L(POK)}$	6V at pin 5			<b>2</b>	$\mu A$
$\overline{POK}$ Threshold	$V_{TH(POK)}$		$0.92 \times V_{OUT}$	$0.95 \times V_{OUT}$	$0.98 \times V_{OUT}$	V
$\overline{POK}$ Hysteresis	$V_{HYST}$			50		mV
Feedback Voltage (ILC6383CIR-ADJ only)	$V_{FB}$		1.225 <b>1.212</b>	1.250	1.275 <b>1.288</b>	V
Output Voltage Adjustment Range (ILC6383CIR-ADJ only)	$V_{OUT(ADJ) min}$ $V_{OUT(ADJ) max}$	$V_{IN} = 0.9V$ , $I_{OUT} = 50mA$ $V_{IN} = 3V$ , $I_{OUT} = 50mA$		2.5V 6V		V
Minimum Startup Voltage	$V_{IN(start)}$	$I_{OUT} = 10mA$ , PWM mode		0.9	<b>1</b>	V

**General Electrical Characteristics** (continued)

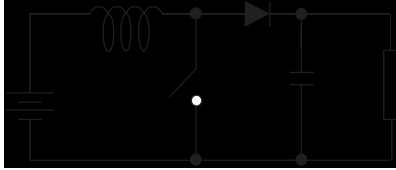
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Input Voltage Range	$V_{IN}$	$V_{OUT} = V_{OUT(nominal)} \pm 4\%$ $I_{OUT} = 10mA$	0.9 <b>1</b>		$V_{OUT(nominal)}$ +0.5V	V
Battery Input Current in Load Disconnect Mode	$I_{IN(SD)}$	$V_{LBI/SD} \leq 0.4V$ , $V_{OUT} = 0V$ (short circuit)		1	<b>10</b>	$\mu A$
Switch on resistance	$R_{ds(on)}$	N-Channel MOSFET P-Channel MOSFET		400 750		$m\Omega$
Oscillator Frequency	$f_{OSC}$		<b>255</b>	300	<b>345</b>	kHz
LBI Input Threshold	$V_{REF}$		1.175 <b>1.150</b>	1.250	1.325 <b>1.350</b>	
Input Leakage Current	$I_{LEAK}$	Pins $\overline{LB/SD}$ , SEL and $V_{FB}$ , (Note 3)			200	nA
LBI Hold Time	$t_{HOLD(LBI)}$	(Note 4)	<b>100</b>	120		mS

**Notes:**

1. Absolute maximum ratings indicate limits which, when exceeded, may result in damage to the component. Electrical specifications do not apply when operating the device outside its rated operating conditions.
2. Specified min/max limits are production tested or guaranteed through correlation based on statistical control methods. Measurements are taken at constant junction temperature as close to ambient temperature as possible using low duty cycle pulse testing.
3. Guaranteed by design.
4. In order to get a valid low-battery-output ( $\overline{LBO}$ ) signal, the input voltage must be lower than the low-battery-input (LBI) threshold for a duration greater than the low battery hold time ( $t_{HOLD(LBI)}$ ). This feature eliminates false triggering due to voltage transients at the battery terminal.

## Applications Information

The ILC6383 performs boost DC-DC conversion by controlling the switch element as shown in the simplified circuit in Figure 3 below.



**Figure 3. Basic Boost Circuit**

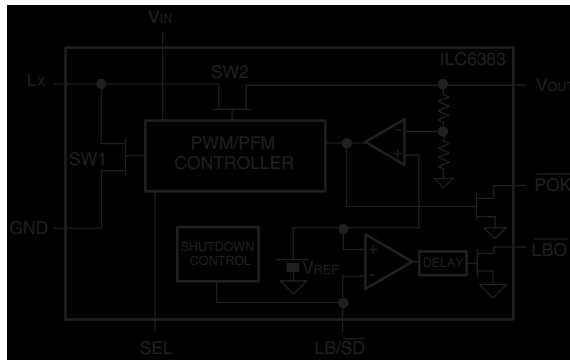
When the switch is closed, current is built up through the inductor. When the switch opens, this current is forced through the diode to the output. As this on and off switching continues, the output capacitor voltage builds up due to the charge it is storing from the inductor current. In this way, the output voltage is boosted relative to the input.

In general, the switching characteristic is determined by the output voltage desired and the current required by the load. The energy transfer is determined by the power stored in the coil during each switching cycle.

$$P_L = f(t_{ON}, V_{IN})$$

### Synchronous Rectification

The ILC6383 also uses a technique called “synchronous rectification” which removes the need for the external diode used in other circuits. The diode is replaced with a second switch or in the case of the ILC6383, an FET as shown in Figure 4 below.



**Figure 4. Simplified ILC6382 block diagram**

The two switches now open and close in opposition to each other, directing the flow of current to either charge the inductor or to feed the load. The ILC6383 monitors the voltage on the output capacitor to determine how much and how often to drive the switches.

### PWM Mode Operation

The ILC6383 uses a PWM or Pulse Width Modulation technique. The switches are constantly driven at typically 300kHz. The control circuitry varies the power being delivered to the load by varying the on-time, or duty cycle, of the switch SW1 (see Fig. 5). Since more on-time translates to higher current build-up in the inductor, the maximum duty cycle of the switch determines the maximum load current that the device can support. The minimum value of the duty cycle determines the minimum load current that can maintain the output voltage within specified values.

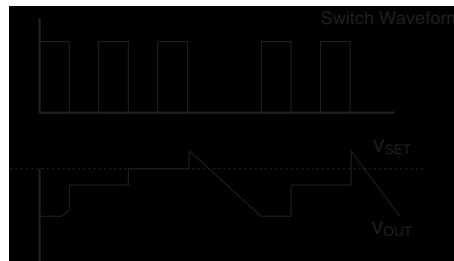
There are two key advantages of the PWM type controllers. First, because the controller automatically varies the duty cycle of the switch's on-time in response to changing load conditions, the PWM controller will always have an optimized waveform for a steady-state load. This translates to very good efficiency at high currents and minimal ripple on the output. Ripple is due to the output cap constantly accepting and storing the charge received from the inductor, and delivering charge as required by the load. The “pumping” action of the switch produces a sawtooth-shaped voltage as seen by the output.

The other key advantage of the PWM type controllers over pulse frequency modulated (PFM) type is that the radiated noise due to the switching transients will always occur at the (fixed) switching frequency. Many applications do not care much about switching noise, but certain types of applications, especially communication equipment, need to minimize the high frequency interference within their system as much as possible. Use of the PWM converter in those cases is desirable.

### PFM Mode Operation

For light loads the ILC6383 can be switched to PFM technique at low currents. This technique conserves power loss by only switching the output if the current drain requires it. As shown in the Figure 5, the waveform actually skips pulses depending on the power needed by the output. This technique is also called “pulse skipping” because of this characteristic.

In the ILC6383, the switchover from PWM to PFM mode is determined by the user to improve efficiency and conserve power.



**Figure 5. PFM Waveform**

The Dual PWM/PFM mode architecture was designed specifically for applications such as wireless communications, which need the spectral predictability of a PWM-type DC-DC converter, yet also need the highest efficiencies possible, especially in Standby mode.

**Other Considerations**

The other limitation of PWM techniques is that, while the fundamental switching frequency is easier to filter out since it's constant, the higher order harmonics of PWM will be present and may have to be filtered out, as well. Any filtering requirements, though, will vary by application and by actual system design and layout, so generalizations in this area are difficult, at best.

However, PWM control for boost DC-DC conversion is widely used, especially in audio-noise sensitive applications or applications requiring strict filtering of the high frequency components.

**Low Battery Detector**

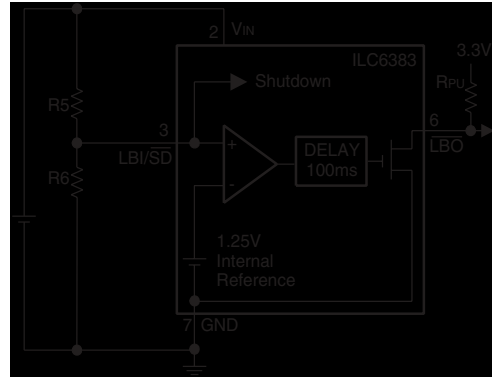
The ILC6383's low battery detector is based on a CMOS comparator. The negative input of the comparator is tied to an internal 1.25V (nominal) reference,  $V_{REF}$ . The positive input is the LBI/ $\overline{SD}$  pin. It uses a simple potential divider arrangement with two resistors to set the LBI threshold as shown in Figure 6. The input bias current of the LBI pin is only 200nA. This means that the resistor values R1 and R2 can be set quite high. The formula for setting the LBI threshold is:

$$V_{LBI} = V_{REF} \times (1 + R5/R6)$$

Since the LBI input current is negligible (<200nA), this equation is derived by applying voltage divider formula across R6. A typical value for R6 is 100k $\Omega$ .

$$R5 = 100k\Omega \times [(V_{LBI}/V_{REF}) - 1], \text{ where } V_{REF} = 1.25V \text{ (nom.)}$$

The LBI detector has a built in delay of 120ms. In order to get a valid low-battery-output (LBO) signal, the input voltage must be lower than the low-battery-input (LBI) threshold for a duration greater than the low battery hold time ( $t_{hold(LBI)}$ ) of 120msec. This feature eliminates false triggering due to voltage transients at the battery terminal caused by high frequency switching currents.

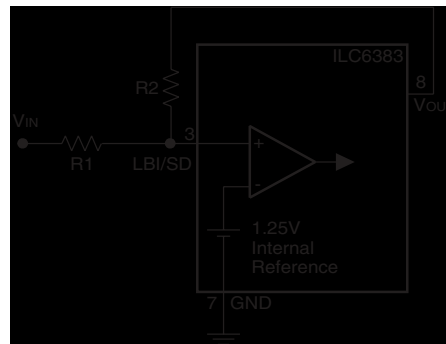


**Figure 6. Low Battery Detector**

The output of the low battery detector is an open drain capable of sinking 2mA. A 10k $\Omega$  pull-up resistor is recommended on this output.

**For  $V_{LBI} < 1.25V$**

The low battery detector can also be configured for voltages <1.25V by bootstrapping the LBI input from  $V_{OUT}$ . The circuitry for this is shown in Figure 7.



**Figure 7.  $V_{LBI} < 1.25V$**

The following equation is used when  $V_{IN}$  is lower than 1.25V:

$$R1 = R2 \times [(V_{REF} - V_{IN}) / (V_{OUT} - V_{REF})], \text{ where } V_{REF} = 1.25V \text{ (nom.)}$$

This equation can also be derived using voltage divider formula across R2. A typical value for R2 is 100k $\Omega$ .

### Shut Down

The LBI pin is shared with the shutdown pin. A low voltage (<0.4V) will put the ILC6383 into a power down state. The simplest way to implement this is with an FET across R6 as shown in Figure 8. Note that when the device is not in PWM mode or is in shutdown the low battery detector does not operate.

When the ILC6383 is shut down, the synchronous rectifier disconnects the output from the input. This ensures that there is only leakage ( $I_{IN} < 1\mu A$  typical) from the input to the output so that the battery is not drained when the ILC6383 is shut down.

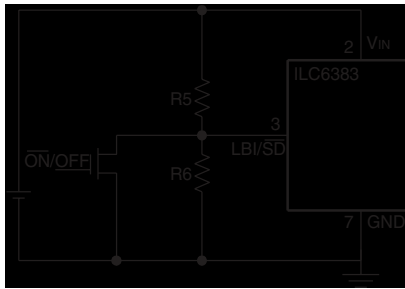


Figure 8. Shut Down Control

### Power Good Output (POK)

The POK output of the ILC6383 indicates when  $V_{OUT}$  is within the regulation tolerance of the set output voltage. POK output is an open drain device output capable of sinking 2mA. It will remain pulled low until the output voltage has risen to typically 95% of the specified  $V_{OUT}$ . Note that a pull-up resistor must be connected from the POK output (pin 5 of ILC6383CIR-XX) to either ILC6383's output or to some other system voltage source.

### Adjustable Output Voltage Selection

The ILC6383-ADJ allows the output voltage to be set using a potential divider. The formula for setting the adjustable output voltage is;

$$V_{OUT} = V_{FB} \times (1 + R1/R2), R1 + R2 \leq 100K\Omega$$

where  $V_{FB}$  is the threshold set which is 1.25V nominal.

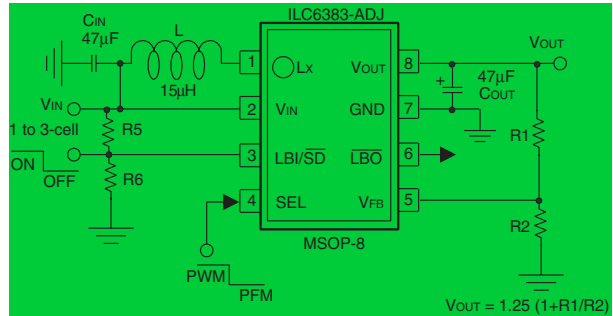


Figure 9. Adjustable Voltage Configuration

### Negative Voltage Output

It is possible to generate a negative output voltage as a secondary supply using the ILC6383. This negative voltage may be useful in some applications where a negative bias voltage at low current is required.

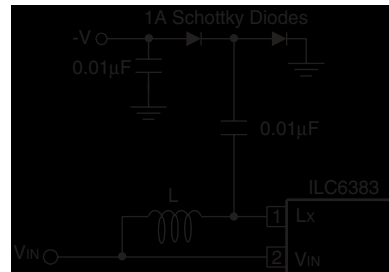


Figure 10. Negative Output Voltage



## External Component Selection

### Inductors

The ILC6383 is designed to work with a 15µH inductor in most applications. There are several vendors who supply standard surface mount inductors to this value. Suggested suppliers are shown in Table 1. Higher values of inductance will improve efficiency, but will reduce peak inductor current and consequently ripple and noise, but will also limit output current.

Vendor	Part No.	Contact
Coilcraft	D03308P-153 D03316P-153 D01608C-153	(847) 639-6400
muRata	LQH4N150K LQH3C150K	(814) 237-1431
Sumida	CDR74B-150MC CD43-150 CD54-150	(847) 956-0666
TDK	NLC453232T-150K	(847) 390-4373

### Capacitors

#### Input Capacitor

The input capacitor is necessary to minimize the peak current drawn from the battery. Typically a 10µF tantalum capacitor is recommended. Low equivalent series resistance (ESR) capacitors will help to minimize battery voltage ripple.

#### Output Capacitor

Low ESR capacitors should be used at the output of the ILC6383 to minimize output ripple. The high switching speeds and fast changes in the output capacitor current, mean that the equivalent series impedance of the capacitor can contribute greatly to the output ripple. In order to minimize these effects choose an output capacitor with less than 10nH of equivalent series inductance (ESL) and less than 100mΩ of equivalent series resistance (ESR). Typically these characteristics are met with ceramic capacitors, but may also be met with certain types of tantalum capacitors. Suitable vendors are shown in Table 2.

Description	Vendor	Contact
T495 series tantalum	Kemet	(864) 963-6300
595D series tantalum	Sprague	(603) 224-1961
TAJ, TPS series tantalum	AVX	(803) 946-0690
X5R, X7R Ceramic	TDK	(847) 390-4373
	AVX	(803) 946-0690
	muRata	www.murata.com

### Layout and Grounding Considerations

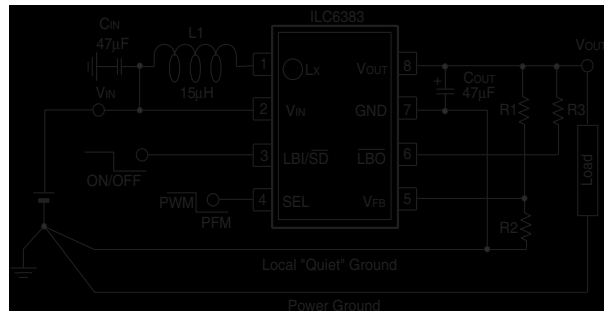
High frequency switching and large peak currents means PCB design for DC-DC converters requires careful consideration. As a general rule, place the DC-DC converter circuitry well away from any sensitive RF or analog components. The layout of the DC-DC converters and its external components are also based on some simple rules to minimize EMI and output voltage ripple.

#### Layout

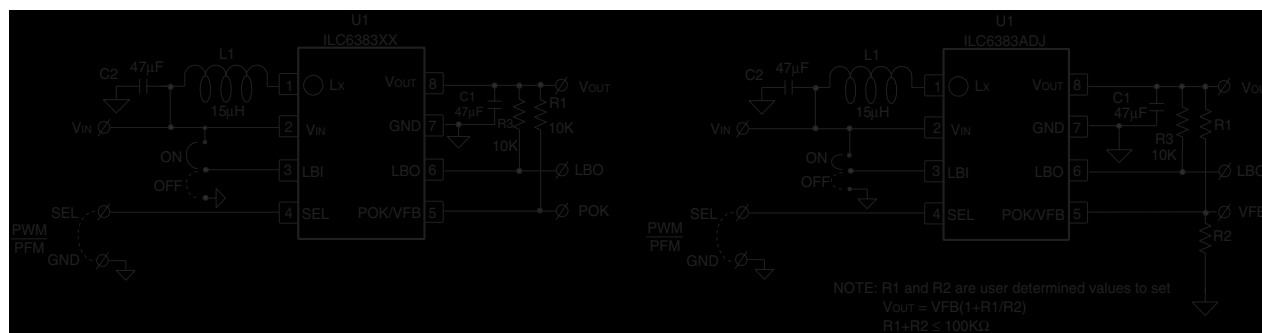
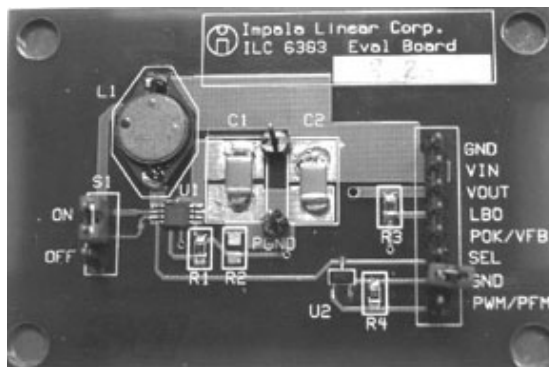
1. Place all power components, ILC6383, inductor, input capacitor and output capacitor as close together as possible.
2. Keep the output capacitor as close to the ILC6383 as possible with very short traces to the V<sub>OUT</sub> and GND pins. Typically it should be within 0.25 inches or 6mm.
3. Keep the traces for the power components wide, typically >50mil or 1.25mm.
4. Place the external networks for LBI and V<sub>FB</sub> close to the ILC6383, but away from the power components as far as possible.

#### Grounding

1. Use a star grounding system with separate traces for the power ground and the low power signals such as LBI/ $\overline{SD}$  and V<sub>FB</sub>. The star should radiate from where the power supply enters the PCB.
2. On multilayer boards use component side copper for grounding around the ILC6383 and connect back to a quiet ground plane using vias.



Recommended application circuit schematic for ILC6383CIR-ADJ



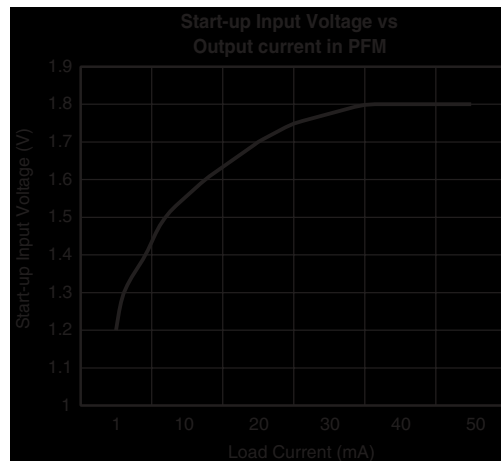
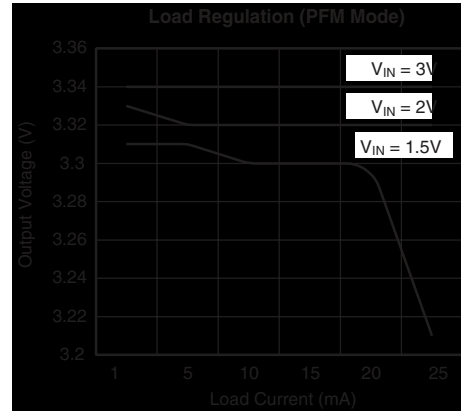
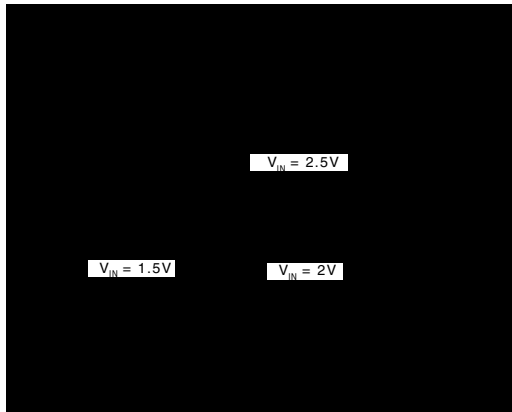
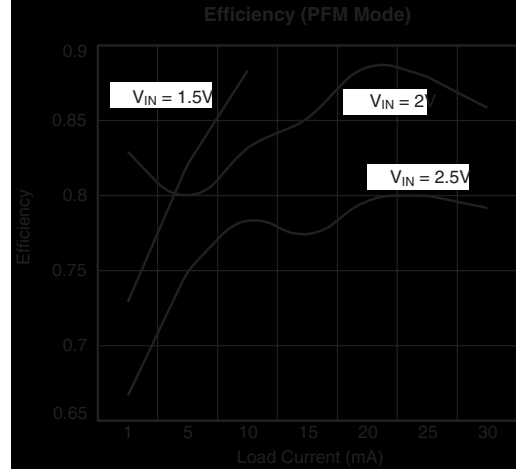
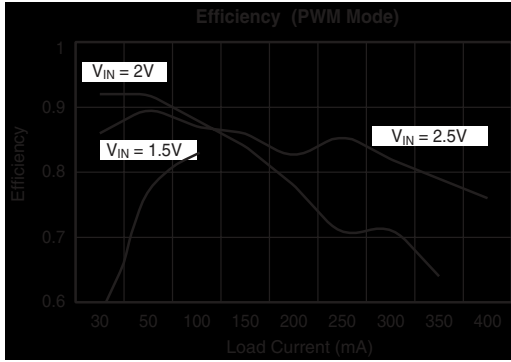
### Evaluation Board Parts List For Printed Circuit Board Shown Above

Label	Part Number	Manufacturer	Description
U1	ILC6383CIR-ADJ	Fairchild Semiconductor	Step-up DC-DC converter
C	GRM43-2X5R476K6.3	muRata	47µF, ceramic capacitor
L1	LQS66C150M04	muRata	15µH, 1.3A
R1 and R2	—	Dale, Panasonic	User Determined Values
R3	—	Dale, Panasonic	10kΩ, 1/10W, SMT

Label	Part Number	Manufacturer	Description
U1	ILC6383CIR-XX	Fairchild Semiconductor	Step-up DC-DC converter
C	GRM43-2X5R476K6.3	muRata	47µF, ceramic capacitor
L1	LQS66CA150M04	muRata	15µH, 1.3A
R1 and R3	—	Dale, Panasonic	10kΩ, 1/10W, SMT

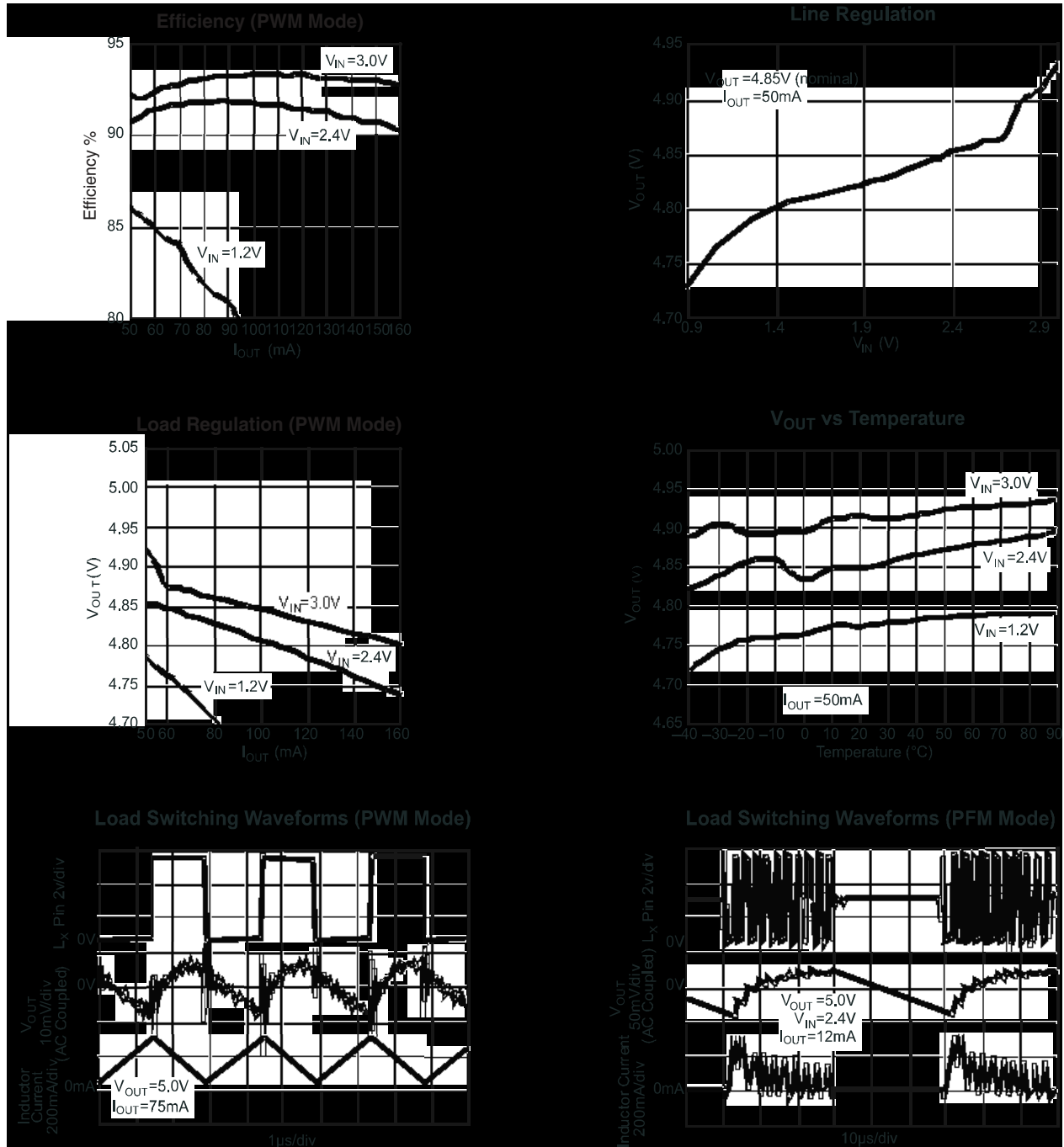
### Typical Performance Characteristics ILC6383CIR-33 ( $V_{OUT} = 3.3\text{ V}$ )

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $C_{IN} = 47\mu\text{F}$ ,  $C_{OUT} = 47\mu\text{F}$ ,  $L = 15\mu\text{H}$ .



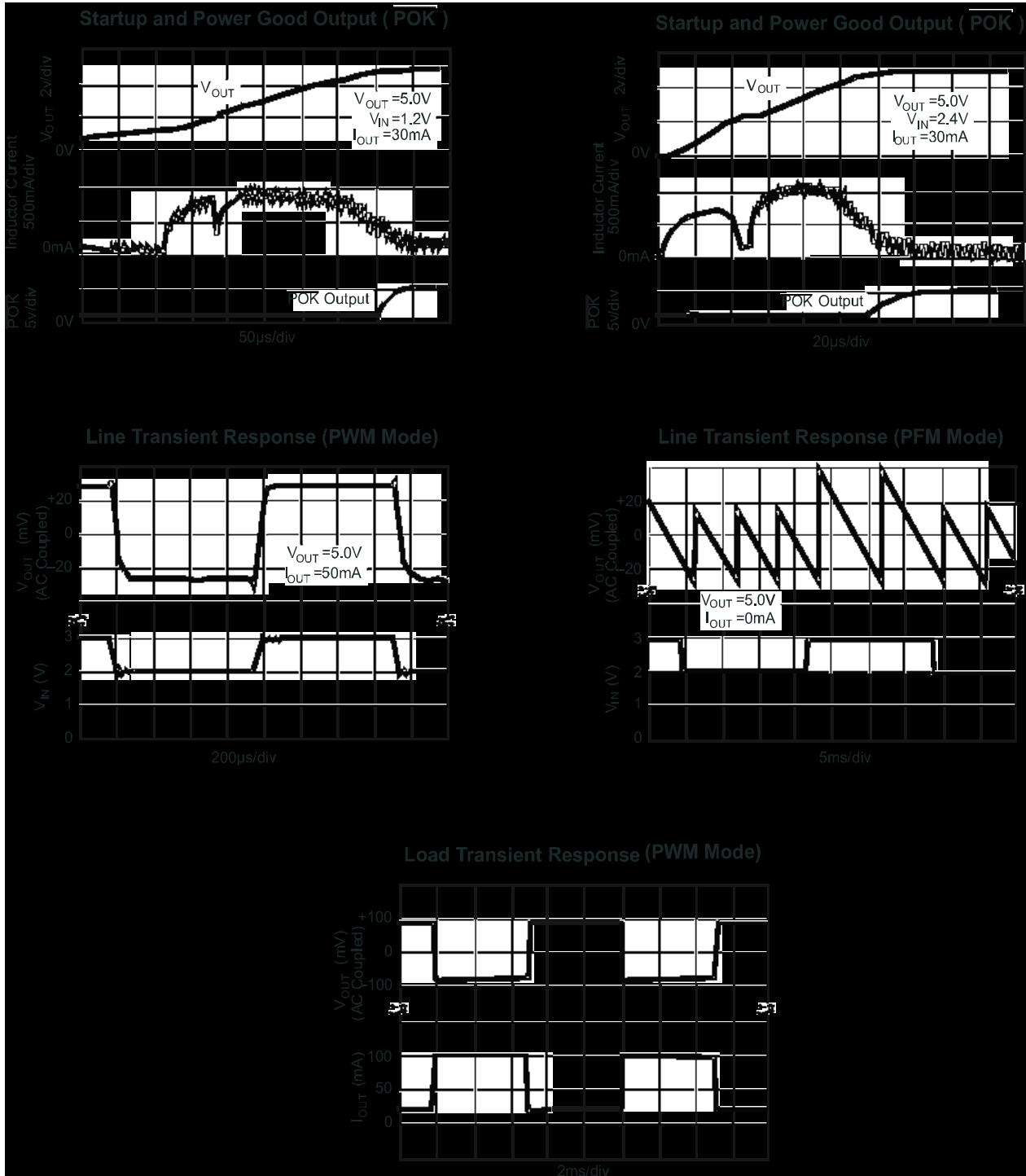
### Typical Performance Characteristics ILC6383CIR-50 ( $V_{OUT} = 5.0\text{ V}$ )

Unless otherwise specified:  $T_A = 25^\circ\text{C}$ ,  $C_{IN} = 47\mu\text{F}$ ,  $C_{OUT} = 47\mu\text{F}$ ,  $L = 15\mu\text{H}$ .



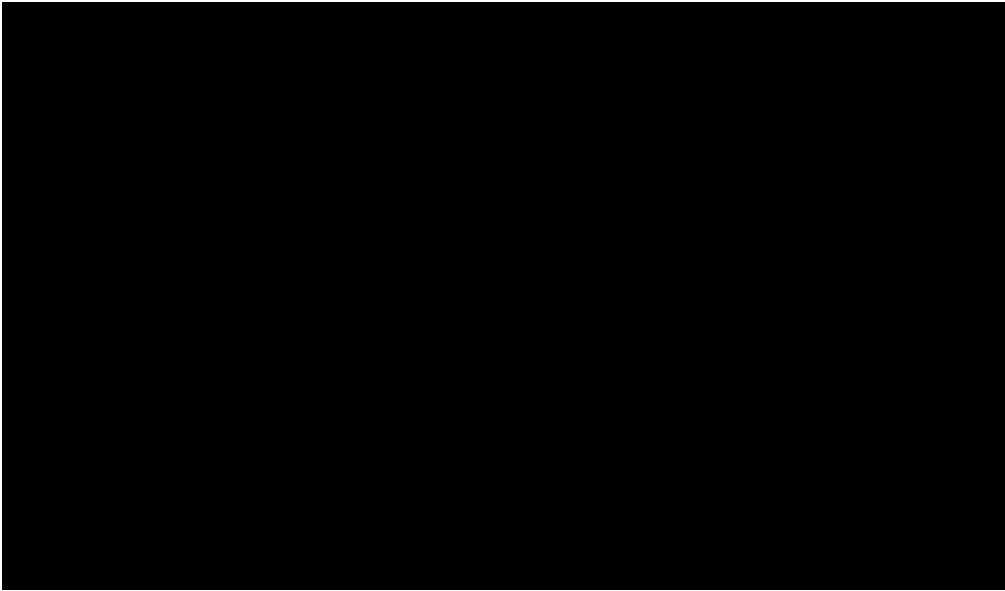
### Typical Performance Characteristics ILC6383CIR-50 ( $V_{OUT} = 5.0V$ ) (Continued)

Unless otherwise specified:  $T_A = 25^\circ C$ ,  $C_{IN} = 47\mu F$ ,  $C_{OUT} = 47\mu F$ ,  $L = 15\mu H$ .



## Mechanical Dimensions

### 8-Lead MSOP



## Ordering Information for Ta = -40°C to +85°C, MSOP-8 Package

Part Number	Output Voltage
ILC6383CIR33X	3.3V
ILC6383CIR50X	5.0V
ILC6383CIRADJX	Adjustable

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