NCV8512

5.0 V Micropower 150 mA LDO Linear Regulator with DELAY, Adjustable $\overline{\text{RESET}}$, and Monitor FLAG

The NCV8512 is a 5.0 V precision micropower voltage regulator. The output current capability is 150 mA.

The output voltage is accurate within ±2.0% with a maximum dropout voltage of 0.6 V at 150 mA. Low quiescent current is a feature drawing only 130 μA with a 100 μA load. This part is ideal for any and all battery operated microprocessor equipment.

Microprocessor control logic includes an active $\overline{\text{RESET}}$ (with DELAY), and a FLAG monitor which can be used to provide an early warning signal to the microprocessor of a potential impending $\overline{\text{RESET}}$ signal. The use of the FLAG monitor allows the microprocessor to finish any signal processing before the $\overline{\text{RESET}}$ shuts the microprocessor down.

The active $\overline{\text{RESET}}$ circuit operates correctly at an output voltage as low as 1.0 V. The $\overline{\text{RESET}}$ function is activated during the power up sequence or during normal operation if the output voltage drops outside the regulation limits.

The reset threshold voltage can be decreased by the connection of an external resistor divider to R_{ADJ} lead.

The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments.

Features

- 5.0 V ± 2.0% Output
- Low 130 μA Quiescent Current
- Active $\overline{\text{RESET}}$
- Adjustable Reset
- 150 mA Output Current Capability
- Fault Protection
  - +60 V Peak Transient Voltage
  - −15 V Reverse Voltage
  - Short Circuit
  - Thermal Overload
- Early Warning through $\overline{\text{FLAG}}$/MON Leads
- Thermally Enhanced in SOW−16 Exposed Pad
- NCV Prefix for Automotive and Other Applications Requiring Site and Control Changes
- AEC Qualified
- PPAP Capable
- These are Pb−Free Devices

ON Semiconductor®

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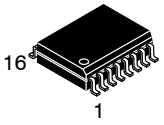
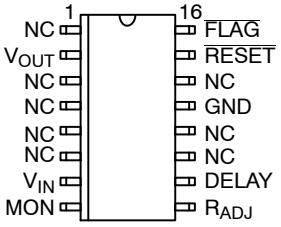


SOIC 16 LEAD WIDE BODY EXPOSED PAD PW SUFFIX CASE 751AG

MARKING DIAGRAM

A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb−Free Device

PIN CONNECTIONS*



*Pin connections for reference only.

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

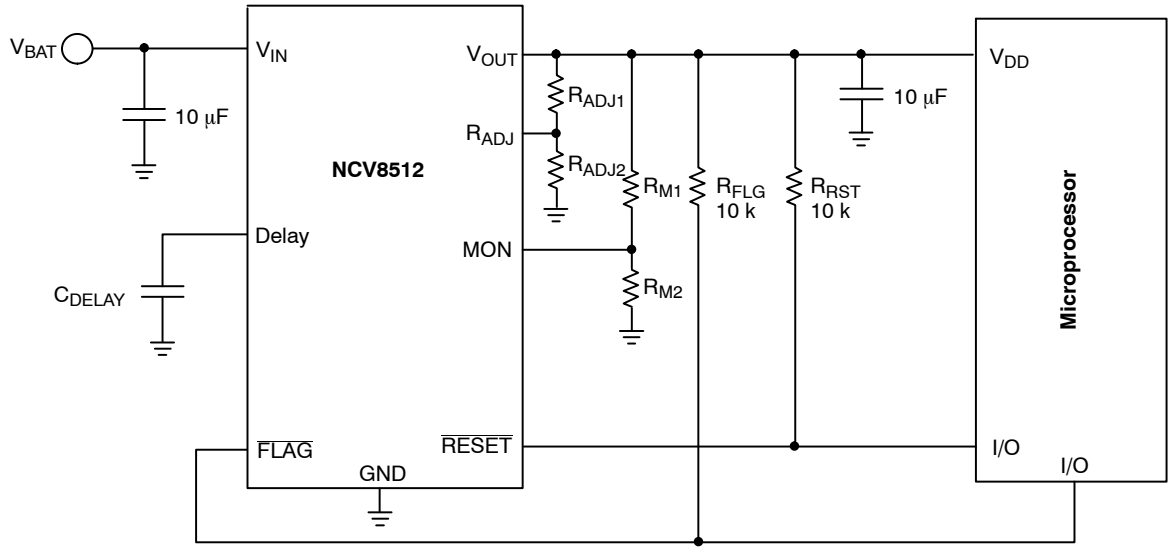


Figure 1. Application Diagram

MAXIMUM RATINGS†

Rating	Value	Unit
V_{IN} (DC)	−15 to 45	V
Peak Transient Voltage (46 V Load Dump @ V_{IN} = 14 V). Voltage with respect to ground.	60	V
Operating Voltage	45	V
V_{OUT} (DC)	16	V
Voltage Range ($\overline{RESET}$, $\overline{FLAG}$)	−0.3 to 10	V
Input Voltage Range (MON)	−0.3 to 10	V
V_{DELAY}	−0.3 to 4.0	V
V_{RADJ}	−0.3 to 10	V
ESD Susceptibility (Human Body Model)	2.0	kV
Junction Temperature, T_J	−40 to +150	°C
Storage Temperature, T_S	−55 to 150	°C
Package Thermal Resistance, SOW−16 E Pad: Junction−to−Case, $R_{\theta JC}$ Junction−to−Ambient, $R_{\theta JA}$	 16 57	°C/W
Lead Temperature Soldering: Reflow: (SMD styles only) (Notes 1, 2. and 3)	265 peak	°C
Moisture Sensitivity Level at 260°C	1	

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

†During the voltage range which exceeds the maximum tested voltage of V_{IN}, operation is assured, but not specified. Wider limits may apply. Thermal dissipation must be observed closely.

1. 60 second maximum above 217°C.
2. −5°C/+0°C allowable conditions.
3. Per IPC/JEDEC J−STD−020C.

ELECTRICAL CHARACTERISTICS (I_{OUT} = 1.0 mA, −40°C ≤ T_J ≤ 125°C; 6.0 V < V_{IN} < 26 V; unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
OUTPUT STAGE					
Output Voltage	9.0 V < V_{IN} < 16 V, 100 μA ≤ I_{OUT} ≤ 150 mA 6.0 V < V_{IN} < 26 V, 100 μA ≤ I_{OUT} ≤ 150 mA	4.90 4.85	5.0 5.0	5.10 5.15	V V
Dropout Voltage (V_{IN} − V_{OUT})	I_{OUT} = 150 mA I_{OUT} = 1.0 mA	– –	400 100	600 150	mV mV
Load Regulation	V_{IN} = 14 V, 5.0 mA ≤ I_{OUT} ≤ 150 mA	-30	5.0	30	mV
Line Regulation	[V_{OUT}(typ) + 1.0] < V_{IN} < 26 V, I_{OUT} = 1.0 mA	–	15	60	mV
Quiescent Current, (I_Q) Active Mode	I_{OUT} = 100 μA, V_{IN} = 12 V, Delay = 3.0 V, MON = 3.0 V I_{OUT} = 75 mA, V_{IN} = 14 V, Delay = 3.0 V, MON = 3.0 V I_{OUT} ≤ 150 mA, V_{IN} = 14 V, Delay = 3.0 V, MON = 3.0 V	– – –	130 4.0 12	200 6.0 19	μA mA mA
Current Limit	–	151	300	–	mA
Short Circuit Output Current	V_{OUT} = 0 V	40	190	–	mA
Thermal Shutdown	(Guaranteed by Design)	150	180	–	°C
RESET FUNCTION (RESET)					
$\overline{\text{RESET}}$ Threshold HIGH (V_{RH}) LOW (V_{RL})	 V_{OUT} Increasing V_{OUT} Decreasing	 4.55 4.50	 4.70 4.60	 0.98 × V_{OUT} 0.97 × V_{OUT}	 V V
Output Voltage Low (V_{RLO})	1.0 V ≤ V_{OUT} ≤ V_{RL}, $R_{\overline{\text{RESET}}}$ = 10 k	–	0.1	0.4	V
Delay Switching Threshold (V_{DT})	–	1.4	1.8	2.2	V
Lower Delay Switching Threshold (V_{LD})	–	0.3	0.45	0.6	V
Reset Delay Low Voltage	V_{OUT} < $\overline{\text{RESET}}$ Threshold Low(min)	–	–	0.1	V
Delay Charge Current	DELAY = 1.0 V, V_{OUT} > V_{RH}	6.0	9.0	15	μA
Delay Discharge Current	DELAY = 1.0 V, V_{OUT} = 1.5 V	5.0	–	–	mA
Reset Adjust Switching Voltage ($V_{R(ADJ)}$)	–	1.23	1.31	1.39	V
$\overline{\text{FLAG}}$/MONITOR					
Monitor Threshold	Increasing and Decreasing	1.10	1.20	1.31	V
Hysteresis	–	20	50	100	mV
Input Current	MON = 2.0 V	−0.5	0.1	0.5	μA
Output Saturation Voltage	MON = 0 V, I_{FLAG} = 1.0 mA	–	0.1	0.4	V

PACKAGE PIN DESCRIPTION

Package Pin Number SOW−16 Exposed Pad	Pin Symbol	Function
1, 3−6, 11, 12, 14	NC	No connection.
2	V_{OUT}	±2.0%, 150 mA output.
7	V_{IN}	Input Voltage.
8	MON	Monitor. Input for early warning comparator. If not needed connect to V_{OUT}.
9	R_{ADJ}	Reset Adjust. If not needed connect to ground.
10	DELAY	Timing capacitor for $\overline{\text{RESET}}$ function.
13	GND	Ground. All GND leads must be connected to Ground.
15	$\overline{\text{RESET}}$	Active reset (accurate to $V_{OUT} \geq 1.0$ V).
16	$\overline{\text{FLAG}}$	Open collector output from early warning comparator.

TYPICAL PERFORMANCE CHARACTERISTICS

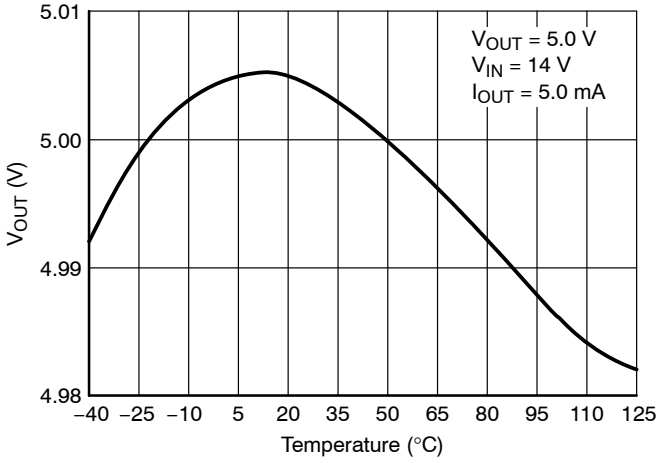


Figure 2. Output Voltage vs. Temperature

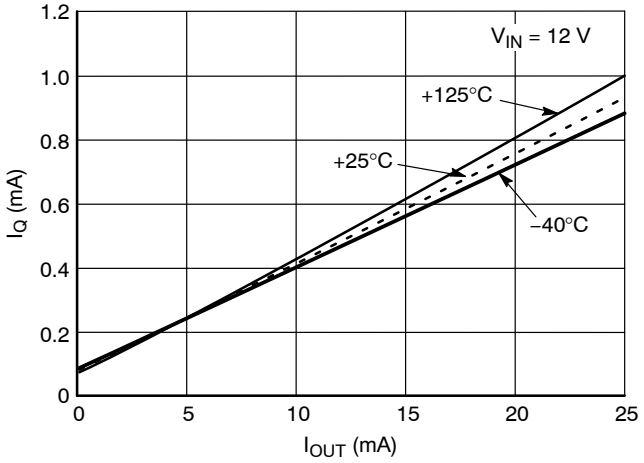


Figure 3. Quiescent Current vs. Output Current

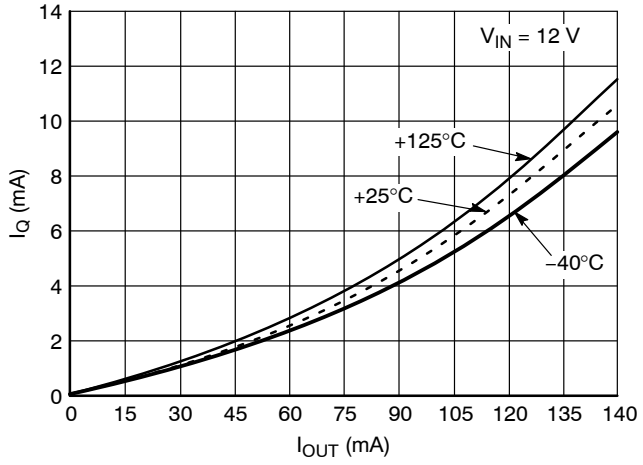


Figure 4. Quiescent Current vs. Output Current

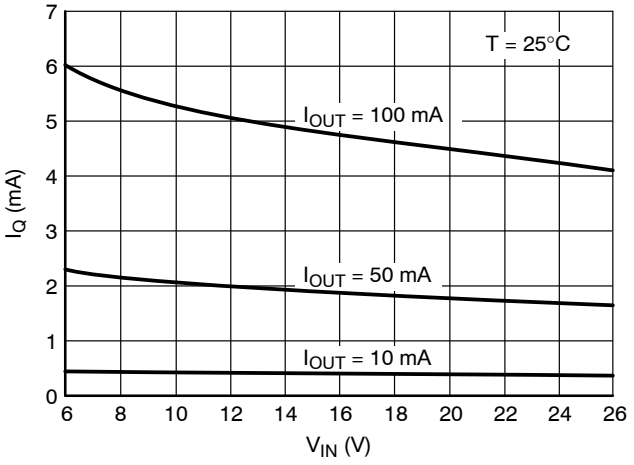


Figure 5. Quiescent Current vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

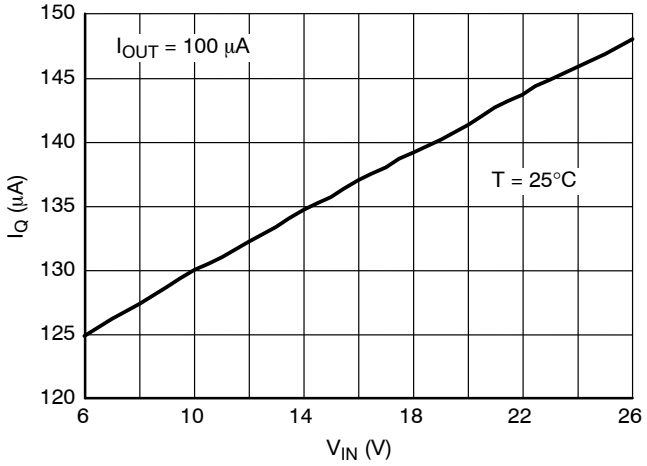


Figure 6. Quiescent Current vs. Input Voltage

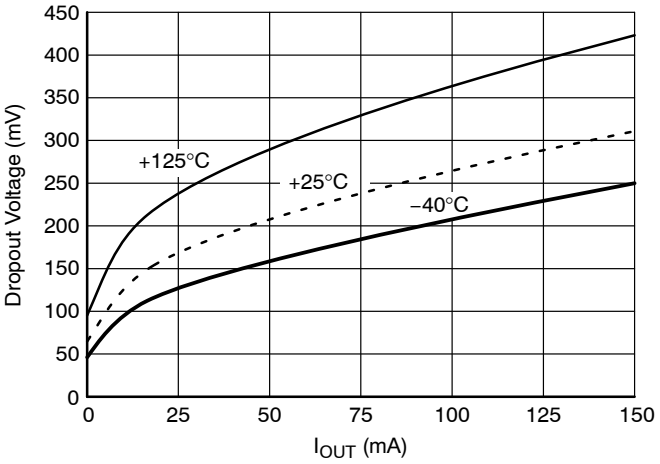


Figure 7. Dropout Voltage vs. Output Current

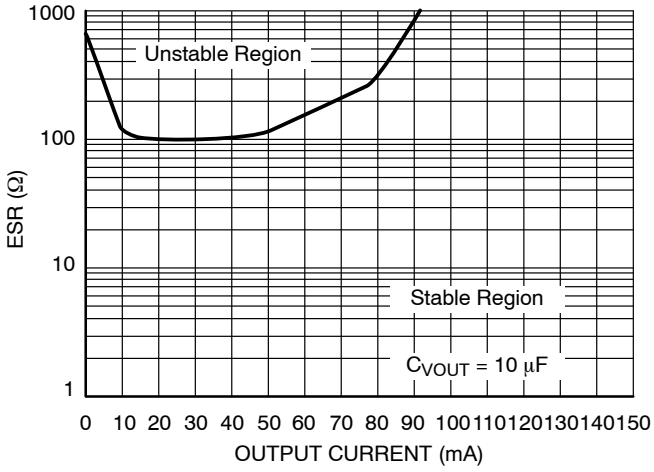


Figure 8. Output Capacitor ESR

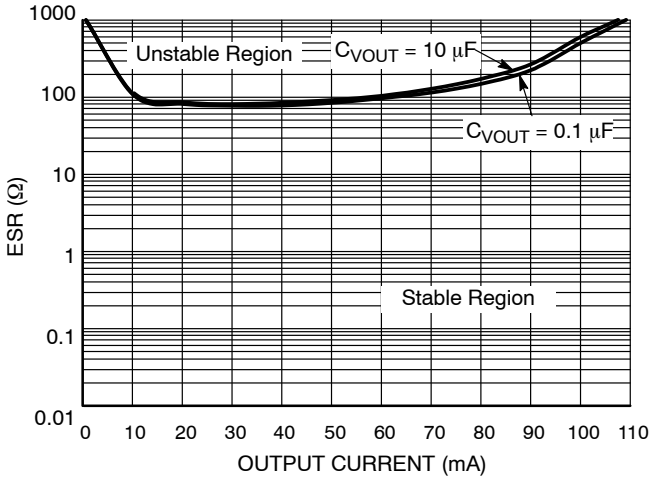


Figure 9. Output Stability with Output Capacitor Change

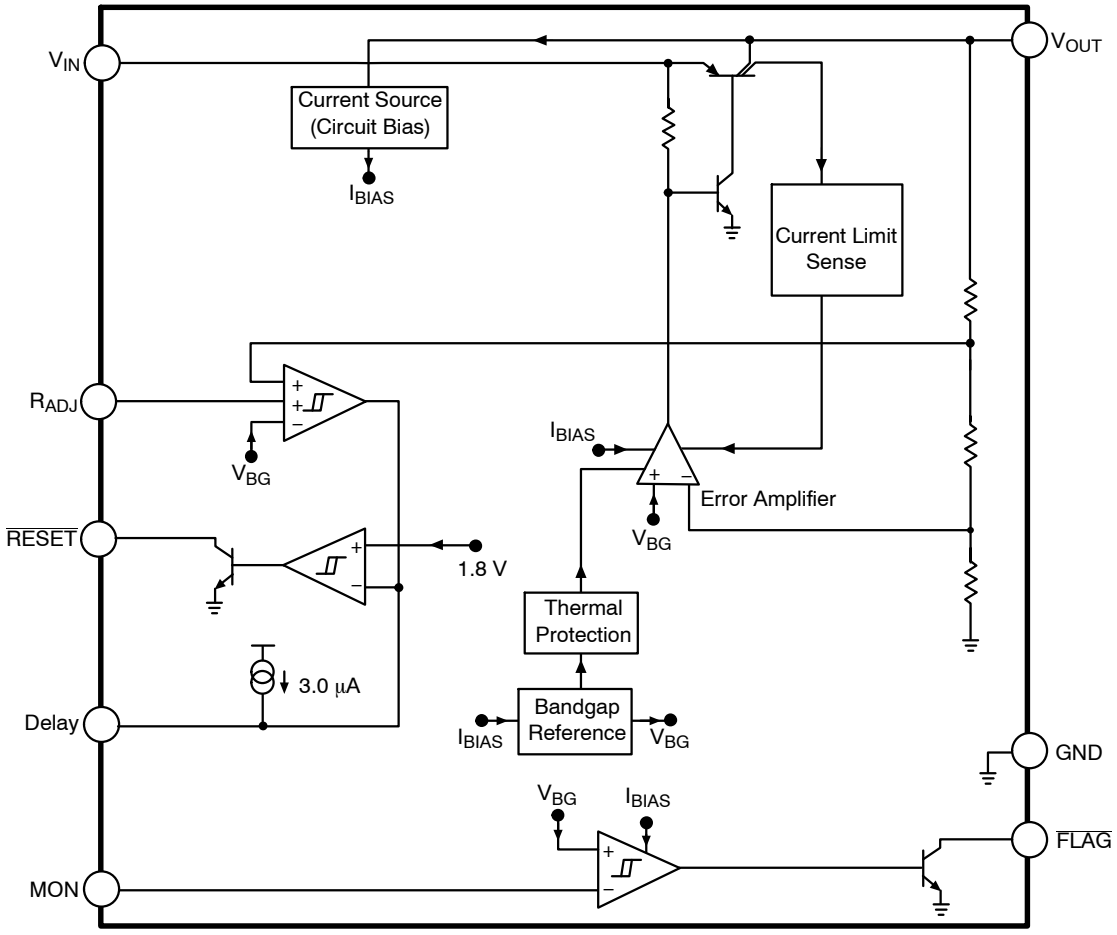


Figure 10. Block Diagram

CIRCUIT DESCRIPTION

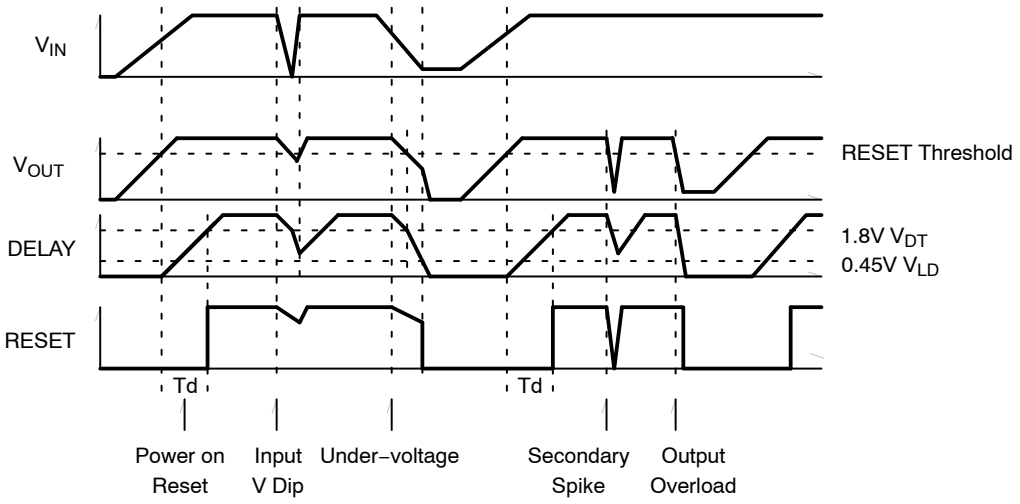


Figure 11. Reset and Delay Circuit Wave Forms

REGULATOR CONTROL FUNCTIONS

The NCV8512 contains a microprocessor−compatible control function $\overline{\text{RESET}}$ (Figure 11).

$\overline{\text{RESET}}$ Function

A $\overline{\text{RESET}}$ signal (low voltage) is generated as the IC powers up. After V_{OUT} increases above the $\overline{\text{RESET}}$ threshold, the DELAY timer is started. When the DELAY timer passes 1.8 V, the $\overline{\text{RESET}}$ signal goes high. A discharge of the DELAY timer is started when V_{OUT} drops and stays below the $\overline{\text{RESET}}$ threshold. When the DELAY timer level drops below 0.45 V, the $\overline{\text{RESET}}$ signal is brought low.

The $\overline{\text{RESET}}$ output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC thereby guaranteeing that the $\overline{\text{RESET}}$ signal is valid for V_{OUT} as low as 1.0 V.

Adjustable Reset Function

The reset threshold VRL can be decreased from a typical value of 4.65 V to as low as 3.5 V by using an external voltage divider connected from V_{OUT} to the pin R_{ADJ} as displayed in Figure 12. The resistor divider keeps the voltage above the $V_{RADJ.TH}$ (typical 1.31 V) and overrides the internal threshold detector. Adjust the voltage divider according to the following relationship:

$$V_{THRES} = V_{RADJ.TH} \times \frac{RADJ1 + RADJ2}{RADJ2} \quad (2)$$

Where;

V_{THRES} is the desired output threshold voltage that starts the time delay for Power on Reset Delay.

$V_{RADJ.TH}$ is the default threshold voltage of 1.31 V typ.

R_{ADJ1} is the resistor connected from the 5 V output to the R_{ADJ} pin.

R_{ADJ2} is the resistor connected from the R_{ADJ} pin to ground.

If the reset adjust option is not needed, the R_{ADJ} pin should be connected to GND causing the reset threshold to go to its default value (4.65 V typical).

As an example, select resistors to give a threshold voltage of 4.0 V. This will allow the delay timer to start when the output crosses the 4.0 V level.

V_{THRES} = 4.0 V = 1.31 V x (R_{ADJ1} + R_{ADJ2}) / R_{ADJ2}

Let R_{ADJ2} be 100 kΩ for low current consumption.

R_{ADJ1} = 2.05 x 100 k = 205 kΩ

With 5 V on the output, the voltage on the R_{ADJ} pin will be 1.64 V.

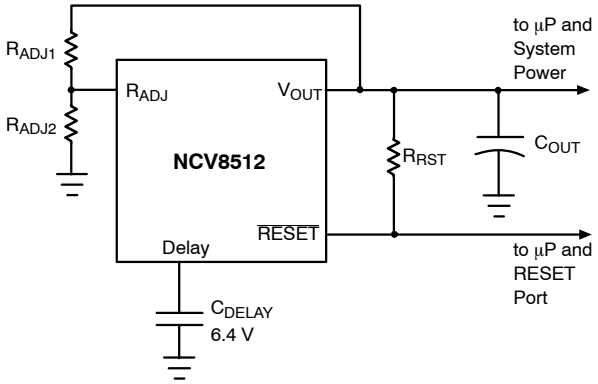


Figure 12. Adjustable $\overline{\text{RESET}}$

DELAY Function

The reset delay circuit provides a delay (programmable by external capacitor) on the $\overline{\text{RESET}}$ output lead.

The DELAY lead provides source current (typically 9 μA) to the external DELAY capacitor at the following times:

1. During Power Up (once the regulation threshold has been exceeded).

2. After a reset event has occurred and the device is back in regulation. The DELAY capacitor is discharged when the regulation ($\overline{\text{RESET}}$ threshold) has been violated. When the DELAY capacitor discharges to 0.45 V, the $\overline{\text{RESET}}$ signal pulls low.

$\overline{\text{FLAG}}$/Monitor Function

An on−chip comparator is available to provide an early warning to the microprocessor of a possible reset signal. The reset signal typically turns the microprocessor off instantaneously. This can cause unpredictable results with the microprocessor. The signal received from the $\overline{\text{FLAG}}$ pin will allow the microprocessor time to complete its present task before shutting down. This function is performed by a comparator referenced to the bandgap voltage. The actual trip point can be programmed externally using a resistor divider to the input monitor (MON) (Figure 13). The typical threshold is 1.20 V on the MON Pin.

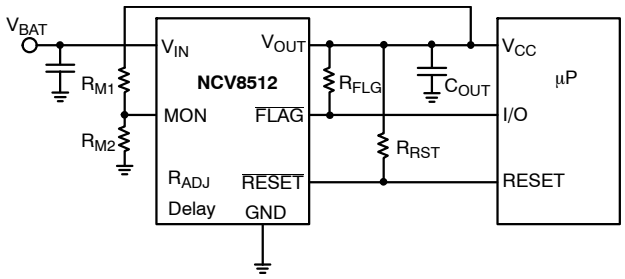


Figure 13. $\overline{\text{FLAG}}$/Monitor Function

APPLICATION NOTES

FLAG MONITOR

Figure 14 shows the FLAG Monitor waveforms taken from the circuit depicted in Figure 13. As the output voltage falls (V_{OUT}), the Monitor threshold is crossed. This causes the voltage on the $\overline{\text{FLAG}}$ output to go low sending a warning signal to the microprocessor that a $\overline{\text{RESET}}$ signal may occur in a short period of time. $T_{WARNING}$ is the time the microprocessor has to complete the function it is currently working on and get ready for the $\overline{\text{RESET}}$ shutdown signal.

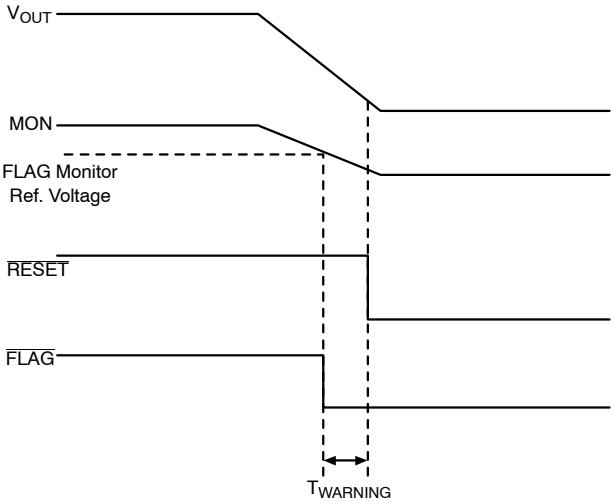


Figure 14. FLAG Monitor Circuit Waveform

SETTING THE DELAY TIME

The delay time is controlled by the Reset Delay Low Voltage, Delay Switching Threshold, and the Delay Charge Current. The delay follows the equation:

$$t_{DELAY} = \frac{\left[C_{DELAY}(V_{DT} - \text{Reset Delay Low Voltage})\right]}{\text{Delay Charge Current}}$$

Example:

Using C_{DELAY} = 33 nF.

Use the typical value for Delay Low Voltage = 0.04 V.

Use the typical value for V_{DT} = 1.8 V.

Use the typical value for Delay Charge Current = 9.0 µA.

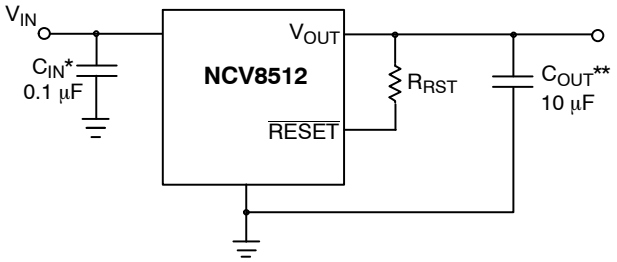
$$t_{DELAY} = \frac{\left[33\ \text{nF}(1.8 - 0.04\ \text{V})\right]}{9.0\ \mu\text{A}} = 6.45\ \text{ms}$$

STABILITY CONSIDERATIONS

The output or compensation capacitor helps determine three main characteristics of a linear regulator: startup delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints. A tantalum or aluminum electrolytic capacitor is best, since a film or ceramic capacitor with almost zero ESR can cause instability. The aluminum electrolytic capacitor is the least expensive solution, but, if the circuit operates at low temperatures (−25°C to −40°C), both the value and ESR of the capacitor will vary considerably. The capacitor manufacturer's data sheet usually provides this information.

The value for the output capacitor C_{OUT} shown in Figure 15 should work for most applications, but is not necessarily the optimized solution.



*C_{IN} required if regulator is located far from the power supply filter.
**C_{OUT} required for stability. Capacitor must operate at minimum temperature expected.

Figure 15. Test and Application Circuit Showing Output Compensation

CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 16) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}]I_{OUT(max)} + V_{IN(max)}I_Q \quad (1)$$

where:

$V_{IN(max)}$ is the maximum input voltage,

$V_{OUT(min)}$ is the minimum output voltage,

$I_{OUT(max)}$ is the maximum output current for the application, and

I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150°C - T_A}{P_D} \quad (2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C.

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

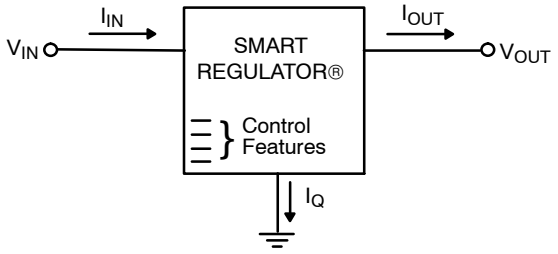


Figure 16. Single Output Regulator with Key Performance Parameters Labeled

HEATSINKS

A heatsink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (3)$$

where:

$R_{\theta JC}$ = the junction−to−case thermal resistance,

$R_{\theta CS}$ = the case−to−heatsink thermal resistance, and

$R_{\theta SA}$ = the heatsink−to−ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heatsink data sheets of heat sink manufacturers.

Further mounting and cooling information is available in the application note, AN1040/D, "Mounting Considerations for Power Semiconductors" located in the ON Semiconductor web site.

ORDERING INFORMATION

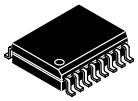
Device	Output Voltage	Package	Shipping†
NCV8512PW50G	5.0 V	SOW−16 E Pad (Pb−Free)	47 Units / Rail
NCV8512PW50R2G			1000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

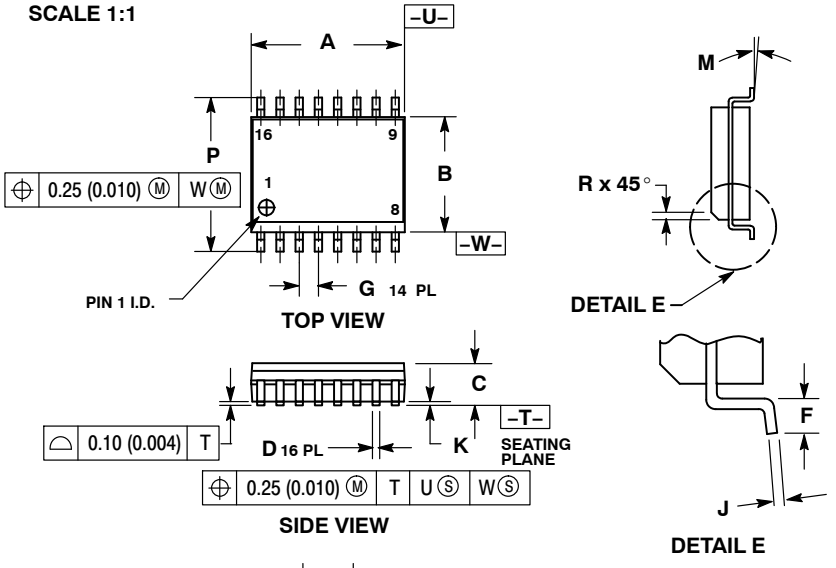
SOIC 16 LEAD WIDE BODY, EXPOSED PAD

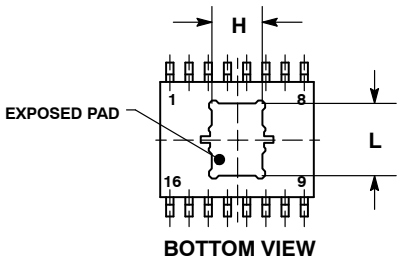
CASE 751AG
ISSUE B

DATE 31 MAY 2016



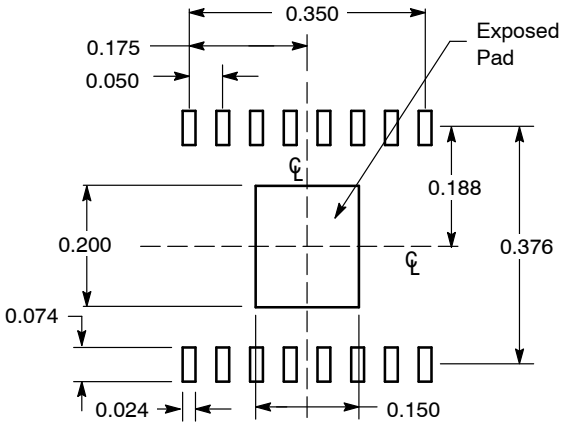
SCALE 1:1





BOTTOM VIEW

SOLDERING FOOTPRINT*



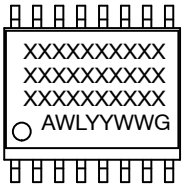
DIMENSIONS: INCHES

*For additional information on our Pb–Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751R–01 OBSOLETE, NEW STANDARD 751R–02.

	MILLIMETERS		INCHES	
DIM	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
H	3.45	3.66	0.136	0.144
J	0.25	0.32	0.010	0.012
K	0.00	0.10	0.000	0.004
L	4.72	4.93	0.186	0.194
M	0 °	7 °	0 °	7 °
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

GENERIC MARKING DIAGRAM*



XXXXX = Specific Device Code
A = Assembly Location
WL = Wafer Lot
YY = Year
WW = Work Week
G = Pb–Free Package

*This information is generic. Please refer to device data sheet for actual part marking. Pb–Free indicator, “G” or microdot “ ▪”, may or may not be present.

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DESCRIPTION:	**SOIC–16, WB EXPOSED PAD**		**PAGE 1 OF 1**

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